ISO124 入力電圧範囲±10Vの高精度絶縁アンプ

1 特長

- 100%高電圧破壊試験済み
- 定格1500Vrms
- 高IMR: 140dB (60Hz時)
- 最大非線形性: 0.010%
- バイポーラ動作: V_O＝±10V
- パッケージ: PDIP-16およびSOIC-28
- 使いやすい: 固定ユニティ・ゲイン構成
- 電源電圧範囲: ±4.5V～±18V

2 アプリケーション

- 産業用プロセス制御:
  - トランスデューサ・アイソレータ、熱電対/RTD/圧力ブリッジ/流量計用アイソレータ、4mA～20mAループ絶縁
- グランド・ループの除去
- モータおよびSCR制御
- 電力監視
- PCによるデータ収集
- 試験用機器

3 概要

ISO124は、新しいデューティ・サイクル変調/復調方式を採用した高精度絶縁アンプです。2pFの差動容量性バリアを通して信号をデジタル送信します。デジタル変調方式により、バリア特性が信号の完全性に影響しないため、バリアを通して優れた信頼性と適切な高周波過渡耐性を実現できます。2つのバリア容量はパッケージのプラスチック体に組み込まれています。

ISO124は使いやすく、外付け部品を必要としません。主な仕様は、最大非線形性0.010%、信号帯域幅50kHz、V_{OS}ドリフト200µV/℃となっています。電源電圧範囲は±4.5V～±18V、静止電流はV_{S1}で±5mA、V_{S2}で±5.5mAであることから、幅広いアプリケーションに適しています。

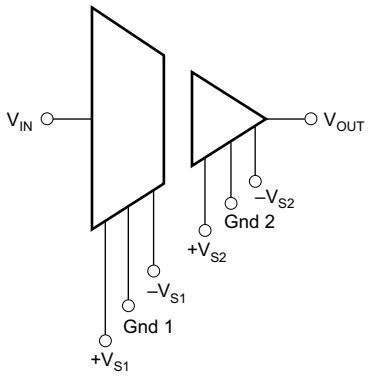
ISO124は16ピンPDIPおよび28リードSOICプラスチック表面実装パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ISO124	PDIP (16)	17.90mm×7.50mm
	SOIC (28)	20.01mm×6.61mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

概略回路図



目次

4 改訂履歴

Revision D (July 2016) から **Revision E** に変更 **Page**

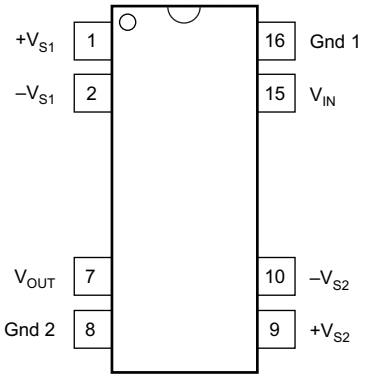
- このデータシートの末尾にあるパッケージ・オプションの内容と一致するように16ピンSOICパッケージを16ピンPDIPパッケージに 変更 ... 1
- Changed DVA and NVF pin configuration labels to match content shown in the package option addendum at the end of the data sheet ... 3
- Changed parameter name from "vs temperature" to "Input offset drift" in *Electrical Characteristics* table ... 5
- Changed parameter name from "vs power supply" to "Power-supply rejection ratio" in *Electrical Characteristics* table ... 5
- Changed location of supply voltage specifications from the *Electrical Characteristics* table to the *Recommended Operating Conditions* table ... 5
- Changed parameter name from "Quiescent current" to "High-side analog supply current", and changed symbol from "V_{S1}" to "I_{VS1}" in *Electrical Characteristics* table ... 5
- Changed parameter name from "Quiescent current" to "Low-side analog supply current", and changed symbol from "V_{S2}" to "I_{VS2}" in Electrical Characteristics table ... 5
- Changed location of Temperature specifications from the *Electrical Characteristics* table to the *Recommended Operating Conditions* table ... 5
- Deleted Thermal resistance parameters from *Electrical Characteristics* table; see *Thermal Information* table ... 5

Revision C (September 2005) から **Revision D** に変更 **Page**

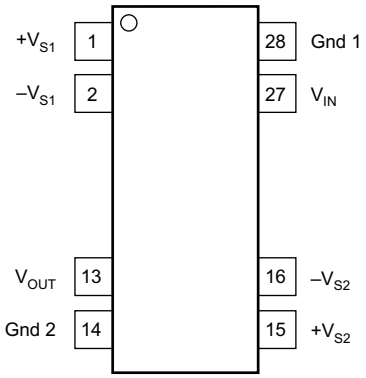
- 「*ESD定格*」の表、「*機能概要*」セクション、「*デバイスの機能モード*」、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを 追加 ... 1

5 Pin Configuration and Functions

NVF Package
16-Pin PDIP
Top View



DVA Package
28-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PDIP	SOIC		
Gnd 1	16	28	—	High-side ground reference
Gnd 2	8	14	—	Low-side ground reference
V_{IN}	15	27	I	High-side analog input
V_{OUT}	7	13	O	Low-side analog output
$+V_{S1}$	1	1	—	High-side positive analog supply
$–V_{S1}$	2	2	—	High-side negative analog supply
$+V_{S2}$	9	15	—	Low-side positive analog supply
$–V_{S2}$	10	16	—	Low-side negative analog supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage		±18	V
Analog input voltage, V_{IN}		100	V
Continuous isolation voltage		1500	Vrms
Junction temperature		125	°C
Output short to common		Continuous	
Storage temperature, T_{stg}	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S1}	High-side analog supply voltage (±V_{S1} to GND1)	±4.5	±15	±18	V
V_{S2}	Low-side analog supply voltage (±V_{S2} to GND2)	±4.5	±15	±18	V
V_{IN}	Analog input voltage		±10		V
T_A	Operating temperature	–25		85	°C

6.4 Thermal Information

THERMAL METRIC (1)		ISO124		UNIT
		DVA (SOIC)	NVF (PDIP)	
		28 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.8	51.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	32.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	29.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.9	29.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

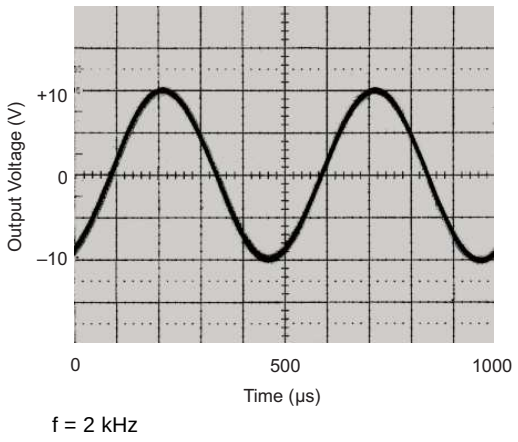
at T_A = +25°C , V_{S1} = V_{S2} = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOLATION						
	Rated voltage	Continuous ac 60 Hz	1500			Vac
	100% test(1)	Test time = 1 s, partial discharge ≤ 5 pC	2400			Vac
	Isolation mode rejection	60 Hz		140		dB
	Barrier impedance			10^{14} || 2		Ω || pF
	Leakage current at 60 Hz	V_{ISO} = 240 Vrms		0.18	0.5	µArms
GAIN						
	Nominal gain	V_O = ±10 V		1		V/V
	Gain error	V_O = ±10 V		±0.05	±0.50	%FSR
	Gain vs temperature			±10		ppm/°C
	Nonlinearity(2)			±0.005	±0.010	%FSR
INPUT OFFSET VOLTAGE						
	Initial offset			±20	±50	mV
	Input offset drift			±200		µV/°C
PSRR	Power-supply rejection ratio			±2		mV/V
	Noise			4		µV/√Hz
INPUT						
	Input voltage		±10	±12.5		V
	Resistance			200		kΩ
OUTPUT						
	Output voltage		±10	±12.5		V
	Current drive		±5	±15		mA
	Capacitive load drive			0.1		µF
	Ripple voltage(3)			20		mVp-p
FREQUENCY RESPONSE						
	Small-signal bandwidth			50		kHz
	Slew rate			2		V/µs
	Settling Time 0.10%	V_O = ±10 V		50		µs
	Settling Time 0.01%	V_O = ±10 V		350		µs
	Overload recovery time			150		µs
POWER SUPPLIES						
I_{VS1}	High-side analog supply current			±5.0	±7.0	mA
I_{VS2}	Low-side analog supply current			±5.5	±7.0	mA

(1) Tested at 1.6x rated, fail on 5-pC partial discharge.
(2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line, and is expressed as the ratio of deviation to FSR.
(3) Ripple frequency is at carrier frequency (500 kHz).

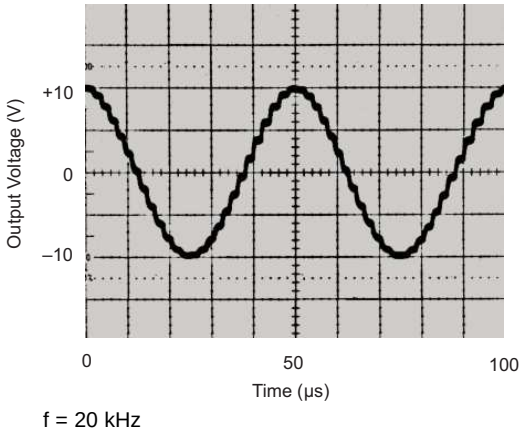
6.6 Typical Characteristics

at T_A = +25°C, and V_S = ±15 V (unless otherwise noted)



f = 2 kHz

Figure 1. Sine Response



f = 20 kHz

Figure 2. Sine Response

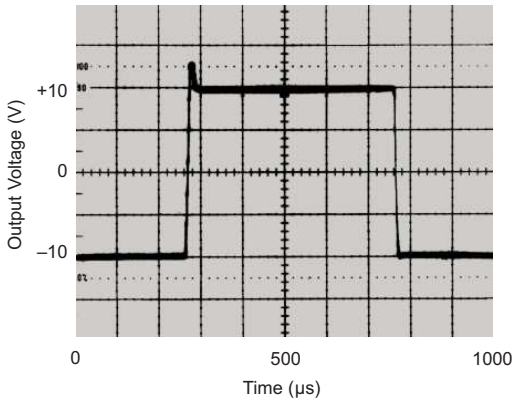


Figure 3. Step Response

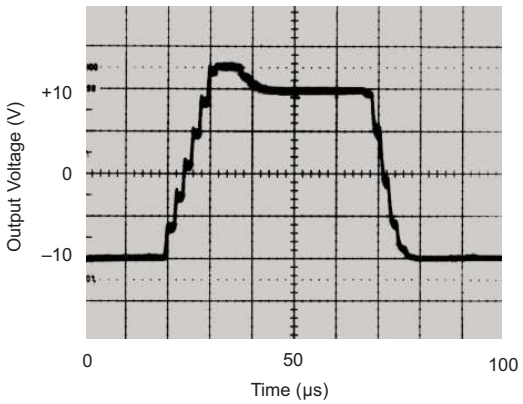


Figure 4. Step Response

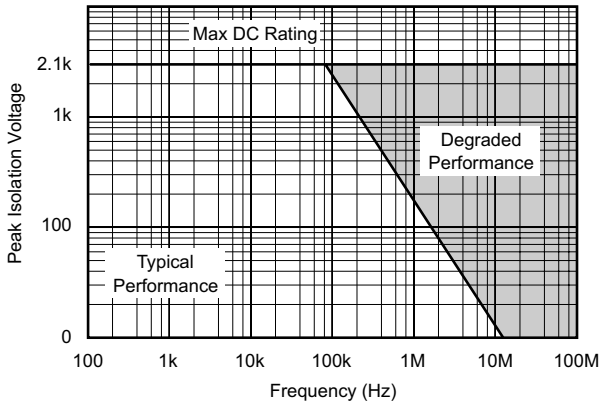


Figure 5. Isolation Voltage vs Frequency

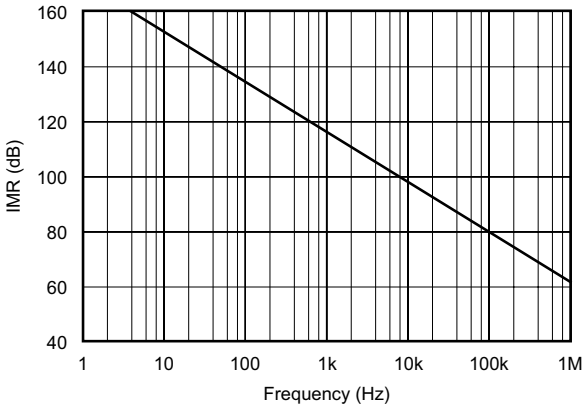


Figure 6. IMR vs Frequency

Typical Characteristics (continued)

at T_A = +25°C, and V_S = ±15 V (unless otherwise noted)

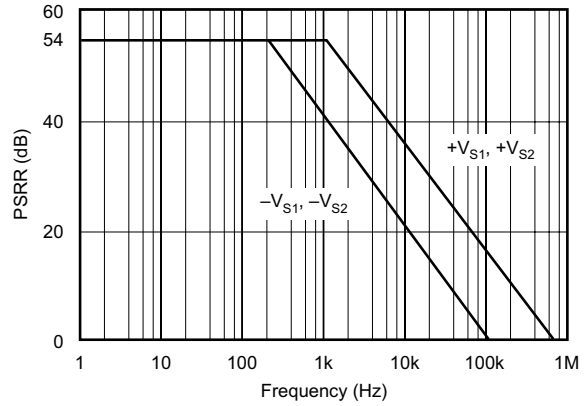


Figure 7. PSRR vs Frequency

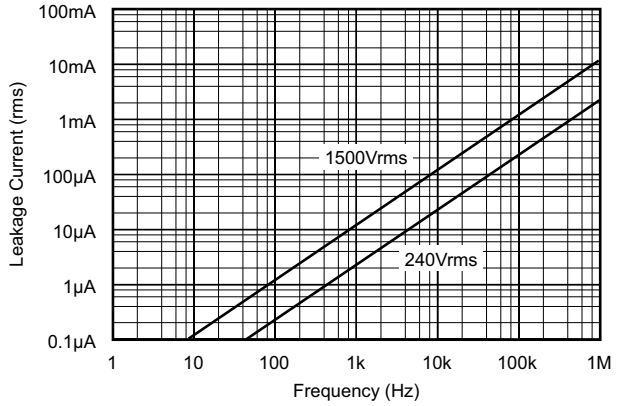
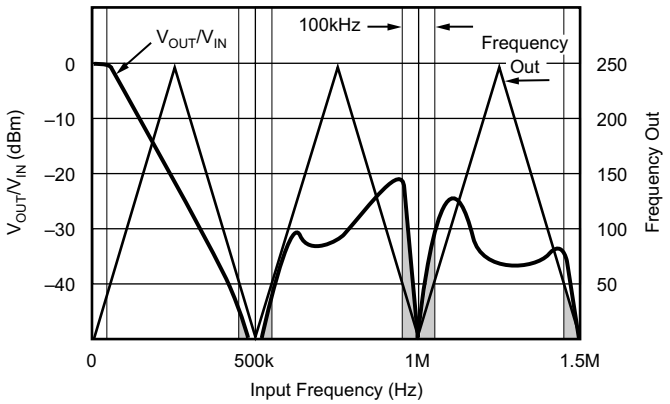


Figure 8. Isolation Leakage Current vs Frequency



NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.

Figure 9. Signal Response to Inputs Greater than 250 kHz

7 Detailed Description

7.1 Overview

The ISO124 isolation amplifier uses an input and an output section galvanically isolated by matched 1-pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections. The ISO124 contains 250 transistors.

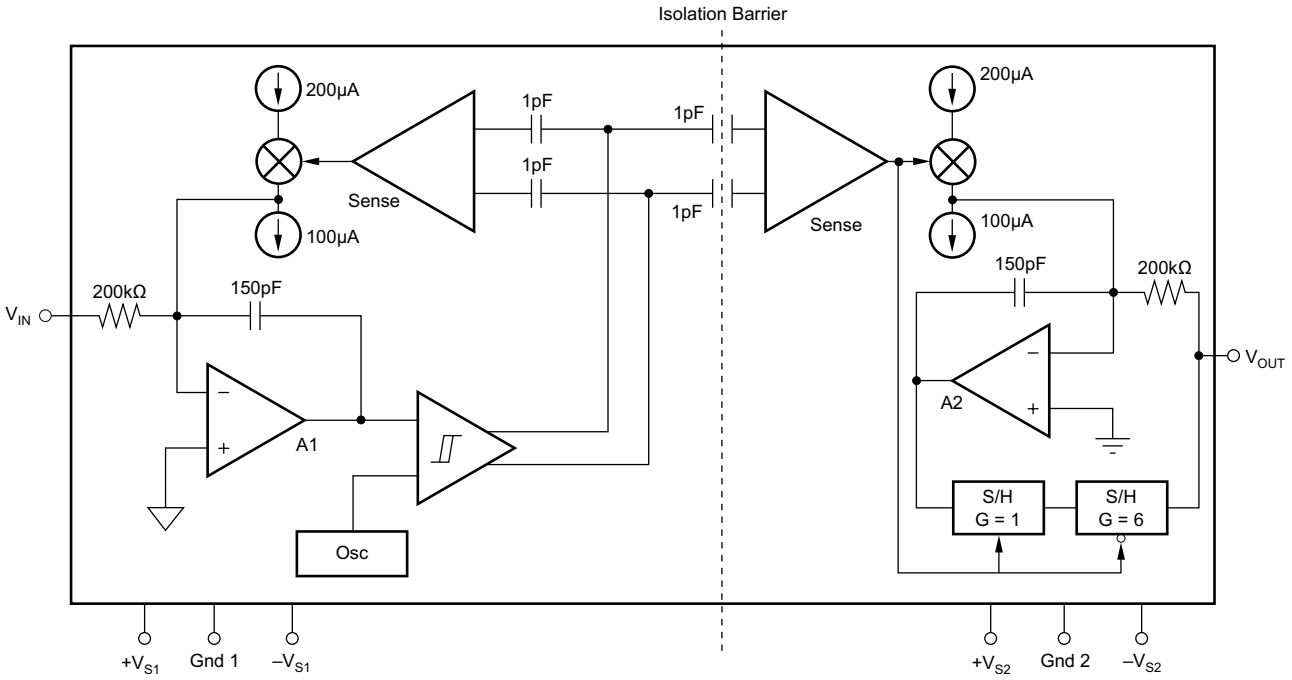
7.1.1 Modulator

An input amplifier (A1, as shown in *Functional Block Diagram*) integrates the difference between the input current (V_{IN}/200 kΩ) and a switched ±100-µA current source. This current source is implemented by a switchable 200-µA source and a fixed 100-µA current sink. To understand the basic operation of the modulator, assume that V_{IN} = 0 V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500 kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave

7.1.2 Demodulator

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200-kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample-and-hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Isolation Amplifier

The ISO124 is a precision analog isolation amplifier. The input signal is transmitted digitally across a high-voltage differential capacitive barrier. With digital modulation, the barrier characteristics do affect signal integrity, resulting in excellent reliability and high-frequency transient immunity.

7.4 Device Functional Modes

The ISO124 device does not have any additional functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Carrier Frequency Considerations

The ISO124 amplifier transmits the signal across the isolation barrier by a 500-kHz duty-cycle modulation technique. For input signals having frequencies below 250 kHz, this system works like any linear amplifier. But for frequencies above 250 kHz, the behavior is similar to that of a sampling amplifier. Figure 9 shows this behavior graphically; at input frequencies above 250 kHz, the device generates an output signal component of reduced magnitude at a frequency below 250 kHz. This is the aliasing effect of sampling at frequencies less than two times the signal frequency (the Nyquist frequency). At the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

8.1.2 Isolation Mode Voltage Induced Errors

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250 kHz, the output also will display spurious outputs (aliasing) in a manner similar to that for V_{IN} > 250 kHz and the amplifier response will be identical to that shown in Figure 9.This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in Figure 11 and compute the amplifier response to this input-referred error signal from the data shown in Figure 9. For example, if a 800-kHz 1000-Vrms IMR is present, then a total of [(–60 dB) + (–30 dB)] x (1000 V) = 32-mV error signal at 200 kHz plus a 1-V, 800-kHz error signal will be present at the output.

8.1.3 High IMV dV/dt Errors

As the IMV frequency increases and the dV/dt exceeds 1000 Vμs, the sense amp may start to false trigger, and the output will display spurious errors. The common-mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power-supply voltages below ±15 V may decrease the dV/dt to 500 V/M s for typical performance.

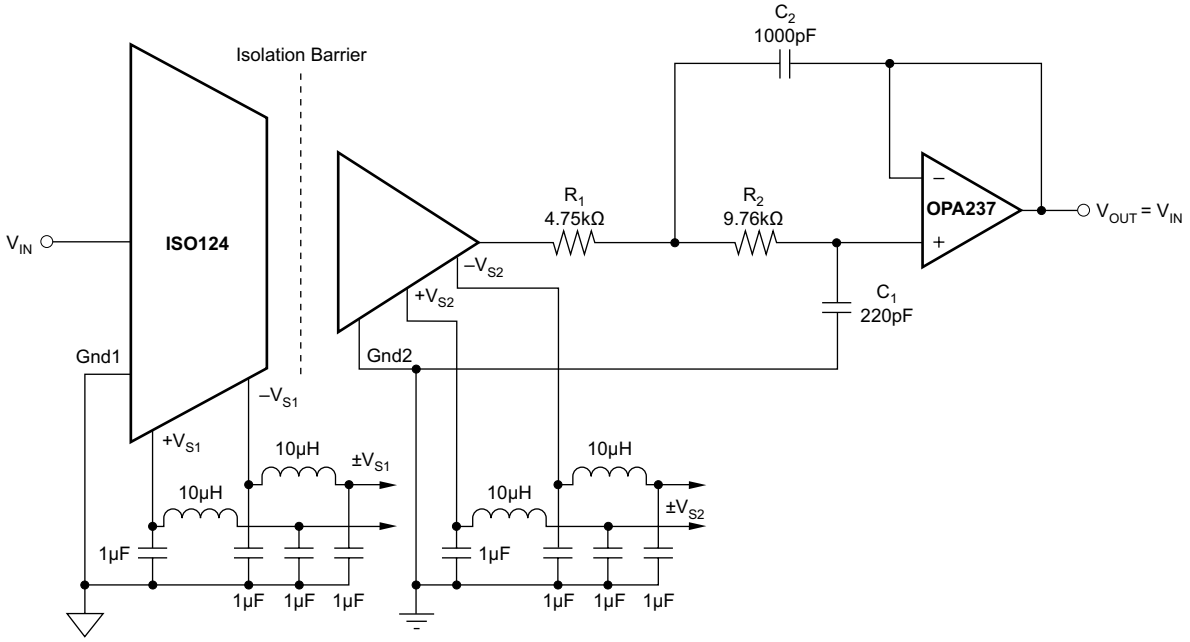
8.1.4 High Voltage Testing

TI has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (< 5 pC) while applying 2400-Vrms, 60-Hz high-voltage stress across every ISO124 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 × 1500 Vrms) protection without damage to the ISO124. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the art" for nondestructive high-voltage reliability testing. It is based on the effects of nonuniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void nonuniformities, electric field stress begins to ionize the void region before bridging the entire high-voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01–0.1-μs current pulses that repeat on each ac voltage cycle. The minimum ac barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." The package insulation processes have been characterized and developed to yield an inception voltage in excess of 2400 Vrms so that transient overvoltages below this level will not damage the ISO124. The extinction voltage is above 1500 Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500-Vrms (rated) level. Older high-voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

8.2 Typical Applications

8.2.1 Output Filters



For more information concerning output filters, see *Simple Output Filter Elminiates ISO Amp Output Ripple and Keeps Full Bandwidth* and *FilterPro™ MFB and Sallen-Key Low-Pass Filter Design Program User Guide*.

Figure 10. ISO124 With Output Filter for Improved Ripple

8.2.1.1 Design Requirements

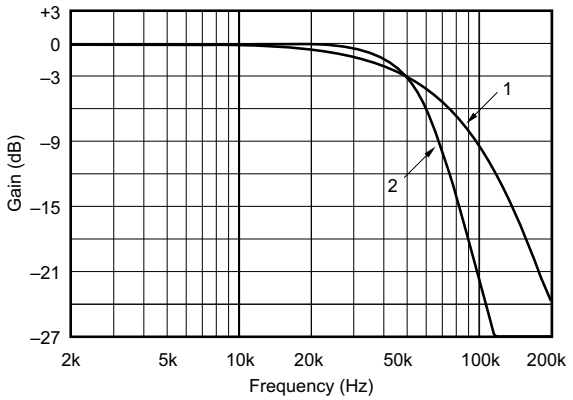
The ISO124 isolation amplifiers (ISO amps) have a small (10 to 20 mVp-p typical) residual demodulator ripple at the output. A simple filter can be added to eliminate the output ripple without decreasing the 50kHz signal bandwidth of the ISO amp.

8.2.1.2 Detailed Design Procedure

The ISO124 device is designed to have a 50-kHz single-pole (Butterworth) signal response. By cascading the ISO amp with a simple 50-kHz, Q = 1, two-pole, low-pass filter, the overall signal response becomes three-pole Butterworth. The result is a maximally flat 50-kHz magnitude response and the output ripple reduced below the noise level. Figure 10 shows the complete circuit. The two-pole filter is a unity-gain Sallen-Key type consisting of A1, R1, R2, C1, and C2. The values shown give Q = 1 and f–3dB bandwidth = 50 kHz. Because the op amp is connected as a unity-gain follower, gain and gain accuracy of the ISO amp are unaffected. Using a precision op amp such as the OPA602 also preserves the DC accuracy of the ISO amp.

Typical Applications (continued)

8.2.1.3 Application Curves



1) Standard ISO124 has 50kHz single-pole (Butterworth) response.

2) ISO124 with cascaded 50kHz, Q = 1, two-pole, low-pass filter has three-pole Butterworth response.

Figure 11. Gain vs. Frequency

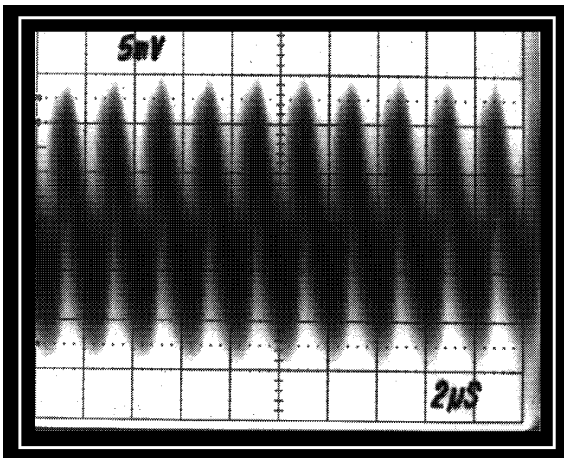


Figure 12. Standard ISO124 (Approximately 20-mVp-p Output Ripple)

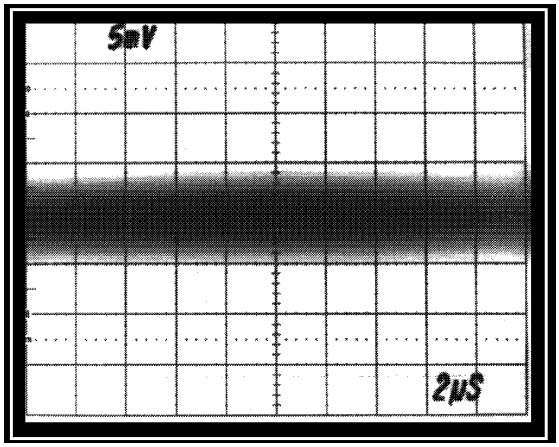


Figure 13. Filtered ISO124 (No Visible Output Ripple)

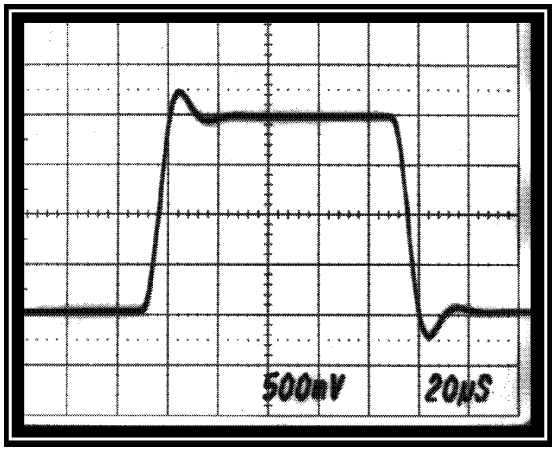


Figure 14. Step Response of Standard ISO124

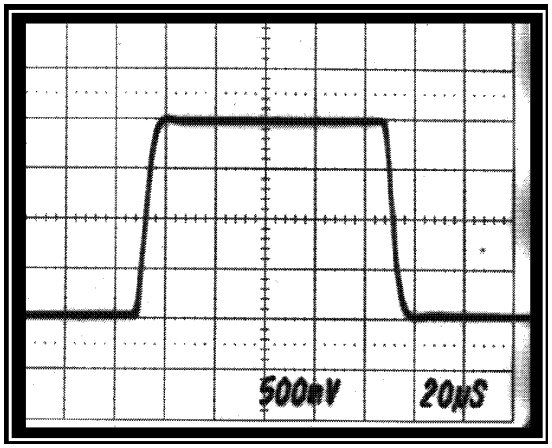


Figure 15. Step Response of ISO124 With Added Twopole Output Filter

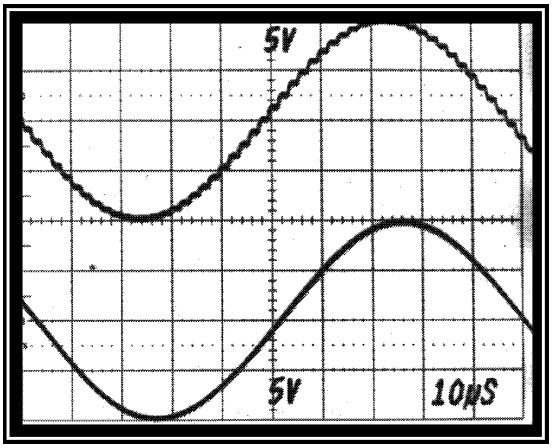
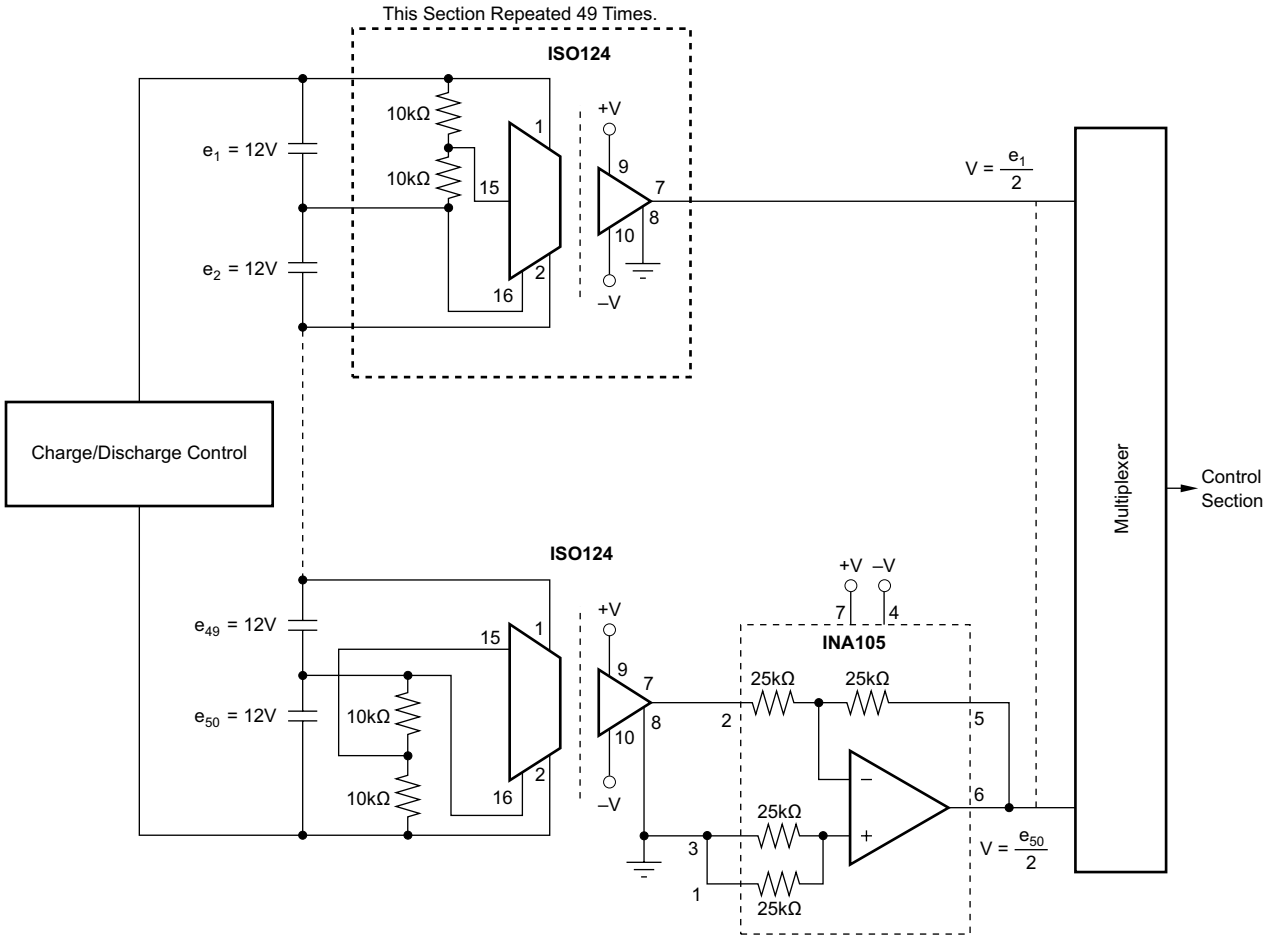


Figure 16. Large-signal, 10-kHz Sine-wave Response of ISO124 With and Without Output Filter

Typical Applications (continued)

8.2.2 Battery Monitor

Figure 17 provides a means to monitor the cell voltage on a 600-V battery stack by using the battery as a power source for the isolated voltage.



(Derives input power from the battery.)

Figure 17. Battery Monitor for a 600-V Battery Power System

Typical Applications (continued)

8.2.3 Programmable Gain Amplifier

In applications where variable gain configurations are required, a programmable gain amplifier like the PGA102 can be used with the ISO124 device. Figure 18 uses an ISO150 device to provide gain pin selection options to the PGA102 device.

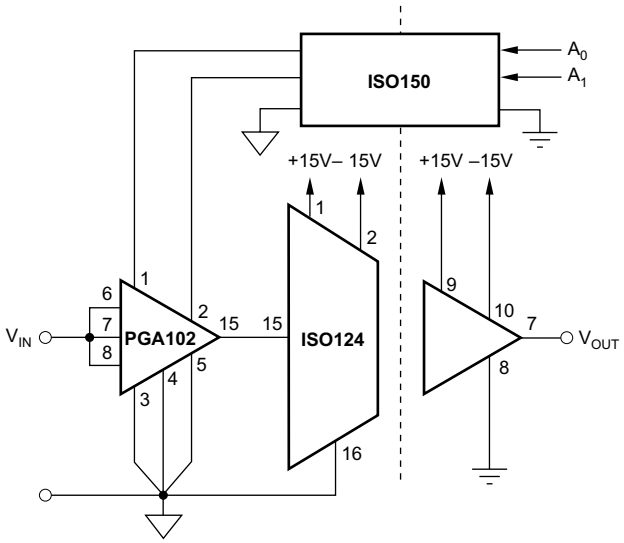
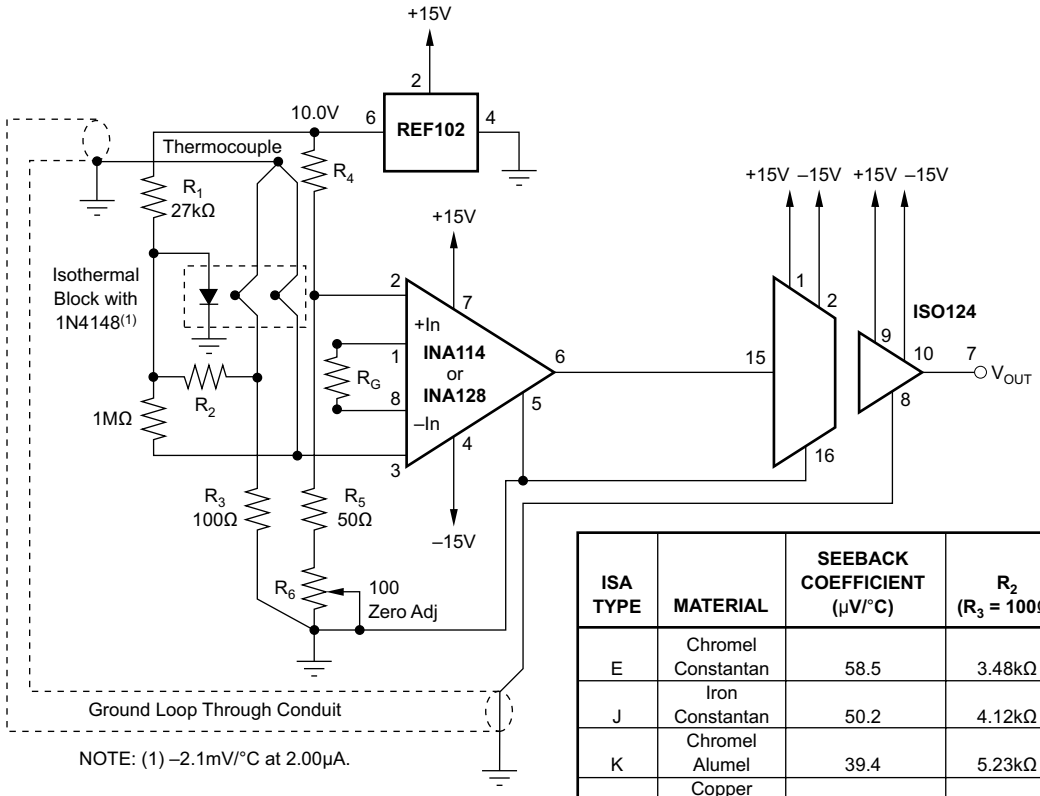


Figure 18. Programmable-Gain Isolation Channel With Gains of 1, 10, and 100

Typical Applications (continued)

8.2.4 Thermocouple Amplifier

For isolated temperature measurements, Figure 19 provides an application solution using the INA114 or INA128 devices, feeding the input stage of the ISO124 device. The table provides suggested resistor values based on the type of thermistor used in the application.



ISA TYPE	MATERIAL	SEEBACK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

Figure 19. Thermocouple Amplifier With Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out

Typical Applications (continued)

8.2.5 Isolated 4-mA to 20-mA Instrument Loop

For isolated temperature measurements in a 4-mA to 20-mA loop, Figure 20 provides a solution using the XTR101 and RCV420 devices. A high-performance PT100 resistance temperature detector (RTD) provides the user with an isolated 0-V to 5-V representation of the isolated temperature measurement.

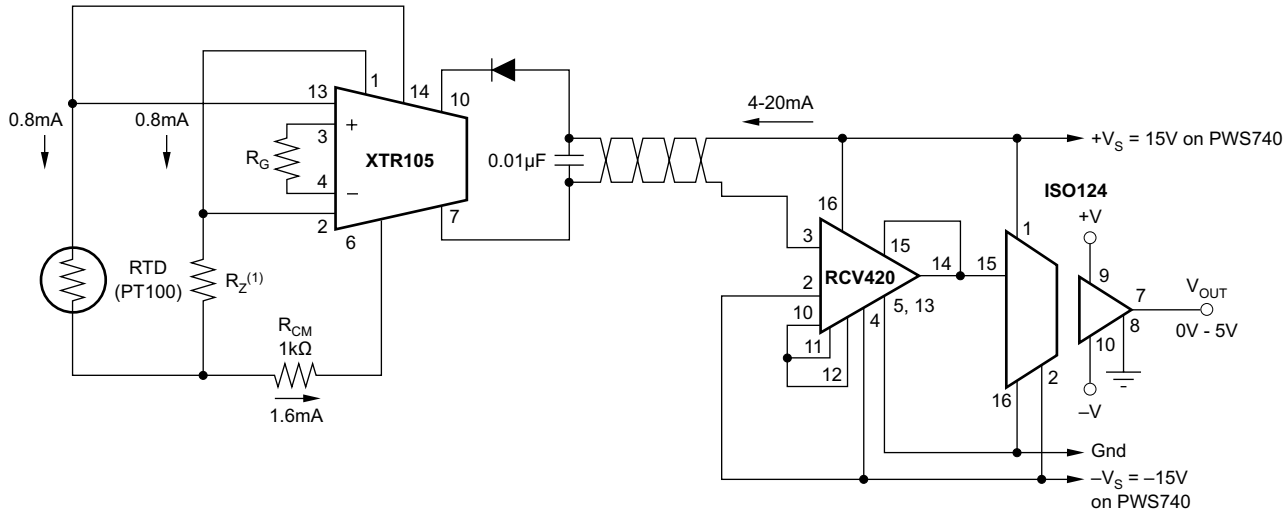
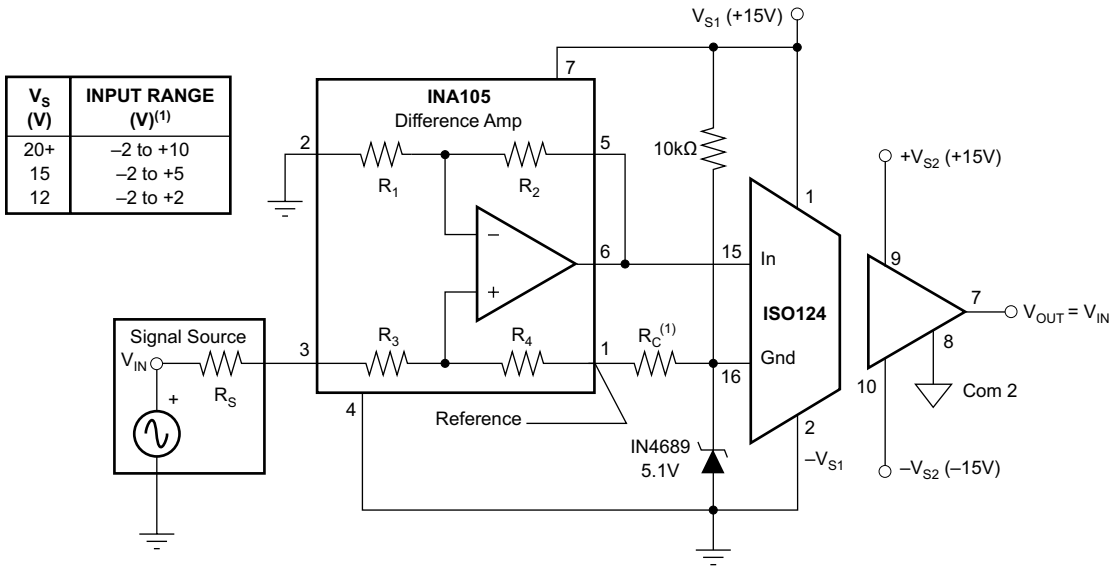


Figure 20. Isolated 4- to 20-mA Instrument Loop (RTD Shown)

8.2.6 Single-Supply Operation of the ISO124 Isolation Amplifier

The circuit shown in Figure 21 uses a 5.1-V Zener diode to generate the negative supply for an ISO12x from a single supply on the high-voltage side of the isolation amplifier. The input measuring range will be dependent on the applied voltage as noted in the accompanying table.

V_S (V)	INPUT RANGE (V)(1)
20+	–2 to +10
15	–2 to +5
12	–2 to +2



NOTE: Because the amplifier is unity gain, the input range is also the output range. The output can go to –2 V because the output section of the ISO amp operates from dual supplies.

For additional information see *Single-Supply Operation of Isolation Amplifiers*.

Figure 21. Single-Supply Operation of the ISO124 Isolation Amplifier Schematic

Typical Applications (continued)

8.2.7 Input-Side Powered ISO Amplifier

The user side of the ISO124 device can be powered from the high voltage side using an isolated DC-DC converter as shown in Figure 22.

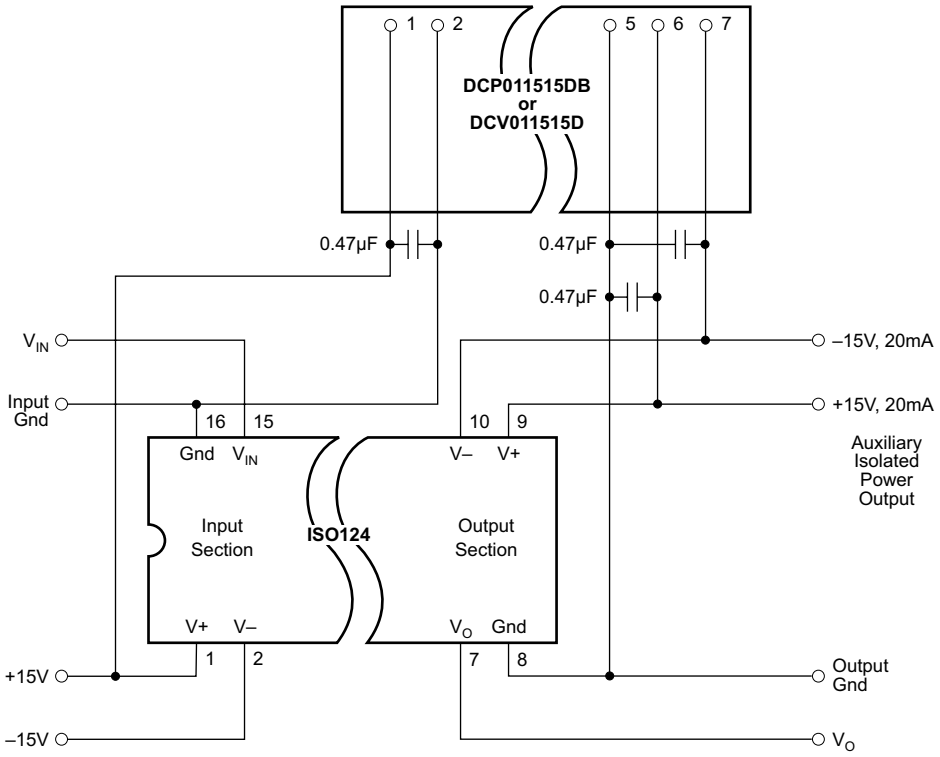


Figure 22. Input-Side Powered ISO Amplifier Schematic

Typical Applications (continued)

8.2.8 Powered ISO Amplifier With Three-Port Isolation

Figure 23 illustrates an application solution that provides isolated power to both the user and high-voltage sides of the ISO124 amplifier.

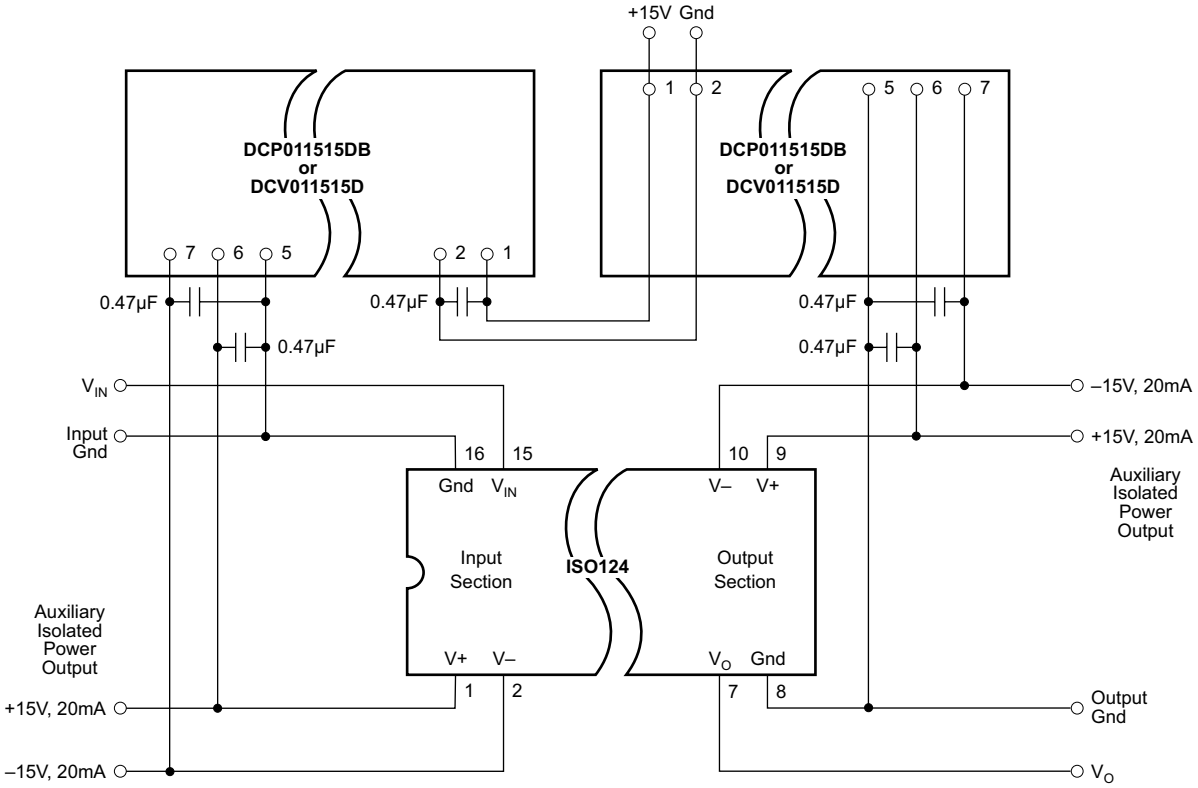


Figure 23. Powered ISO Amplifier With Three-Port Isolation Schematic

9 Power Supply Recommendations

9.1 Signal and Supply Connections

Each power-supply pin should be bypassed with 1-µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500 kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC-DC converter, use a π filter on the supplies (see Figure 10). The ISO124 output has a 500-kHz ripple of 20 mV, which can be removed with a simple 2-pole low-pass filter with a 100-kHz cutoff using a low-cost op amp (see Figure 10).

The input to the modulator is a current (set by the 200-kΩ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least ±15 V. It is therefore possible, when using an unregulated DC-DC converter, to minimize PSR related output errors with ±5-V voltage regulators on the isolated side and still get the full ±10-V input and output swing.

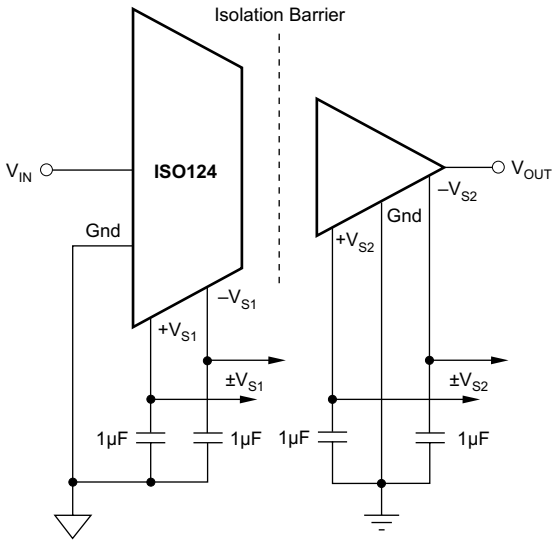


Figure 24. Basic Signal and Power Connections

10 Layout

10.1 Layout Guidelines

To maintain the isolation barrier of the device, the distance between the high-side ground (pin 16 or 28) and the low-side ground (pin 8 or 14) should be kept at maximum; that is, the entire area underneath the device should be kept free of any conducting materials.

10.2 Layout Example

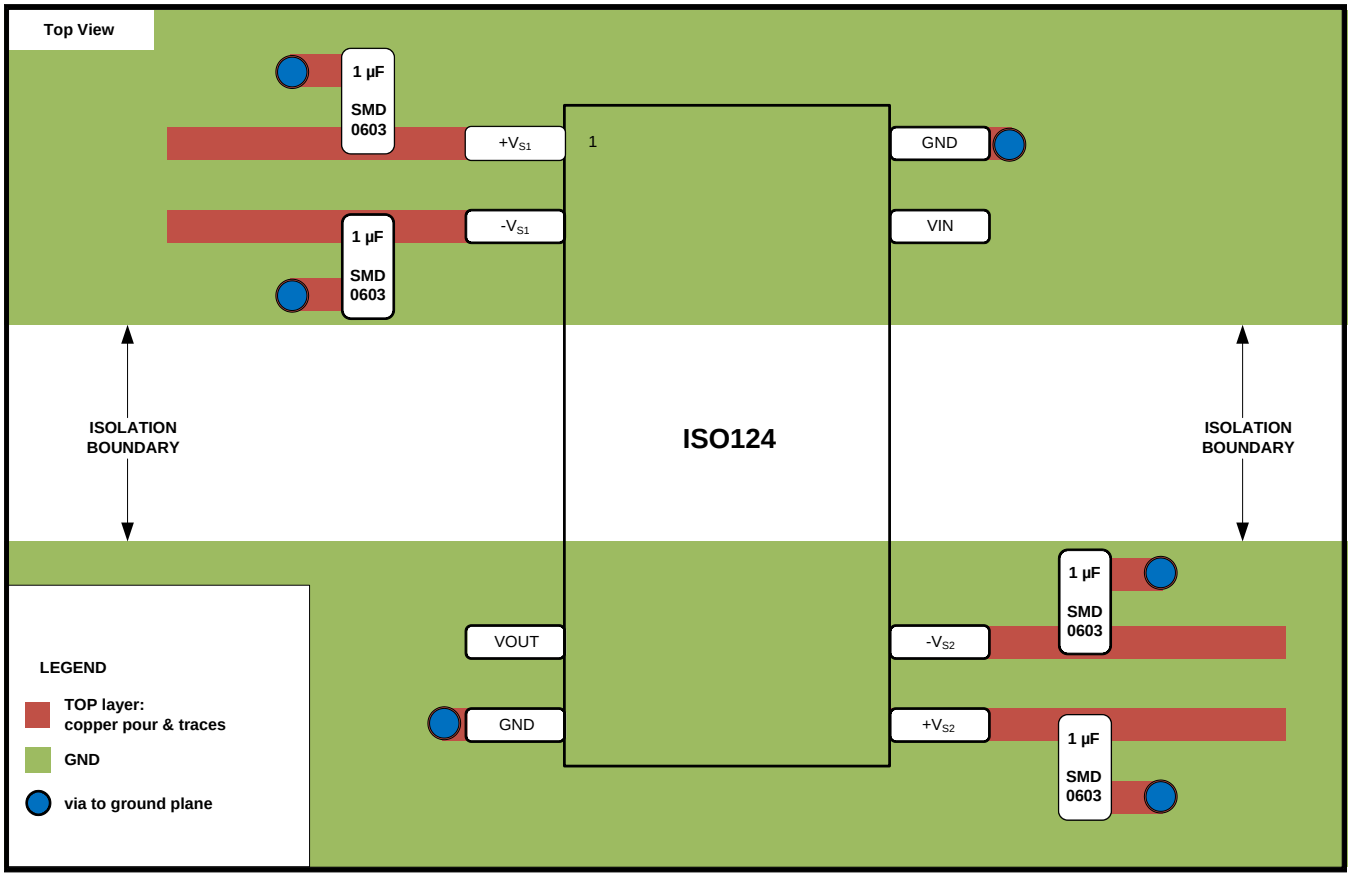


Figure 25. ISO124 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- *『絶縁アンプの単一電源動作』*
- *『単純な出力フィルタでISOアンプの出力リップルを除去し、全帯域幅を確保』*
- *『FilterPro™ユーザー・ガイド』*

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11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO124P	Active	Production	PDIP (NVF) | 8	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	ISO124P
ISO124P.A	Active	Production	PDIP (NVF) | 8	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	ISO124P
ISO124U	Active	Production	SOIC (DVA) | 8	20 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U
ISO124U.A	Active	Production	SOIC (DVA) | 8	20 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U
ISO124U/1K	Active	Production	SOIC (DVA) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U
ISO124U/1K.A	Active	Production	SOIC (DVA) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U
ISO124U/1KE4	Active	Production	SOIC (DVA) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U
ISO124UE4	Active	Production	SOIC (DVA) | 8	20 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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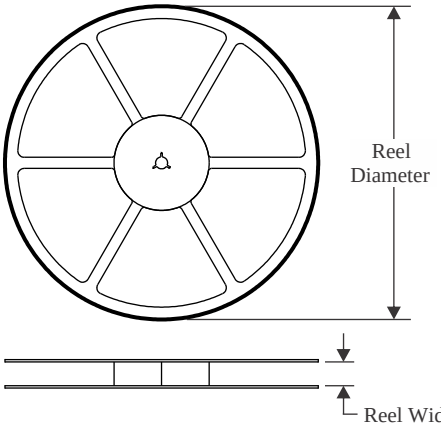
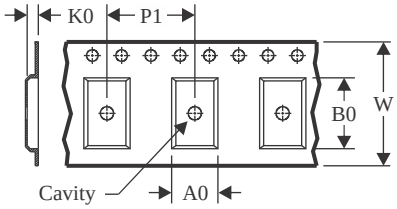
TAPE AND REEL INFORMATION

REEL DIMENSIONS

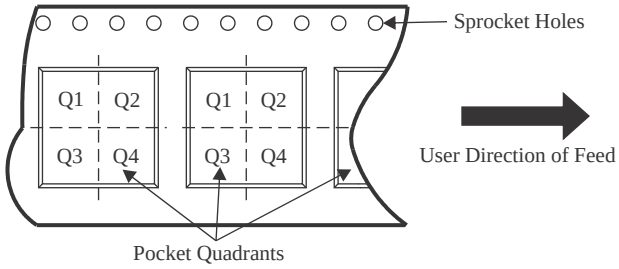


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

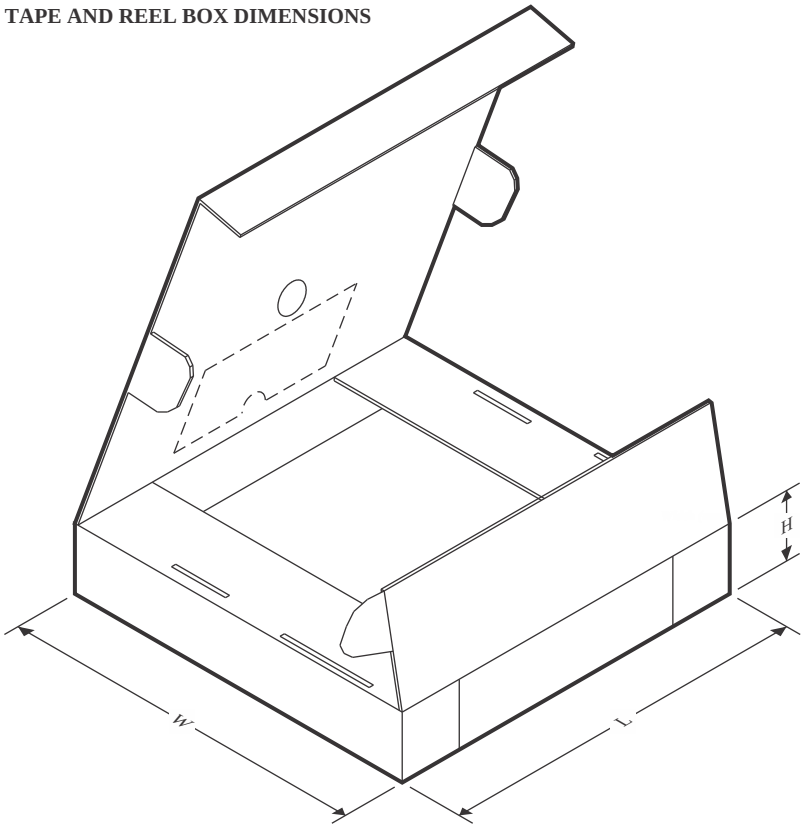
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO124U/1K	SOIC	DVA	8	1000	330.0	24.4	10.9	18.3	3.2	12.0	24.0	Q1

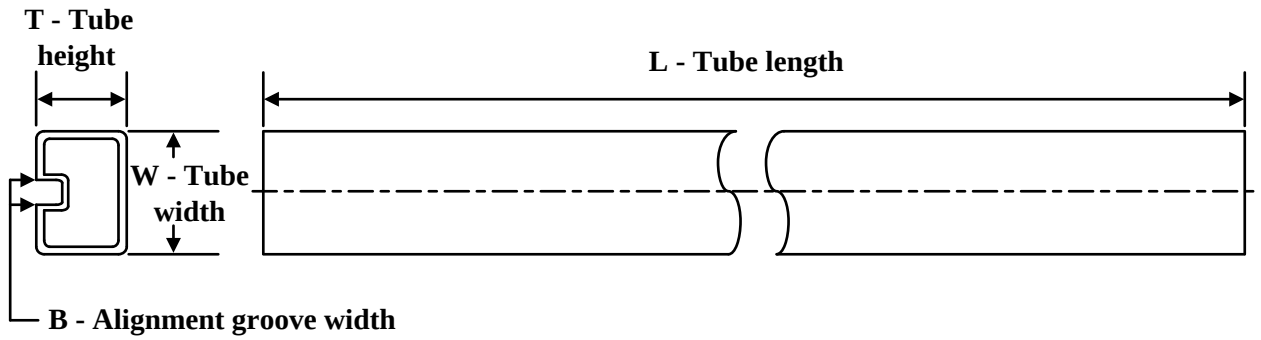
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO124U/1K	SOIC	DVA	8	1000	356.0	356.0	45.0

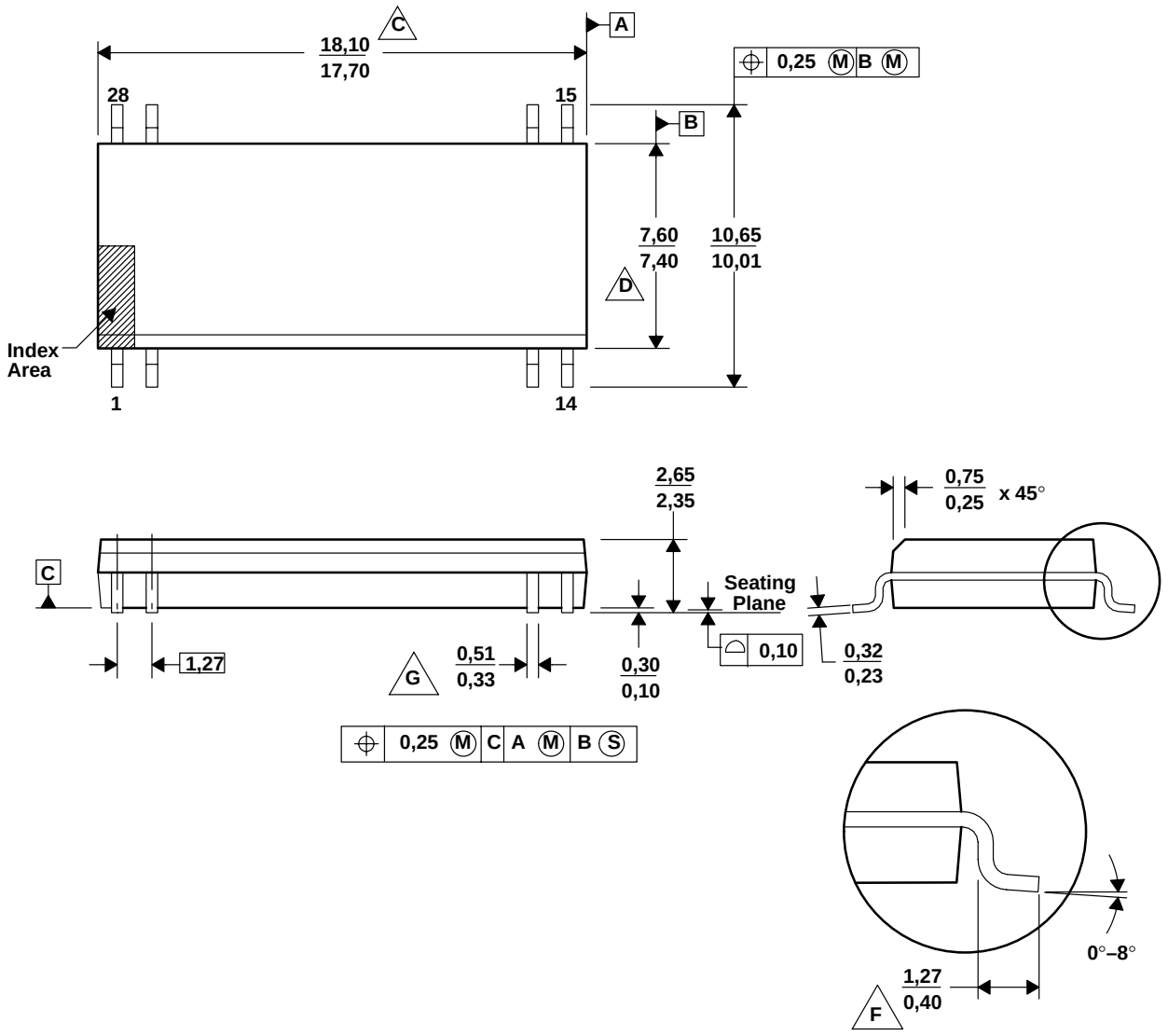
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO124P	NVF	PDIP	8	25	506	13.97	11230	4.32
ISO124P.A	NVF	PDIP	8	25	506	13.97	11230	4.32
ISO124U	DVA	SOIC	8	20	507	12.83	5080	6.6
ISO124U.A	DVA	SOIC	8	20	507	12.83	5080	6.6
ISO124UE4	DVA	SOIC	8	20	507	12.83	5080	6.6

DVA (R-PDSO-G8/28) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

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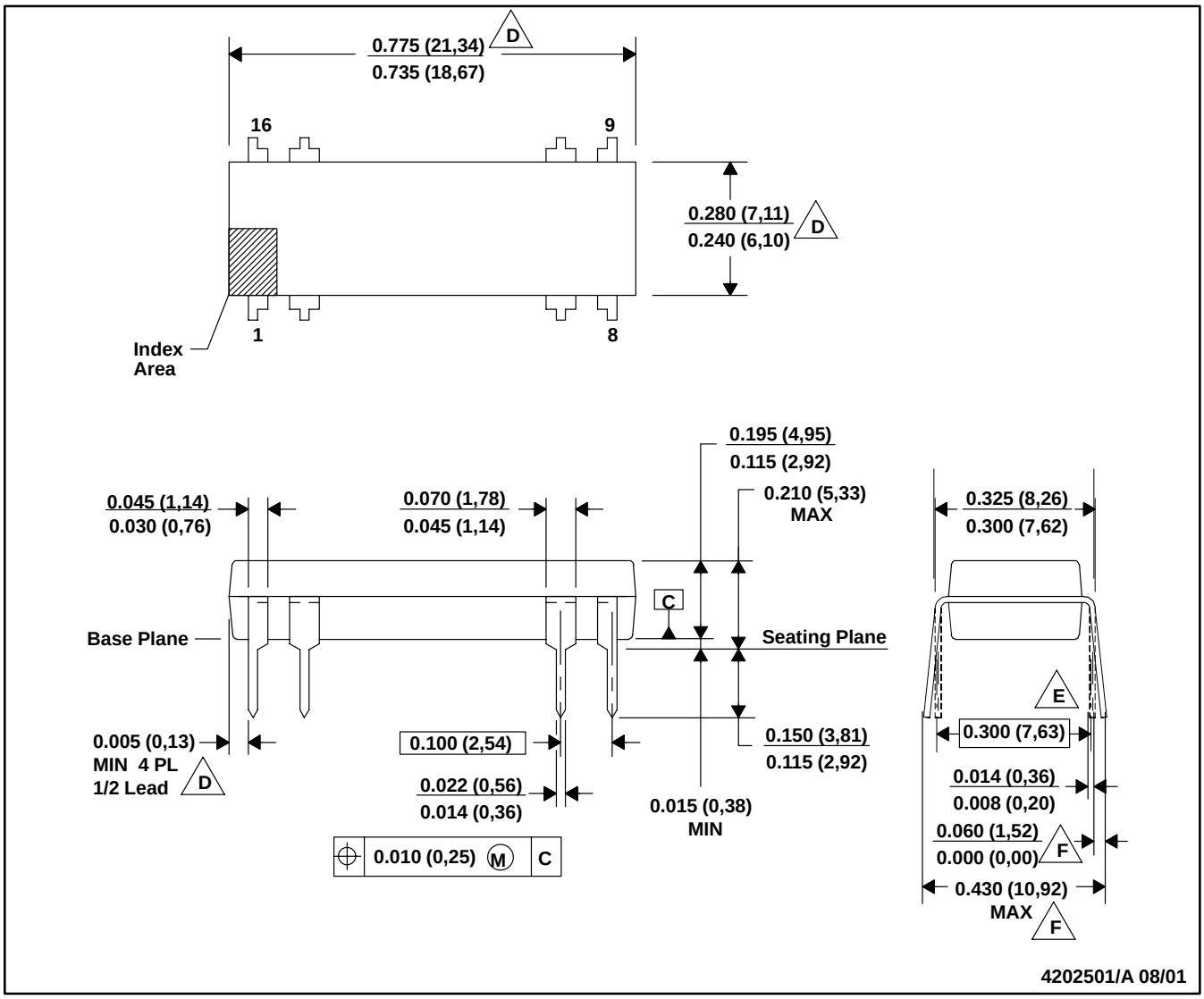
NVF (R-PDIP-T8/16) **PLASTIC DUAL-IN-LINE**



A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-BB with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

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