TEXAS INSTRUMENTS
ISO5852S-Q1
JAJSCI4 – SEPTEMBER 2016

# ISO5852S-Q1 分割出力とアクティブ安全機能を搭載した高CMTI 2.5Aおよび5A 強化絶縁IGBT、MOSFETゲート・ドライバ

## 1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～125°C
  - デバイスHBM分類レベル3A
  - デバイスCDM分類レベルC6
- $V_{CM}$ = 1500Vのとき、最小同相過渡耐性(CMTI) 100kV/µs
- 分割出力により2.5Aのピーク・ソースおよび5Aのピーク・シンク電流を供給
- 短い伝搬遅延: 76ns (標準値)、110ns (最大値)
- 2Aのアクティブ・ミラー・クランプ
- 出力短絡クランプ
- 短絡時のソフト電源オフ(STO)機能
- 不飽和化検出時のフォルト・アラームは$\overline{FLT}$により通知され、$\overline{RST}$によりリセット
- 入出力低電圧誤動作防止(UVLO)、レディ(RDY)ピンによる標示付き
- 低電源またはフローティング入力時のアクティブ出力プルダウンおよびデフォルトLOW出力
- 入力電源電圧: 2.25V～5.5V
- 出力ドライバ供給電圧: 15V～30V
- CMOS互換の入力
- 20ns未満の入力パルスと過渡ノイズを除去
- 絶縁サージ耐久電圧: 12800$V_{PK}$
- 安全関連の認定:
  - 8000$V_{PK}$ $V_{IOTM}$および2121$V_{PK}$ $V_{IORM}$の、DIN V VDE V 0884-10 (VDE V 0884-10):2006-12準拠の強化絶縁
  - UL1577準拠で5700$V_{RMS}$において1分間の絶縁
  - CSA Component Acceptance Notice 5A、IEC-60950-1、およびIEC 60601-1最終機器標準
  - EN 61010-1およびEN 60950-1準拠のTUV認定
  - GB4943.1-2011 CQC認定
  - UL、VDE、CQC、TUV準拠の認定は完了、CSAは計画中

## 2 アプリケーション

- 次のような用途の絶縁IGBTおよびMOSFETドライブ
  - HEVおよびEVの電源モジュール
  - 産業用モータ制御ドライブ
  - 産業用電源
  - ソーラー・インバータ
  - 誘導加熱

## 3 概要

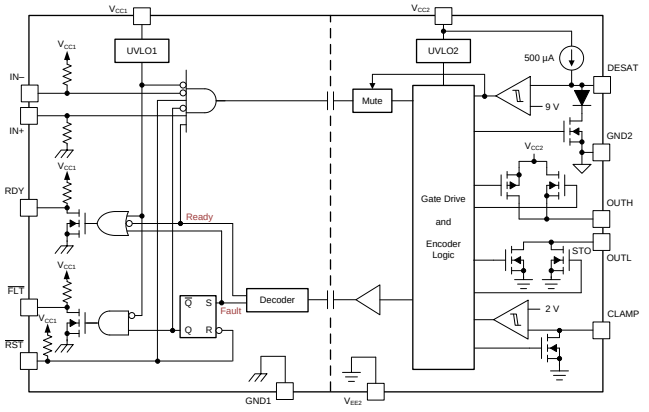
ISO5852S-Q1デバイスは、IGBTおよびMOSFET用の5.7$kV_{RMS}$強化絶縁ゲート・ドライバで、分割出力のOUTHとOUTLがあり、2.5Aのソース電流と5Aのシンク電流を供給できます。入力側は、単一の2.25V～5.5V電源で動作します。出力側は、最低15V、最高30Vの電源を供給できます。2つの相補CMOS入力により、ゲート・ドライバの出力状態が制御されます。伝搬時間が76nsと短いため、出力ステージを正確に制御できます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| ISO5852S-Q1 | SOIC (16) | 10.30mm×7.50mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**機能ブロック図**

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 日付 | 改訂内容 | 注 |
|---|---|---|
| 2016年9月 | * | 初版 |


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## 5 概要（続き）

内部不飽和化(DESAT)フォルト検出により、IGBTが過電流状況にあることが認識されます。DESATが検出されると、ミュート・ロジックによりアイソレータの出力がただちにブロックされ、ソフト電源オフ手順が開始されて、OUTHピンがディセーブルされ、OUTLピンが2µsの間LOWになります。OUTLピンが、負の方向に最も大きい供給電圧である$V_{EE2}$との比較で2Vに達すると、ゲート・ドライバ出力が$V_{EE2}$の電位に強制的に設定され、IGBTはただちにオフになります。

不飽和化がアクティブのとき、絶縁バリアを通してフォルト信号が送信され、入力側の$\overline{FLT}$出力がLOWになって、アイソレータ入力がブロックされます。ソフト電源オフ期間の間は、ミュート・ロジックがアクティブになります。$\overline{FLT}$出力状況はラッチされ、RDYピンがHIGHに移行した後でのみ、$\overline{RST}$入力のLOWアクティブ・パルスを使用してリセット可能です。

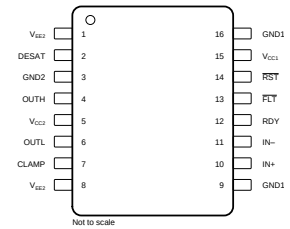
バイポーラ電源による通常動作時にIGBTがオフになると、出力は$V_{EE2}$にハード・クランプされます。出力電源がユニポーラの場合、アクティブなミラー・クランプを使用でき、低インピーダンスのパスを通してミラー電流をシンクできるため、高電圧の過渡状況でIGBTが動的にオンになることを防止できます。

ゲート・ドライバの動作準備は、入力側と出力側の電源を監視する2つの低電圧誤動作防止回路により制御されます。いずれかの側の電源が不十分な場合はRDY出力がLOWになり、そうでない場合はこの出力がHIGHになります。

ISO5852S-Q1デバイスは、16ピンのSOICパッケージで供給されます。デバイスの動作は、-40℃～+125℃の周囲温度範囲について規定されています。

## 6 Pin Configuration and Function

**DW Package**
**16-Pin SOIC**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CLAMP | 7 | O | Miller clamp output |
| DESAT | 2 | I | Desaturation voltage input |
| $\overline{FLT}$ | 13 | O | Fault output, active-low during DESAT condition |
| GND1 | 9 | — | Input ground |
| | 16 | | |
| GND2 | 3 | — | Gate drive common. Connect to IGBT emitter. |
| IN+ | 10 | I | Non-inverting gate drive voltage control input |
| IN– | 11 | I | Inverting gate drive voltage control input |
| OUTH | 4 | O | Positive gate drive voltage output |
| OUTL | 6 | O | Negative gate drive voltage output |
| RDY | 12 | O | Power-good output, active high when both supplies are good. |
| $\overline{RST}$ | 14 | I | Reset input, apply a low pulse to reset fault latch. |
| $V_{CC1}$ | 15 | — | Positive input supply (2.25-V to 5.5-V) |
| $V_{CC2}$ | 5 | — | Most positive output supply potential. |
| $V_{EE2}$ | 1 | — | Output negative supply. Connect to GND2 for unipolar supply application. |
| | 8 | | |

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# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC1}$ | Supply-voltage input side | | GND1 – 0.3 | 6 | V |
| $V_{CC2}$ | Positive supply-voltage output side | ($V_{CC2}$ – GND2) | –0.3 | 35 | V |
| $V_{EE2}$ | Negative supply-voltage output side | ($V_{EE2}$ – GND2) | –17.5 | 0.3 | V |
| $V_{(SUP2)}$ | Total-supply output voltage | ($V_{CC2}$ - $V_{EE2}$) | –0.3 | 35 | V |
| $V_{(OUTH)}$ | Positive gate-driver output voltage | | $V_{EE2}$ – 0.3 | $V_{CC2}$ + 0.3 | V |
| $V_{(OUTL)}$ | Negative gate-driver output voltage | | $V_{EE2}$ – 0.3 | $V_{CC2}$ + 0.3 | V |
| $I_{(OUTH)}$ | Gate-driver high output current | Maximum pulse width = 10 μs, Maximum duty cycle = 0.2%) | | 2.7 | A |
| $I_{(OUTL)}$ | Gate-driver low output current | Maximum pulse width = 10 μs, Maximum duty cycle = 0.2%) | | 5.5 | A |
| $V_{(LIP)}$ | Voltage at IN+, IN–,$\overline{FLT}$, RDY, $\overline{RST}$ | | GND1 – 0.3 | $V_{CC1}$ + 0.3 | V |
| $I_{(LOP)}$ | Output current of $\overline{FLT}$, RDY | | | 10 | mA |
| $V_{(DESAT)}$ | Voltage at DESAT | | GND2 – 0.3 | $V_{CC2}$ + 0.3 | V |
| $V_{(CLAMP)}$ | Clamp voltage | | $V_{EE2}$ – 0.3 | $V_{CC2}$ + 0.3 | V |
| $T_J$ | Junction temperature | | –40 | 150 | °C |
| $T_{STG}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC1}$ | Supply-voltage input side | 2.25 | | 5.5 | V |
| $V_{CC2}$ | Positive supply-voltage output side ($V_{CC2}$ – GND2) | 15 | | 30 | V |
| $V_{(EE2)}$ | Negative supply-voltage output side ($V_{EE2}$ – GND2) | –15 | | 0 | V |
| $V_{(SUP2)}$ | Total supply-voltage output side ($V_{CC2}$ – $V_{EE2}$) | 15 | | 30 | V |
| $V_{(IH)}$ | High-level input voltage (IN+, IN–, $\overline{RST}$) | 0.7 × $V_{CC1}$ | | $V_{CC1}$ | V |
| $V_{(IL)}$ | Low-level input voltage (IN+, IN–, $\overline{RST}$) | 0 | | 0.3 × $V_{CC1}$ | V |
| $t_{UI}$ | Pulse width at IN+, IN– for full output ($C_{LOAD}$ = 1 nF) | 40 | | | ns |
| $t_{RST}$ | Pulse width at $\overline{RST}$ for resetting fault latch | 800 | | | ns |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |


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## 7.4 Thermal Information

| THERMAL METRIC(1) | | ISO5852S-Q1 DW (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 99.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 29.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Power Ratings

Full-chip power dissipation is derated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that the junction temperature does not exceed 150°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = 5.5-V, $V_{CC2}$ = 30-V, $T_A$ = 25°C | | | 1255 | mW |
| $P_{ID}$ | Maximum input power dissipation | $V_{CC1}$ = 5.5-V, $V_{CC2}$ = 30-V, $T_A$ = 25°C | | | 175 | mW |
| $P_{OD}$ | Maximum output power dissipation | $V_{CC1}$ = 5.5-V, $V_{CC2}$ = 30-V, $T_A$ = 25°C | | | 1080 | mW |

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## 7.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| **GENERAL** | | | | |
| CLR | External clearance(1) | Shortest terminal-to-terminal distance through air | 8 | mm |
| CPG | External creepage(1) | Shortest terminal-to-terminal distance across the package surface | 8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | 21 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112; Material Group I according to IEC 60664-1; UL 746A | >600 | V |
| | Material group | | I | |
| | Overvoltage Category | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-III | |
| **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(2)** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 2121 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test, see Figure 1 | 1500 | $V_{RMS}$ |
| | | DC voltage | 2121 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$; t = 60 s (qualification); t = 1 s (100% production) | 8000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification) | 8000 | |
| $q_{pd}$ | Apparent charge(4) | Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, $t_m$ = 10 s | ≤5 | pC |
| | | Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, $t_m$ = 10 s | ≤5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$, $t_m$ = 10 s | ≤5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.4 sin (2πft), f = 1 MHz | 1 | pF |
| $R_{IO}$ | Isolation resistance, input to output(5) | $V_{IO}$ = 500 V, $T_A$ = 25°C | $> 10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | $> 10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | $> 10^{9}$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 s (100% production) | 5700 | VRMS |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device


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## 7.7 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 99.6°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 2 | | | 456 | mA |
| | | $R_{\theta JA}$ = 99.6°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 2 | | | 346 | |
| | | $R_{\theta JA}$ = 99.6°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 2 | | | 228 | |
| | | $R_{\theta JA}$ = 99.6°C/W, $V_I$ = 15 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 2 | | | 84 | |
| | | $R_{\theta JA}$ = 99.6°C/W, $V_I$ = 30 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 2 | | | 42 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 99.6°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 3 | | | 255 (1) | mW |
| $T_S$ | Maximum ambient safety temperature | | | | 150 | °C |

(1) Input, output, or the sum of input and output power should not exceed this value

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## 7.8 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV |
|---|---|---|---|---|
| Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07 | Plan to certify under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB4943.1-2011 | Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 |
| Reinforced Insulation Maximum Transient isolation voltage, 8000 $V_{PK}$; Maximum surge isolation voltage, 8000 $V_{PK}$, Maximum repetitive peak isolation voltage, 2121 $V_{PK}$ | Isolation Rating of 5700 $V_{RMS}$; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 (2nd Ed.), 800 $V_{RMS}$ max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 $V_{RMS}$ (354 $V_{PK}$) max working voltage | Single Protection, 5700 $V_{RMS}$ (1) | Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 $V_{RMS}$ maximum working voltage | 5700 $V_{RMS}$ Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 $V_{RMS}$ 5700 $V_{RMS}$ Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 $V_{RMS}$ |
| Certification completed Certificate number: 40040142 | Certificate planned | Certification completed File number: E181974 | Certification completed Certificate number: CQC16001141761 | Certification completed Client ID number: 77311 |

(1) Production tested ≥ 6840 VRMS for 1 second in accordance with UL 1577.

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## 7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A$ = 25°C, $V_{CC1}$ = 5 V, $V_{CC2}$ – GND2 = 15 V, GND2 – $V_{EE2}$ = 8 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VOLTAGE SUPPLY** | | | | | | |
| $V_{IT+(UVLO1)}$ | Positive-going UVLO1 threshold-voltage input side ($V_{CC1}$ – GND1) | | | | 2.25 | V |
| $V_{IT-(UVLO1)}$ | Negative-going UVLO1 threshold-voltage input side ($V_{CC1}$ – GND1) | | 1.7 | | | V |
| $V_{HYS(UVLO1)}$ | UVLO1 Hysteresis voltage ($V_{IT+}$ – $V_{IT–}$) input side | | | 0.2 | | V |
| $V_{IT+(UVLO2)}$ | Positive-going UVLO2 threshold-voltage output side ($V_{CC2}$ – GND2) | | | 12 | 13 | V |
| $V_{IT–(UVLO2)}$ | Negative-going UVLO2 threshold-voltage output side ($V_{CC2}$ – GND2) | | 9.5 | 11 | | V |
| $V_{HYS(UVLO2)}$ | UVLO2 hysteresis voltage ($V_{IT+}$ – $V_{IT–}$) output side | | | 1 | | V |
| $I_{Q1}$ | Input-supply quiescent current | | | 2.8 | 4.5 | mA |
| $I_{Q2}$ | Output-supply quiescent current | | | 3.6 | 6 | mA |
| **LOGIC I/O** | | | | | | |
| $V_{IT+(IN,\overline{RST})}$ | Positive-going input-threshold voltage (IN+, IN–, $\overline{RST}$) | | | | 0.7 × $V_{CC1}$ | V |
| $V_{IT–(IN,\overline{RST})}$ | Negative-going input-threshold voltage (IN+, IN–, $\overline{RST}$) | | 0.3 × $V_{CC1}$ | | | V |
| $V_{HYS(IN,\overline{RST})}$ | Input hysteresis voltage (IN+, IN–, $\overline{RST}$) | | | 0.15 × $V_{CC1}$ | | V |
| $I_{IH}$ | High-level input leakage at (IN+) (1) | IN+ = $V_{CC1}$ | | 100 | | µA |
| $I_{IL}$ | Low-level input leakage at (IN–, $\overline{RST}$) (2) | IN– = GND1, $\overline{RST}$ = GND1 | | -100 | | µA |
| $I_{PU}$ | Pullup current of $\overline{FLT}$, RDY | $V_{(RDY)}$ = GND1, $V_{(FLT)}$ = GND1 | | 100 | | µA |
| $V_{(OL)}$ | Low-level output voltage at $\overline{FLT}$, RDY | $I_{(FLT)}$ = 5 mA | | | 0.2 | V |
| **GATE DRIVER STAGE** | | | | | | |
| $V_{(OUTPD)}$ | Active output pulldown voltage | $I_{(OUTH/L)}$ = 200 mA, $V_{CC2}$ = open | | | 2 | V |
| $V_{OUTH}$ | High-level output voltage | $I_{(OUTH)}$ = –20 mA | $V_{CC2}$ – 0.5 | $V_{CC2}$ – 0.24 | | V |
| $V_{OUTL}$ | Low-level output voltage | $I_{(OUTL)}$ = 20 mA | | $V_{EE2}$ + 13 | $V_{EE2}$ + 50 | mV |
| $I_{(OUTH)}$ | High-level output peak current | IN+ = high, IN– = low, $V_{(OUTH)}$ = $V_{CC2}$ - 15 V | 1.5 | 2.5 | | A |
| $I_{(OUTL)}$ | Low-level output peak current | IN+ = low, IN– = high, $V_{(OUTL)}$ = $V_{EE2}$ + 15 V | 3.4 | 5 | | A |
| $I_{(OLF)}$ | Low-level output current during fault condition | | | 130 | | mA |
| **ACTIVE MILLER CLAMP** | | | | | | |
| $V_{(CLP)}$ | Low-level clamp voltage | $I_{(CLP)}$ = 20 mA | | $V_{EE2}$ + 0.015 | $V_{EE2}$ + 0.08 | V |
| $I_{(CLP)}$ | Low-level clamp current | $V_{(CLAMP)}$ = $V_{EE2}$ + 2.5 V | 1.6 | 2.5 | 3.3 | A |
| $V_{(CLTH)}$ | Clamp threshold voltage | | 1.6 | 2.1 | 2.5 | V |
| **SHORT CIRCUIT CLAMPING** | | | | | | |
| $V_{(CLP-OUTH)}$ | Clamping voltage ($V_{OUTH}$ – $V_{CC2}$) | IN+ = high, IN– = low, $t_{CLP}$ = 10 µs, $I_{(OUTH)}$ = 500 mA | | 1.1 | 1.3 | V |
| $V_{(CLP-OUTL)}$ | Clamping voltage ($V_{OUTL}$ – $V_{CC2}$) | IN+ = high, IN– = low, $t_{CLP}$ = 10 µs, $I_{(OUTL)}$ = 500 mA | | 1.3 | 1.5 | V |
| $V_{(CLP-CLP)}$ | Clamping voltage ($V_{CLP}$ – $V_{CC2}$) | IN+ = high, IN– = low, $t_{CLP}$ = 10 µs, $I_{(CLP)}$ = 500 mA | | 1.3 | | V |
| $V_{(CLP-CLAMP)}$ | Clamping voltage at CLAMP | IN+ = High, IN– = Low, $I_{(CLP)}$ = 20 mA | | 0.7 | 1.1 | V |
| $V_{(CLP-OUTL)}$ | Clamping voltage at OUTL ($V_{CLP}$ – $V_{CC2}$) | IN+ = High, IN– = Low, $I_{(OUTL)}$ = 20 mA | | 0.7 | 1.1 | V |
| **DESAT PROTECTION** | | | | | | |
| $I_{(CHG)}$ | Blanking-capacitor charge current | $V_{(DESAT)}$ – GND2 = 2 V | 0.42 | 0.5 | 0.58 | mA |
| $I_{(DCHG)}$ | Blanking-capacitor discharge current | $V_{(DESAT)}$ – GND2 = 6 V | 9 | 14 | | mA |

(1) $I_{IH}$ for IN–, $\overline{RST}$ pin is zero as they are pulled high internally
(2) $I_{IL}$ for IN+ is zero, as it is pulled low internally


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## Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A$ = 25°C, $V_{CC1}$ = 5 V, $V_{CC2}$ – GND2 = 15 V, GND2 – $V_{EE2}$ = 8 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(DSTH)}$ | DESAT threshold voltage with respect to GND2 | | 8.3 | 9 | 9.5 | V |
| $V_{(DSL)}$ | DESAT voltage with respect to GND2, when OUTH or OUTL is driven low | | 0.4 | | 1 | V |

## 7.10 Switching Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A$ = 25°C, $V_{CC1}$ = 5 V, $V_{CC2}$ – GND2 = 15 V, GND2 – $V_{EE2}$ = 8 V

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_r$ | Output-signal rise time at OUTH | $C_{LOAD}$ = 1 nF | See Figure 44, Figure 45, and Figure 46 | 12 | 18 | 35 | ns |
| $t_f$ | Output-signal fall time at OUTL | $C_{LOAD}$ = 1 nF | | 12 | 20 | 37 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay | $C_{LOAD}$ = 1 nF | | | 76 | 110 | ns |
| $t_{sk-p}$ | Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$ | $C_{LOAD}$ = 1 nF | | | | 20 | ns |
| $t_{sk-pp}$ | Part-to-part skew | $C_{LOAD}$ = 1 nF | | | | 30(1) | ns |
| $t_{GF\ (IN,/RST)}$ | Glitch filter on IN+, IN–, $\overline{RST}$ | $C_{LOAD}$ = 1 nF | | 20 | 30 | 40 | ns |
| $t_{DS\ (90\%)}$ | DESAT sense to 90% $V_{OUTH/L}$ delay | $C_{LOAD}$ = 10 nF | | | 553 | 760 | ns |
| $t_{DS\ (10\%)}$ | DESAT sense to 10% $V_{OUTH/L}$ delay | $C_{LOAD}$ = 10 nF | | | 2 | 3.5 | µs |
| $t_{DS\ (GF)}$ | DESAT-glitch filter delay | $C_{LOAD}$ = 1 nF | | | 330 | | ns |
| $t_{DS\ (\overline{FLT})}$ | DESAT sense to $\overline{FLT}$-low delay | See Figure 46 | | | | 1.4 | µs |
| $t_{LEB}$ | Leading-edge blanking time | See Figure 44 and Figure 45 | | 310 | 400 | 480 | ns |
| $t_{GF(RSTFLT)}$ | Glitch filter on $\overline{RST}$ for resetting $\overline{FLT}$ | | | 300 | | 800 | ns |
| $C_I$ | Input capacitance(2) | $V_I = V_{CC1} / 2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, $V_{CC1}$ = 5 V | | | 2 | | pF |
| CMTI | Common-mode transient immunity | $V_{CM}$ = 1500 V, see Figure 47 | | 100 | 120 | | kV/µs |

(1) Measured at same supply voltage and temperature condition
(2) Measured from input pin to ground.

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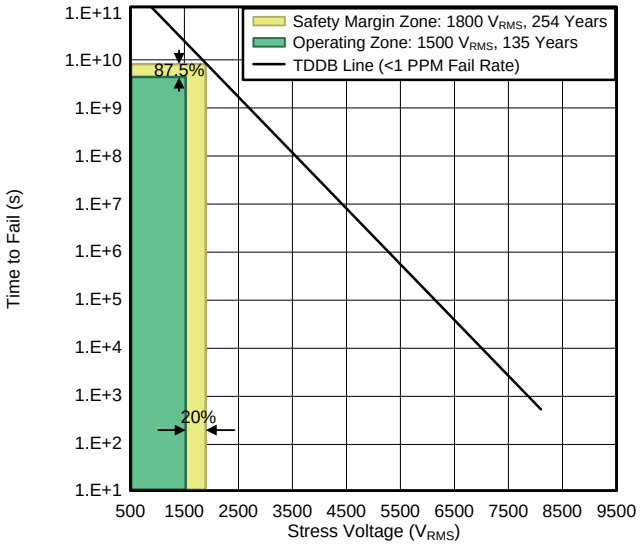
## 7.11 Safety and Insulation Characteristics Curves




$T_A$ upto 150°C Stress-voltage frequency = 60 Hz

**Figure 1. Reinforced High-Voltage Capacitor Lifetime Projection**

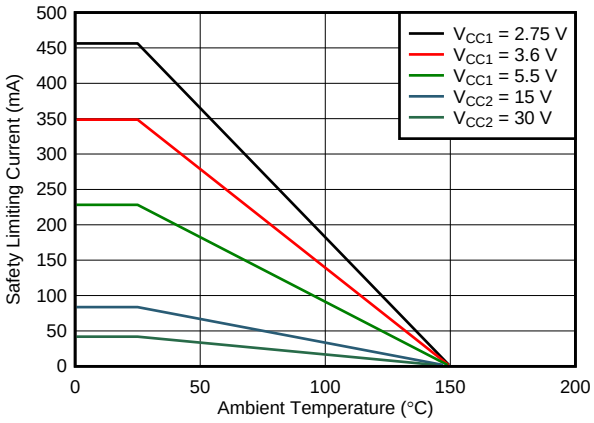



**Figure 2. Thermal Derating Curve for Safety Limiting Current per VDE**

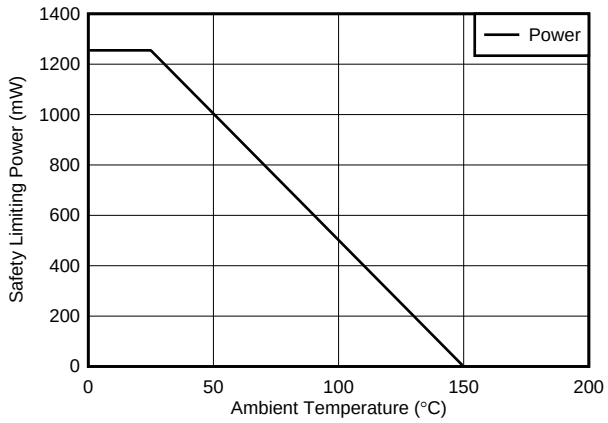



**Figure 3. Thermal Derating Curve for Safety Limiting Power per VDE**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## 7.12 Typical Characteristics

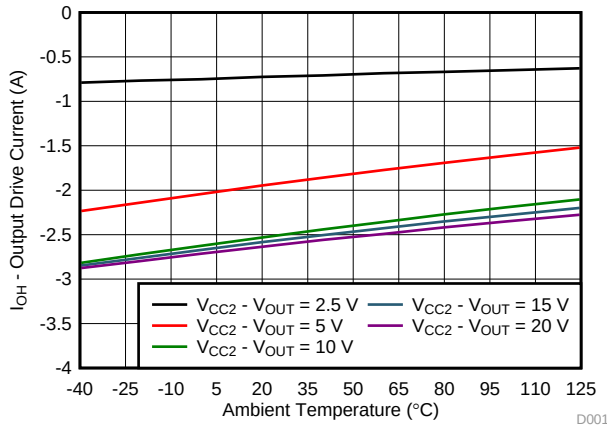



**Figure 4. Output High Drive Current vs Temperature**

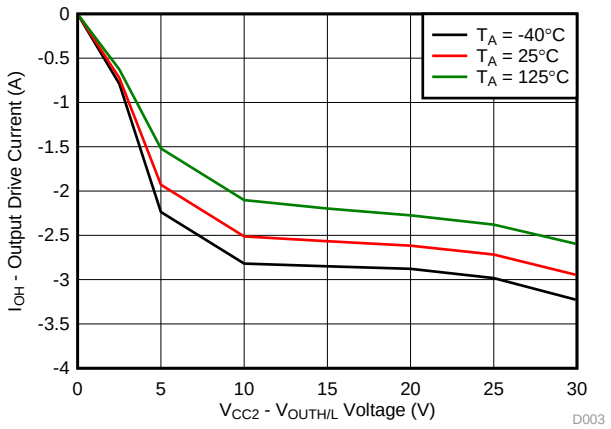



**Figure 5. Output High Drive Current vs Output Voltage**

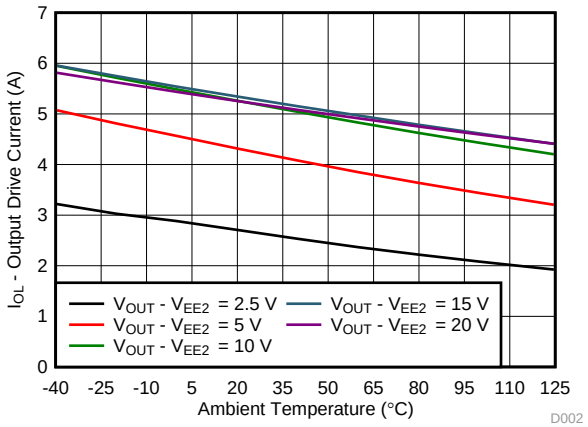



**Figure 6. Output Low Drive Current vs Temperature**

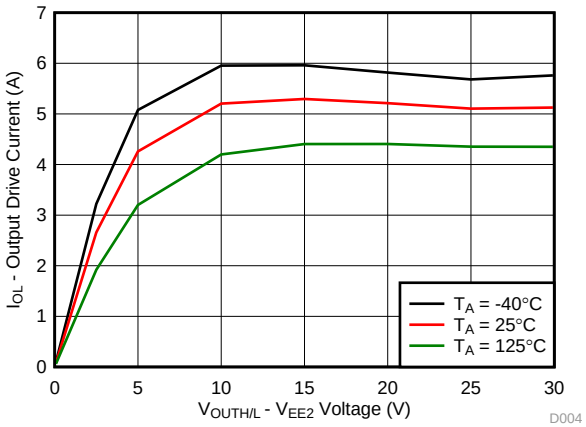
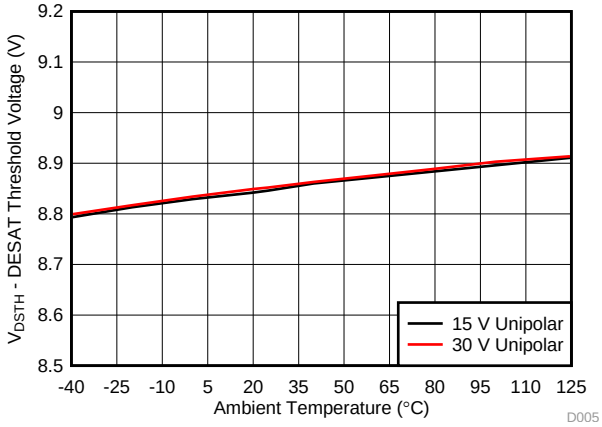


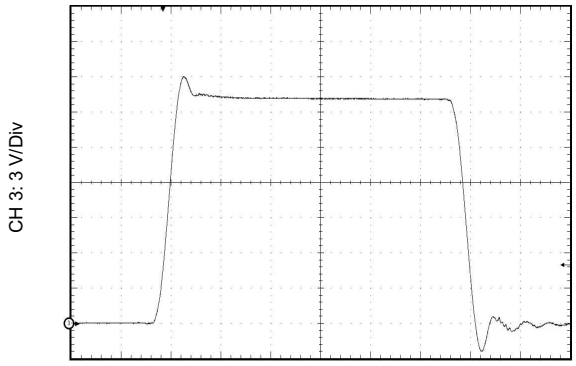

**Figure 7. Output Low Drive Current vs Output Voltage**




Unipolar: $V_{CC2} – V_{EE2} = V_{CC2} – GND2$

**Figure 8. DESAT Threshold Voltage vs Temperature**

## Typical Characteristics (continued)

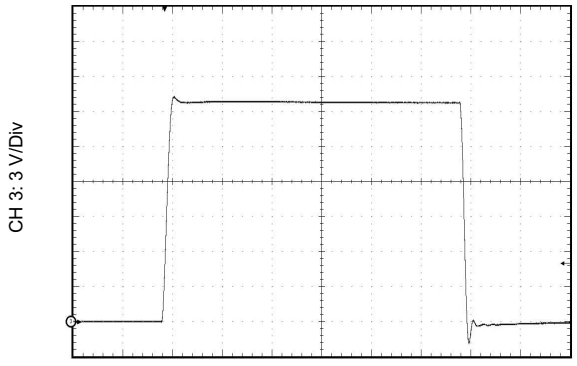



50 ns / Div

$C_L$ = 1 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω

$V_{CC2} – V_{EE2} = V_{CC2} – GND2 = 20$ V

**Figure 9. Output Transient Waveform**

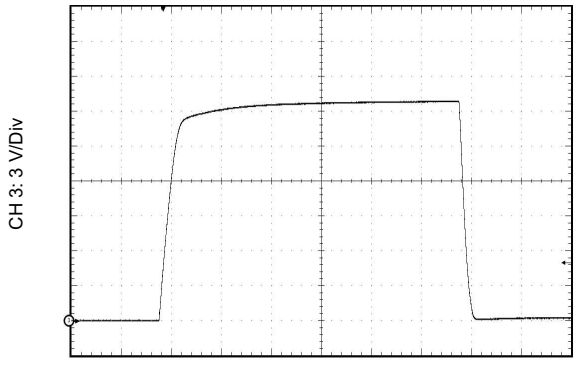



500 ns / Div

$C_L$ = 10 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω

$V_{CC2} – V_{EE2} = V_{CC2} – GND2 = 20$ V

**Figure 10. Output Transient Waveform**

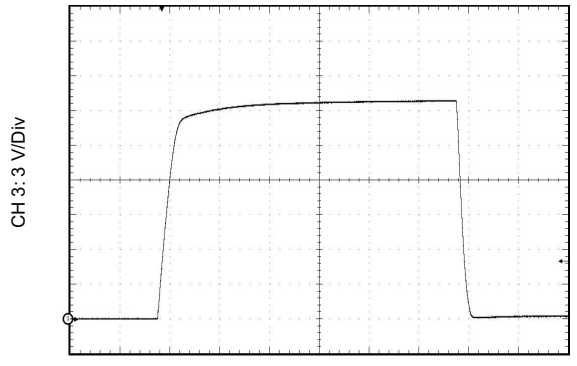



2 μs / Div

$C_L$ = 100 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω

$V_{CC2} – V_{EE2} = V_{CC2} – GND2 = 20$ V

**Figure 11. Output Transient Waveform**

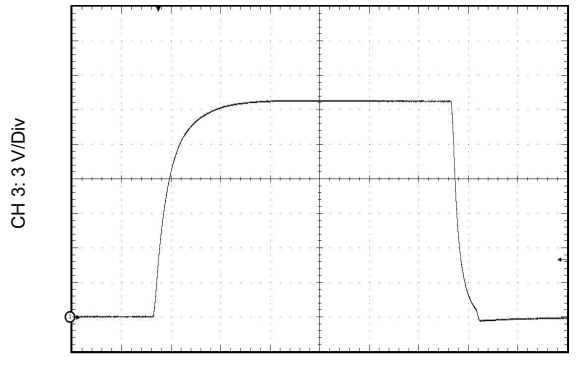



50 ns / Div

$C_L$ = 1 nF $R_{GH}$ = 10 Ω $R_{GL}$ = 5 Ω

$V_{CC2} – V_{EE2} = V_{CC2} – GND2 = 20$ V

**Figure 12. Output Transient Waveform**

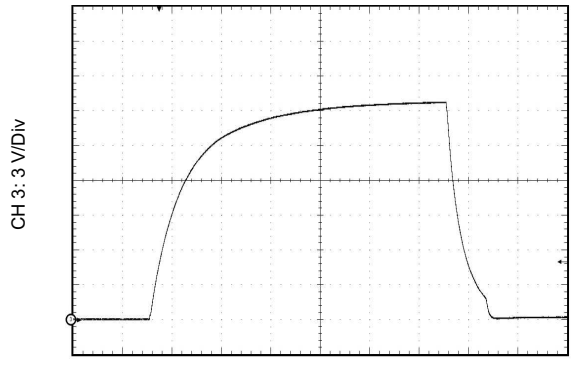



500 ns / Div

$C_L$ = 10 nF $R_{GH}$ = 10 Ω $R_{GL}$ = 5 Ω

$V_{CC2} – V_{EE2} = V_{CC2} – GND2 = 20$ V

**Figure 13. Output Transient Waveform**




2 μs / Div

$C_L$ = 100 nF $R_{GH}$ = 10 Ω $R_{GL}$ = 5 Ω

$V_{CC2} – V_{EE2} = V_{CC2} – GND2 = 20$ V

**Figure 14. Output Transient Waveform**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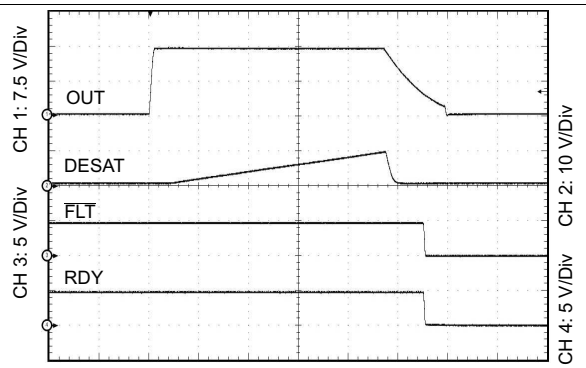
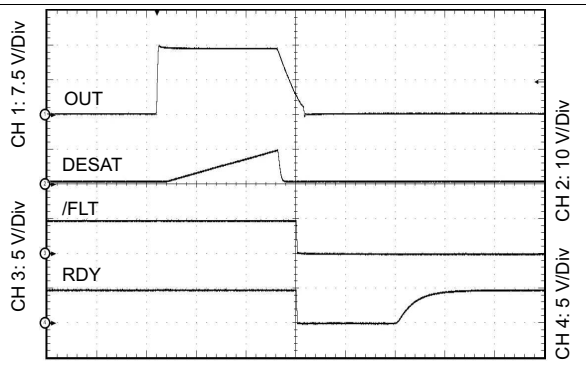
## Typical Characteristics (continued)




1 µs/Div

$C_L$ = 10 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2} – GND2$ = 15 V DESAT = 220 pF

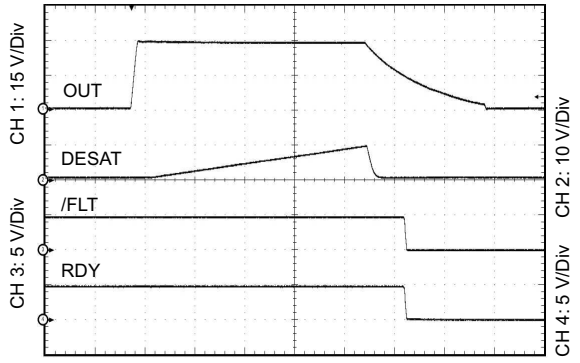
**Figure 15. Output Transient Waveform DESAT, RDY, and $\overline{FLT}$**




2 µs / Div

$C_L$ = 10 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2} – GND2$ = 15 V DESAT = 220 pF

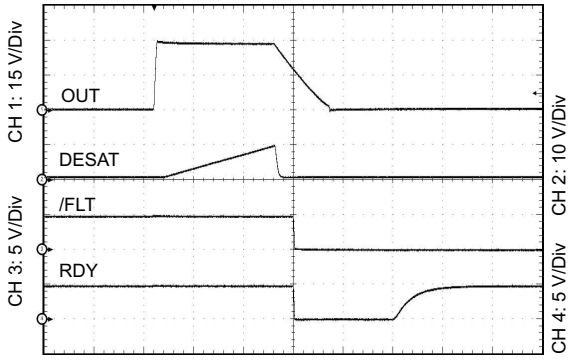
**Figure 16. Output Transient Waveform DESAT, RDY, and $\overline{FLT}$**




1 µs / Div

$C_L$ = 10 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2} – GND2$ = 30 V DESAT = 220 pF

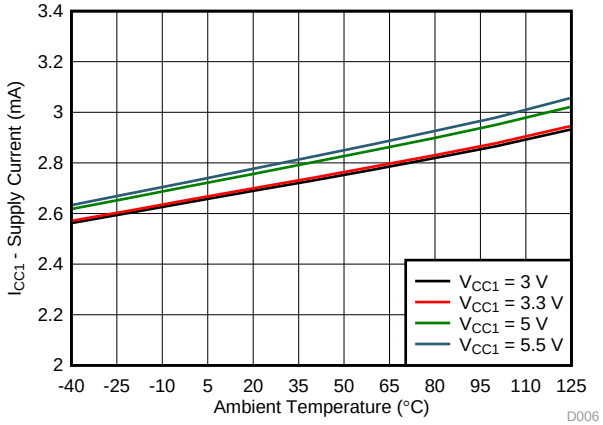
**Figure 17. Output Transient Waveform DESAT, RDY, and $\overline{FLT}$**




2 µs / Div

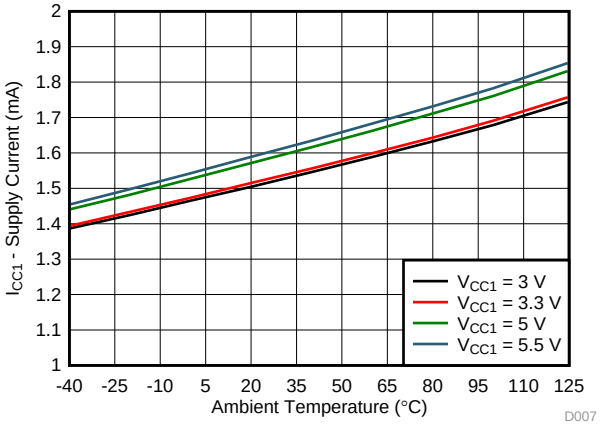
$C_L$ = 10 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω
$V_{CC2} – V_{EE2} = V_{CC2} – GND2$ = 30 V DESAT = 220 pF

**Figure 18. Output Transient Waveform DESAT, RDY, and $\overline{FLT}$**




IN+ = High IN– = Low

**Figure 19. $I_{CC1}$ Supply Current vs Temperature**




IN+ = Low IN– = Low

**Figure 20. $I_{CC1}$ Supply Current vs Temperature**

## Typical Characteristics (continued)

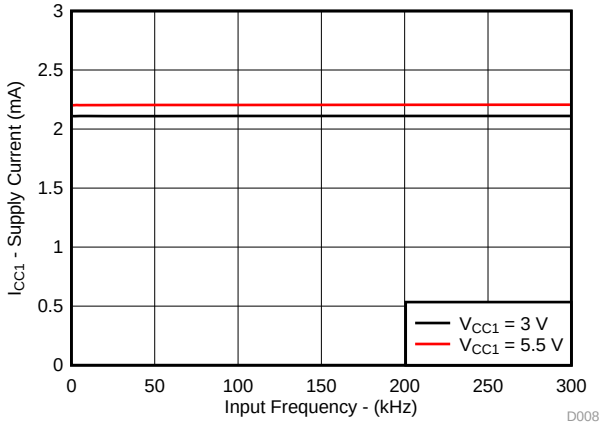
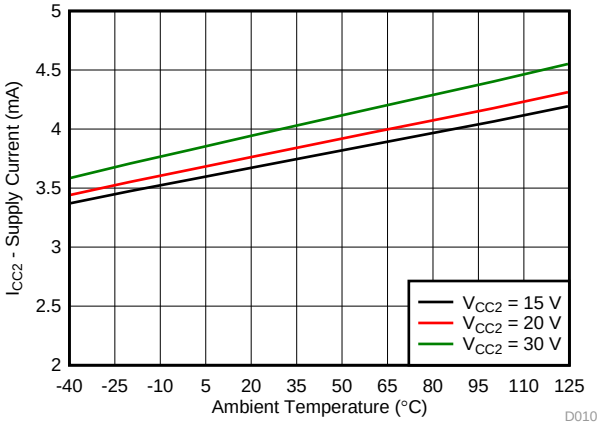
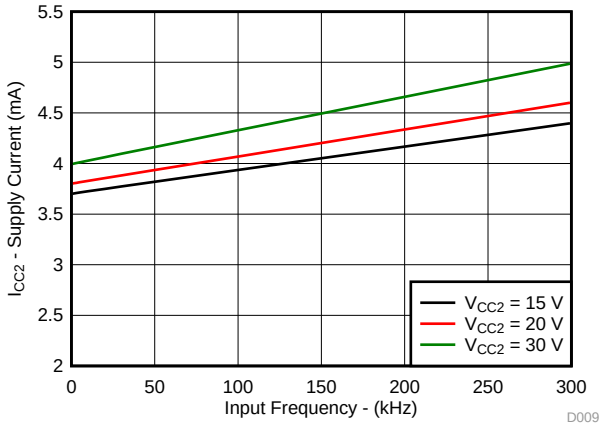



**Figure 21. $I_{CC1}$ Supply Current vs Input Frequency**



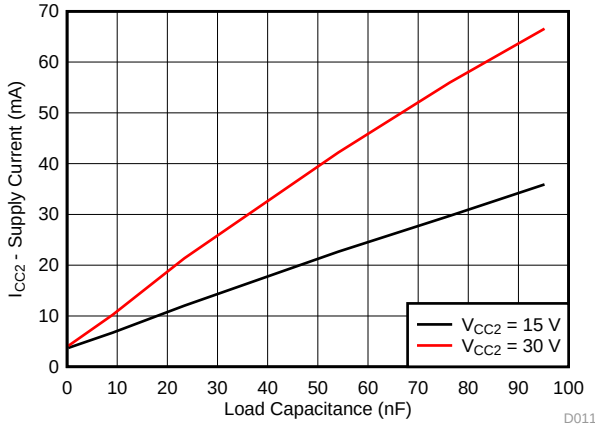

Input frequency = 1 kHz

**Figure 22. $I_{CC2}$ Supply Current vs Temperature**



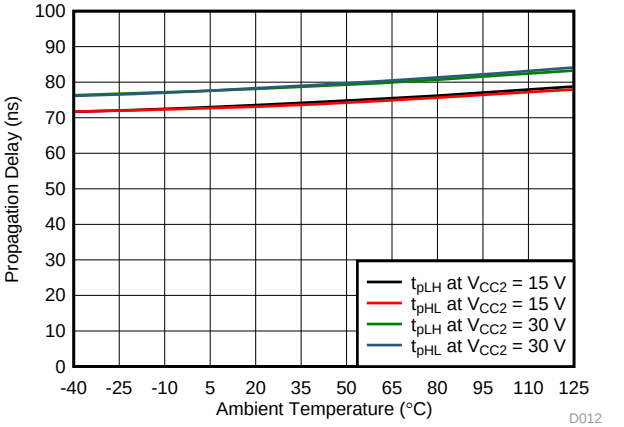

No $C_L$

**Figure 23. $I_{CC2}$ Supply Current vs Input Frequency**



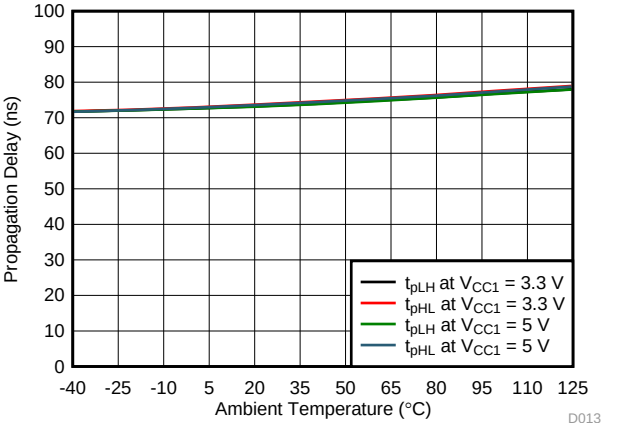

$R_{GH}$ = 10 Ω $R_{GL}$ = 5 Ω, 20 kHz

**Figure 24. $I_{CC2}$ Supply Current vs Load Capacitance**




$C_L$ = 1 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω
$V_{CC1}$ = 5 V

**Figure 25. Propagation Delay vs Temperature**




$C_L$ = 1 nF $R_{GH}$ = 0 Ω $R_{GL}$ = 0 Ω
$V_{CC2}$ = 15 V

**Figure 26. Propagation Delay vs Temperature**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## Typical Characteristics (continued)

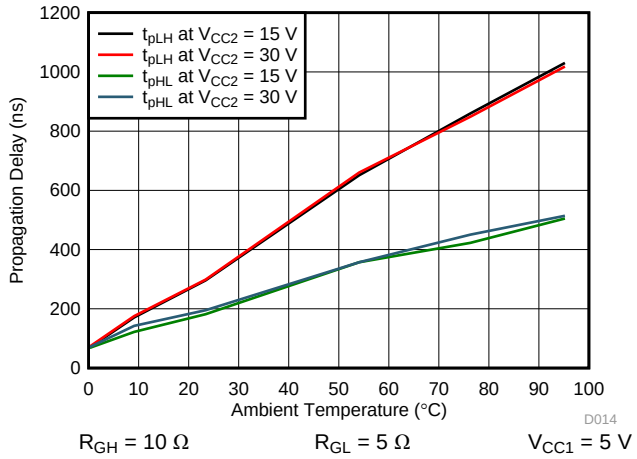


**Figure 27. Propagation Delay vs Load Capacitance**

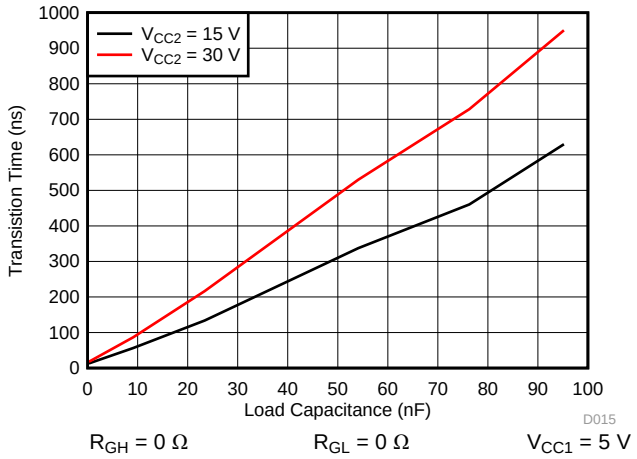


**Figure 28. $t_r$ Rise Time vs Load Capacitance**

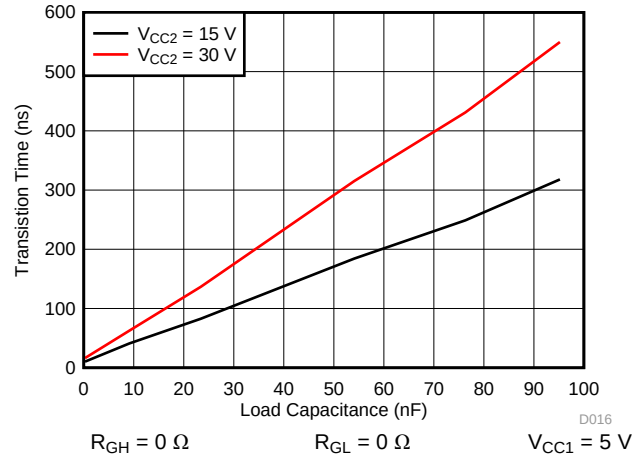


**Figure 29. $t_f$ Fall Time v. Load Capacitance**

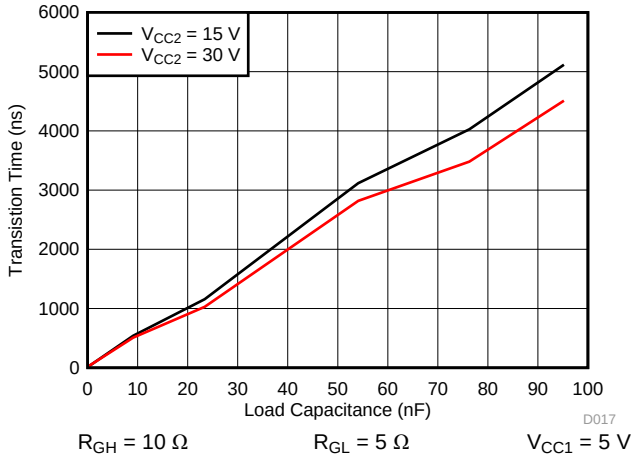


**Figure 30. $t_r$ Rise Time vs Load Capacitance**

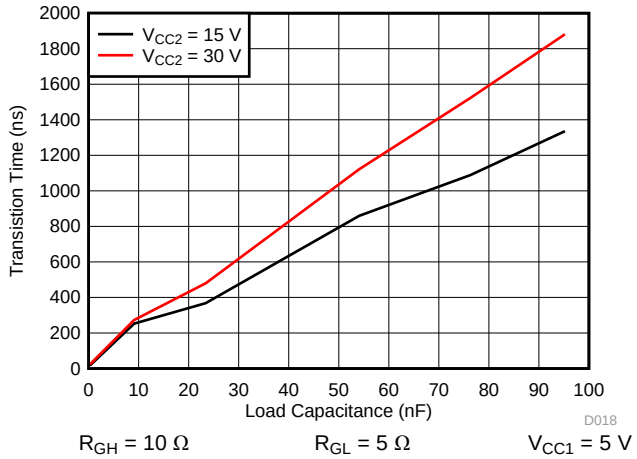


**Figure 31. $t_f$ Fall Time vs Load Capacitance**

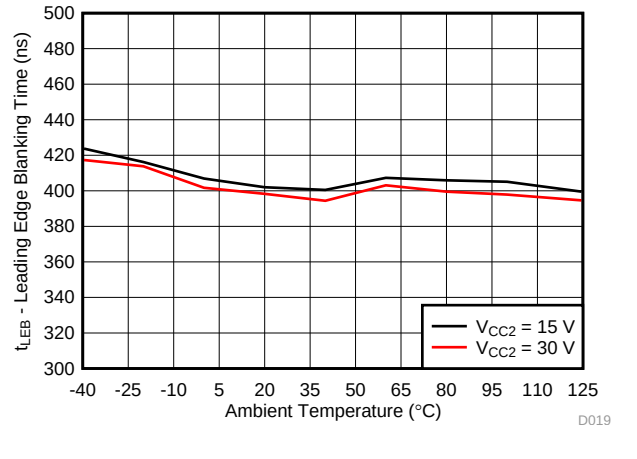


**Figure 32. Leading Edge Blanking Time With Temperature**

## Typical Characteristics (continued)

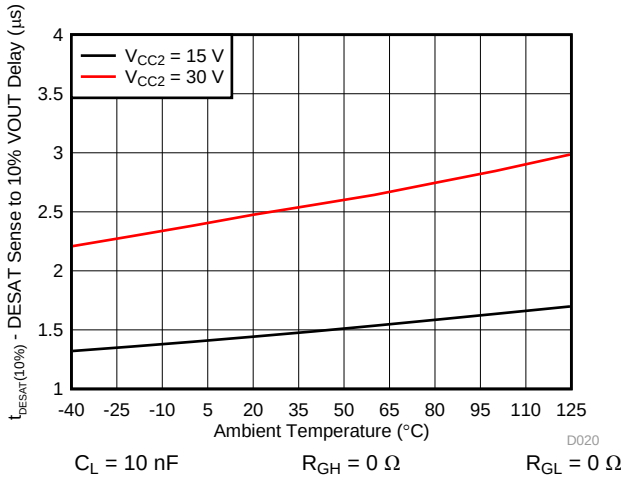


**Figure 33. DESAT Sense to $V_{OUT}$ 10% Delay vs Temperature**

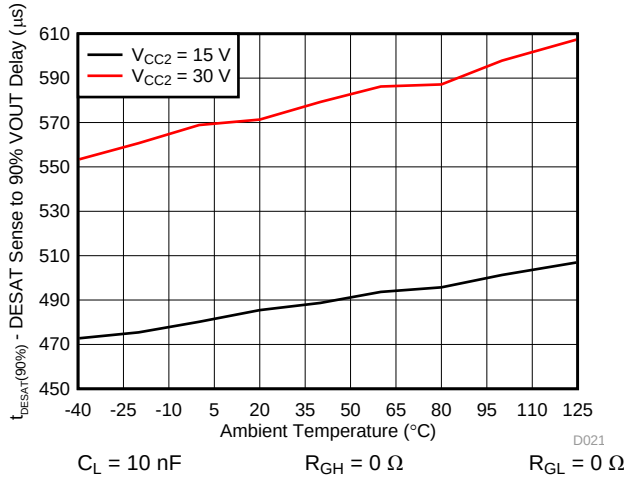


**Figure 34. DESAT Sense to $V_{OUT}$ 90% Delay vs Temperature**

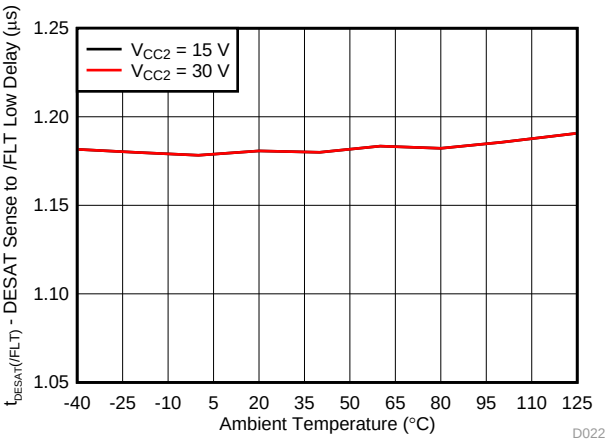


**Figure 35. DESAT Sense to Fault Low Delay vs Temperature**

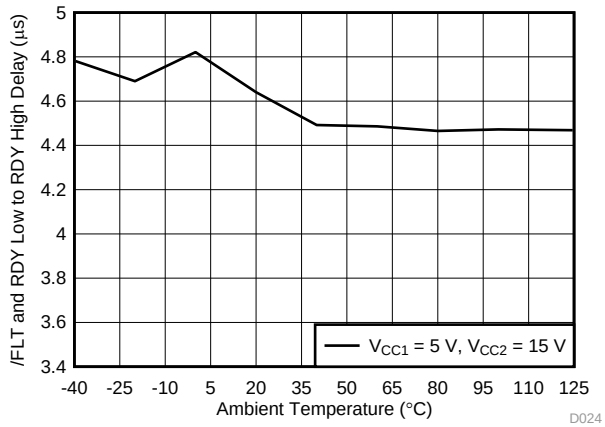


**Figure 36. Fault and RDY Low to RDY High Delay vs Temperature**

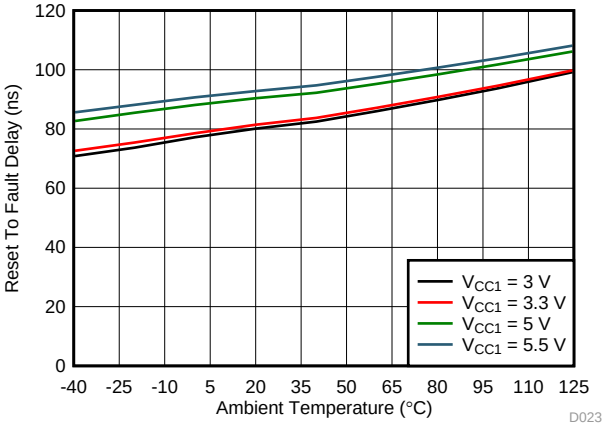


**Figure 37. Reset to Fault Delay Across Temperature**

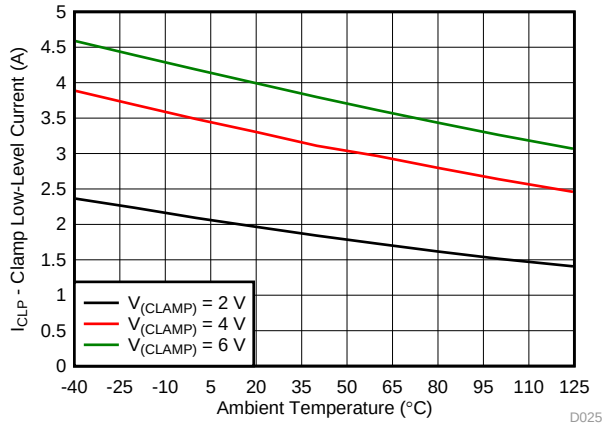


**Figure 38. Miller Clamp Current vs Temperature**


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## Typical Characteristics (continued)

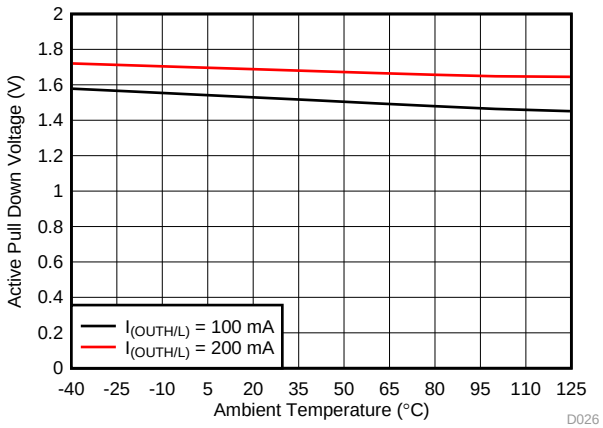



**Figure 39. Active Pulldown Voltage vs Temperature**

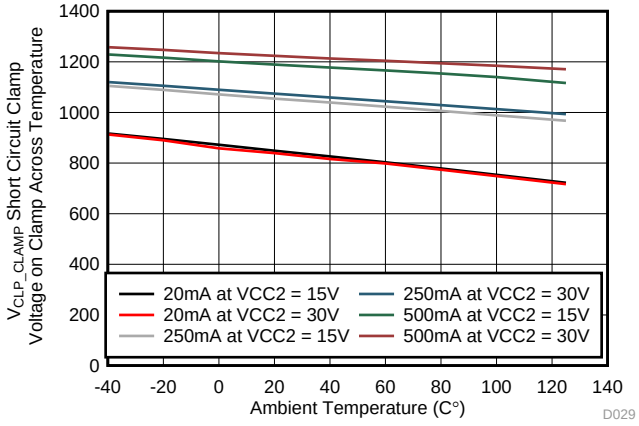



**Figure 40. $V_{CLP_CLAMP}$ - Short-Circuit Clamp Voltage on Clamp Across Temperature**

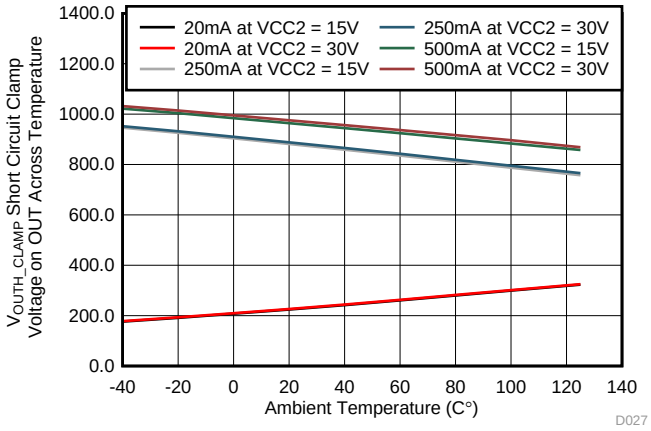



**Figure 41. $V_{OUTH_CLAMP}$ - Short-Circuit Clamp Voltage on OUTH Across Temperature**

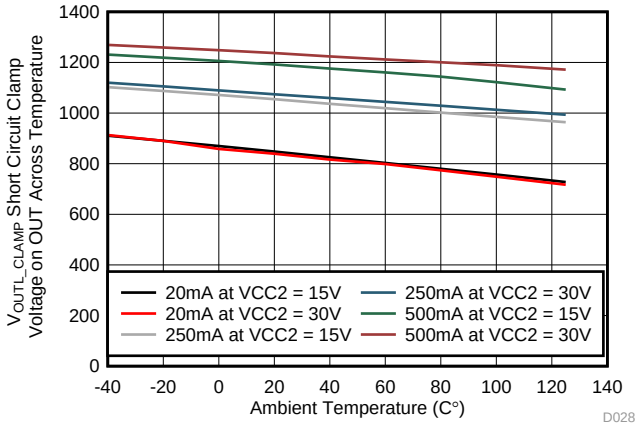
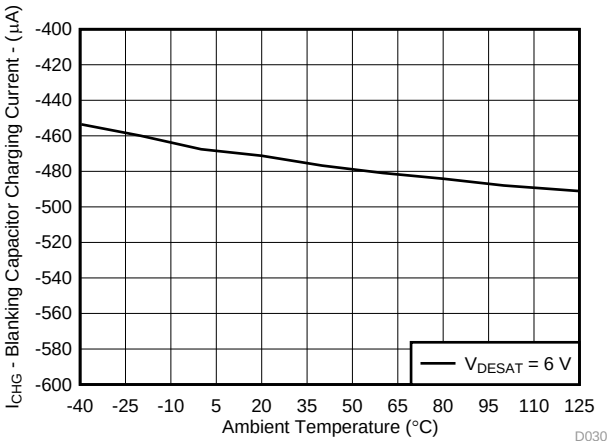



**Figure 42. $V_{OUTL_CLAMP}$ - Short-Circuit Clamp Voltage on OUTL Across Temperature**




$V_{CC2}$ = 15 V DESAT = 6 V

**Figure 43. Blanking Capacitor Charging Current vs Temperature**

# 8 Parameter Measurement Information

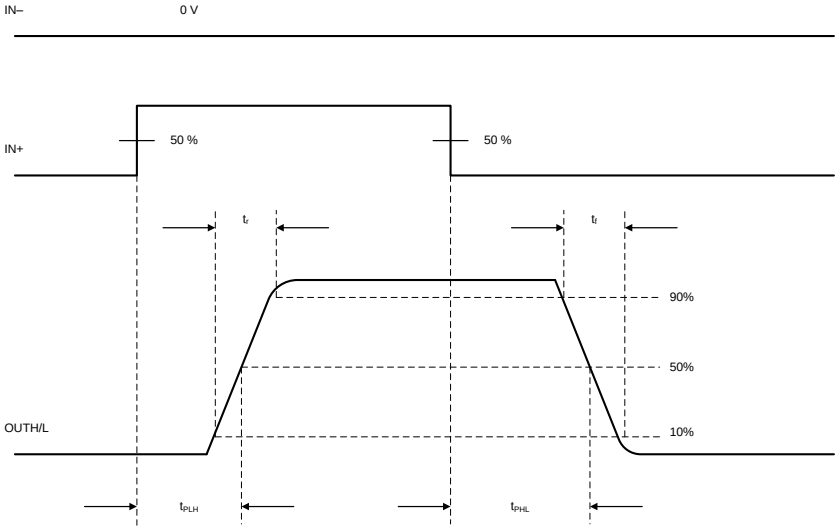



**Figure 44. OUTH and OUTL Propagation Delay, Non-Inverting Configuration**

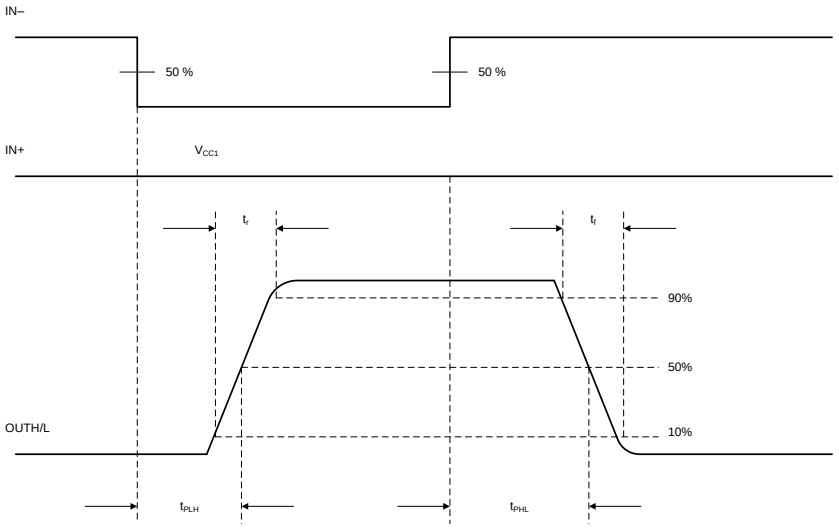



**Figure 45. OUTH and OUTL Propagation Delay, Inverting Configuration**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## Parameter Measurement Information (continued)

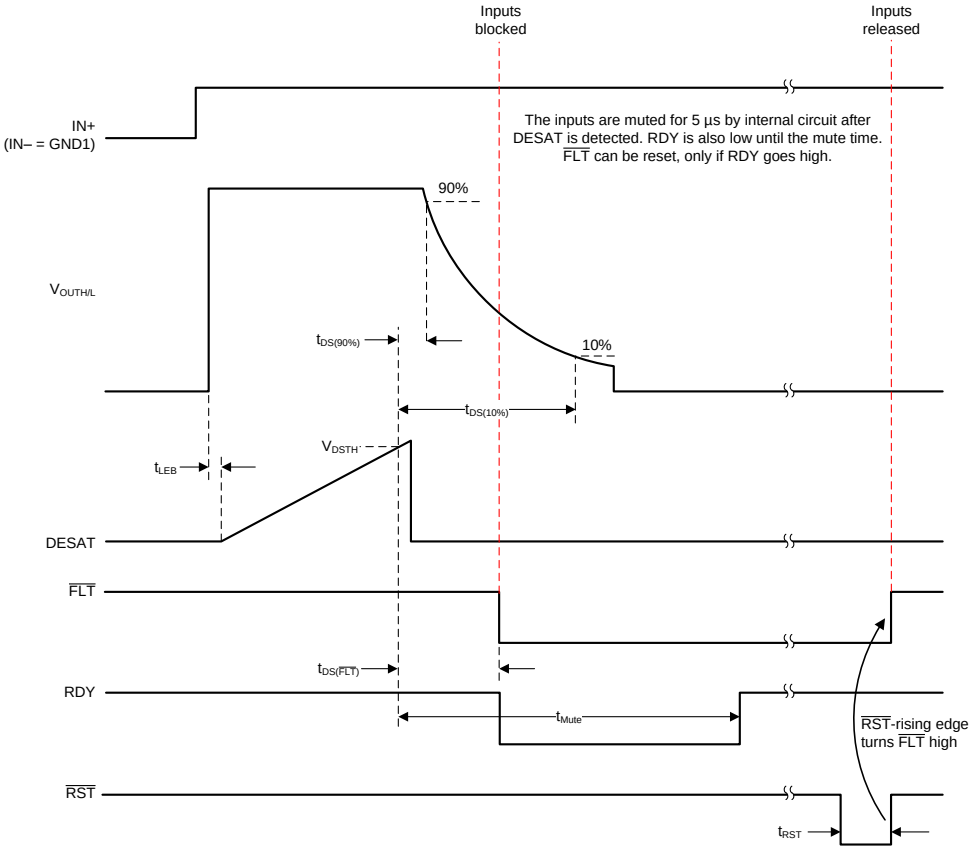



**Figure 46. DESAT, OUTH/L, $\overline{FLT}$, $\overline{RST}$ Delay**

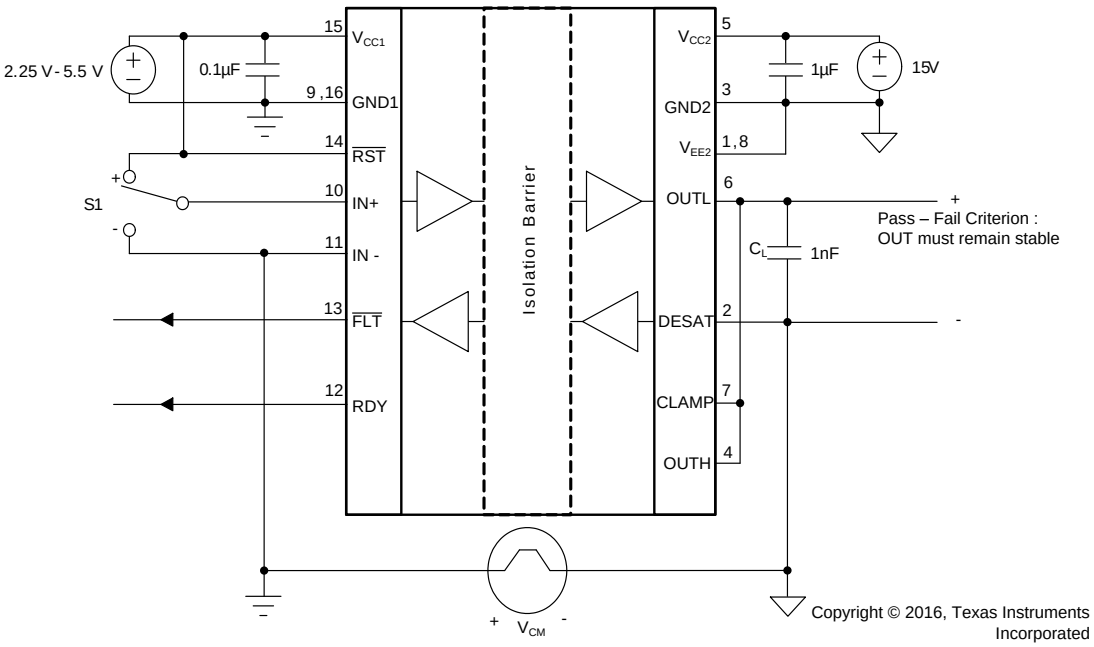



**Figure 47. Common-Mode Transient Immunity Test Circuit**

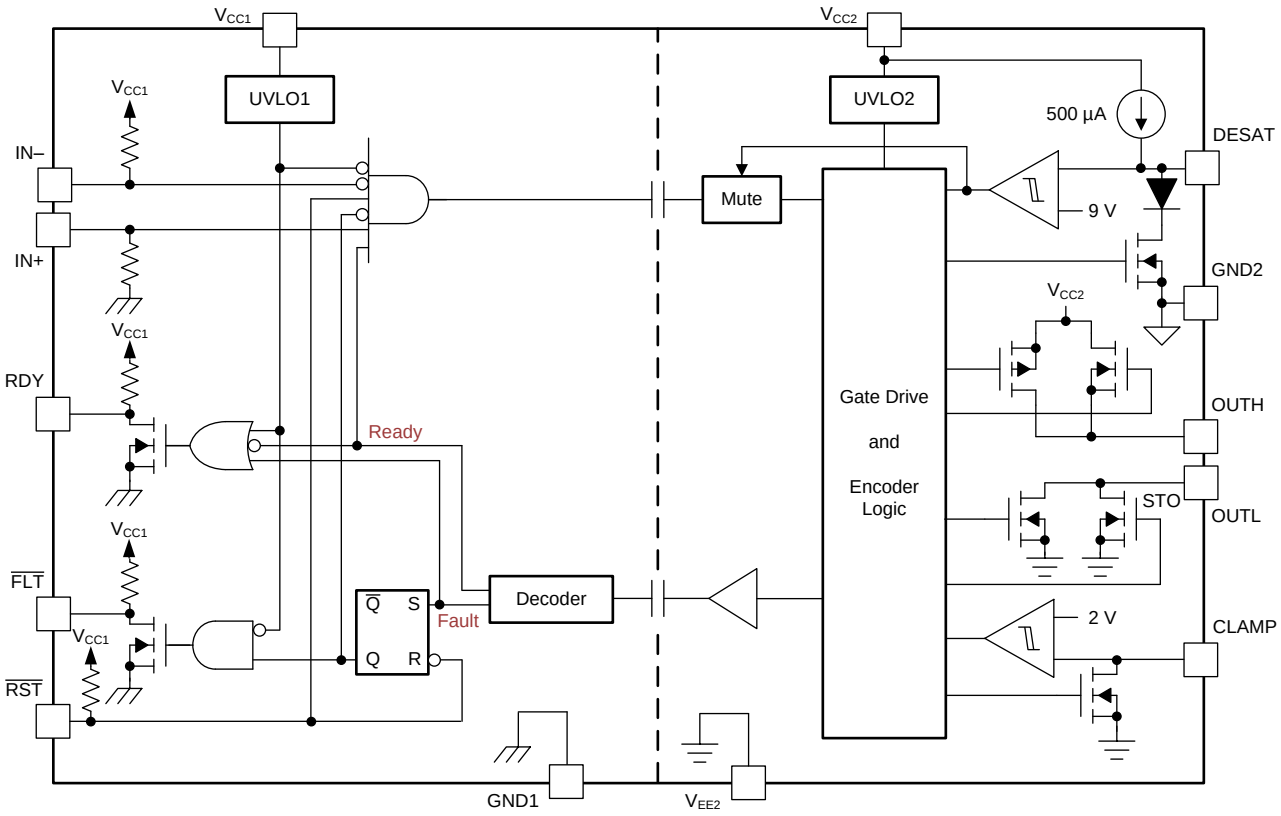
# 9 Detailed Description

## 9.1 Overview

The ISO5852S-Q1 is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a Silicon dioxide ($SiO_2$) capacitive isolation.

The IO circuitry on the input side interfaces with a micro controller and consists of gate drive control and RESET ($\overline{RST}$) inputs, READY (RDY) and FAULT ($\overline{FLT}$) alarm outputs. The power stage consists of power transistors to supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5852S-Q1 also contains under voltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pulldown feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5852S-Q1 also has an active Miller clamp function which can be used to prevent parasitic turn-on of the external power transistor, due to Miller effect, for unipolar supply operation.

## 9.2 Functional Block Diagram

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## 9.3 Feature Description

### 9.3.1 Supply and Active Miller clamp

The ISO5852S-Q1 supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on its gate with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of $V_{CC2}$ and $V_{EE2}$ for bipolar operation are 15-V and -8-V with respect to GND2.

For operation with unipolar supply, typically, $V_{CC2}$ is connected to 15-V with respect to GND2, and $V_{EE2}$ is connected to GND2. In this use case, the IGBT can turn on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected to IGBT gate and Miller current is sinked through a low impedance CLAMP transistor.

Miller CLAMP is designed for Miller current up to 2-A. When the IGBT is turned-off and the gate voltage transitions below 2-V the CLAMP current output is activated.

### 9.3.2 Active Output Pulldown

The Active output pulldown feature ensures that the IGBT gate OUTH/L is clamped to $V_{EE2}$ to ensure safe IGBT off-state, when the output side is not connected to the power supply.

### 9.3.3 Undervoltage Lockout (UVLO) With Ready (RDY) Pin Indication Output

Undervoltage Lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned-off, if the supply $V_{CC1}$ drops below $V_{IT-(UVLO1)}$, irrespective of IN+, IN– and RST input till $V_{CC1}$ goes above $V_{IT+(UVLO1)}$.

In similar manner, the IGBT is turned-off, if the supply $V_{CC2}$ drops below $V_{IT-(UVLO2)}$, irrespective of IN+, IN– and RST input till $V_{CC2}$ goes above $V_{IT+(UVLO2)}$.

Ready (RDY) pin indicates status of input and output side Under Voltage Lock-Out (UVLO) internal protection feature. If either side of device have insufficient supply ($V_{CC1}$ or $V_{CC2}$), the RDY pin output goes low; otherwise, RDY pin output is high. RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

### 9.3.4 Soft Turnoff, Fault ($\overline{\text{FLT}}$) and Reset ($\overline{\text{RST}}$)

During IGBT overcurrent condition, a mute logic initiates a soft-turn-off procedure which disables, OUTH, and pulls OUTL to low over a time span of 2 μs. When desaturation is active, a fault signal is sent across the isolation barrier pulling the $\overline{\text{FLT}}$ output at the input side low and blocking the isolator input. mute logic is activated through the soft-turn-off period. The $\overline{\text{FLT}}$ output condition is latched and can be reset only after RDY goes high, through a active-low pulse at the $\overline{\text{RST}}$ input. $\overline{\text{RST}}$ has an internal filter to reject noise and glitches. By asserting $\overline{\text{RST}}$ for at-least the specified minimum duration (800 ns), device input logic can be enabled or disabled.

### 9.3.5 Short Circuit Clamp

Under short circuit events it is possible that currents are induced back into the gate-driver OUTH/L and CLAMP pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUTH/L and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

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## 9.4 Device Functional Modes

In ISO5852S-Q1 OUTH/L to follow IN+ in normal functional mode, $\overline{FLT}$ pin must be in the high state. Table 1 lists the device functions.

**Table 1. Function Table(1)**

| $V_{CC1}$ | $V_{CC2}$ | IN+ | IN– | $\overline{RST}$ | RDY | OUTH/L |
|---|---|---|---|---|---|---|
| PU | PD | X | X | X | Low | Low |
| PD | PU | X | X | X | Low | Low |
| PU | PU | X | X | Low | High | Low |
| PU | Open | X | X | X | Low | Low |
| PU | PU | Low | X | X | High | Low |
| PU | PU | X | High | X | High | Low |
| PU | PU | High | Low | High | High | High |

(1) PU: Power Up ($V_{CC1}$ ≥ 2.25 V, $V_{CC2}$ ≥ 13 V), PD: Power Down ($V_{CC1}$ ≤ 1.7 V, $V_{CC2}$ ≤ 9.5 V), X: Irrelevant


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# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The ISO5852S-Q1 device is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. It is intended for use in applications such as motor control, industrial inverters and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a microcontroller, and are at low voltage levels such as 2.5 V, 3.3 V or 5 V. The gate controls required by the MOSFETs and IGBTs, however, are in the range of 30-V (using unipolar output supply) to 15-V (using bipolar output supply), and require high-current capability to drive the large capacitive loads offered by those power transistors. The gate drive must also be applied with reference to the emitter of the IGBT (source for MOSFET), and by construction, the emitter node in a gate-drive system may swing between 0 to the DC-bus voltage, which can be several 100s of volts in magnitude.

The ISO5852S-Q1 device is therefore used to level shift the incoming 2.5-V, 3.3-V, and 5-V control signals from the microcontroller to the 30-V (using unipolar output supply) to 15-V (using bipolar output supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

## 10.2 Typical Applications

Figure 48 shows the typical application of a three-phase inverter using six ISO5852S-Q1 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high-power applications such as high-voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one ISO5852S-Q1. The switches are driven on and off at high switching frequency with specific patterns that to converter dc bus voltage to three-phase AC voltages.

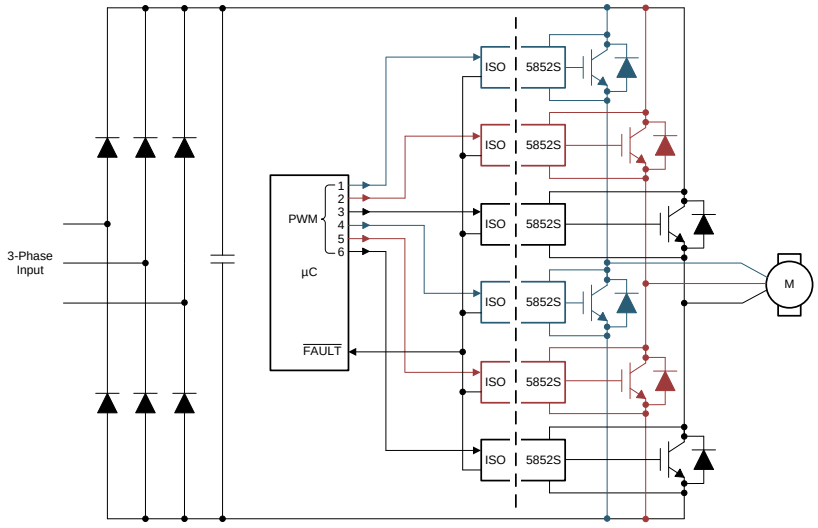


**Figure 48. Typical Motor-Drive Application**

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## Typical Applications (continued)

### 10.2.1 Design Requirements

Unlike optocoupler-based gate drivers which required external current drivers and biasing circuitry to provide the input control signals, the input control to the ISO5852S-Q1 device is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common-drain $\overline{FLT}$ output signal and $\overline{RST}$ input signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. Table 2 lists the allowed range for input and output supply voltage, and the typical current output available from the gate-driver.

**Table 2. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input supply voltage | 2.25 V to 5.5 V |
| Unipolar output-supply voltage ($V_{CC2}$ – GND2 = $V_{CC2}$ – $V_{EE2}$) | 15 V to 30 V |
| Bipolar output-supply voltage ($V_{CC2}$ – $V_{EE2}$) | 15 V to 30 V |
| Bipolar output-supply voltage (GND2 – $V_{EE2}$) | 0 V to 15 V |
| Output current | 2.5 A |

### 10.2.2 Detailed Design Procedure

#### *10.2.2.1 Recommended ISO5852S-Q1 Application Circuit*

The ISO5852S-Q1 device has both, inverting and noninverting gate-control inputs, an active-low reset input, and an open-drain fault output suitable for wired-OR applications. The recommended application circuit in Figure 49 shows a typical gate-driver implementation with unipolar output supply. Figure 50 shows a typical gate-driver implementation with bipolar output supply using the ISO5852S-Q1 device.

A 0.1-µF bypass capacitor, recommended at the input supply pin $V_{CC1}$, and 1-µF bypass capacitor, recommended at the $V_{CC2}$ output supply pin, provide the large transient currents required during a switching transition to ensure reliable operation. The 220-pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode ($D_{DST}$) and the 1-kΩ series resistor on the DESAT pin are external protection components. The $R_G$ gate resistor limits the gate-charge current and indirectly controls the rise and fall times of the IGBT collector voltage. The open-drain $\overline{FLT}$ output and RDY output have a passive 10-kΩ pullup resistor. In this application, the IGBT gate driver is disabled when a fault is detected and does not resume switching until the microcontroller applies a reset signal.

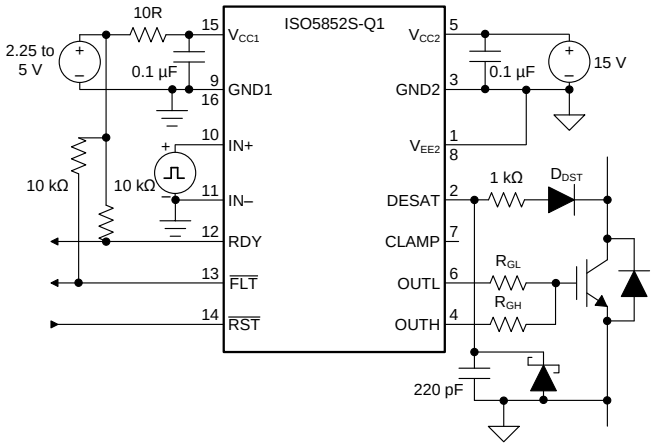


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**Figure 49. Unipolar Output Supply**

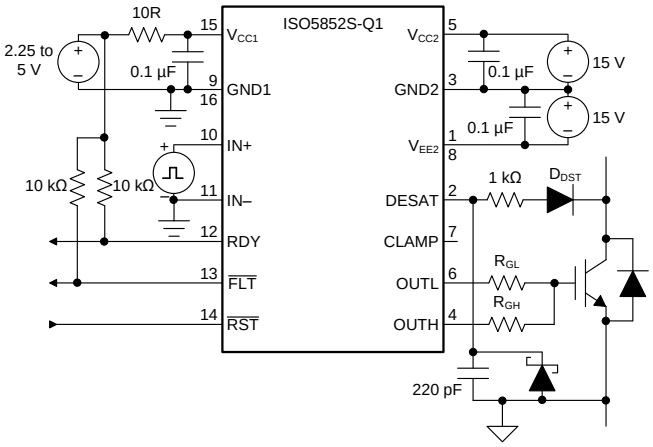


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**Figure 50. Bipolar Output Supply**


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#### 10.2.2.2 $\overline{FLT}$ and RDY Pin Circuitry

A is 50-kΩ pullup resistor exists internally on $\overline{FLT}$ and RDY pins. The $\overline{FLT}$ and RDY pins are an open-drain output. A 10-kΩ pullup resistor can be used to make it faster rise and to provide logic high when $\overline{FLT}$ and RDY is inactive, as shown in Figure 51.

Fast common-mode transients can inject noise and glitches on $\overline{FLT}$ and RDY pins because of parasitic coupling. The injection of noise and glitches is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the $\overline{FLT}$ and RDY pins.

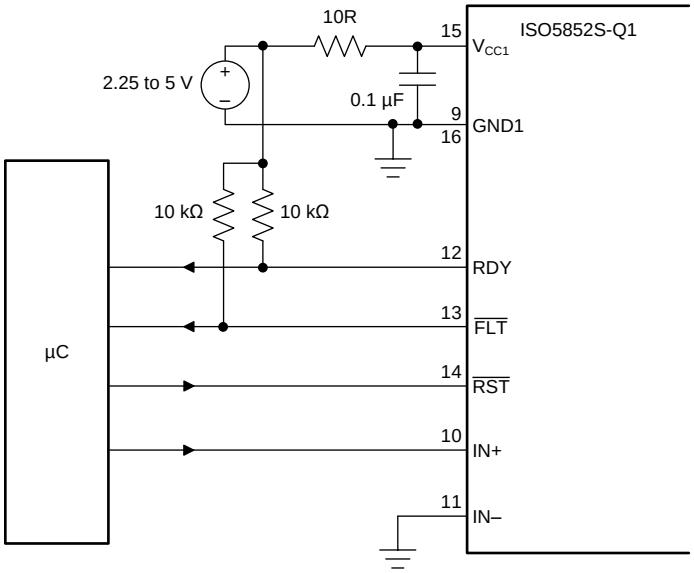


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**Figure 51. $\overline{FLT}$ and RDY Pin Circuitry for High CMTI**

#### 10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5852S-Q1 device. For maximum CMTI performance, the digital control inputs, IN+ and IN–, must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5852S-Q1 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pullup resistors, must be avoided. A 20-ns glitch filter exists that can filter a glitch up to 20 ns on IN+ or IN–.

### *10.2.2.4 Local Shutdown and Reset*

In applications with local shutdown and reset, the $\overline{\text{FLT}}$ output of each gate driver is polled separately, and the individual reset lines are independently asserted low to reset the motor controller after a fault condition.

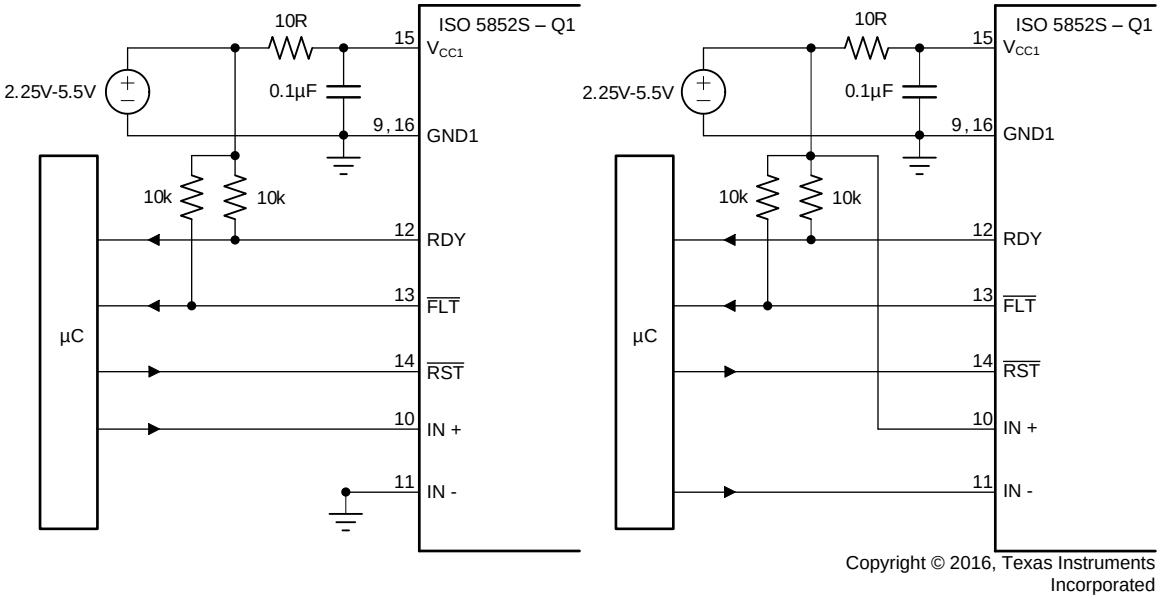


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**Figure 52. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)**


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#### *10.2.2.5 Global-Shutdown and Reset*

When configured for inverting operation, the ISO5852S-Q1 device can be configured to shutdown automatically in the event of a fault condition by tying the $\overline{FLT}$ output to IN+. For high reliability drives, the open drain $\overline{FLT}$ outputs of multiple ISO5852S-Q1 devices can be wired together forming a single, common fault bus for interfacing directly to the microcontroller. When any of the six gate drivers of a three-phase inverter detects a fault, the active-low $\overline{FLT}$ output disables all six gate drivers simultaneously.

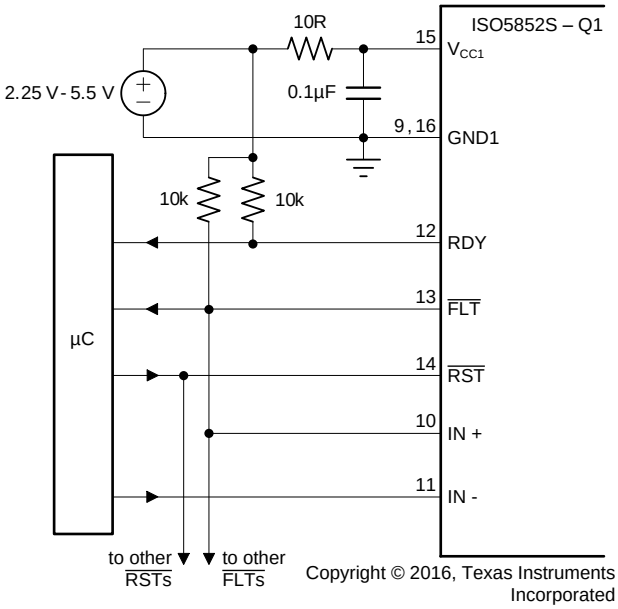


**Figure 53. Global Shutdown With Inverting Input Configuration**

### *10.2.2.6 Auto-Reset*

In this case, the gate control signal at IN+ is also applied to the $\overline{RST}$ input to reset the fault latch every switching cycle. Incorrect $\overline{RST}$ makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the *gate-low* state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch is always reset before IN+ goes high again. This configuration protects the IGBT on a cycle-by-cycle basis and automatically resets before the next *on* cycle.

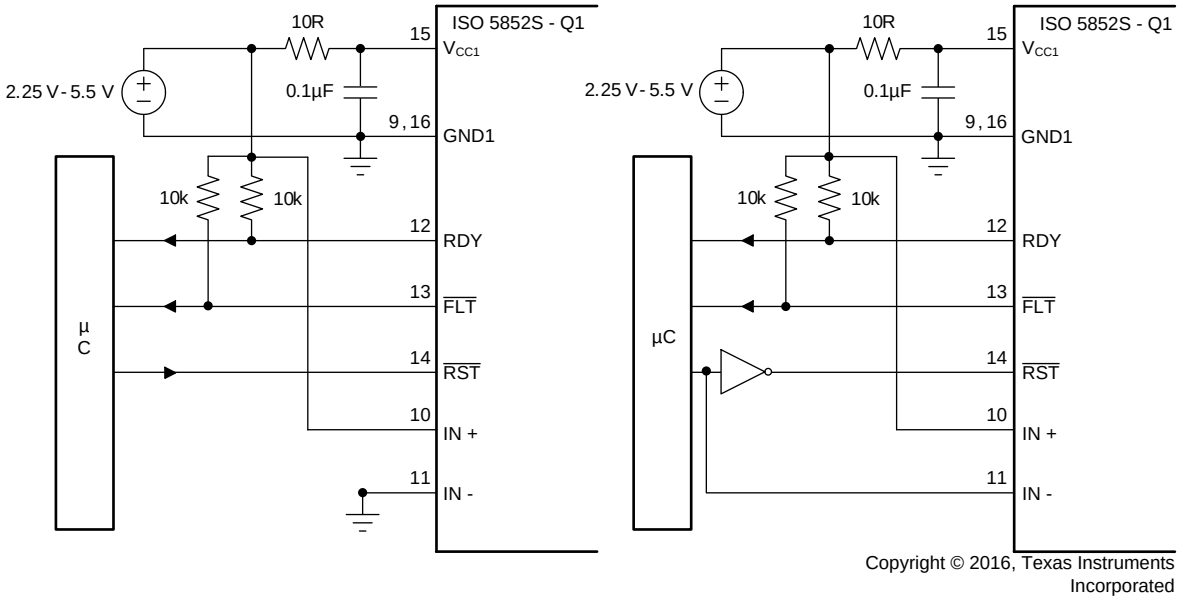


**Figure 54. Auto Reset for Noninverting and Inverting Input Configuration**


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### 10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large, instantaneous forward-voltage transients across the freewheeling diodes of the IGBTs. These transients result in large negative-voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low-forward voltage assures clamping of the DESAT input to GND2 potential at low-voltage levels.

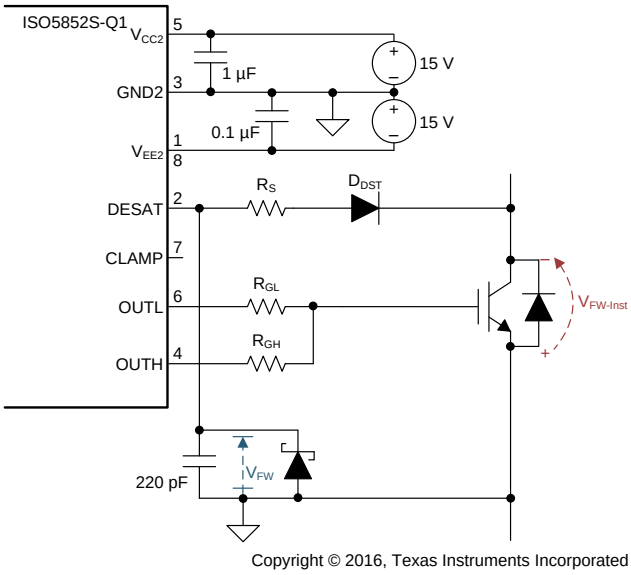


**Figure 55. DESAT Pin Protection With Series Resistor and Schottky Diode**

#### 10.2.2.8 DESAT Diode and DESAT Threshold

The function of the DESAT diode is to conduct forward current, allowing sensing of the saturated collector-to-emitter voltage of the IGBT, $V_{(DESAT)}$, (when the IGBT is *on*), and to block high voltages (when the IGBT is *off*). During the short transition time when the IGBT is switching, a commonly high $dV_{CE}/dt$ voltage ramp rate occurs across the IGBT. This ramp rate results in a charging current $I_{(CHARGE)} = C_{(D\text{-}DESAT)} \times d_{VCE}/dt$, charging the blanking capacitor. $C_{(D\text{-}DESAT)}$ is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of $1+ C_{(BLANK)} / C_{(D\text{-}DESAT)}$.

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{(DESAT)}$, the $V_{CE}$ level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series: $V_{CE\text{-}FAULT(TH)} = 9\ V – n \times VF$ (where n is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating can be selected.

#### 10.2.2.9 Determining the Maximum Available, Dynamic Output Power, $P_{OD\text{-}max}$

The ISO5852S-Q1 maximum-allowed total power consumption of $P_D = 251$ mW consists of the total input power, $P_{ID}$, the total output power, $P_{OD}$, and the output power under load, $P_{OL}$:

$$P_D = P_{ID} + P_{OD} + P_{OL} \quad (1)$$

With:

$$P_{ID} = V_{CC1\text{-}max} \times I_{CC1\text{-}max} = 5.5\ V \times 4.5\ mA = 24.75\ mW \quad (2)$$

and:

$$P_{OD} = (V_{CC2} – V_{EE2}) \times I_{CC2\text{-}max} = (15\ V – [–8\ V]) \times 6\ mA = 138\ mW \quad (3)$$

then:

$$P_{OL} = P_D – P_{ID} – P_{OD} = 251\ mW – 24.75\ mW – 138\ mW = 88.25\ mW \quad (4)$$

In comparison to $P_{OL}$, the actual dynamic output power under worst case condition, $P_{OL\text{-}WC}$, depends on a variety of parameters:

$$P_{OL\text{-}WC} = 0.5 \times f_{INP} \times Q_G \times \left(V_{CC2} – V_{EE2}\right) \times \left( \frac{r_{on\text{-}max}}{r_{on\text{-}max} + R_G} + \frac{r_{off\text{-}max}}{r_{off\text{-}max} + R_G} \right) \quad (5)$$

where

- $f_{INP}$ = signal frequency at the control input IN+
- $Q_G$ = power device gate charge
- $V_{CC2}$ = positive output supply with respect to GND2
- $V_{EE2}$ = negative output supply with respect to GND2
- $r_{on\text{-}max}$ = worst case output resistance in the on-state: 4 Ω
- $r_{off\text{-}max}$ = worst case output resistance in the off-state: 2.5 Ω
- $R_G$ = gate resistor


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When $R_G$ is determined, Equation 5 is to be used to verify whether $P_{OL-WC} < P_{OL}$. Figure 56 shows a simplified output stage model for calculating $P_{OL-WC}$.

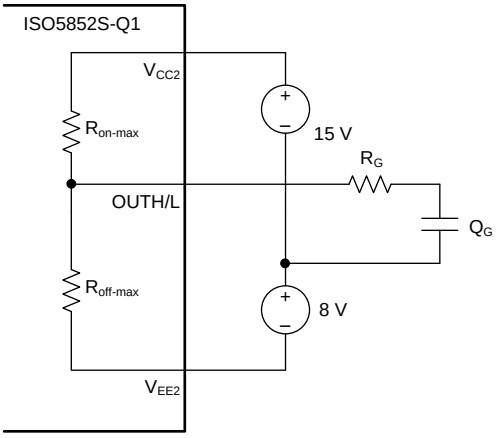


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**Figure 56. Simplified Output Model for Calculating $P_{OL-WC}$**

#### *10.2.2.10 Example*

This examples considers an IGBT drive with the following parameters:

- $I_{ON-PK}$ = 2 A
- $Q_G$ = 650 nC
- $f_{INP}$ = 20 kHz
- $V_{CC2}$ = 15 V
- $V_{EE2}$ = –8 V

Applying the value of the gate resistor $R_G$ = 10 Ω.

Then, calculating the worst-case output-power consumption as a function of $R_G$, using Equation 5 $r_{on-max}$ = worst case output resistance in the on-state: 4 Ω, $r_{off-max}$ = worst case output resistance in the off-state: 2.5 Ω, $R_G$ = gate resistor yields

$$P_{OL-WC} = 0.5 \times 20\ \text{kHz} \times 650\ \text{nC} \times (15\ \text{V} - (-8\ \text{V})) \times \left( \frac{4\ \Omega}{4\ \Omega + 10\ \Omega} + \frac{2.5\ \Omega}{2.5\ \Omega + 10\ \Omega} \right) = 72.61\ \text{mW} \quad (6)$$

Because $P_{OL-WC}$ = 72.61 mW is less than the calculated maximum of $P_{OL}$ = 88.25 mW, the resistor value of $R_G$ = 10 Ω is suitable for this application.

### 10.2.2.11 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 57) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.

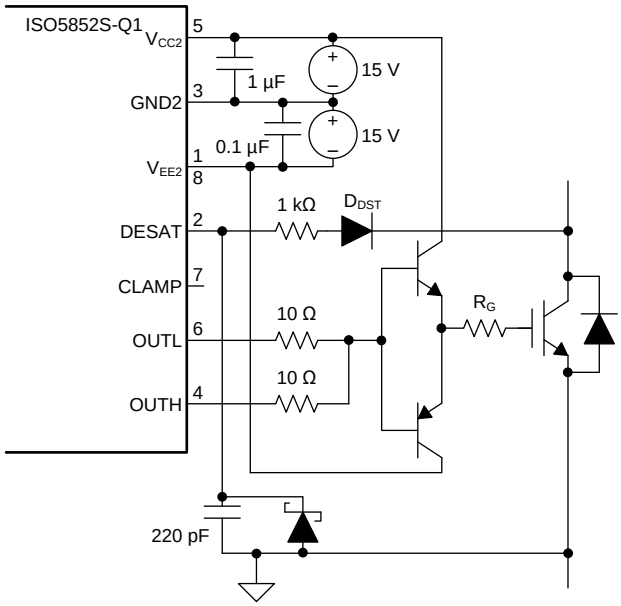


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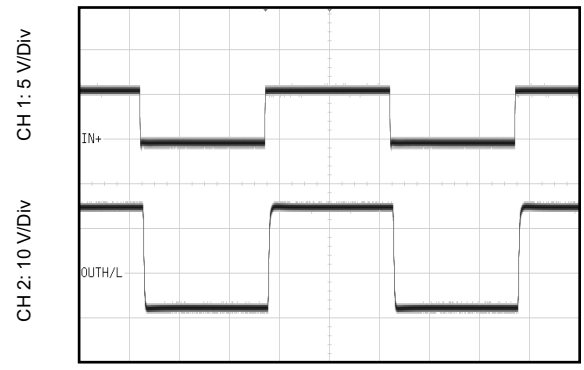
**Figure 57. Current Buffer for Increased Drive Current**

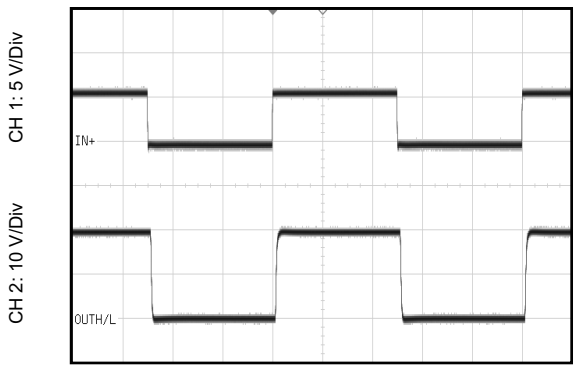
## 10.2.3 Application Curves




5 µs/Div

$C_L$ = 1 nF $R_{GH}$ = 10 Ω $R_{GL}$ = 10 Ω
$V_{CC2}$ – GND2 = 15 V GND2 - $V_{EE2}$ = 8 V
($V_{CC2}$ – $V_{EE2}$ = 23 V)

**Figure 58. Normal Operation - Bipolar Supply**




5 µs/Div

$C_L$ = 1 nF $R_{GH}$ = 10 Ω $R_{GL}$ = 10 Ω
$V_{CC2}$ – $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 59. Normal Operation - Unipolar Supply**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# 11 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the $V_{CC1}$ input supply pin and a 1-μF bypass capacitor is recommended at the $V_{CC2}$output supply pin. The capacitors should be placed as close to the supply pins as possible. The recommended placement of the capacitors is 2 mm (maximum) from the input and output power supply pins ($V_{CC1}$ and $V_{CC2}$).

# 12 Layout

## 12.1 Layout Guidelines

minimum of four layers is required to accomplish a low EMI PCB design (see Figure 60). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, Gate driver output OUTH/L and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch$^2$. On the gate-driver $V_{EE2}$ and $V_{CC2}$ can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For more detailed layout recommendations, including placement of capacitors, impact of vias, reference planes, routing, and other details, see the *Digital Isolator Design Guide*.

## 12.2 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 12.3 Layout Example

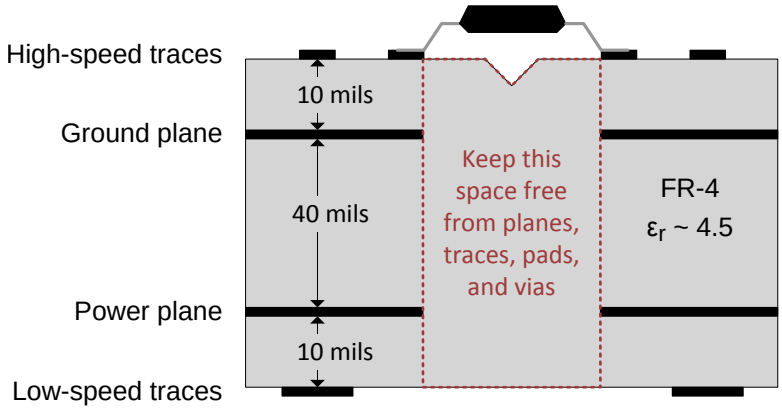


**Figure 60. Recommended Layer Stack**

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# 13 デバイスおよびドキュメントのサポート

## 13.1 ドキュメントのサポート

### 13.1.1 関連資料

関連資料については、以下を参照してください：

- *『デジタル・アイソレータ設計ガイド』*
- *『ISO5852S評価モジュール(EVM)ユーザー・ガイド』*
- *『絶縁の用語集』*

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## 13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。


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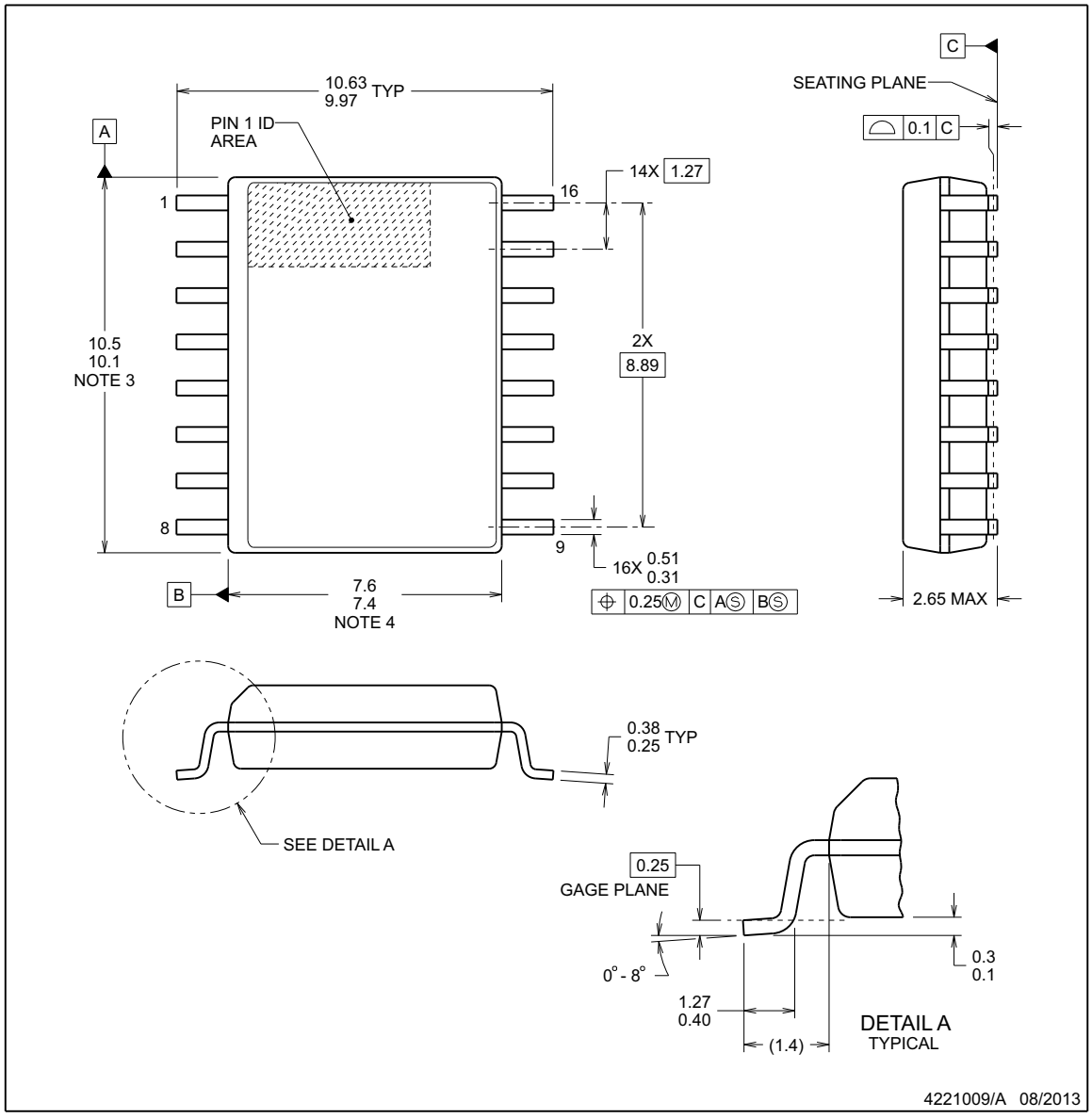
# PACKAGE OUTLINE

## DW0016B

SOIC - 2.65 mm max height

SOIC




NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.



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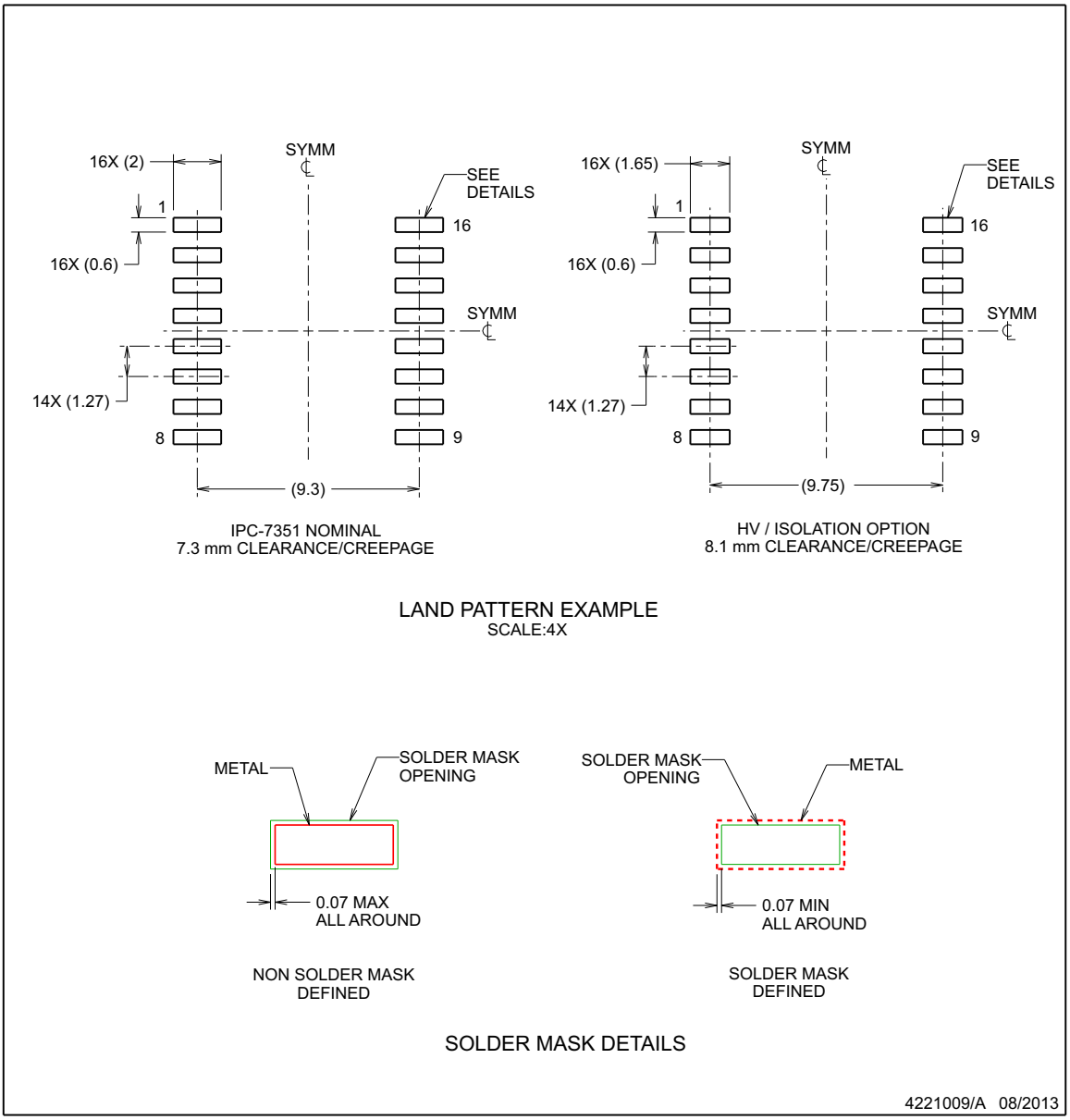
# EXAMPLE BOARD LAYOUT

## DW0016B SOIC - 2.65 mm max height

SOIC




NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.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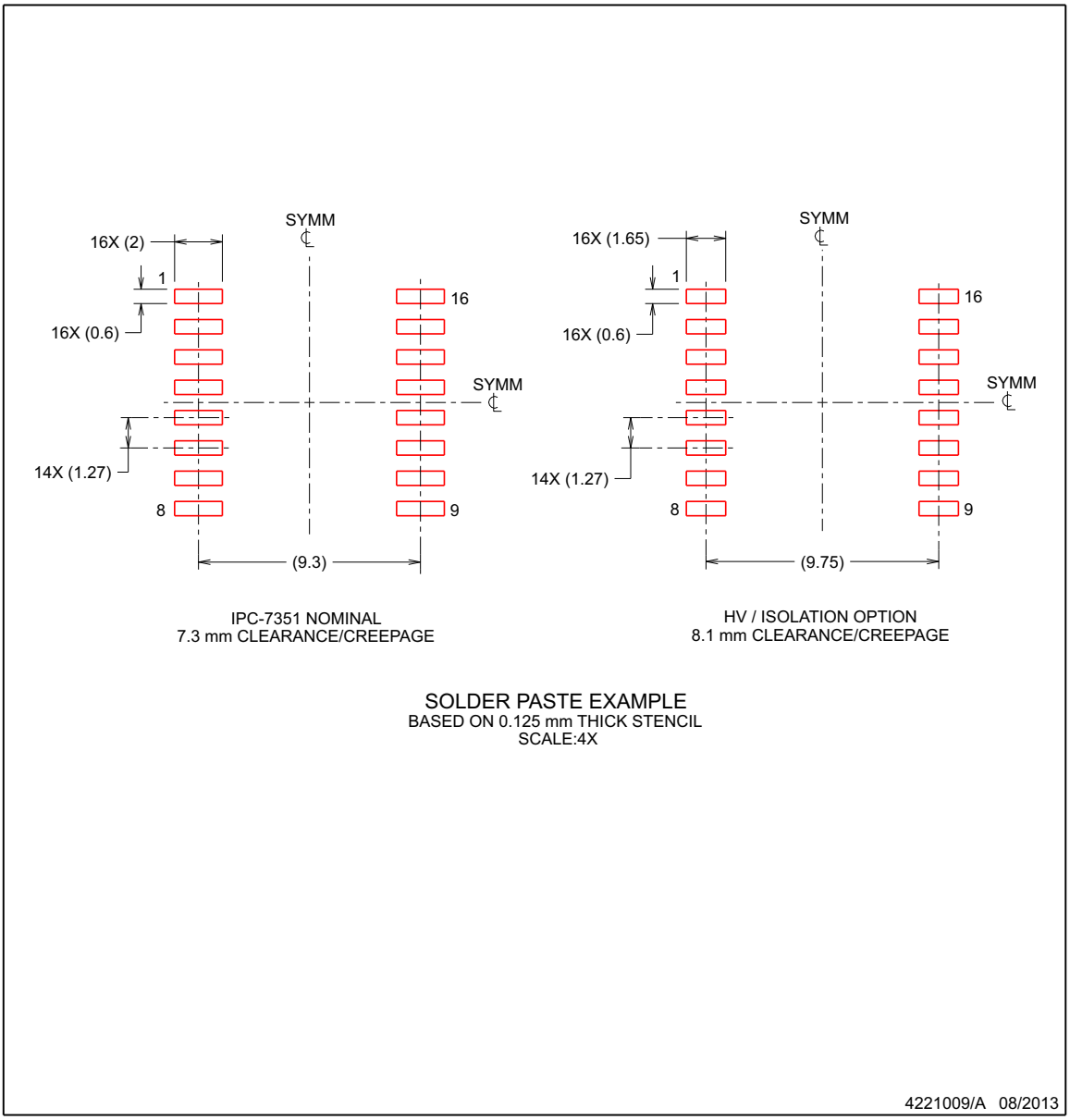
# EXAMPLE STENCIL DESIGN

## DW0016B

SOIC - 2.65 mm max height

SOIC




NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ISO5852SQDWQ1 | Obsolete | Production | SOIC (DW) \| 16 | - | - | Call TI | Call TI | -40 to 125 | ISO5852SQ |
| ISO5852SQDWRQ1 | Active | Production | SOIC (DW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO5852SQ |
| ISO5852SQDWRQ1.A | Active | Production | SOIC (DW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO5852SQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF ISO5852S-Q1 :**

- Catalog : ISO5852S

- Enhanced Product : ISO5852S-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

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