ISO7041 超低消費電力4チャネル・デジタル・アイソレータ

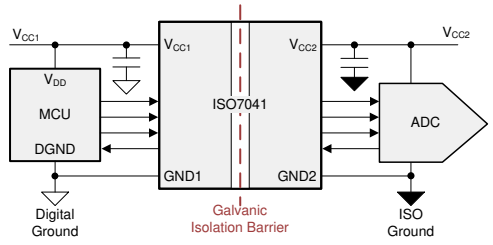
1 特長

- **超低消費電力**
  - チャネルあたり 3.5µA の静止電流 (3.3V)
  - 100kbps 時にチャネルあたり 15µA (3.3V)
  - 1Mbps 時にチャネルあたり 116µA (3.3V)
- **堅牢な絶縁バリア**
  - 推定寿命:100年超
  - 定格絶縁電圧:3000V_{RMS}
  - CMTI:±100kV/µs (標準値)
- **広い電源電圧範囲**:2.25V～5.5V
- **広い温度範囲**:
  - 2.25V～3.6V:–55℃～+125℃
  - 3.6V～5.5V:–40℃～+125℃
- **小型の 16-QSOP パッケージ** (16-DBQ)
- **信号速度**:最高 2Mbps
- **デフォルト出力 *HIGH*** (ISO7041) **および *LOW*** (ISO7041F) **のオプション**
- **堅牢な電磁気互換性** (EMC)
  - システム・レベルでの ESD、EFT、サージ耐性
  - 絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護
  - 超低エミッション
- **安全性関連の認定 (予定)**
  - UL 1577部品認定プログラム
  - DIN V VDE V 0884-11
  - CQC、TUV、CSA 認定
  - IECEx (IEC 60079-0 & IEC 60079-11)および ATEX (EN 60079-11)

2 アプリケーション

- 4mA～20mA ループ駆動のフィールド・トランスミッタ
- ファクトリ・オートメーション、プロセス・オートメーション
- 低消費電力の GPIO、UART、SPI 絶縁

簡略化されたアプリケーション回路図



3 概要

ISO7041は超低消費電力のマルチチャネル・デジタル・アイソレータで、CMOSまたはLVCMOSデジタルI/Oを絶縁できます。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二重の容量性二酸化ケイ素(SiO_2)絶縁バリアによって分離されています。革新的なエッジ・ベースのアーキテクチャとオン/オフ変調方式の組み合わせにより、超低消費電力でありながら、UL1577に準拠した3000V_{RMS}の定格絶縁電圧を実現しています。チャネルごとの動的な消費電流は 120µA/Mbps 未満、チャネルごとの静的な消費電流は 3.3V において 3.5µA なので、ISO7041 は電力と熱の両方において制約のあるシステム設計でも使用できます。

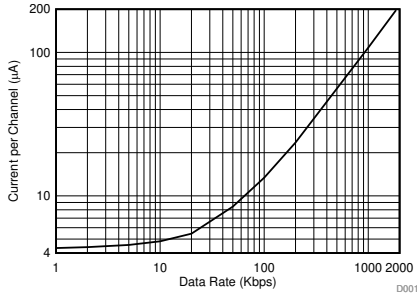
最小 2.25V、最大 5.5V で動作し、絶縁バリアの両側の電源電圧が異なる場合も完全に機能します。4 チャネルのアイソレータは 16-QSOP パッケージで供給されます (順方向チャネルが 3 つ、逆方向チャネルが 1 つ)。このデバイスには、デフォルト出力が HIGH と LOW のオプションがあります。入力電力または信号が消失した場合のデフォルト出力は、接尾辞 F の付かないISO7041 デバイスでは *HIGH*、接尾辞 F が付いた ISO7041F デバイスでは *LOW* です。詳細については、「デバイスの機能モード」セクションを参照してください。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ISO7041	QSOP (16)	4.90mm×3.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

3.3V時のデータ・レートと消費電力との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年10月発行のものから更新 **Page**

- デバイスのステータスを「量産データ」に 変更 ... 1

5 改訂履歴

Revision A (December 2018) から Revision B に変更 **Page**

- 最初のページのチャネル静止電流を表内データと一致するように更新 ... 1
- 「特長」の電源電圧範囲を拡大して 5.5V までサポート ... 1
- 「特長」の温度範囲を分割して 3.6V～5.5V では -40℃をサポート ... 1
- 「特長」に「絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護」を追加 ... 1
- 「概要」の電源電圧範囲を 5.5V まで拡大 ... 1
- Added ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier ... 5
- Added 5 V support to Recommended Operating Conditions ... 5
- Added temperature range for 3.6 V to 5.5 V supply range in Recommended Operating Conditions ... 5
- Added power dissipation maximum numbers to support 5.5 V in Power Ratings ... 6
- Added 5.5 V support in Safety Limiting Values ... 8
- Added 5 V Electrical Characteristics section ... 9
- Added 5 V Supply Current Characteristics section ... 9
- Added 5.5 V support to Thermal Derating Curves in Insulation Characteristics Curves ... 14
- Added 5 V Supply Current Curves to Typical Characteristics ... 15
- Updated Device I/O schematics removing (F version) only text in 図 13 ... 20
- Extended power supply range to 5.5 V in Application Information ... 21

6 Device Comparison Table

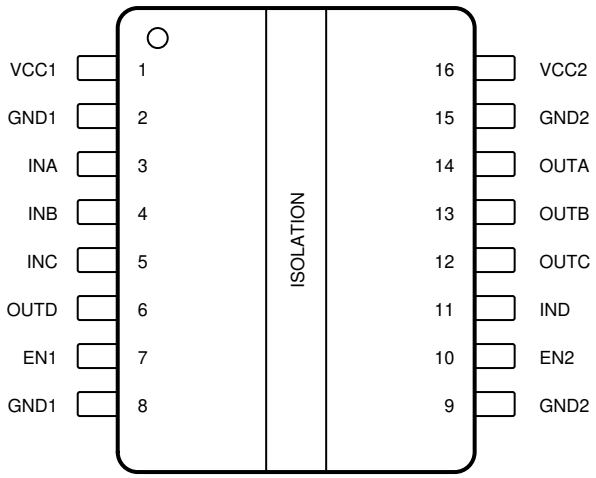
Table 1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO7041	3 Forward, 1 Reverse	2 Mbps	High	DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7041 with F suffix	3 Forward, 1 Reverse	2 Mbps	Low	DBQ-16	3000 V_{RMS} / 4242 V_{PK}

(1) See for detailed isolation ratings.

7 Pin Configuration and Functions

ISO7041 DBQ Package
16-Pin QSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	I	Refresh enable 1. Refresh is enabled when the EN1 pin is connected to GND1. Disable refresh by connecting the EN1 pin high to V_{CC1}. EN1 and EN2 must be connected to the same logic state to enable or disable refresh.
EN2	10	I	Refresh enable 2. Refresh is enabled when the EN2 pin is connected to GND2. Disable refresh by connecting the EN2 pin high to V_{CC2}. EN1 and EN2 must be connected to the same logic state to enable or disable refresh.
GND1	2	—	Ground connection for V_{CC1}
	8		
GND2	9	—	Ground connection for V_{CC2}
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply Voltage	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V_{CCX} + 0.5	V
	OUTx to GNDx	-0.5	V_{CCX} + 0.5	
	ENx to GNDx	-0.5	V_{CCX} + 0.5	
Output Current	Io	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3)(4)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}(1)	Supply Voltage Side 1		2.25		5.5	V
V_{CC2}(1)	Supply Voltage Side 2		2.25		5.5	V
V_{IH}	High level Input voltage		0.7 x V_{CCI}		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			mA
		V_{CCO} = 2.5 V	-1			mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
		V_{CCO} = 2.5 V			1	mA
DR	Data Rate		0		2	Mbps
T_A	Ambient temperature	V_{CC1}, V_{CC2} = 2.25 V to 3.6 V	-55		125	°C
		V_{CC1}, V_{CC2} = 3.6 V to 5.5 V	-40		125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another

8.4 Thermal Information

THERMAL METRIC(1)		ISO7041 DBQ (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 1-MHz 50% duty cycle square wave			7.82	mW
P_{D1}	Maximum power dissipation (side-1)				4.46	mW
P_{D2}	Maximum power dissipation (side-2)				3.36	mW

8.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
			QSOP-16	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	>3.7	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; See 図 15	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 6400\ V_{PK}$ (qualification)	4000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 150°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

8.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV	CSA/Sira
Plan to certify according to DIN V VDE V 0884-11:2017- 01	Certified according to IEC 60950-1 and IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013	Plan to certify for use in intrinsic safety (IS) to IS applications under ATEX and IECEx
Maximum transient isolation voltage, 4242 V_{PK}; Maximum repetitive peak isolation voltage, 566 V_{PK}; Maximum surge isolation voltage, 4000 V_{PK}	3000 V_{RMS} insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1- 14 and IEC 62368-1:2014 370 V_{RMS} (DBQ-16) maximum working voltage (pollution degree 2, material group I)	Single protection, 3000 V_{RMS}	Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	3000 V_{RMS} insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 300 V_{RMS} 3000 V_{RMS} insulation per EN 60950-1:2006/A2:2013 up to working voltage of 370 V_{RMS}	ATEX: EN 60079-0:2012+A11:2013 and EN 60079-11:2012 IECEx:IEC 60079-0:2011 (6th Ed) and IEC60079-11:2011 (6th Ed) II 1G Ex ia IIC Ga
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

8.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16-QSOP PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 87°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			261	mA
		$R_{\theta JA}$ = 87°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			399	mA
		$R_{\theta JA}$ = 87°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			522	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 87°C/W, T_J = 150°C, T_A = 25°C			1435	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

8.9 Electrical Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -4 mA	V_{CCO} - 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

8.10 Supply Current Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7041						
Supply current - DC signal	Refresh disable	I_{CC1}		6.2	14.3	µA
		I_{CC2}		10.1	18.5	µA
	Refresh enable V_I = V_{CC1} (ISO7041); V_I = 0 V (ISO7041 with F suffix)	I_{CC1}		8.2	16.7	µA
		I_{CC2}		10.8	18.5	µA
	Refresh enable V_I = 0 V (ISO7041); V_I = V_{CC1} (ISO7041 with F suffix)	I_{CC1}		9.5	19.9	µA
		I_{CC2}		11.3	19.5	µA
Supply current - AC signal	Refresh disable 10 kbps, No Load	I_{CC1}		6.7	19.7	µA
		I_{CC2}		11.8	20.6	µA
	Refresh disable 100 kbps, No Load	I_{CC1}		37.1	57.4	µA
		I_{CC2}		25.8	37.7	µA
	Refresh disable 1 Mbps, No Load	I_{CC1}		340.5	436.1	µA
		I_{CC2}		167.0	211.1	µA
	Refresh enable 10 kbps, No Load	I_{CC1}		10.6	20.8	µA
		I_{CC2}		11.9	20.4	µA
	Refresh enable 100 kbps, No Load	I_{CC1}		37.1	57.4	µA
		I_{CC2}		25.8	37.7	µA
	Refresh enable 1 Mbps, No Load	I_{CC1}		338.3	436.1	µA
		I_{CC2}		166.0	211.1	µA
Total Supply Current Per Channel, Refresh Disabled	DC Signal	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.1	7.4	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.9	10.7	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		17.4	23.4	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		137.0	164.5	µA

Supply Current Characteristics 5V Supply (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Total Supply Current Per Channel, Refresh Enabled	$V_I = V_{CC1}$ (ISO7041); $V_I = 0$ V (ISO7041 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		4.8	8.5	µA
	$V_I = 0$ V (ISO7041); $V_I = V_{CC1}$ (ISO7041 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		5.3	9.6	µA
	10 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		5.7	10.4	µA
	100 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		16.4	22.3	µA
	1 Mbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		125.9	154.0	µA

8.11 Electrical Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -2mA	V_{CCO} - 0.3	V_{CCO} - 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA		0.2	0.3	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 3.6 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

8.12 Supply Current Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7041						
Supply current - DC signal	Refresh disable	I_{CC1}		5.1	8.8	µA
		I_{CC2}		8.9	14.0	µA
	Refresh enable V_I = V_{CC1} (ISO7041); V_I = 0 V (ISO7041 with F suffix)	I_{CC1}		6.8	12.2	µA
		I_{CC2}		9.6	14.0	µA
	Refresh enable V_I = 0 V (ISO7041); V_I = V_{CC1} (ISO7041 with F suffix)	I_{CC1}		8.1	14.8	µA
		I_{CC2}		10.0	15.6	µA
Supply current - AC signal	Refresh disable 10 kbps, No Load	I_{CC1}		7.9	13.7	µA
		I_{CC2}		10.4	15.9	µA
	Refresh disable 100 kbps, No Load	I_{CC1}		35.9	48.3	µA
		I_{CC2}		22.7	31.4	µA
	Refresh disable 1 Mbps, No Load	I_{CC1}		316.4	395.7	µA
		I_{CC2}		147.2	188.2	µA
	Refresh enable 10 kbps, No Load	I_{CC1}		9.8	16.4	µA
		I_{CC2}		10.5	16.2	µA
	Refresh enable 100 kbps, No Load	I_{CC1}		35.9	48.3	µA
		I_{CC2}		22.7	31.4	µA
	Refresh enable 1 Mbps, No Load	I_{CC1}		315.3	395.7	µA
		I_{CC2}		146.2	188.2	µA
Total Supply Current Per Channel, Refresh Disabled	DC Signal	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.5	5.7	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.2	8.2	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		14.8	19.2	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		115.7	138.7	µA

Supply Current Characteristics 3.3V Supply (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Total Supply Current Per Channel, Refresh Enabled	$V_I = V_{CC1}$ (ISO7041); $V_I = 0$ V (ISO7041 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		4.2	6.8	µA
	$V_I = 0$ V (ISO7041); $V_I = V_{CC1}$ (ISO7041 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		4.6	7.7	µA
	10 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		5.2	8.2	µA
	100 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		14.8	19.2	µA
	1 Mbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		115.7	138.7	µA

8.13 Electrical Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -1mA	V_{CCO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA			0.2	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

8.14 Supply Current Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7041						
Supply current - DC signal	Refresh disable	I_{CC1}		4.7	8.2	µA
		I_{CC2}		8.6	13.0	µA
	Refresh enable V_I = V_{CC1} (ISO7041); V_I = 0 V (ISO7041 with F suffix)	I_{CC1}		6.4	10.9	µA
		I_{CC2}		9.2	13.0	µA
	Refresh enable V_I = 0 V (ISO7041); V_I = V_{CC1} (ISO7041 with F suffix)	I_{CC1}		7.6	13.2	µA
		I_{CC2}		9.6	14.6	µA
Supply current - AC signal	Refresh disable 10 kbps, No Load	I_{CC1}		8.2	12.2	µA
		I_{CC2}		10.0	14.8	µA
	Refresh disable 100 kbps, No Load	I_{CC1}		34.7	44.5	µA
		I_{CC2}		21.3	29.0	µA
	Refresh disable 1 Mbps, No Load	I_{CC1}		301.5	367.4	µA
		I_{CC2}		137.0	173.3	µA
	Refresh enable 10 kbps, No Load	I_{CC1}		9.9	14.6	µA
		I_{CC2}		10.0	15.9	µA
	Refresh enable 100 kbps, No Load	I_{CC1}		34.7	44.5	µA
		I_{CC2}		21.3	29.0	µA
	Refresh enable 1 Mbps, No Load	I_{CC1}		304.8	367.4	µA
		I_{CC2}		136.0	173.3	µA
Total Supply Current Per Channel, Refresh Disabled	DC Signal	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.3	5.3	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.0	7.5	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		14.0	17.6	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		110.0	127.1	µA
Total Supply Current Per Channel, Refresh Enabled	V_I = V_{CC1} (ISO7041); V_I = 0 V (ISO7041 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.0	6.2	µA
	V_I = 0 V (ISO7041); V_I = V_{CC1} (ISO7041 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.4	7.0	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.0	7.5	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		14.0	17.6	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		110	127.1	µA

8.15 Switching Characteristics

V_{CC1}, V_{CC2} = 2.25 V to 5.5 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 9		140	165	ns
$t_{P(dft)}$	Propagation delay drift			15		ps/℃
t_{UI}	Minimum pulse width	See 図 9	500			ns
PWD	Pulse width distortion				10	ns
$t_{sk(o)}$	Channel to channel output skew time	Same-direction channels			10	ns
		Opposite-direction channels			10	ns
$t_{sk(p-p)}$	Part to part skew time				70	ns
t_r	Output signal rise time	See 図 9			5	ns
t_f	Output signal fall time				5	ns
t_{DO}	Default output delay time from input power loss	Refresh enabled, See 図 10		400	750	us
t_{PU}	Time from UVLO to valid output data		1		5	ms
F_R	Refresh rate		5	10		kbps

8.16 Insulation Characteristics Curves

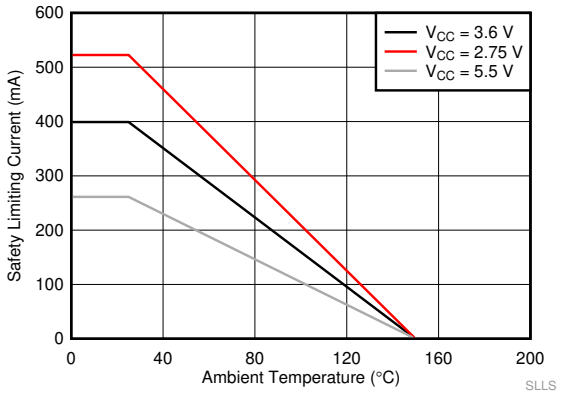


図 1. Thermal Derating Curve for Limiting Current per VDE

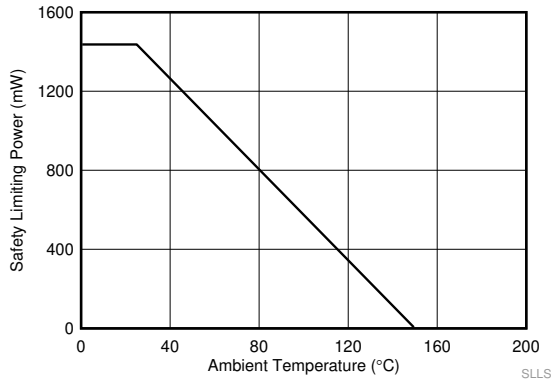
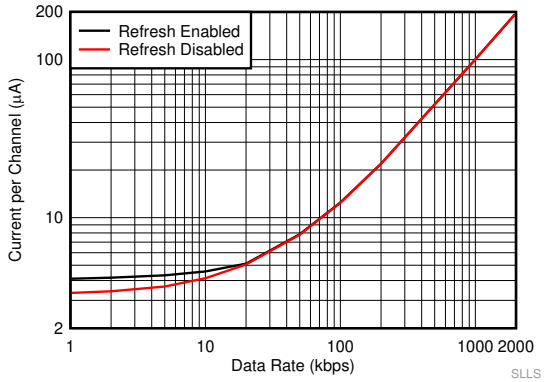


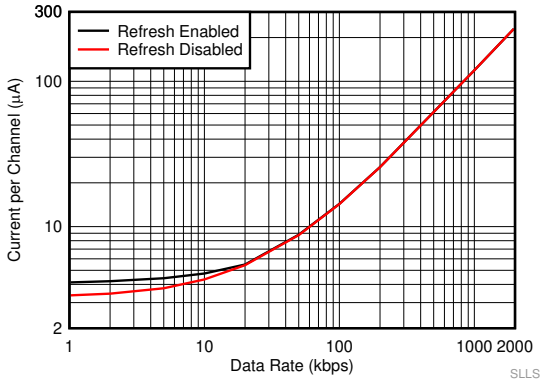
図 2. Thermal Derating Curve for Limiting Power per VDE

8.17 Typical Characteristics



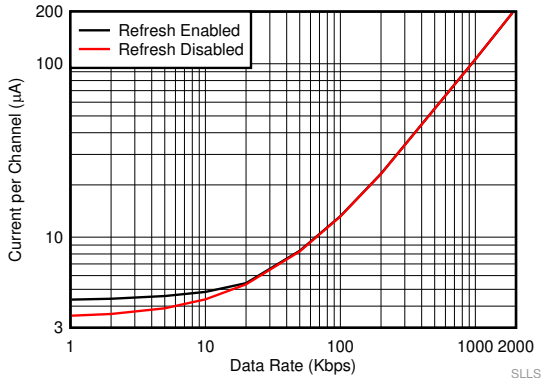
T_A = 25°C C_L = 0 pF

図 3. ISO7041 Supply Current vs Data Rate at 2.5 V (With No Load)



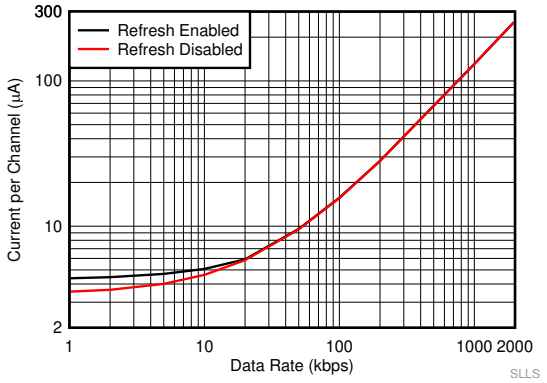
T_A = 25°C C_L = 15 pF

図 4. ISO7041 Supply Current vs Data Rate at 2.5 V (With 15-pF Load)



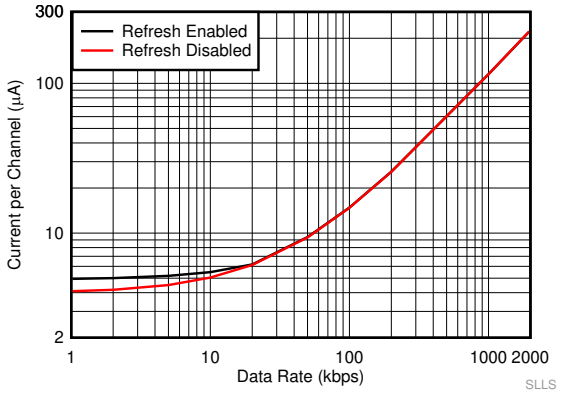
T_A = 25°C C_L = 0 pF

図 5. ISO7041 Supply Current vs Data Rate at 3.3 V (With No Load)



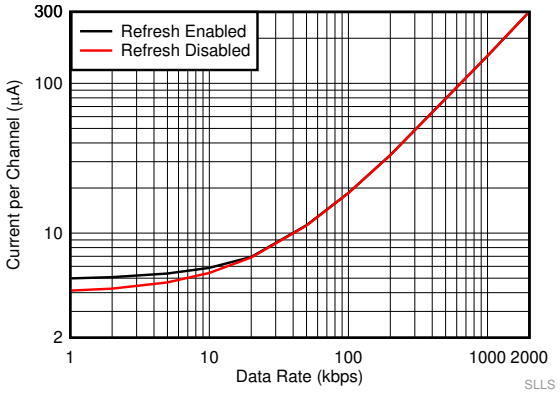
T_A = 25°C C_L = 15 pF

図 6. ISO7041 Supply Current vs Data Rate at 3.3 V (With 15-pF Load)



T_A = 25°C C_L = 0 pF

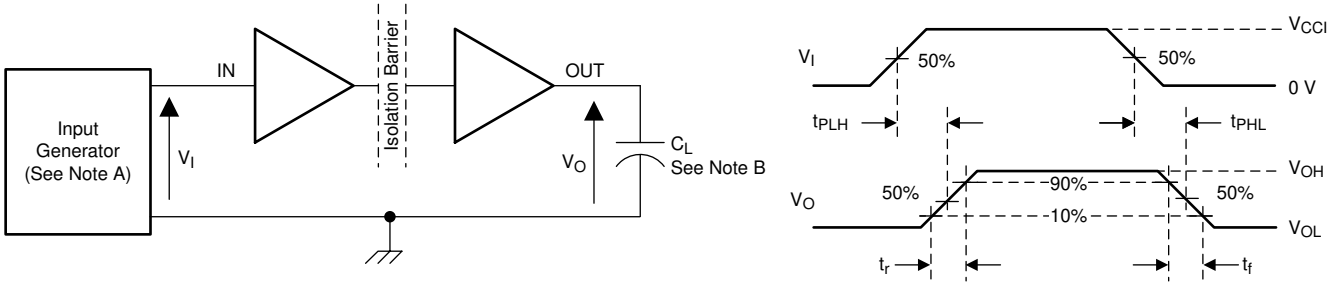
図 7. ISO7041 Supply Current vs Data Rate at 5 V (With No Load)



T_A = 25°C C_L = 15 pF

図 8. ISO7041 Supply Current vs Data Rate at 5 V (With 15-pF Load)

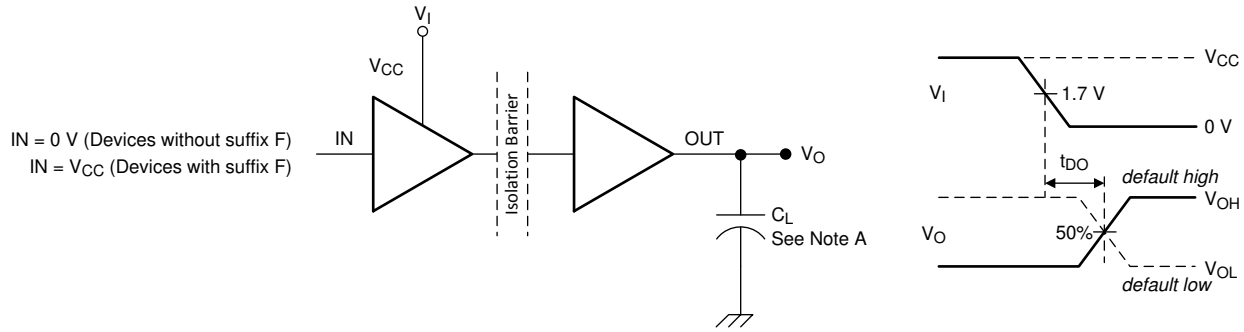
9 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

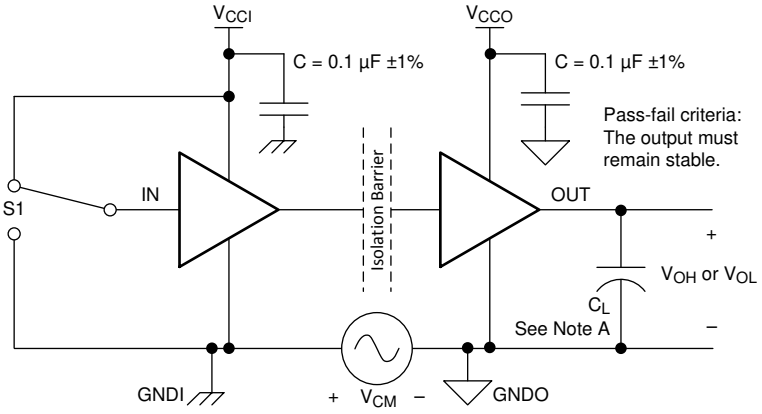
図 9. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

図 10. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 11. Common-Mode Transient Immunity Test Circuit

10 Detailed Description

10.1 Overview

The ISO7041 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. The ENx pins of side A and side B must be tied low to enable refresh or high to disable refresh. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 12, shows a functional block diagram of a typical channel.

10.2 Functional Block Diagram

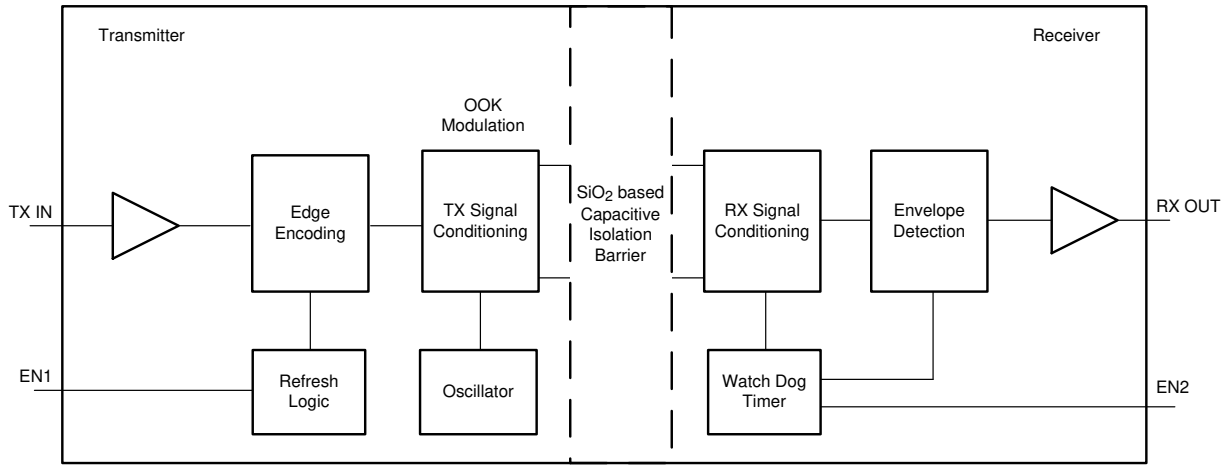


図 12. Conceptual Block Diagram of a Digital Capacitive Isolator

10.3 Feature Description

10.3.1 Refresh Enable

The ISO7041 uses an edge based encoding scheme to transfer an input signal change across the isolation barrier versus sending across the DC state. consistently validates that the DC output state of each isolator channel matches the DC input state. An internal watchdog timer monitors for activity on the individual inputs and transmits the logic state when there is no input signal transition for more than 100 µs. This ensures that the input and output state of the isolator always match. Tie both EN1 and EN2 to their respective grounds to enable refresh.

Disable refresh by tying both EN1 and EN2 to their respective VCC power supplies. Disabling refresh will further decrease the power consumption of the device but the DC state is not guaranteed at startup. System level solutions can be implemented to ensure the isolator channel output matches the input at startup. For example, at start up, an immediate full transition of the input signals from high to low and low to high on the individual isolator lines would allow the states of the outputs to properly track the inputs.

Feature Description (continued)

10.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO70xx family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

The device has no issue being able to meet either CISPR 22 Class A and CISPR22 Class B standards in an unshielded environment.

10.4 Device Functional Modes

表 2 shows the functional modes for the device.

表 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	REFRESH ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	L	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	L	
		X	H	Undetermined	The device needs an input signal transition to validate the output tracks the input state. Without a signal edge transition, the output will be in an undetermined state.
PD	PU	X	L	Default	When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for the device without the F suffix and *Low* for device with the F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
			H	Undetermined	When V_{CCI} is unpowered, a channel output assumes the logic state based on the previous state of the output before V_{CCI} powered down.
X	PD	X	L	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.
			H	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the selected default option.
X	X	X	Open	Undetermined	When ENx is unconnected or open, the device output will be in an undetermined and unknown state. ENx must be connected high or low for the device to behave correctly.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.54); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 2.25 V < V_{CCI}, V_{CCO} < 2.25 V.

10.4.1 Device I/O Schematics

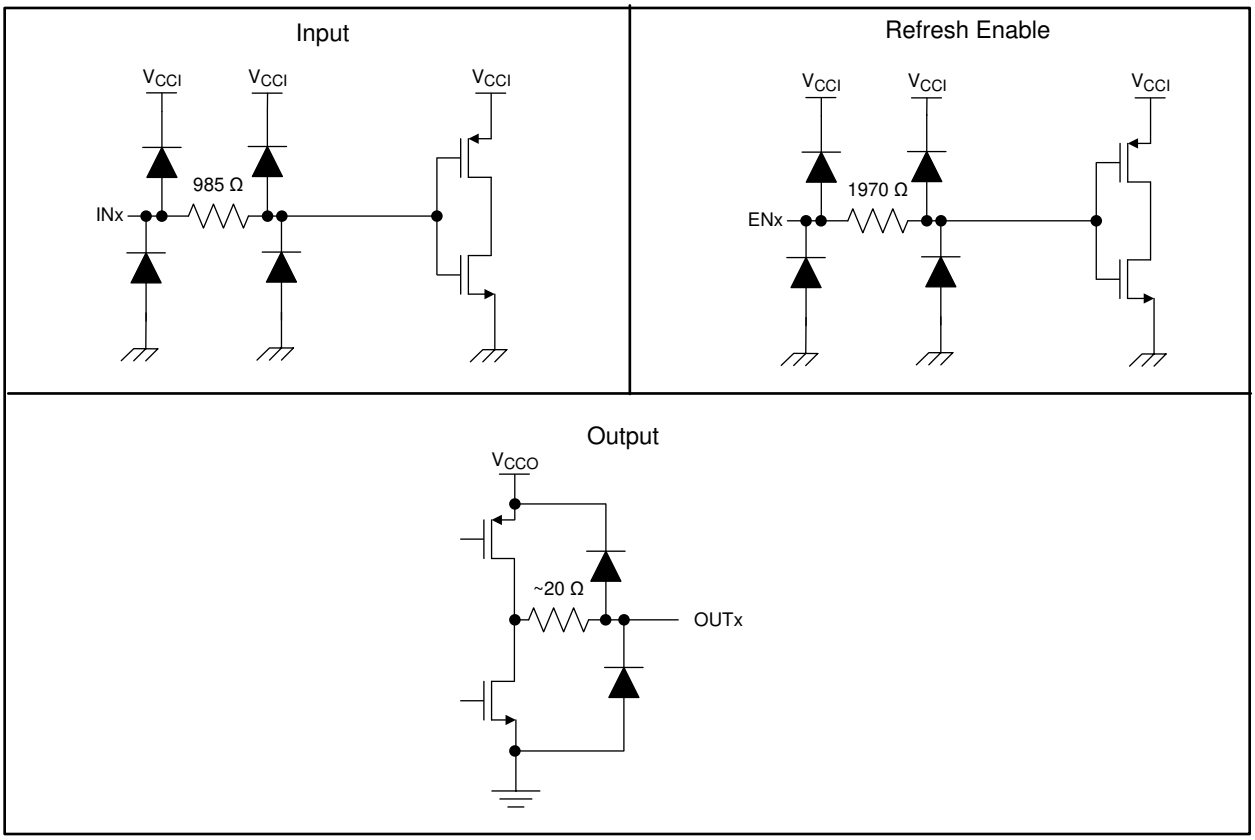


図 13. Device I/O Schematics

11 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The ISO7041 device is an ultra-low power digital isolator. The device uses single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}, and can be set irrespective of one another. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard. See *Isolated power and data interface for low-power applications reference design* TI Design for detailed information on designing the ISO70xx in low-power applications.

11.1.1 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see 図 14 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm) and a minimum insulation lifetime of 20 years. VDE standard also requires additional safety margin of 20% for working voltage and 87.5% for insulation lifetime which translates into minimum required life time of 37.5 years.

図 15 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of these devices is 400 VRMS with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, and so forth can further limit the working voltage of the component. The working voltage of the DBQ-16 package specified up to 400 VRMS. At the lower working voltages, the corresponding insulation barrier life time is much longer.

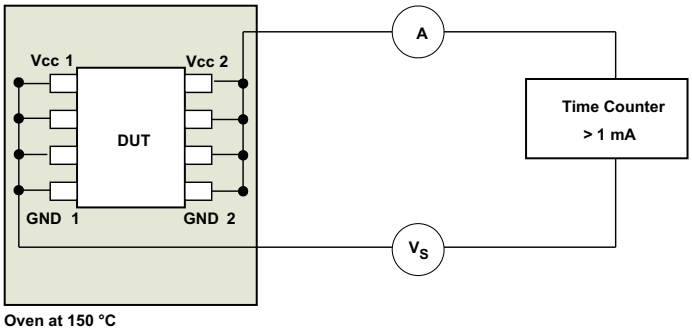


図 14. Test Setup for Insulation Lifetime Measurement

Application Information (continued)

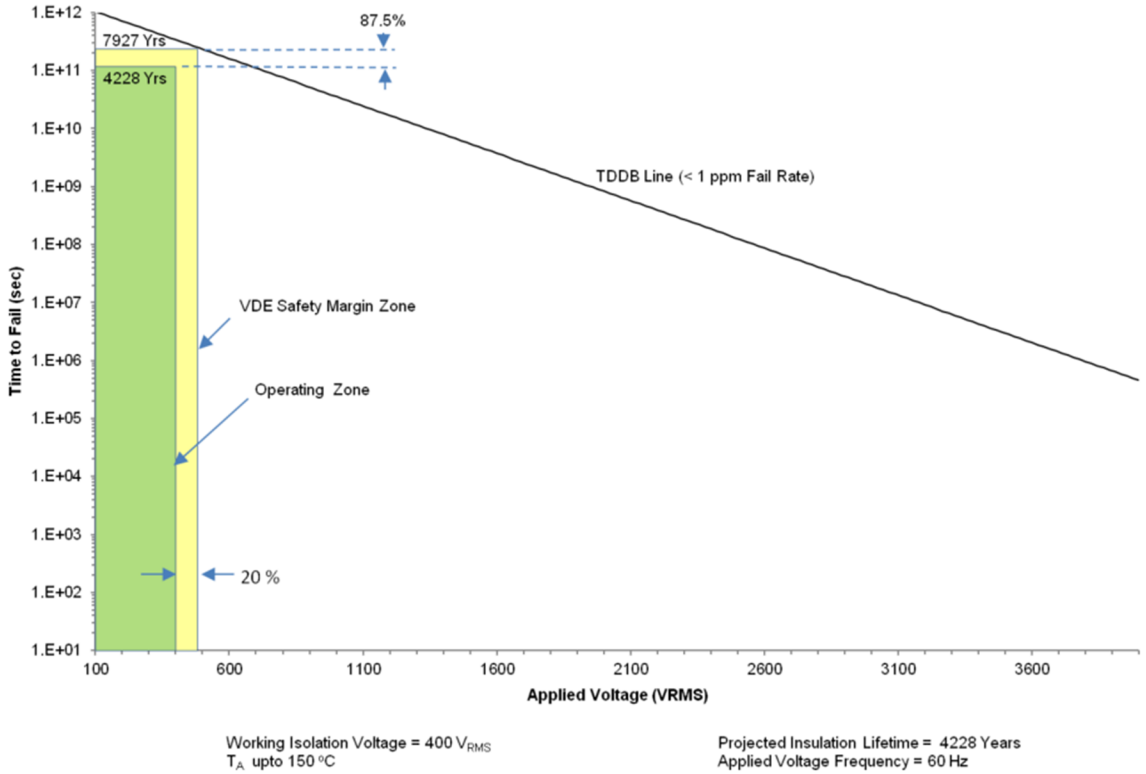


図 15. Insulation Lifetime Projection Data

11.2 Typical Application

図 16 shows the isolated serial peripheral interface (SPI).

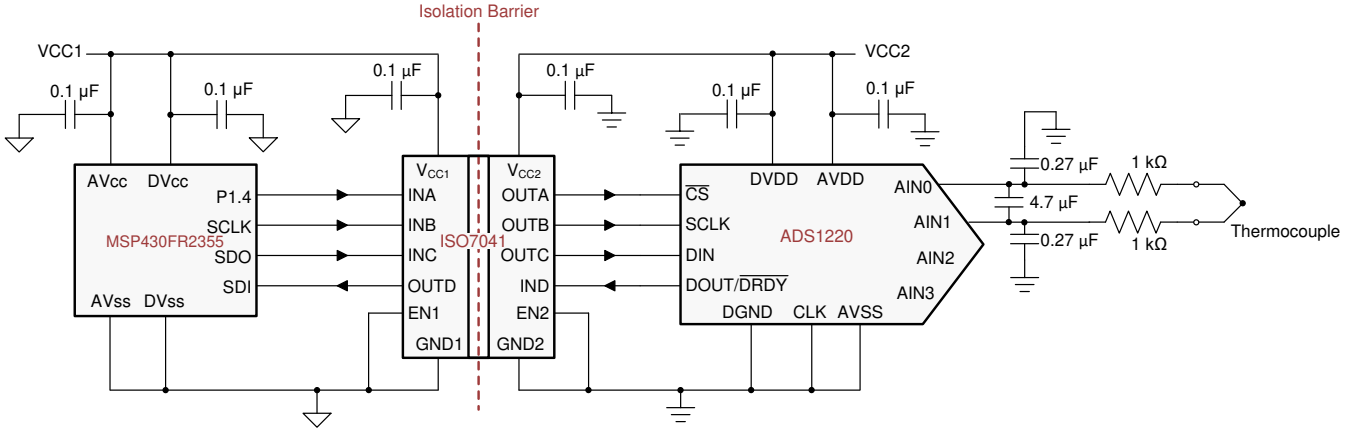


図 16. Isolated SPI for a Temperature Field Transmitter

Typical Application (continued)

11.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 3.

表 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

11.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the device only require two external bypass capacitors to operate.

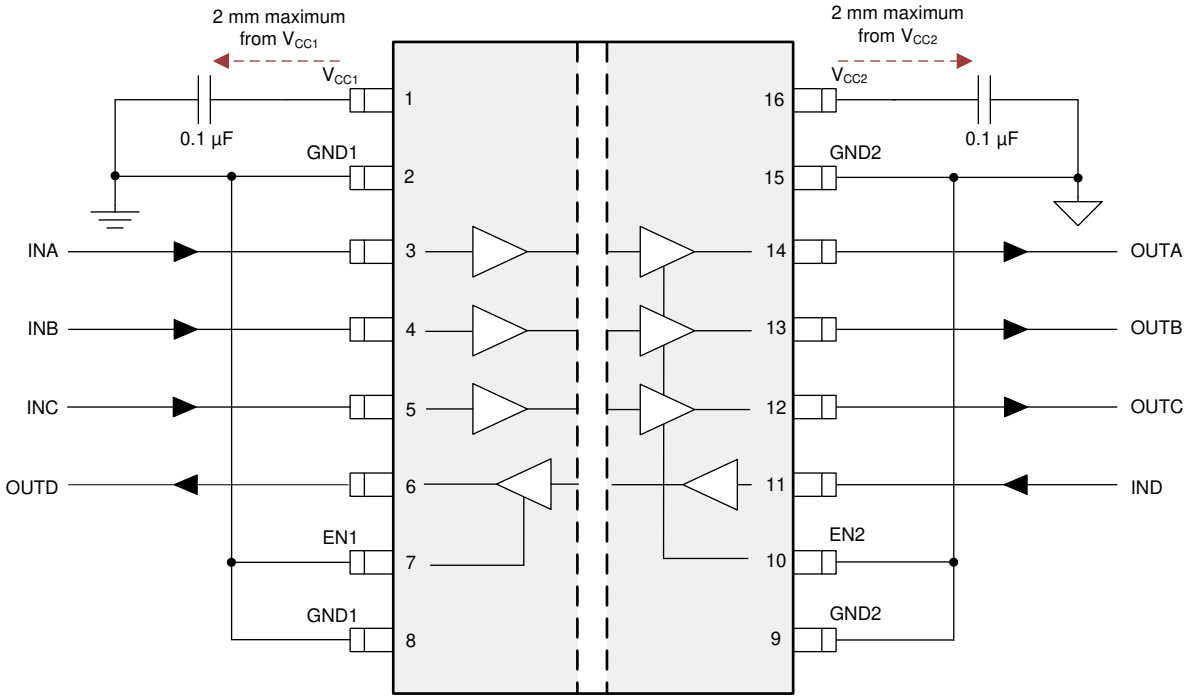


図 17. Typical ISO7041 Circuit Hook-up

11.2.3 Application Curves

The following typical eye diagrams of the device indicates wide open eye at the maximum data rate of 2 Mbps.

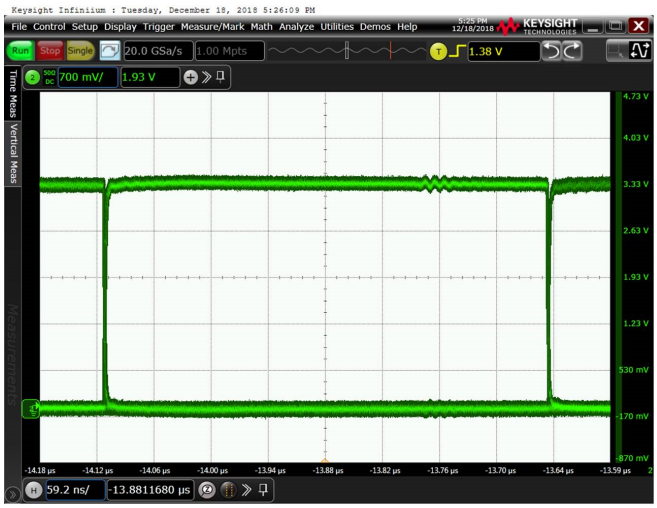


図 18. Eye Diagram at 2 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

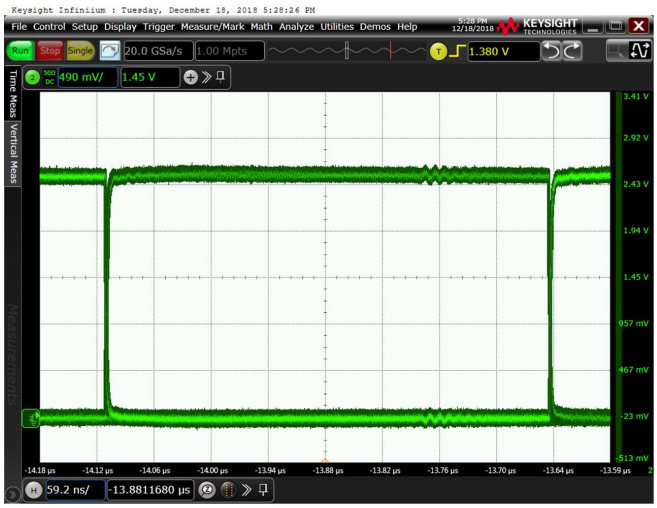


図 19. Eye Diagram at 2 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

12 Power Supply Recommendations

Put a 0.1-µF bypass capacitor at the input and output supply pins (V_{CC1} and V_{CC2}) to make sure that operation is reliable at data rates and supply voltage. Put the capacitors as near to the supply pins as possible. If only one primary-side power supply is available in an application, use a transformer driver to help generate the isolated power for the secondary-side. Texas Instruments recommends the SN6501 device or SN6505A device. Refer to the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet for detailed power supply design and transformer selection recommendations.

13 Layout

13.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 20). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations,.

13.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

13.2 Layout Example

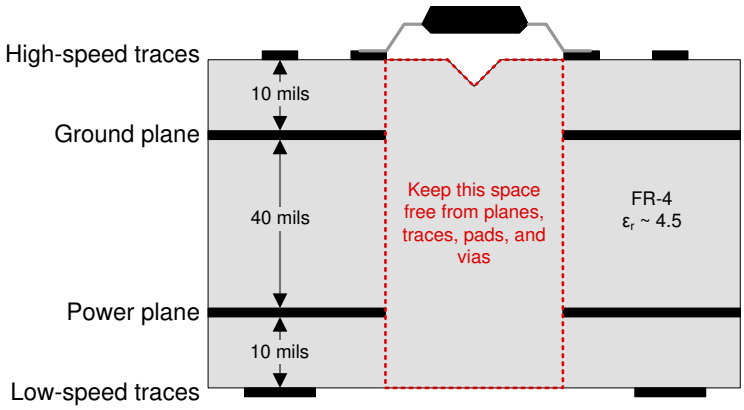


Figure 20. Recommended Layer Stack

14 デバイスおよびドキュメントのサポート

14.1 ドキュメントのサポート

14.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『デジタル・アイソレータ設計ガイド』*
- テキサス・インスツルメンツ、*『絶縁の用語集』*
- テキサス・インスツルメンツ、*『ADS1220　4チャネル、2kSPS、低消費電力、24ビットADC、PGAおよび基準電圧搭載』*データシート
- テキサス・インスツルメンツ、*『ADS122U04　24ビット、4チャネル、2kSPS、デルタ・シグマADC、UARTインターフェイス付き』*データシート
- テキサス・インスツルメンツ、*『ADS124S0x低消費電力、低ノイズ、高度統合、6および12チャネル、4kSPS、24ビット、デルタ-シグマADC、PGAおよび基準電圧搭載』*データシート
- テキサス・インスツルメンツ、*『超低消費電力および低消費電力アプリケーション用の独自の高効率絶縁型DC/DCコンバータ』*TI Design
- テキサス・インスツルメンツ、*『SN6501 絶縁電源用の変圧器ドライバ』*データシート
- テキサス・インスツルメンツ、*『SN6505A 絶縁電源用の低ノイズ、1Aの変圧器ドライバ』*データシート
- テキサス・インスツルメンツ、*『低消費電力アプリケーション用の絶縁型電源およびデータ・インターフェイスのリファレンス・デザイン』*TI Design

14.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

14.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.4 商標

E2E is a trademark of Texas Instruments.

14.5 静電気放電に関する注意事項

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14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7041DBQ	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7041
ISO7041DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7041
ISO7041FDBQ	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7041F
ISO7041FDBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7041F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ISO7041 :

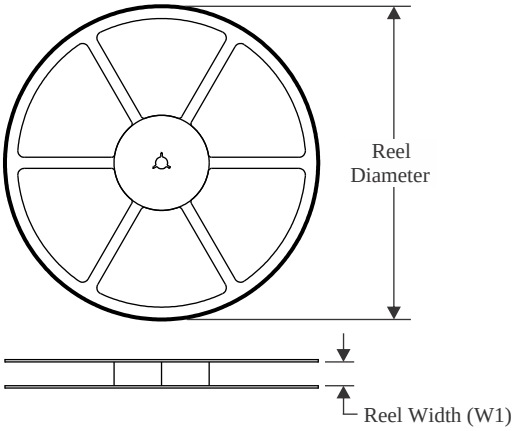
- Automotive : ISO7041-Q1

NOTE: Qualified Version Definitions:

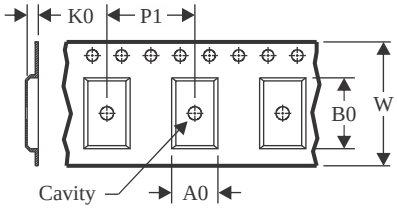
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

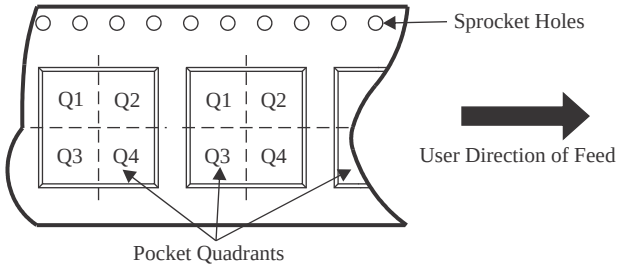


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

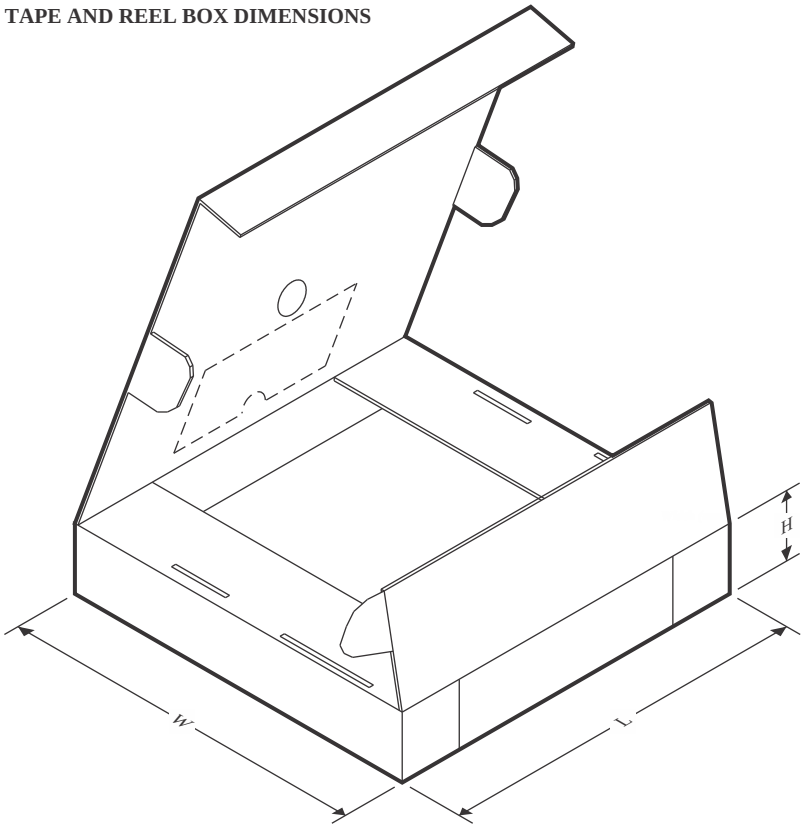
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7041DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7041FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

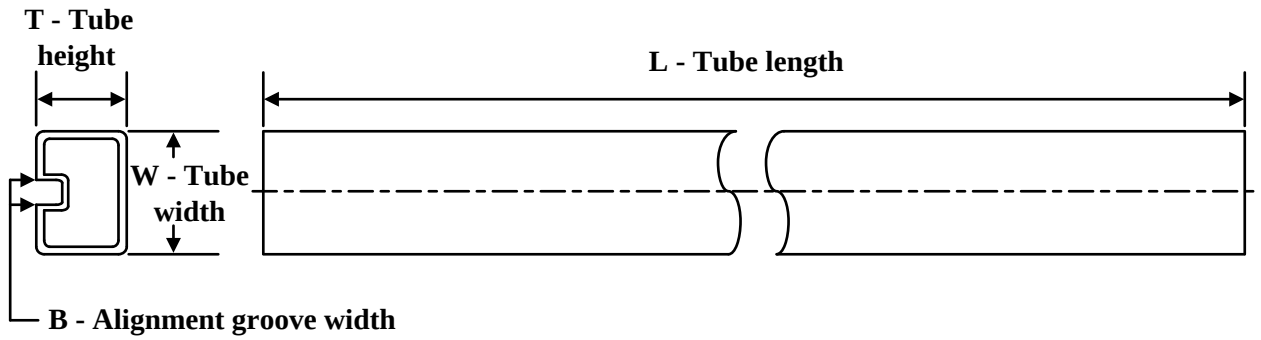
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

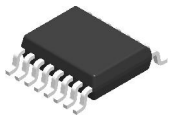
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7041DBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7041FDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7041DBQ	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7041FDBQ	DBQ	SSOP	16	75	505.46	6.76	3810	4

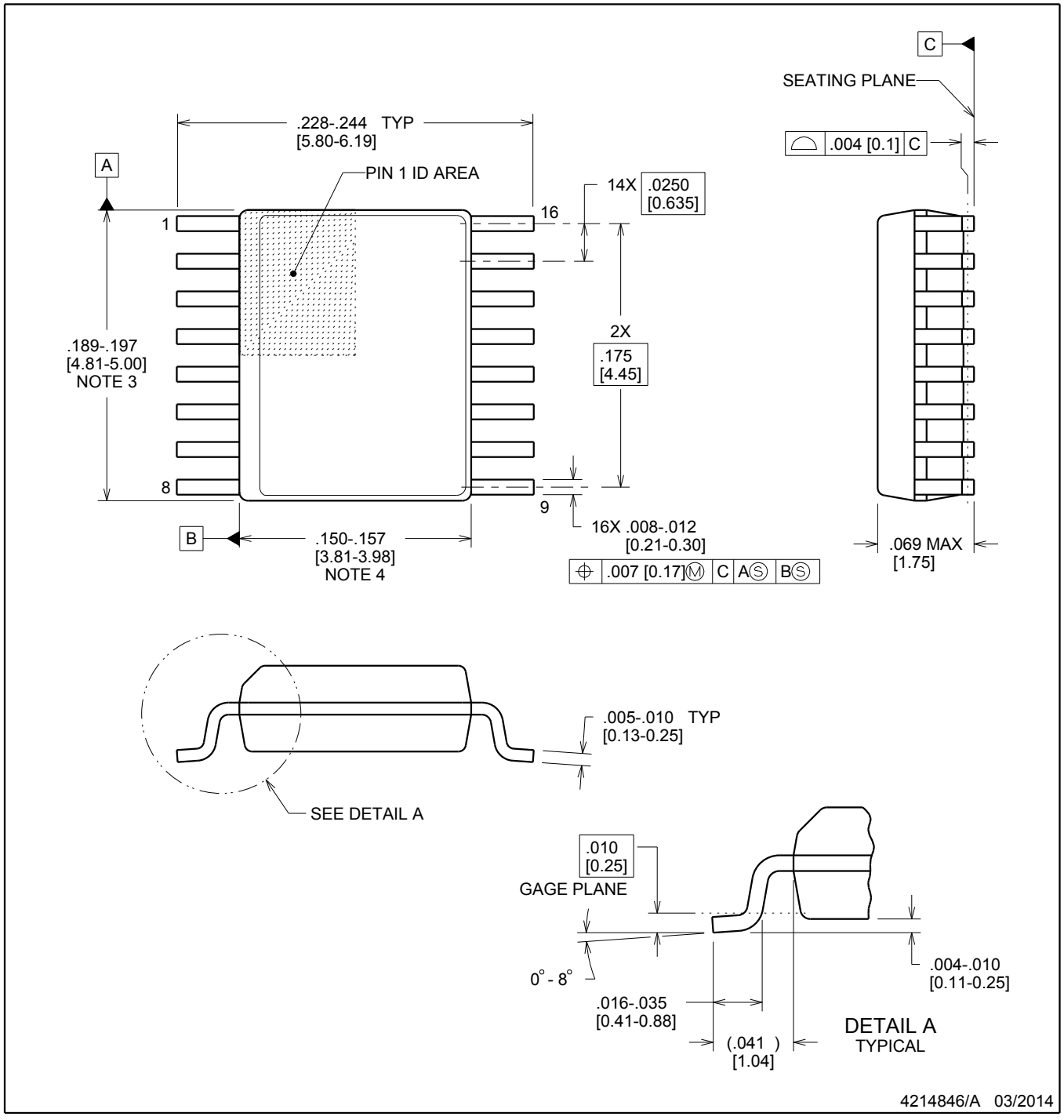


PACKAGE OUTLINE

DBQ0016A

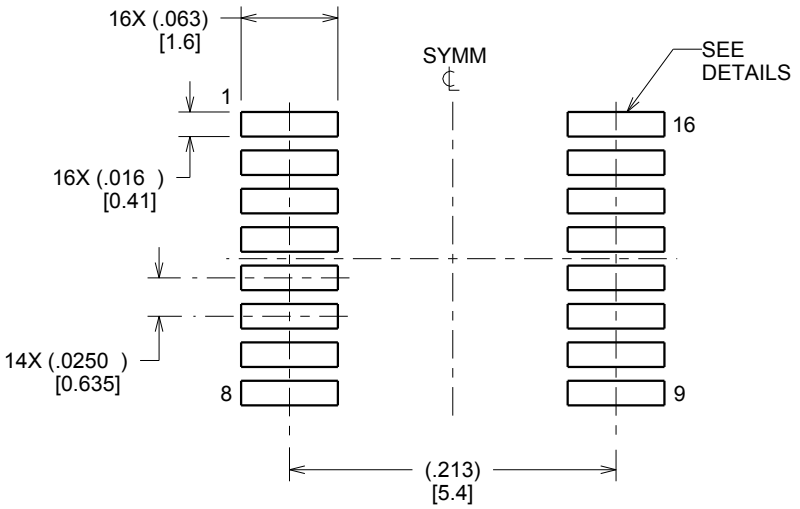
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

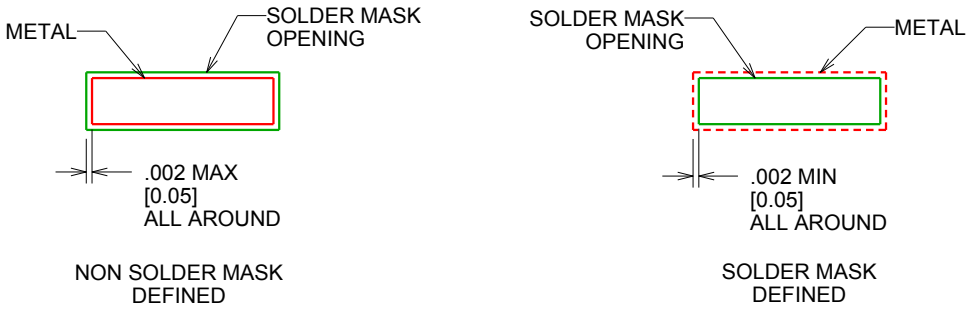


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

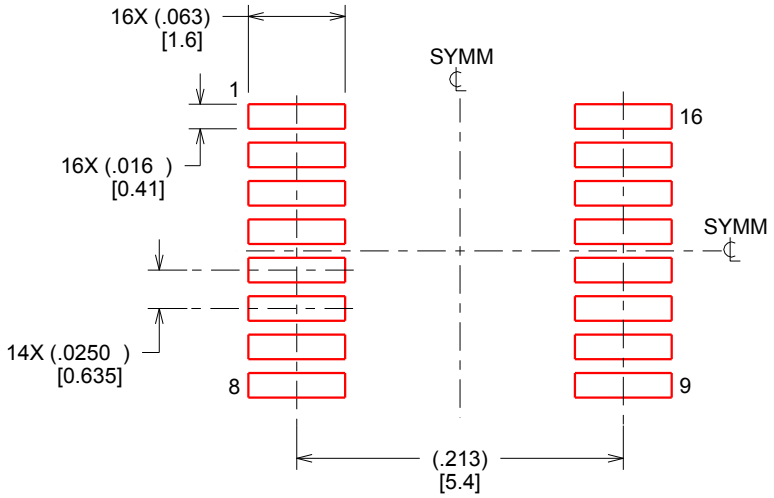
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月