LDC1001-Q1 インダクタンス-デジタル・コンバータ

1 特長

- **車載アプリケーション用にAEC-Q100認定済み:**
  - 温度グレード 0: -40°C～150°C、T_A
- **磁石を使用しない動作**
- **サブミクロン単位の精度**
- **コイルの設計により検出範囲を調整可能**
- **システム・コストの低減**
- **離れた場所にセンサを配置可能 (過酷な環境から LDC を隔離)**
- **非接触動作による高い耐久性**
- **周囲からの干渉 (埃、塵、水、油など) に対する非感受性**
- **電源電圧 (アナログ) : 4.75V～5.25V**
- **電源電圧 (IO) : 1.8V～5.25V**
- **消費電流 (LC タンクなし) : 1.7mA**
- **R_P 分解能 : 16 ビット**
- **L 分解能 : 24 ビット**
- **LC 周波数範囲 : 5kHz～5MHz**

2 アプリケーション

- **タッチ・ボタン**
- **角度位置検出**
- **直線位置検出**
- **金属の近接検出**

3 概要

LDC1001-Q1 デバイスは、並列抵抗 (Rp) およびインダクタンス (L) 測定用に設計された、4.75V～5.25V 動作の車載認定済みインダクタンス-デジタル・コンバータです。誘導性センシング技術により、車載用および産業用アプリケーションにおいて、金属製ターゲットの直線位置または角度位置を正確に測定できます。

誘導性センシングは、埃、塵、油、湿気が存在する環境で導電性ターゲットを高分解能で検出できる非接触式短距離センシング技術です。この技術は、過酷環境の用途で使用できます。

LDC1001-Q1 システムは、誘導型センサ (通常は PCB コイル) と導電性ターゲットで構成されます。

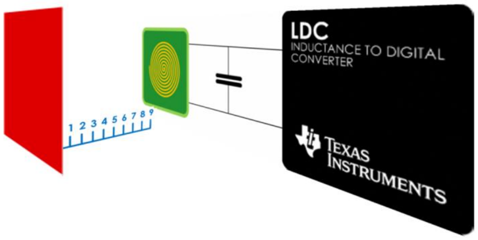
LDC1001-Q1 は 16 ピン TSSOP パッケージで供給され、複数の動作モードを備えています。シリアル・ペリフェラル・インターフェイス (SPI) を備えているため MCU と簡単に接続できます。

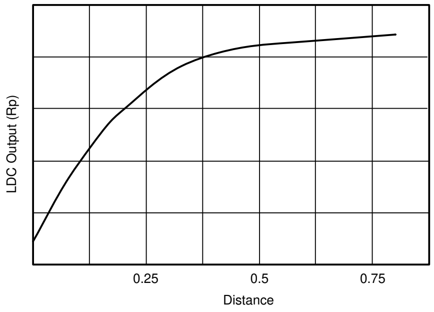
製品情報(1)

型番	パッケージ	本体サイズ(公称)
LDC1001-Q1	TSSOP (16)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション — 軸方向距離検出





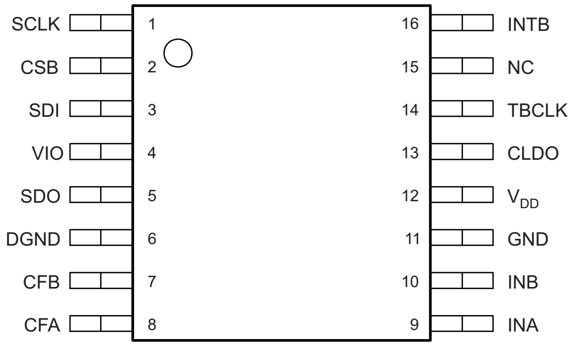
目次

4 改訂履歴

日付	バージョン	注
2019 年 11 月	*	初版

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	SCLK	DI	SPI clock input. The SCLK pin is used to clock-out and clock-in the data from or into the chip
2	CSB	DI	SPI CSB. Multiple devices can be connected on the same SPI bus and the CSB pin can be used to select which device is communicated with.
3	SDI	DI	SPI Slave Data In (Master Out Slave In). This pin should be connected to the Master Out Slave In of the master device.
4	VIO	P	Digital IO Supply
5	SDO	DO	SPI Slave Data Out (Master In Slave Out). This pin is high-Z when the CSB pin is high.
6	DGND	P	Digital ground
7	CFB	A	LDC filter capacitor
8	CFA	A	LDC filter capacitor
9	INA	A	External LC Tank. Connect this pin to an external LC tank.
10	INB	A	External LC Tank. Connect this pin to an external LC tank.
11	GND	P	Analog ground
12	V_{DD}	P	Analog supply
13	CLDO	A	LDO bypass capacitor. Connect a 56-nF capacitor from this pin to GND.
14	TBCLK	DI	External time-base clock
15	NC	NC	This pin should be floating.
16	INTB	DO	Configurable interrupt. This pin can be configured to function in three different ways (threshold detect, wake-up, or DRDYB) by programing the INT pin mode register.

(1) DO: Digital Output, DI: Digital Input, P: Power, A: Analog

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Analog supply voltage	V_{DD} – GND		5.5	V
IO supply voltage	VIO – GND		5.5	V
Voltage	On any pin	–0.3	V_{DD} + 0.3	V
	On any digital pin	–0.3	V_{IO} + 0.3	V
Input Current	INA and INB		8	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM Classification Level C6	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Analog supply voltage (V_{DD} – GND)	4.75	5.25	V
V_{IO}	IO supply voltage (VIO – GND)	1.8	5.25	V
	V_{DD} – VIO	≥0		V
T_A	Operating temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		LDC1001-Q1	UNIT
		PW (TSSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V_{DD} = 5 V, V_{IO} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
V_{DD}	Analog supply voltage		4.75	5	5.25	V
V_{IO}	IO supply voltage	$V_{IO} \leq V_{DD}$	1.8	3.3	5.25	V
I_{DD}	Supply current	Does not include the LC tank current		1.7	2.3	mA
I_{IO}	IO supply current	Static current			14	µA
$I_{DD(LP)}$	Low-power mode supply current	Without LC tank		250		µA
$t_{(start)}$	Start-up time	From POR to ready-to-convert.		2		ms
LDC						
f_{sensor_min}	Minimum sensor frequency			5		kHz
f_{sensor_max}	Maximum sensor frequency			5		MHz
A_{sensor_min}	Minimum sensor amplitude			1		V_{PP}
A_{sensor_max}	Maximum sensor amplitude			4		V_{PP}
t_{rec}	Recovery time	Oscillation start-up time after RP under-range condition		10		1 / f_{sensor}
Z_{RP_min}	Minimum sensor RP range			798		Ω
R_{RP_max}	Maximum sensor RP range			3.93		MΩ
R_{RP_res}	RP measurement resolution			16		Bits
$t_{res(min)}$	Minimum response time	Minimum programmable settling time of digital filter		192 × 1 / f_{sensor}		s
$t_{res(max)}$	Maximum response time	Maximum programmable settling time of digital filter		6144 × 1 / f_{sensor}		s
EXTERNAL CLOCK FOR FREQUENCY COUNTER						
	External clock frequency				8	MHz
	External clock input high voltage				V_{IO}	V
DIGITAL I/O CHARACTERISTICS						
V_{IH}	Logic 1 input voltage		0.8 × V_{IO}			V
V_{IL}	Logic 0 input voltage				0.2 × V_{IO}	V
V_{OH}	Logic 1 output voltage	$I_{(SOURCE)}$ = 400 µA		V_{IO}– 0.3		V
V_{OL}	Logic 0 output voltage	$I_{(SINK)}$ = 400 µA			0.3	V
I_{lkgIO}	Digital IO leakage current		–500		500	nA

6.6 Timing Requirements

Unless otherwise noted, all limits specified at T_A = 25°C, V_{DD} = 5 V, V_{IO} = 3.3 V, 10-pF capacitive load in parallel with a 10-kΩ load on the SDO. Specified by design; not production tested. See Figure 1

			MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency	See Figure 1			4	MHz
t_{wH}	SCLK pulse-width high	f_{SCLK} = 4 Mhz, See Figure 1	0.4 / f_{SCLK}			s
t_{wL}	SCLK pulse-width low	f_{SCLK} = 4 Mhz, See Figure 1	0.4 / f_{SCLK}			s
t_{su}	SDI setup time	See Figure 1	10			ns
t_h	SDI hold time		10			ns
t_{ODZ}	SDO driven-to-tristate time	Measured at 10% / 90% point, See Figure 2			20	ns
t_{OZD}	SDO tristate-to-driven time	Measured at 10% / 90% point, See Figure 2			20	ns
$t_{d(OUTPUT)}$	SDO output delay time	See Figure 2			20	ns
$t_{su(CS)}$	CSB setup time		20			ns
$t_{h(CS)}$	CSB hold time		20			ns
t_{IAG}	inter-access gap	See Figure 16	100			ns
$t_{w(DRDY)}$	Data ready pulse width	Data ready pulse at every 1 / ODR if no data is read		1 / f_{sensor}		s

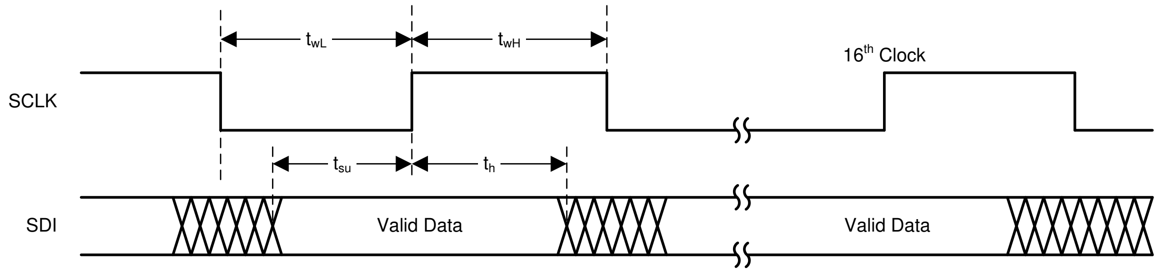


Figure 1. Write Timing Diagram

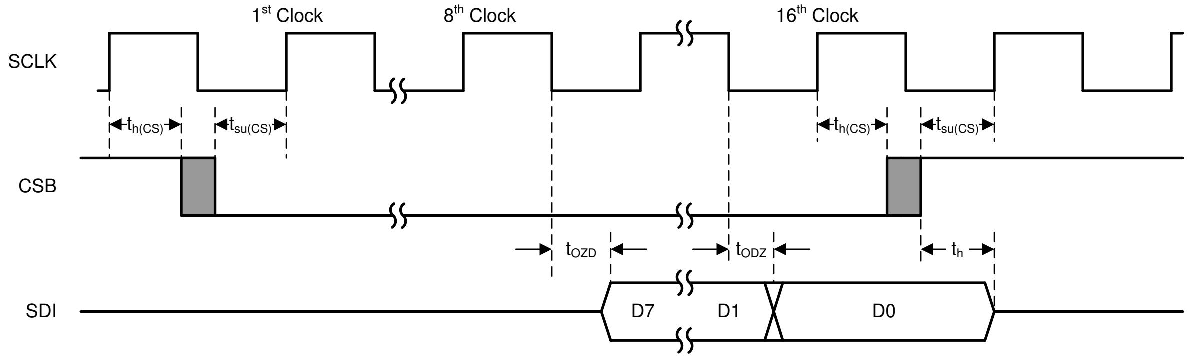
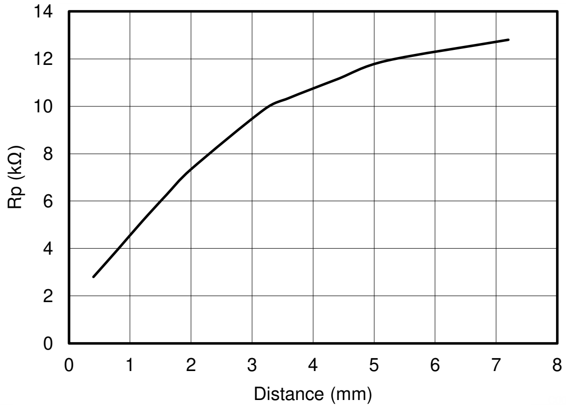


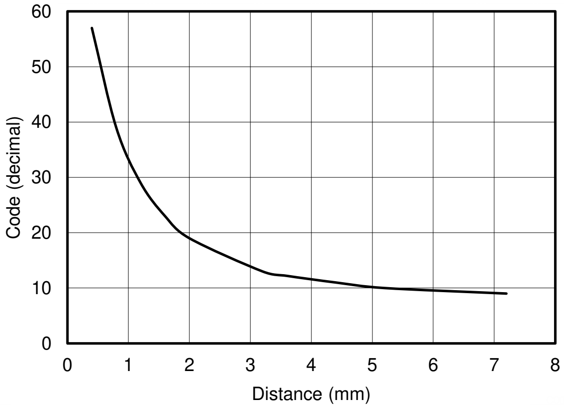
Figure 2. Read Timing Diagram

6.7 Typical Characteristics



Sensor Details: Table 21
Target Material: Stainless Steel
Rp_MIN: 1.347 kΩ
Rp_MAX: 38.785 kΩ

Figure 3. R_P vs Distance



Sensor Details: Table 21
Target Material: Stainless Steel
Rp_MIN: 1.347 kΩ
Rp_MAX: 38.785 kΩ

Figure 4. Proximity Data vs Distance

7 Detailed Description

7.1 Overview

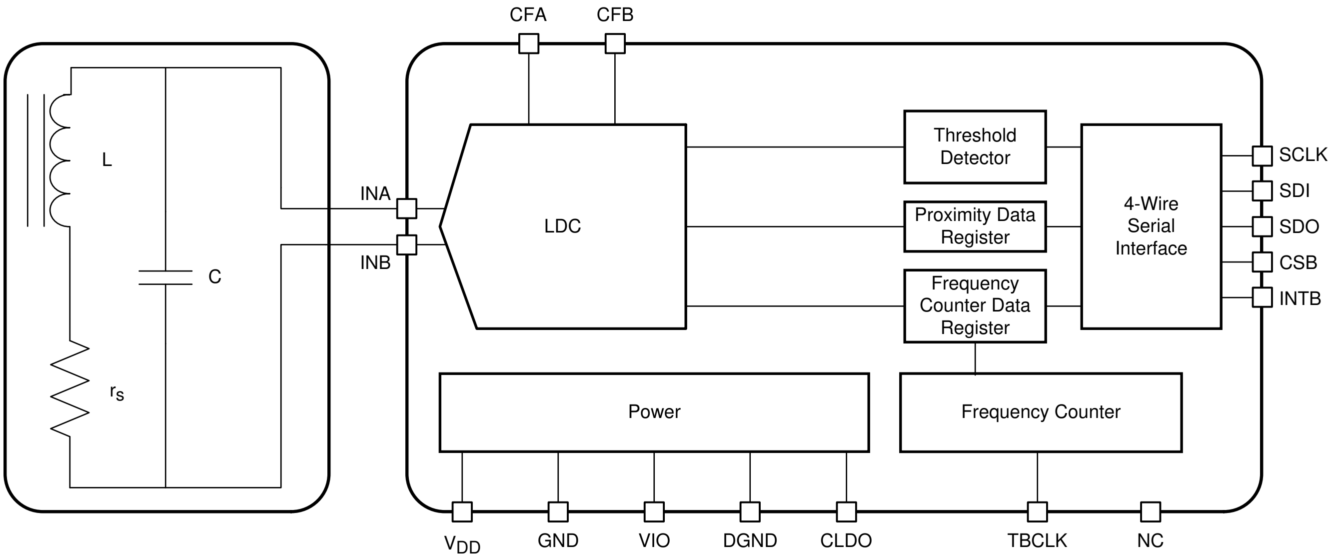
The LDC1001-Q1 device is an inductance-to-digital converter that simultaneously measures the impedance and resonant frequency of an LC resonator. The device accomplishes this task by regulating the oscillation amplitude in a closed-loop configuration to a constant level, while monitoring the energy dissipated by the resonator. By monitoring the amount of power injected into the resonator, the LDC1001-Q1 device can determine the value of R_P. When the value is determined, the device returns this as a digital value which is inversely proportional to R_P. In addition, the LDC1001-Q1 device also measure the oscillation frequency of the LC circuit. This frequency is used to determine the inductance of the LC circuit. The device outputs a digital value that is inversely proportional to frequency.

The threshold detector block provides a comparator with hysteresis. With the threshold registers programed and comparator enabled, the proximity data register is compared with threshold registers and INTB pin indicates the output.

The device has a simple 4-wire SPI interface. The INTB pin provides multiple functions which are programmable with SPI.

The device has separate analog and I/O supplies. The analog supply operates at 5 V and the I/O operates at 1.8 to 5 V. The integrated LDO requires a 56-nF capacitor connected from the CLDO pin to GND.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inductive Sensing

An alternating current (AC) flowing through a coil generates an AC magnetic field. If a conductive material, such as a metal target, is brought into the vicinity of the coil, this magnetic field induces circulating currents (eddy currents) on the surface of the target. These eddy currents are a function of the distance, size, and composition of the target. These eddy currents then generate a magnetic field that opposes the original field generated by the coil. This mechanism is best compared to a transformer, where the coil is the primary core and the eddy current is the secondary core. The inductive coupling between both cores depends on distance and shape. Hence the resistance and inductance of the secondary core (eddy current), shows up as a distant dependent resistive and inductive component on the primary side (coil). Figure 5 through Figure 8 show a simplified circuit model.

Feature Description (continued)

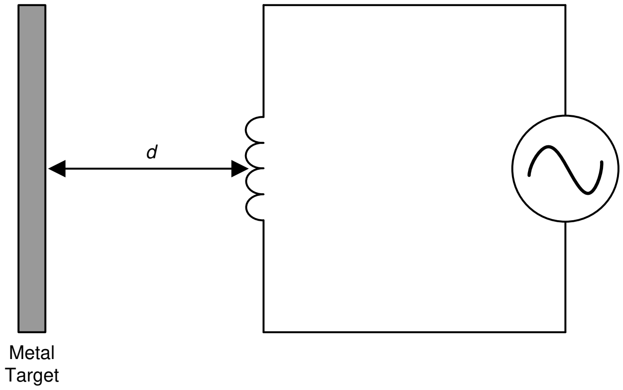


Figure 5. Inductor With a Metal Target

Eddy currents generated on the surface of the target can be modeled as a transformer as shown in Figure 6. The coupling between the primary and secondary coils is a function of the distance and characteristics of the conductor. In Figure 6, the inductance L_s is the inductance of the coil, and r_s is the parasitic series resistance of the coil. The inductance L(d), which is a function of distance, *d*, is the coupled inductance of the metal target. Likewise, R(d) is the parasitic resistance of the eddy currents.

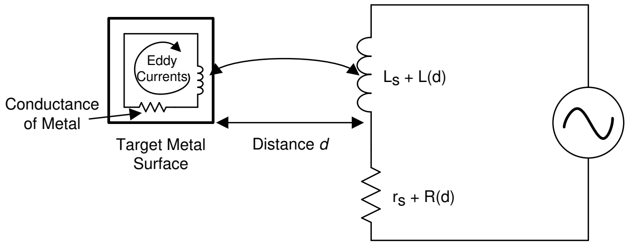


Figure 6. Metal Target Modeled as L and R With Circulating Eddy Currents

Generating an alternating magnetic field with just an inductor consumes a large amount of power. This power consumption can be reduced by adding a parallel capacitor, turning the right part of Figure 6 into a resonator as shown in Figure 7. In this manner the power consumption is reduced to the eddy and inductor losses r_s + R(d) only.

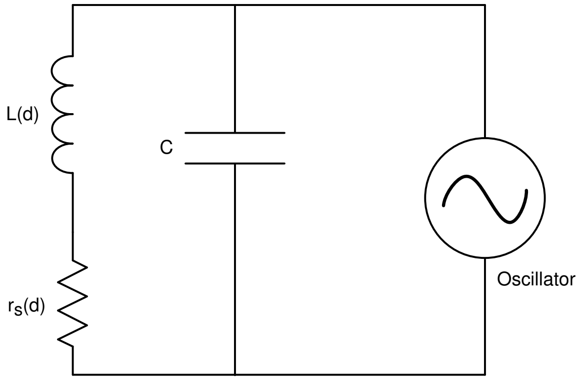


Figure 7. LC Tank Connected to Oscillator

The LDC1001-Q1 device does not directly measure the series resistance. Instead, the device measures the equivalent parallel resonance impedance R_P (see Figure 8). This representation is equivalent to the representation shown in Figure 8, where the parallel resonance impedance R_P(d) is given by Equation 1.

Feature Description (continued)

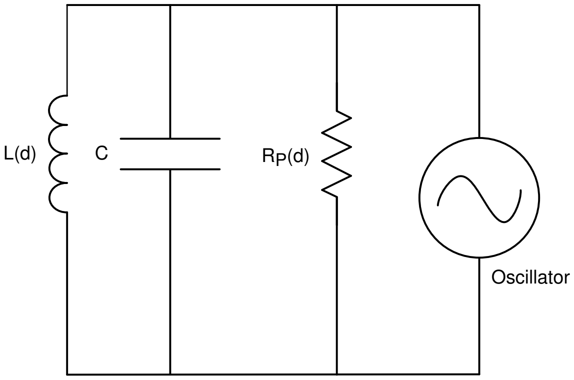


Figure 8. Equivalent Resistance of r_s in Parallel With LC Tank

$$R_P(d) = (1 / ([r_s + R(d)]) \times ([L_s + L(d)]) / C \quad (1)$$

$$R_P = (1 / r_s) \times (L / C) \quad (2)$$

Figure 9 shows the variation in R_P as a function of distance for a 14-mm diameter PCB coil (23 turns, 4-mil trace width, 4-mil spacing between trace, 1-oz copper thickness, FR4). The target metal used is a stainless steel 2-mm thick.

Figure 9. Typical R_P vs Distance With a 14-mm PCB Coil

7.3.2 Measuring Parallel Resonance Impedance and Inductance With LDC1001-Q1

Remember that the LDC1001-Q1 can determine the value of R_P by monitoring the amount of power injected into the resonator. The device returns this value as a digital value which is inversely proportional to R_P. The LDC1001-Q1 device can also measure the oscillation frequency of the LC circuit, which can be used to determine the inductance of the LC circuit. The oscillation frequency is returned as a digital value.

The LDC1001-Q1 device supports a wide range of LC combinations with oscillation frequencies ranging from 5 kHz to 5 MHz and R_P ranging from 798 Ω to 3.93 MΩ. This range of R_P can be viewed as the maximum input range of an ADC. As shown in Figure 9, the range of R_P is typically much smaller than maximum input range supported by the LDC1001-Q1 device. To achieve better resolution in the desired sensing range, the LDC1001-Q1 device offers a programmable input range through the Rp_MIN and Rp_MAX registers. See the *Calculation of Rp_Min and Rp_Max* section for how to set these registers.

When the resonance impedance of the sensor, R_P, drops below the programed Rp_MIN, the R_P output of the LDC will clip at the full scale output. An example occurrence of this situation is when a target comes too close to the coil.

Feature Description (continued)

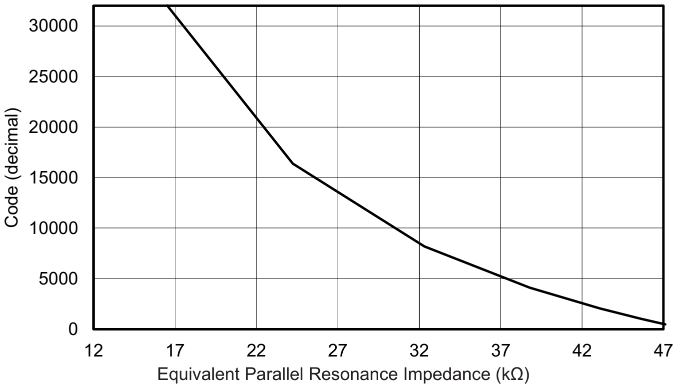


Figure 10. Transfer Characteristics of LDC1001-Q1 With Rp_MIN = 16.160 kΩ and Rp_MAX = 48.481 kΩ

Use Equation 3 to calculate the resonance impedance from the digital output code.

R_P = (Rp_MAX × Rp_MIN) / (Rp_MIN × (1 – Y) + Rp_MAX × Y), in Ω.

Where:

- Y = Proximity Data / 2^{15}
- Proximity data is the LDC output, register address 0x21 and 0x22. (3)

Example: If Proximity data (address 0x22 to 0x21) is 5000, Rp_MIN is 2.394 kΩ, and Rp_MAX is 38.785 kΩ, the resonance impedance is given by:

$Y = 5000 / 2^{15} = 0.1526$ (4)

$R_P = (38785 \times 2394) / (2394 \times (1 - 0.1526) + 38785 \times 0.1526) = (92851290) / (2028.675 + 5918.591)$ (5)

$R_P = 11.683\ \text{k}\Omega$ (6)

Figure 11 and Figure 12 show the change in RMS noise versus distance and a histogram of noise, with the target at an 0.8-mm distance from the sensor coil. Data was collected with a 14-mm PCB coil (23 turns, 4-mil trace width, 4-mil spacing between trace, 1-oz copper thickness, FR4) with a sensing range of 0.125 mm to 1.125 mm. At a distance of 0.8 mm, the RMS noise is approximately 250 nm.

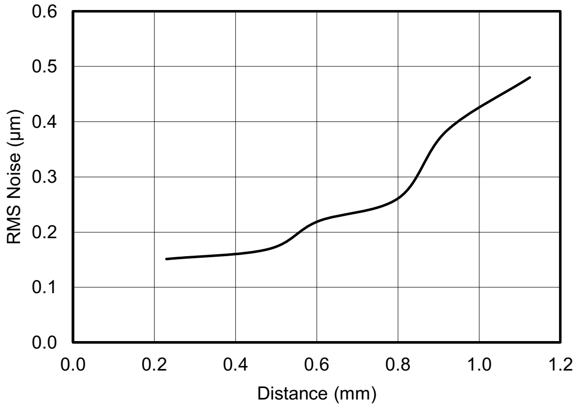


Figure 11. Typical RMS Noise vs Distance With PCB Coil

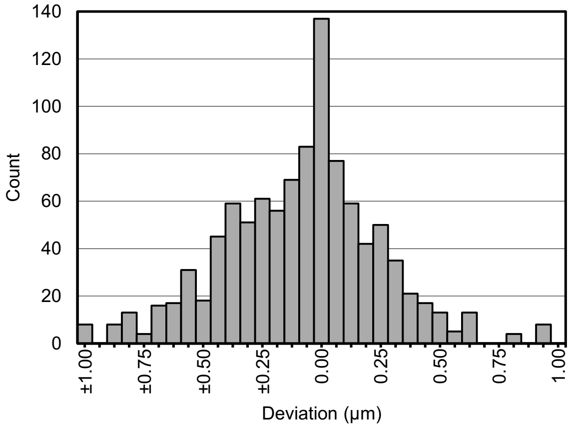


Figure 12. Histogram of Output Codes at 0.8-mm Distance

NOTE

Although the LDC1001-Q1 device has high resolution, the absolute accuracy depends on offset and gain correction which can be achieved by two-point calibration.

Feature Description (continued)

7.3.2.1 Measuring Inductance

The LDC1001-Q1 device measures the frequency of the oscillation of the sensor by a frequency counter. The frequency counter timing is set by an external clock applied on the TBCLK pin. The sensor resonance frequency is derived from the frequency-counter register value (see sections *Frequency Counter LSB (offset = 0x23) [reset = NA]* through *Frequency Counter MSB (offset = 0x25) [reset = NA]*) as shown in Equation 7.

$$f_{sensor} = (1/3) \times (f_{ext} / f_{count}) \times t_{res}$$

where

- f_{sensor} is the sensor frequency
- f_{ext} is the frequency of the external clock
- f_{count} is the value obtained from the Frequency Counter Data register (see the *Frequency Counter LSB (offset = 0x23) [reset = NA]* section through the *Frequency Counter MSB (offset = 0x25) [reset = NA]* section)
- t_{res} is the programmed response time (see the *LDC Configuration (offset = 0x04) [reset = 0x1B]* section) (7)

Use Equation 8 to calculate the inductance in H.

$$L=1 / [C \times (2 \times \pi \times f_{sensor})^2]$$

where

- C is the parallel capacitance of the resonator (8)

7.3.2.1.1 Example

If f_{ext} = 6 Mhz, t_{res} = 6144, C = 10 0pF, and measured f_{count} = 3000 (decimal) (see sections *Frequency Counter LSB (offset = 0x23) [reset = NA]* through *Frequency Counter MSB (offset = 0x25) [reset = NA]*), then use Equation 9 to calculate sensor resonance frequency:

$$f_{sensor} = 1/3 \times (6000000 / 3000) \times (6144) = 4.096 \text{ MHz} \quad (9)$$

Now use Equation 10.

$$L = 1 / [C \times (2 \times \pi \times f_{sensor})^2]$$

where

- L = 15.098 µH (10)

NOTE

The accuracy of a measurement largely depends upon the frequency of the external time-base clock (TBCLK). A higher frequency will provide better measurement accuracy. The maximum supported frequency is 8 MHz.

7.4 Device Functional Modes

7.4.1 INTB Pin Modes

The INTB pin is a configurable output pin which can be used to drive an interrupt on an MCU. The LDC1001-Q1 device provides three different modes on the INTB pin which include:

1. Comparator mode
2. Wake-up mode
3. DRDY mode

The LDC1001-Q1 device has a built-in high trigger and low trigger threshold registers that can be a comparator with programmable hysteresis or a special mode that is used to wake up an MCU. The following sections describe these modes in detail.

7.4.1.1 Comparator Mode

In the comparator mode, the INTB pin is asserted or deasserted when the proximity register value increases above the threshold high registers or decreases below the threshold low registers, respectively. In this mode, the function of the LDC1001-Q1 device is a proximity switch with programmable hysteresis.

Device Functional Modes (continued)

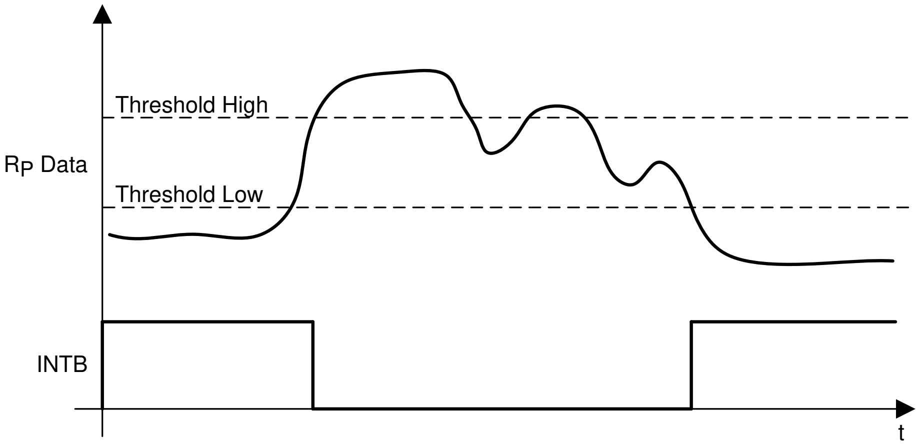


Figure 13. Behavior of the INTB Pin in Comparator Mode

7.4.1.2 Wake-Up Mode

In wake-up mode, the INTB pin is asserted when proximity register value increases above the threshold high registers and is deasserted when wake-up mode is disabled in the INTB pin mode register.

This mode can wake up an MCU that is in sleep mode to conserve power.

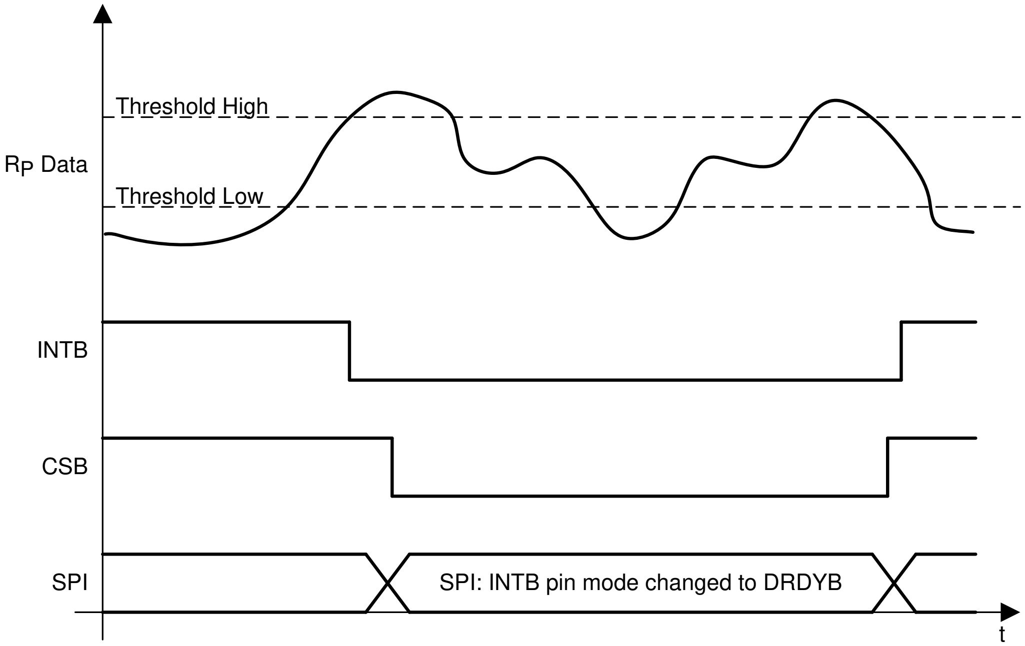


Figure 14. Behavior of the INTB Pin in Wake-Up Mode

7.4.1.3 DRDYB Mode

In DRDY mode (default), the INTB pin is asserted every time the conversion data is available and is deasserted when the read command on register 0x21 is registered internally. If the read command is in progress, the pin is pulsed instead.

Device Functional Modes (continued)

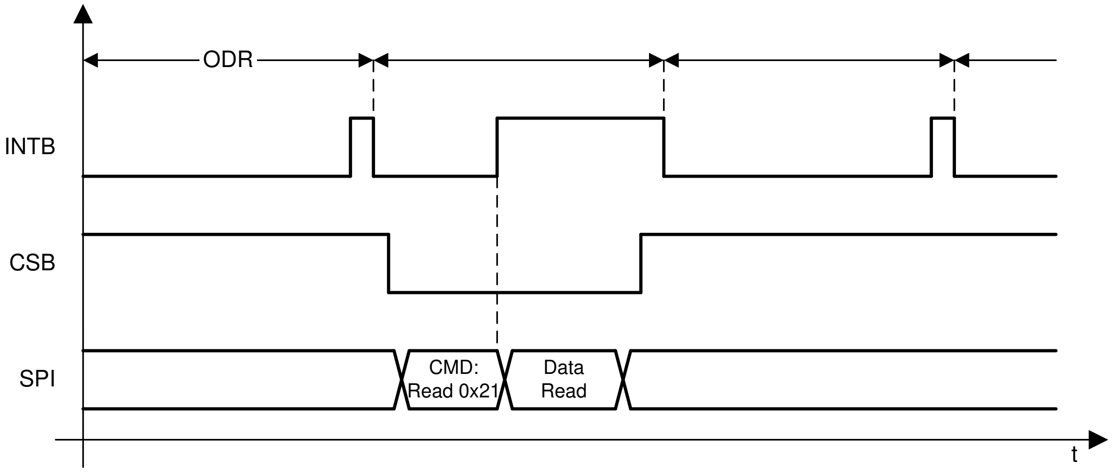


Figure 15. Behavior of the INTB Pin in DRDYB Mode

7.5 Programming

7.5.1 Digital Interface

The LDC1001-Q1 device uses a 4-wire SPI interface to access control and data registers. The LDC1001-Q1 device is an SPI slave device and does not initiate any transactions.

7.5.1.1 SPI Description

A typical serial interface transaction begins with an 8-bit instruction that is comprised of a read-write (R/W) bit (MSB, R = 1) and a 7-bit address of the register followed by a data field that is typically 8 bits. However, the data field can be extended to a multiple of 8 bits by providing sufficient SPI clocks. See the *Extended SPI Transactions* section.

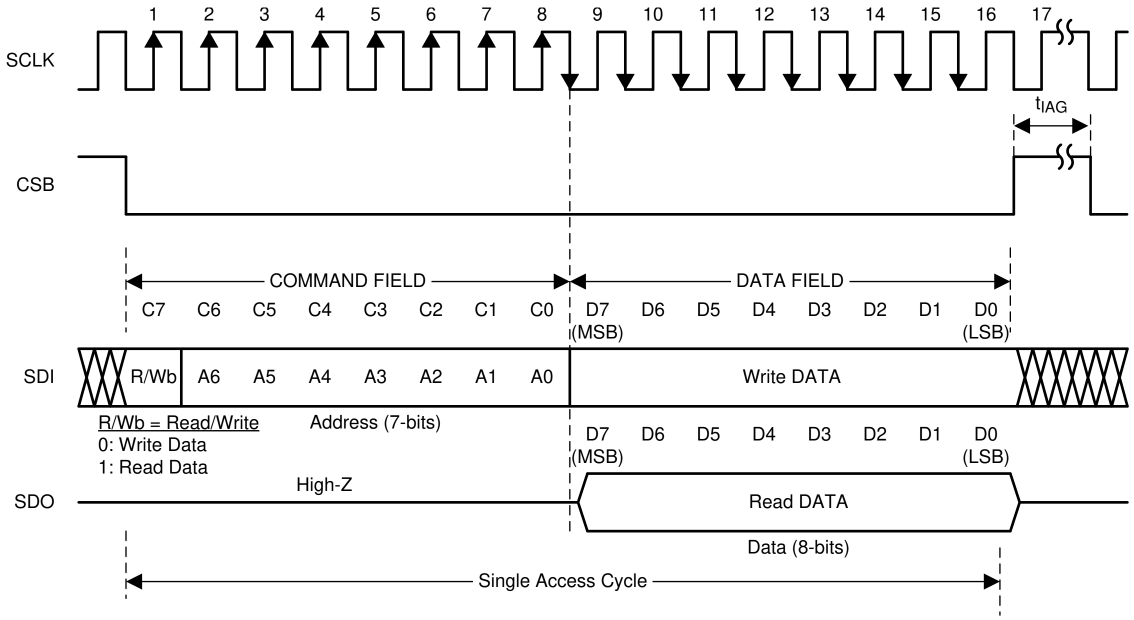


Figure 16. Serial Interface Protocol

Programming (continued)

Each assertion of the chip select bar (CSB) begins a new register access. The R/W bit in the command field configures the direction of the access. A value of 0 indicates a write operation, and a value of 1 indicates a read operation. All output data is driven on the falling edge of the serial clock SCLK, and all input data is sampled on the rising edge of the serial clock SCLK. Data is written into the register on the rising edge of the 16th clock. Deasserting the CSB pin after the 16th clock is required. No data write occurs if the CSB pin is deasserted before the 16th clock.

7.5.1.2 Extended SPI Transactions

A transaction can be extended to multiple registers by keeping the CSB pin asserted beyond the stated 16 clocks. In this mode, the register addresses increment automatically. The CSB pin must be asserted during 8 × (1+ N) clock cycles of SCLK, where N is the amount of bytes to write or read during the transaction.

During an extended read access, the SDO pin outputs register contents every 8 clock cycles after the initial 8 clocks of the command field. During an extended write access, the data is written to the registers every 8 clock cycles after the initial 8 clocks of the command field.

Extended transactions can be used to read 16 bits of proximity data and 24 bits of frequency data—all in one SPI transaction—by initiating a read from register 0x21.

7.6 Register Map

Table 1. Register Map(1)(2)

REGISTER NAME	ADDRESS	TYPE(3)	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device ID	0x00	R	0x80	Device ID							
Rp_MAX	0x01	R/W	0x0E	Rp Maximum							
Rp_MIN	0x02	R/W	0x14	Rp Minimum							
Sensor Frequency	0x03	R/W	0x45	Min Resonating Frequency							
LDC Configuration	0x04	R/W	0x1B	Reserved (000)			Amplitude		Response Time		
Clock Configuration	0x05	R/W	0x01	Reserved (000000)						CLK_SEL	CLK_PD
Comparator Threshold High LSB	0x06	R/W	0xFF	Threshold High LSB							
Comparator Threshold High MSB	0x07	R/W	0xFF	Threshold High MSB							
Comparator Threshold Low LSB	0x08	R/W	0x00	Threshold Low LSB							
Comparator Threshold Low MSB	0x09	R/W	0x00	Threshold Low MSB							
INTB Pin Configuration	0x0A	R/W	0x00	Reserved (00000)					INTB_MODE		
Power Configuration	0x0B	R/W	0x00	Reserved (0000000)							PWR_MODE
Status	0x20	R		OSC Dead	DRDYB	Wake-up	Comparator	Don't Care			
Proximity Data LSB	0x21	R		Proximity Data[7-0]							
Proximity Data MSB	0x22	R		Proximity Data[15-8]							
Frequency Counter Data LSB	0x23	R		ODR LSB							
Frequency Counter Data Mid-Byte	0x24	R		ODR Mid Byte							
Frequency Counter Data MSB	0x25	R		ODR MSB							

(1) Values of bits which are unused should be set to default values only.
(2) LEGEND R/W = read/write. R = read only. W = write only
(3) When the device is in active mode (the PWR_MODE bit is SET), registers 0x01 through 0x05 are read only (R).

7.6.1 Register Description

7.6.1.1 Revision ID (offset = 0x00) [reset = 0x80]

Figure 17. Revision ID Register

7	6	5	4	3	2	1	0
Revision ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 2. Revision ID Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Revision ID	R	0x080	Revision ID of silicon.

7.6.1.2 Rp_MAX (offset = 0x01) [reset = 0x0E]

Figure 18. Rp_MAX Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">Rp Maximum</td></tr>
<tr><td colspan="8">R/W</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. Rp_MAX Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Rp Maximum	R/W	0x0E	Maximum R_P that the LDC1001-Q1 device must measure. Configures the input dynamic range of the LDC1001-Q1 device. Register setting for Rp_MAX (kΩ): 0x00 = 3926.991 0x01 = 3141.593 0x02 = 2243.995 0x03 = 1745.329 0x04 = 1308.997 0x05 = 981.748 0x06 = 747.998 0x07 = 581.776 0x08 = 436.332 0x09 = 349.066 0x0A = 249.333 0x0B = 193.926 0x0C = 145.444 0x0D = 109.083 0x0E = 83.111 0x0F = 64.642 0x10 = 48.481 0x11 = 38.785 0x12 = 27.704 0x13 = 21.547 0x14 = 16.16 0x15 = 12.12 0x16 = 9.235 0x17 = 7.182 0x18 = 5.387 0x19 = 4.309 0x1A = 3.078 0x1B = 2.394 0x1C = 1.796 0x1D = 1.347 0x1E = 1.026 0x1F = 0.798

7.6.1.3 Rp_MIN (offset = 0x02) [reset = 0x14]

Figure 19. Rp_MIN Register

7	6	5	4	3	2	1	0
Rp Minimum							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Rp_MIN Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Rp Minimum	R/W	0x014	Minimum R_P that the LDC1001-Q1 device must measure. Configures the input dynamic range of the LDC1001-Q1 device. Register setting for Rp_MIN (kΩ): 0x20 = 3926.991 0x21 = 3141.593 0x22 = 2243.995 0x23 = 1745.329 0x24 = 1308.997 0x25 = 981.748 0x26 = 747.998 0x27 = 581.776 0x28 = 436.332 0x29 = 349.066 0x2A = 249.333 0x2B = 193.926 0x2C = 145.444 0x2D = 109.083 0x2E = 83.111 0x2F = 64.642 0x30 = 48.481 0x31 = 38.785 0x32 = 27.704 0x33 = 21.547 0x34 = 16.16 0x35 = 12.12 0x36 = 9.235 0x37 = 7.182 0x38 = 5.387 0x39 = 4.309 0x3A = 3.078 0x3B = 2.394 0x3C = 1.796 0x3D = 1.347 0x3E = 1.026 0x3F = 0.798

7.6.1.4 Sensor Frequency (offset = 0x03) [reset = 0x45]

Figure 20. Sensor Frequency Register

7	6	5	4	3	2	1	0
Min Resonating Frequency							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Sensor Frequency Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Min Resonating Frequency	R/W	0x45	Sets the minimum resonating frequency to approximately 20% below the lowest resonating frequency of the sensor with no target in front. Use Equation 11 to determine the value of register. $N = 68.94 \times \log_{10}(f / 2000)$ where • N = Register Value. Round to nearest value. • f = 20% below resonating frequency, Hz (11) **Example:** Sensor frequency (f_{sensor}) = 1 MHz $f = 0.8 \times 1\text{ MHz} = 800\text{ KHz}$ (12) $N = 68.94 \times \log_{10}(800\text{ KHz} / 2000)$ = Round to nearest whole number (179.38) = 179 (Value to be programmed in the sensor frequency register) (13)

7.6.1.5 LDC Configuration (offset = 0x04) [reset = 0x1B]

Figure 21. LDC Configuration Register

7	6	5	4	3	2	1	0
Reserved			Amplitude		Response Time		
—			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. LDC Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	—	—	Reserved to 0
4-3	Amplitude	R/W	0x1B	Sets the oscillation amplitude 00: 1 V 01: 2 V 10: 4 V 11: Reserved
2-0	Response Time	R/W	0x1B	Sets the response time 000: Reserved 001: Reserved 010: 192 011: 384 100: 768 101: 1536 110: 3072 111: 6144

7.6.1.6 Clock Configuration (offset = 0x05) [reset = 0x01]

Figure 22. Clock Configuration Register

7	6	5	4	3	2	1	0
Reserved						CLK_SEL	CLK_PD
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Clock Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	—	—	Reserved to 0
1	CLK_SEL	R/W	0x01	1: Do not use **0: External time-base clock used for frequency counter (TBCLK).**
0	CLK_PD	R/W	0x01	**1: Disable external time base clock (for lower power consumption in standby mode)** 0: Enable External time base clock.

7.6.1.7 Comparator Threshold High LSB (offset = 0x06) [reset = 0xFF]

Figure 23. Comparator Threshold High LSB Register

7	6	5	4	3	2	1	0
Threshold High[7:0]	Threshold High[6]	Threshold High[5]	Threshold High[4]	Threshold High[3]	Threshold High[2]	Threshold High[1]	Threshold High[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Comparator Threshold High LSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Threshold High LSB Threshold High[7:0]	R/W	0xFF	Least Significant byte (LSB) of the threshold high register. This register is a buffer. A read reflects the current value of the threshold high[7:0] register. See the *Comparator Threshold High MSB (offset = 0x07) [reset = 0xFF]* section for details on updating the threshold high register.

7.6.1.8 Comparator Threshold High MSB (offset = 0x07) [reset = 0xFF]

Figure 24. Comparator Threshold High MSB Register

7	6	5	4	3	2	1	0
Threshold High[15]	Threshold High[14]	Threshold High[13]	Threshold High[12]	Threshold High[11]	Threshold High[10]	Threshold High[9]	Threshold High[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Comparator Threshold High MSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Threshold High MSB Threshold High[15:8]	R/W	0xFF	Most significant byte (MSB) of the threshold high register. A write to this register copies the contents of the 0x06 register and writes to the threshold high register[15:0]. A read returns the threshold high [15:8] register. To update the threshold high register write register 0x06 first and then 0x07.

7.6.1.9 Comparator Threshold Low LSB (offset = 0x08) [reset = 0x00]

Figure 25. Comparator Threshold Low LSB Register

7	6	5	4	3	2	1	0
Threshold Low[7:0]	Threshold Low[6]	Threshold Low[5]	Threshold Low[4]	Threshold Low[3]	Threshold Low[2]	Threshold Low[1]	Threshold Low[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Comparator Threshold Low LSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Threshold Low LSB Threshold Low[7:0]	R/W	0x00	Least significant byte of the threshold low value. This register is a buffer. A read reflects the current value of the threshold low [7:0] register. See the *Comparator Threshold Low MSB (offset = 0x09) [reset = 0x00]* section for details on updating the threshold low register.

7.6.1.10 Comparator Threshold Low MSB (offset = 0x09) [reset = 0x00]

Figure 26. Comparator Threshold Low MSB Register

7	6	5	4	3	2	1	0
Threshold Low[15]	Threshold Low[14]	Threshold Low[13]	Threshold Low[12]	Threshold Low[11]	Threshold Low[10]	Threshold Low[9]	Threshold Low[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Comparator Threshold Low MSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Threshold Low MSB Threshold Low[15:8]	R/W	0x00	Most significant byte of the threshold low register. A write to this register copies the contents of the 0x08 register and writes to the threshold low register[15:0]. A read returns the threshold low [15:8] register. To update the threshold low register write register address 0x08 first and then 0x09.

7.6.1.11 INTB Pin Configuration (offset = 0x0A) [reset = 0x00]

Figure 27. INTB Pin Configuration Register

7	6	5	4	3	2	1	0
Reserved					Mode		
—					R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. INTB Pin Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	—	—	Reserved to 0
2:0	Mode	R/W	0x00	100: DRDYB enabled on the INTB pin 010: The INTB pin indicates the status of the comparator output 001: Wake-up enabled on the INTB pin **000: All modes disabled** All other combinations are reserved

7.6.1.12 Power Configuration (offset = 0x0B) [reset = 0x00]

Figure 28. Power Configuration Register

7	6	5	4	3	2	1	0
Reserved							PWR_MODE
—							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Power Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7:1	Reserved	—	—	Reserved to 0
0	PWR_MODE	R/W	0x00	**0: Stand-by mode** 1: Active mode. Conversion is enabled

7.6.1.13 Status (offset = 0x20) [reset = NA]

Figure 29. Status Register

7	6	5	4	3	2	1	0
OSC status	Data Ready	Wake-up	Comparator	Don't Care			
R	R	R	R	R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Status Field Descriptions

Bit	Field	Type	Reset	Description
7	OSC status	R	NA	1: Indicates that the oscillator is overloaded and has stopped 0: Oscillator is working
6	Data Ready	R	NA	0: Data is ready to be read 1: No new data is available
5	Wake-up	R	NA	0: Wake-up triggered. Proximity data is more than the threshold high value. 1: Wake-up is disabled
4	Comparator	R	NA	0: Proximity data is more than the threshold high value 1: Proximity data is less than the threshold low value
3:0	Don't Care	R	NA	

7.6.1.14 Proximity Data LSB (offset = 0x21) [reset = NA]

Figure 30. Proximity Data LSB Register

7	6	5	4	3	2	1	0
Proximity Data[7]	Proximity Data[6]	Proximity Data[5]	Proximity Data[4]	Proximity Data[3]	Proximity Data[2]	Proximity Data[1]	Proximity Data[0]
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Proximity Data LSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Proximity Data[7:0]	R	NA	Least significant byte of proximity data

7.6.1.15 Proximity Data MSB (offset = 0x22) [reset = NA]

Figure 31. Proximity Data MSB Register

7	6	5	4	3	2	1	0
Proximity Data[15]	Proximity Data[14]	Proximity Data[13]	Proximity Data[12]	Proximity Data[11]	Proximity Data[10]	Proximity Data[9]	Proximity Data[8]
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Proximity Data MSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Proximity data[15:8]	R	NA	Most significant byte of proximity data

7.6.1.16 Frequency Counter LSB (offset = 0x23) [reset = NA]

Figure 32. Frequency Counter LSB Register

7	6	5	4	3	2	1	0
ODR[7]	ODR[6]	ODR[5]	ODR[4]	ODR[3]	ODR[2]	ODR[1]	ODR[0]
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Frequency Counter LSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ODR LSB ODR[7:0]	R	NA	LSB of output data rate. Sensor frequency can be calculated using the output data rate. See the *Measuring Inductance* section.

7.6.1.17 Frequency Counter Mid-Byte (offset = 0x24) [reset = NA]

Figure 33. Frequency Counter Mid-Byte Register

7	6	5	4	3	2	1	0
ODR[15]	ODR[14]	ODR[13]	ODR[12]	ODR[11]	ODR[10]	ODR[9]	ODR[8]
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Frequency Counter Mid-Byte Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ODR Mid byte ODR[15:8]	R	NA	Middle byte of output data rate

7.6.1.18 Frequency Counter MSB (offset = 0x25) [reset = NA]

Figure 34. Frequency Counter MSB Register

7	6	5	4	3	2	1	0
ODR[23]	ODR[22]	ODR[21]	ODR[20]	ODR[19]	ODR[18]	ODR[17]	ODR[16]
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Frequency Counter MSB Field Descriptions(1)

Bit	Field	Type	Reset	Description
7:0	ODR MSB ODR[23:16]	R	NA	MSB of Output data rate

(1) Take care to ensure that the proximity data[15:0] and Frequency Counter[23:0] registers are all from same conversion. Conversion data is updated to these registers only when a read is initiated on 0x21 register. If the read is delayed between subsequent conversions, these registers are not updated until another read is initiated on 0x21.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Calculation of Rp_Min and Rp_Max

Different sensing applications may have different ranges of the resonance impedance R_P to measure. The LDC1001-Q1 measurement range of R_P is controlled by setting two registers: Rp_MIN and Rp_MAX. For a given application, R_P must never be outside the range set by these register values, otherwise the measured value will be clipped. For optimal sensor resolution, the range of Rp_MIN to Rp_MAX should not be unnecessarily large. The following procedure is recommended to determine the Rp_MIN and Rp_MAX register values.

8.1.1.1 Rp_MAX

Rp_MAX sets the upper limit of the LDC1001-Q1 resonant impedance input range.

- Configure the sensor such that the eddy-current losses are minimized. As an example, for a proximity sensing application, set the distance between the sensor and the target to the maximum sensing distance.
- Measure the resonant impedance R_P using an impedance analyzer.
- Multiply R_P by 2 and use the next higher value from the register settings listed in Table 3.

For example, if R_P is measured at 18 kΩ, 18000 × 2 = 36000. Referring to Table 3, 38.785 kΩ is the smallest value larger than 36 kΩ, therefore Rp_MAX should be set to 0x11.

Setting Rp_MAX to a value not listed in Table 3 can result in indeterminate behavior.

8.1.1.2 Rp_MIN

Rp_MIN sets the lower limit of the LDC1001-Q1 resonant impedance input range.

- Configure the sensor such that the eddy current losses are maximized. As an example, for a proximity sensing application, set the distance between the sensor and the metal target to the minimum sensing distance.
- Measure the resonant impedance R_P using an impedance analyzer.
- Divide the R_P value by 2 and then select the next lower R_P value from the register settings listed in Table 4.

For example, if R_P at 1 mm is measured to be 5 kΩ, 5000 / 2 = 2500. Referring to Table 4, 2.394 kΩ is the smallest value smaller than 2.5 kΩ, which corresponds to an Rp_MIN value of 0x3B.

Setting Rp_MIN to a value not listed on Table 4 can result in indeterminate behavior. In addition, Rp_MIN powers on with a default value of 0x14 which must be set to a value from Table 4 prior to powering on the LDC.

8.1.2 Output Data Rate

The output data rate of the LDC1001-Q1 device depends on the sensor frequency, f_{sensor} and the Response Time[2-0] field in the LDC configuration register (address: 0x04).

$$\text{Output data rate} = f_{sensor} / (\text{Response Time[2-0]} / 3) \text{ in SPS (samples per second)} \quad (14)$$

8.1.2.1 Example

If f_{sensor}= 5 Mhz and Response Time[2-0] = 192, then:

$$\text{Output data rate} = 5 \text{ MHz} / (192 / 3) = 78.125 \text{ KSPS} \quad (15)$$

Application Information (continued)

8.1.3 Selecting a Filter Capacitor (CFA and CFB Pins)

The filter capacitor is critical to the operation of the LDC1001-Q1 device. The capacitor should be low leakage, temperature stable, and it must not generate any piezoelectric noise (the dielectrics of many capacitors exhibit piezoelectric characteristics and any such noise is coupled directly through R_P into the converter). The optimal capacitance values range from 20 pF to 100 nF. The value of the capacitor is based on the time constant and resonating frequency of the LC tank.

If a ceramic capacitor is used, then a C0G (or NP0) grade dielectric is recommended. The voltage rating should be 10 V or higher. The traces connecting the CFA and CFB pins to the capacitor should be as short as possible to minimize any parasitics.

For optimal performance, the selected filter capacitor connected between the CFA and CFB pins must be as small as possible, but large enough such that the active filter does not saturate. The size of this capacitor depends on the time constant of the sense coil, which is given by L / r_S (L = inductance, r_S = series resistance of the inductor at oscillation frequency). The larger this time constant, the larger filter capacitor is required. Therefore the time constant reaches the maximum when there is no target present in front of the sensing coil.

Use the following procedure to find the optimal filter capacitance:

1. Use with a large filter capacitor. For a ferrite core coil, a value of 10 nF is generally large enough. For an air coil or PCB coil, a value of 100 pF is generally large enough.
2. Power on the LDC and set the desired register values.
3. Minimize the eddy currents losses by ensuring maximum clearance between the target and the sensing coil.
4. Observe the signal on the CFB pin using a scope. Because this node is very sensitive to capacitive loading, the use of an active probe is recommended. As an alternative, a passive probe with a 1-kΩ series resistance between the tip and the CFB pin can be used.
5. Vary the values of the filter capacitor until the signal observed on the CFB pin has an amplitude of approximately 1 V_{PP}. This signal scales linearly with the reciprocal of the filter capacitance. For example, if a 100-pF filter capacitor is applied and the signal observed on the CFB pin has a peak-to-peak value of 200 mV, the desired 1-V_{PP} value is obtained using a filter capacitor value that is calculated in Equation 16.

$$200\text{ mV} / 1\text{ V} \times 100\text{ pF} = 20\text{ pF} \tag{16}$$

8.2 Typical Application

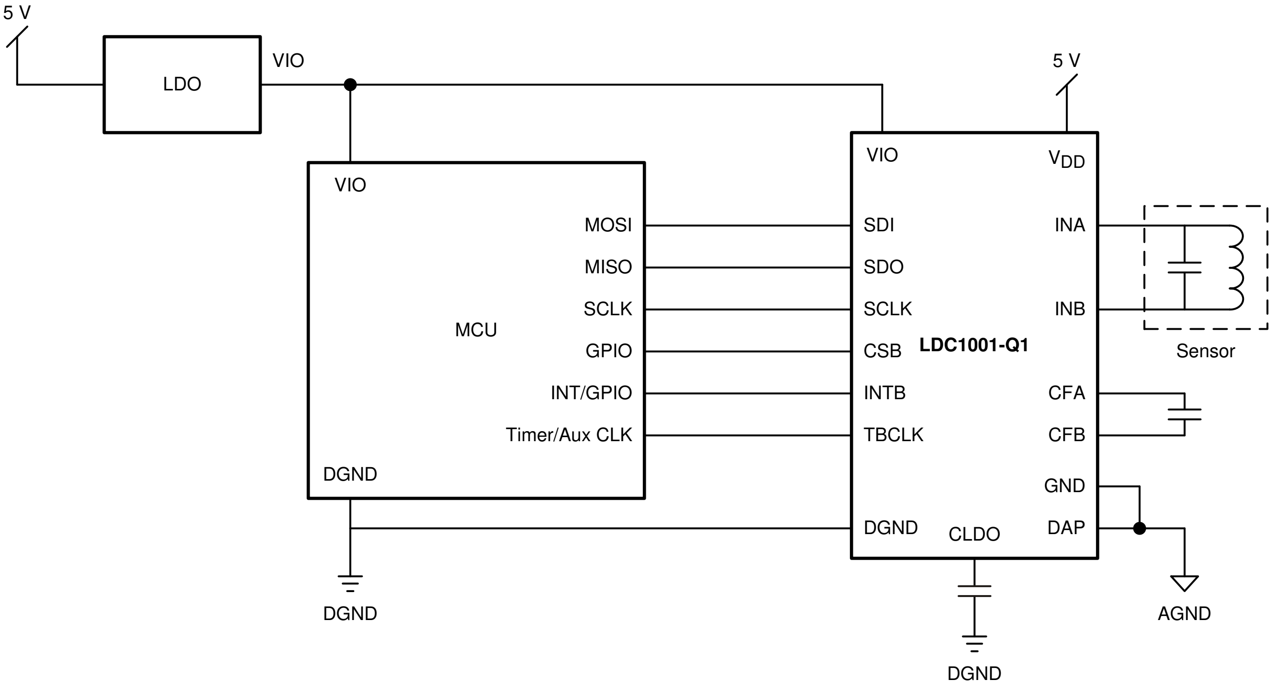


Figure 35. Typical Application Schematic

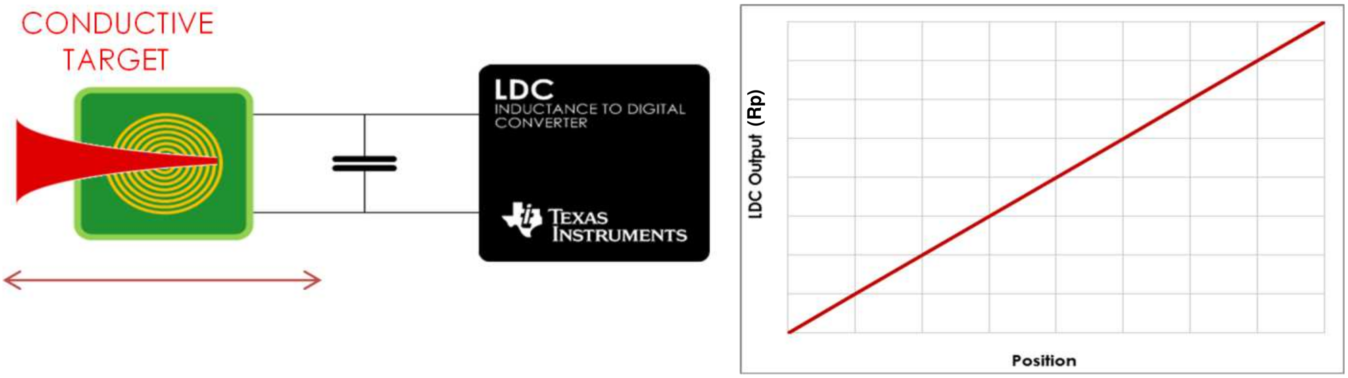


Figure 36. Linear Position Sensing

Typical Application (continued)

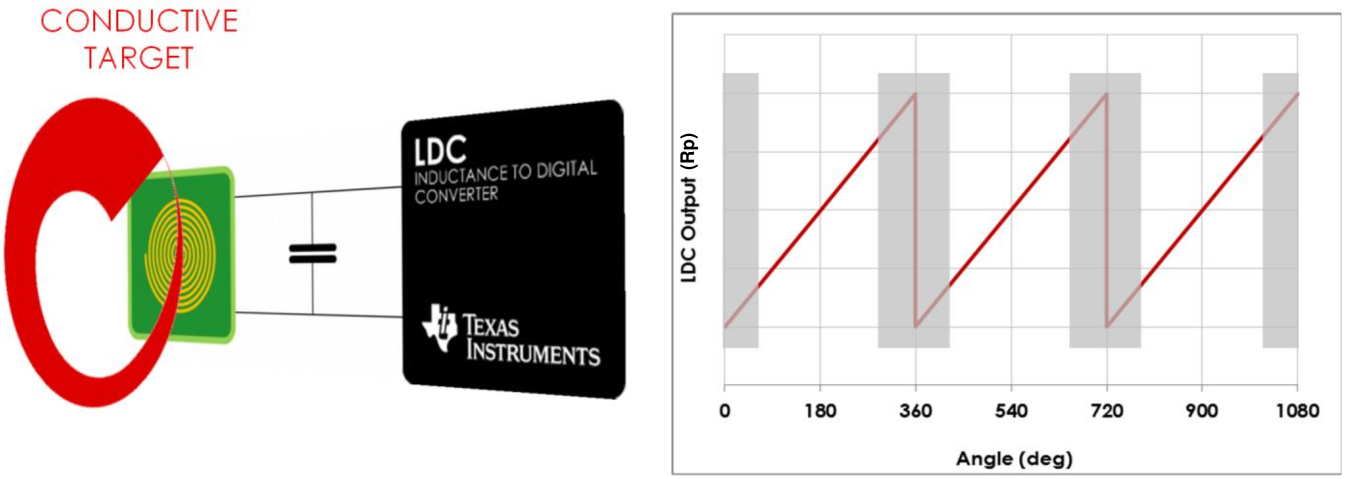


Figure 37. Angular Position Sensing

8.2.1 Design Requirements

For this design example, use the design parameters listed in Table 20 as the input parameters.

Table 20. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum sensing distance	1 mm
Maximum sensing distance	8 mm
Output data rate	78 KSPS (Max data rate with LDC10xx series)
Number of PCB layers for sensor	2 layers

8.2.2 Detailed Design Procedure

8.2.2.1 Sensor and Target

In this example, consider a sensor with the characteristics listed in Table 21.

Table 21. Sensor Characteristics

PARAMETER	VALUE
Layers	2
Thickness of copper	1 oz
Coil shape	Circular
Number of turns	23
Trace thickness	4 mil
Trace spacing	4 mil
PCB core material	FR4
R_P at 1 mm	5 kΩ
R_P at 8 mm	12.5 kΩ
Nominal Inductance	18 µH

The target material used is stainless steel.

8.2.2.2 Calculating a Sensor Capacitor

Sensor frequency depends on various factors in the application. In this example, use Equation 17 to calculate the sensor frequency to achieve an output data rate of 78 KSPS per the design parameter.

$$\text{Output Data Rate} = \frac{f_{\text{sensor}}}{\left(\dfrac{\text{Response time}}{3}\right)} \tag{17}$$

With the lowest response time (t_{res}) of 192 and output data rate of 78 KSPS, the calculated sensor frequency using Equation 17 is 4.99 MHz.

Use Equation 18 to calculate the sensor capacitor as 55 pF with a sensor inductance of 18 µH.

$$L = \frac{1}{C \times (2\pi \times f_{\text{sensor}})^2} \tag{18}$$

8.2.2.3 Selecting a Filter Capacitor

Use the steps listed in the *Selecting a Filter Capacitor (CFA and CFB Pins)* section to calculate a filter capacitor. For this example, the selected capacitor value is 20 pF. The following waveforms were taken on the CFB pin with a 14-mm, 2-layer PCB coil (23 turns, 4-mil trace width, 4-mil spacing between trace, 1-o.z copper thickness, FR4).

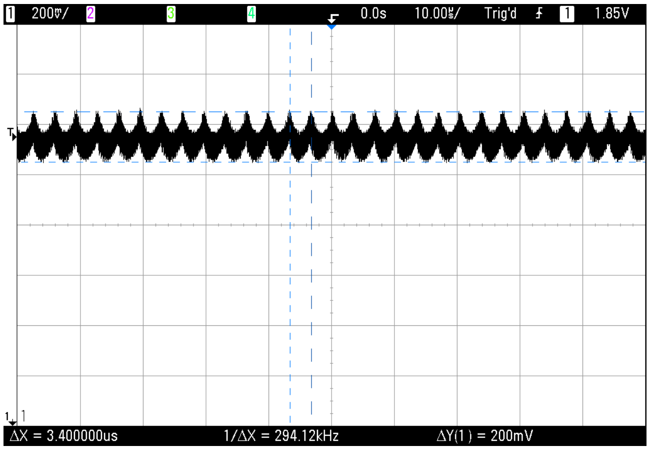


Figure 38. Waveform on CFB With 100 pF

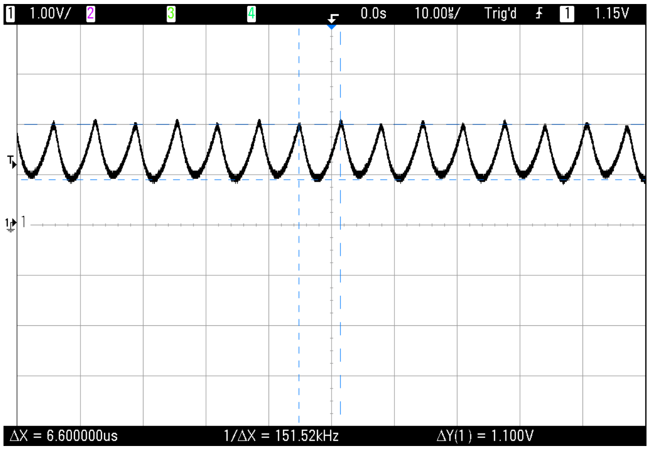


Figure 39. Waveform on CFB With 20 pF

8.2.2.4 Setting Rp_MIN and Rp_MAX

To calculate the value for the Rp_MAX register, use the following value: Rp at 8 mm is 12.5 kΩ, 12500 × 2 = 25000. Then 27.704 kΩ is the nearest value larger than 25 kΩ. Referring to Table 3, this value corresponds to a Rp_MAX value of 0x12.

To calculate the value for the Rp_MAX register, use the following value: Rp at 1 mm is 5 kΩ, 5000 / 2 = 2500. Then 2.394 kΩ is the nearest value lower than 2.5 kΩ. Referring to Table 4, this value corresponds to Rp_MIN value of 0x3B.

8.2.2.5 Calculating Minimum Sensor Frequency

Use Equation 19 to calculate the minimum sensor frequency.

$$N = 68.94 \times \log_{10}\left(\frac{F}{2500}\right)$$

where

- N is 227.51 (19)

For this example, round the value of N up to 228. This value must be written into the watchdog timer register, which is used to wake up the internal circuit when the sensor is saturated.

8.2.3 Application Curves

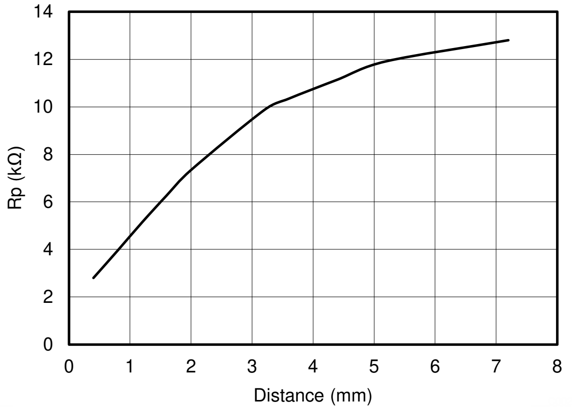


Figure 40. R_P vs Distance

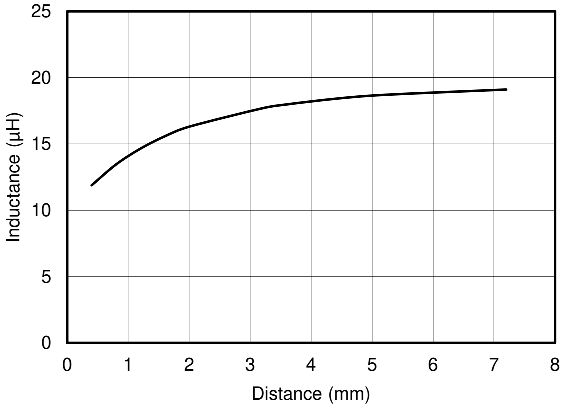


Figure 41. Inductance vs Distance

9 Power Supply Recommendations

The LDC1001-Q1 device is designed to operate from an analog supply range of 4.75 V to 5.25 V and digital I/O supply range of 1.8 to 5.25 V. The analog supply voltage should be greater than or equal to the digital supply voltage for proper operation of the device. The supply voltage should be well regulated. If the supply is placed more than a few inches from the LDC1001-Q1 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

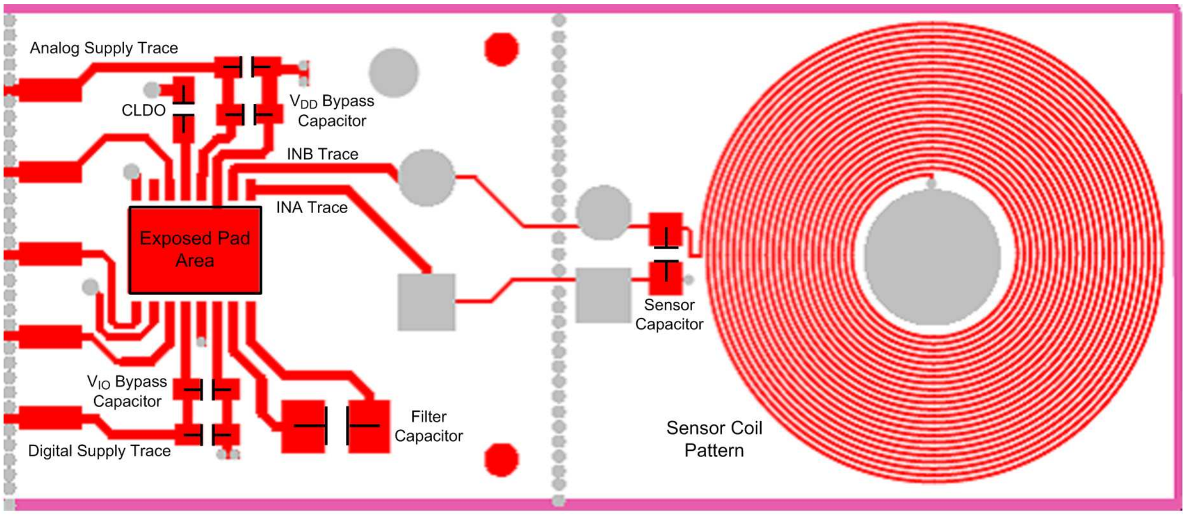
10 Layout

10.1 Layout Guidelines

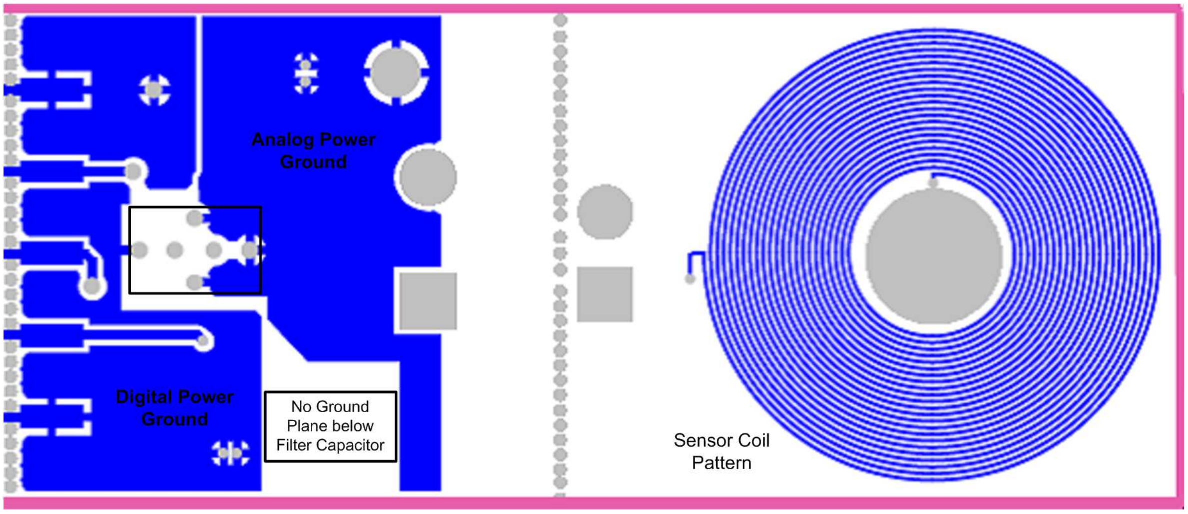
Use the following guidelines:

- Bypass the V_{DD} and VIO pin to ground with a low-ESR ceramic bypass capacitor. A ceramic X7R dielectric capacitor with a value of 0.1 µF is recommend.
- Place the VDD, VIO, GND, and DGND pins as close to the device as possible. Take care to minimize the loop area formed by the bypass capacitor connection and the V_{DD}, VIO, GND, and DGND pins of the IC. See Figure 42 for a PCB layout example.
- Bypass the CLDO pin to the digital ground (DGND) with a ceramic bypass capacitor with a value of 56 nF.
- Connect the filter capacitor that is selected using the procedure listed in the *Selecting a Filter Capacitor (CFA and CFB Pins)* section between the CFA and CFB pins. Place the capacitor close to the CFA and CFB pins. Do not use any ground or power planes below the capacitor and the trace connecting the capacitor and the CFx pins.
- Use two separate ground planes for the ground (GND) and digital ground (DGND) for a star connection as recommended. See Figure 42 for a PCB layout example.

10.2 Layout Example



Top Layer



Bottom Layer

Figure 42. LDC10xx Board Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LDC1001EPWRQ1	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	LDC1001E
LDC1001EPWRQ1.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	LDC1001E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LDC1001-Q1 :

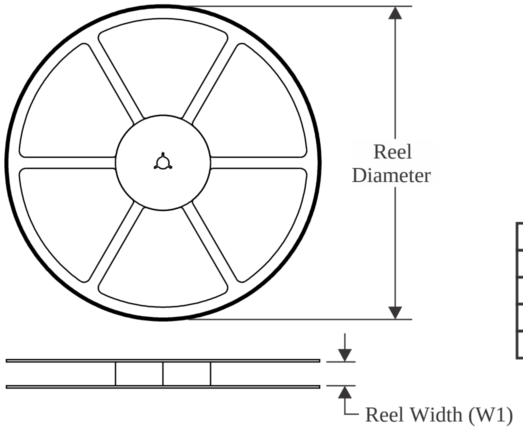
- Catalog : LDC1001

NOTE: Qualified Version Definitions:

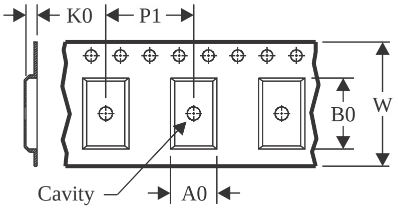
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

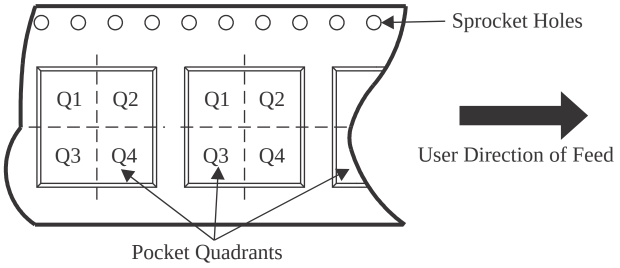


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

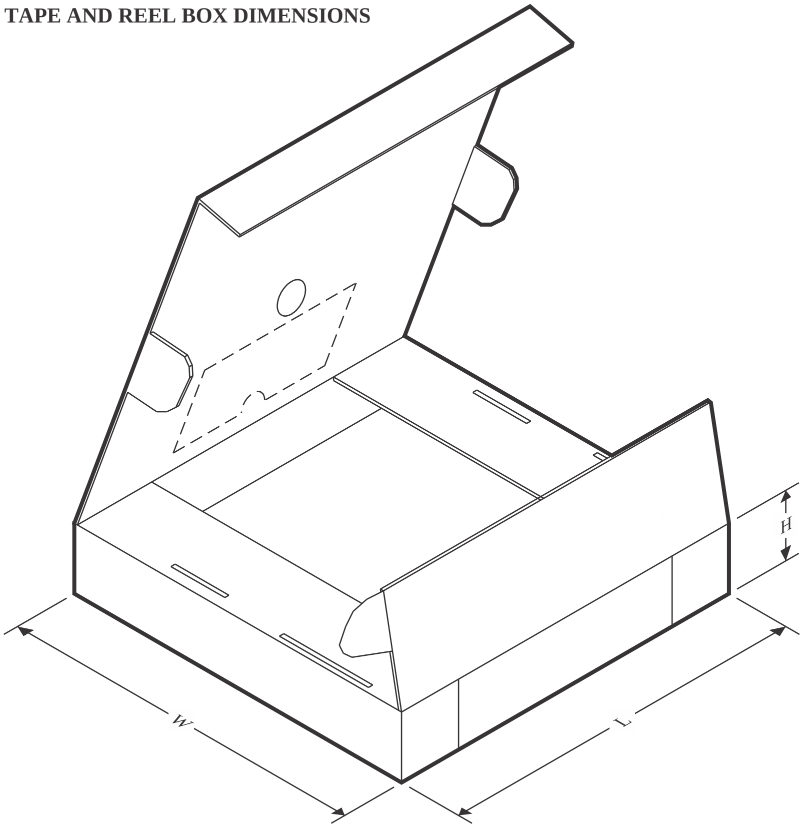
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

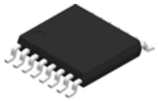
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC1001EPWRQ1	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC1001EPWRQ1	TSSOP	PW	16	2500	356.0	356.0	36.0

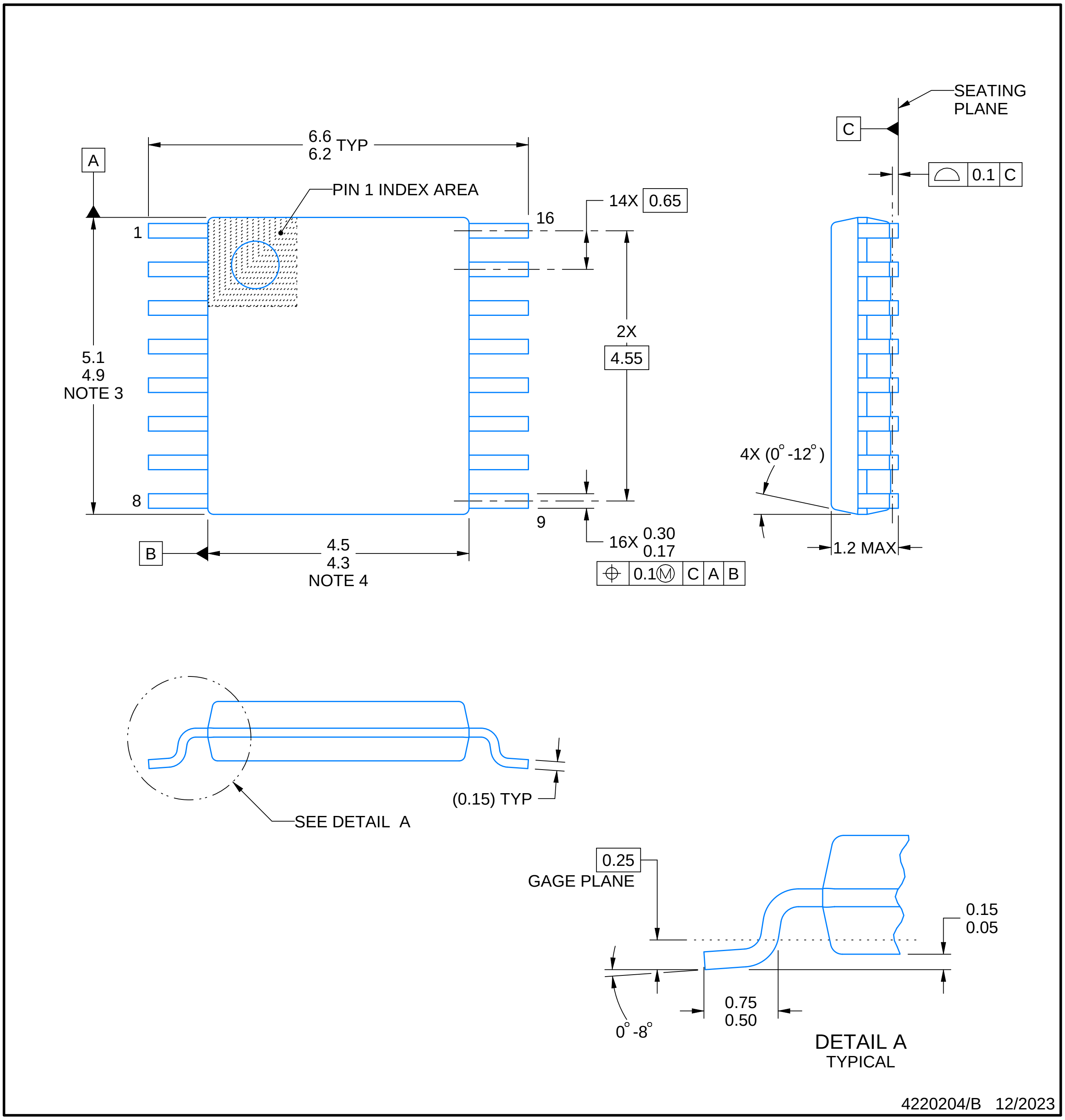


PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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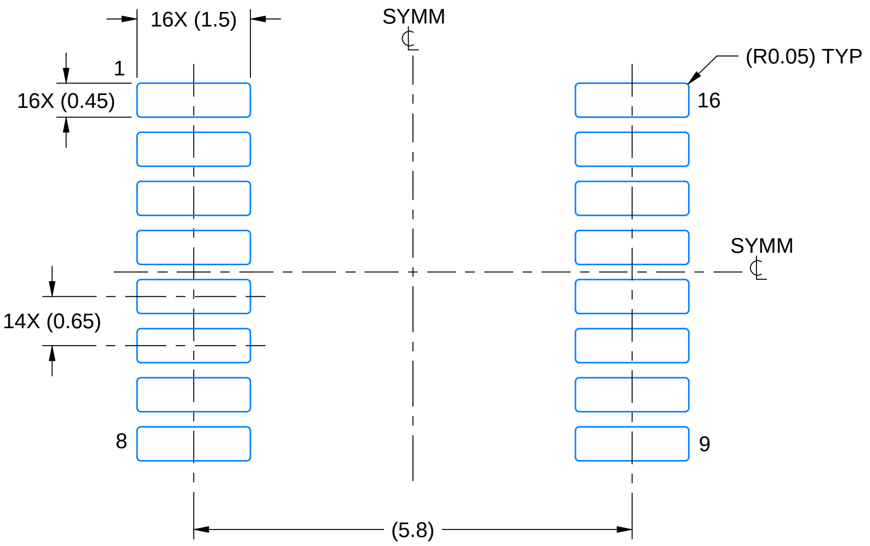
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

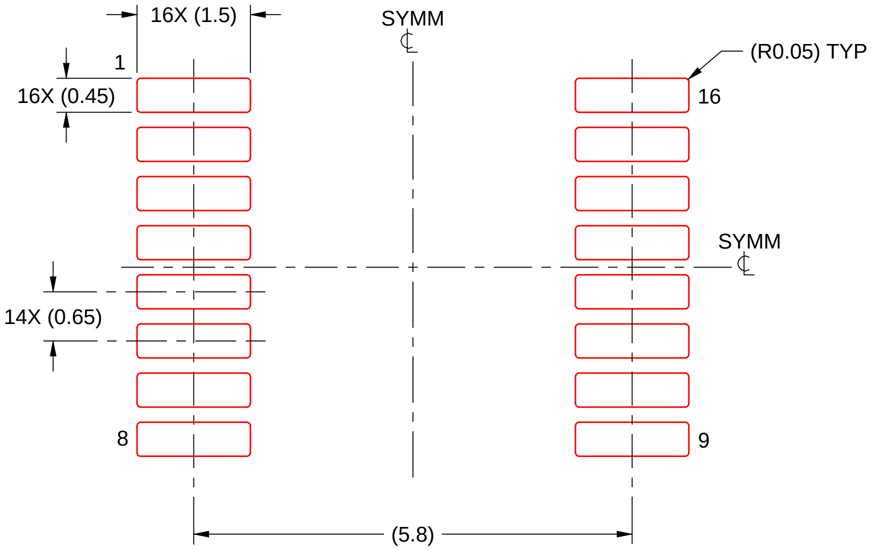
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項