LF347, LF347B JFET-Input Quad Operational Amplifiers

1 Features

- Low Input Bias Current: 50 pA Typical
- Low Input Noise Current: 0.01 pA/$\sqrt{\text{Hz}}$ Typical
- Low Total Harmonic Distortion
- Low Supply Current: 8 mA Typical
- Gain Bandwidth: 3 MHz Typical
- High Slew Rate: 13 V/ms Typical

2 Applications

- Motor Integrated Systems: UPS
- Drives and Control Solutions: AC Inverters and VF Drives
- Renewables: Solar Inverters
- Pro Audio Mixers
- Oscilloscopes

3 Description

The LF347 and LF347B devices are low-cost, high-speed, JFET-input operational amplifiers. They require low supply current yet maintain a large gain-bandwidth product and a fast slew rate. In addition, their matched high-voltage JFET inputs provide very low input bias and offset current.

The LF347 and LF347B can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

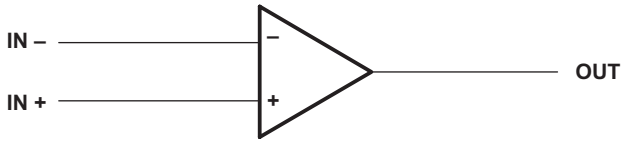
The LF347 and LF347B devices are characterized for operation from 0°C to 70°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF347D, LF347BD	SOIC (14)	8.65 mm × 3.91 mm
LF347N, LF347BN	PDIP (14)	19.30 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol (Each Amplifier)



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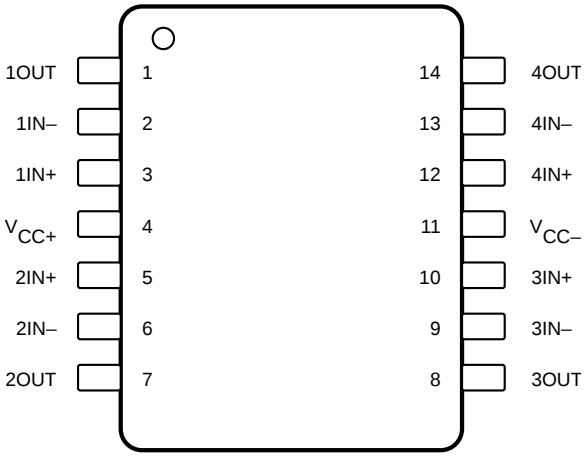
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 1994) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

D or N Package
14-Pin SOIC or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1OUT	O	Output pin of amplifier 1
2	1IN–	I	Inverting input pin of amplifier 1
3	1IN+	I	Noninverting input pin of amplifier 1
4	V_{CC+}	—	Positive Supply
5	2IN+	I	Noninverting input pin of amplifier 2
6	2IN–	I	Inverting input pin of amplifier 2
7	2OUT	O	Output pin of amplifier 2
8	3OUT	O	Output pin of amplifier 3
9	3IN–	I	Inverting input pin of amplifier 3
10	3IN+	I	Noninverting input pin of amplifier 3
11	$V_{CC–}$	—	Negative Supply
12	4IN+	I	Noninverting input pin of amplifier 4
13	4IN–	I	Inverting input pin of amplifier 4
14	4OUT	O	Output pin of amplifier 4

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage		18	V
V_{CC-}	Supply voltage		–18	V
V_{ID}	Differential input voltage	–30	30	V
V_I	Input voltage(2)	–15	15	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	free-air temperature	0	70	°C
V_{CC+}	Supply voltage	3.5	18	V
V_{CC-}	Supply voltage	–3.5	–18	V
V_{CM}	Common-mode voltage	V_{CC-} + 4	V_{CC+} – 4	V
T_A	Operating temperature	0	70	°C

6.4 Thermal Information

THERMAL METRIC(1)		LF347, LF347B		UNIT
		D (SOIC)	N (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.4	42.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.5	29.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.9	22.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.6	22.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: LF347

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	25°C		5	10	mV
			Full range[1]			13	
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			18		µV/°C
I_{IO}	Input offset current[2]	V_{IC} = 0	25°C		25	100	pA
			70°C			4	nA
I_{IB}	Input bias current[2]	V_{IC} = 0	25°C		50	200	pA
			70°C			8	nA
V_{ICR}	Common-mode input voltage	Lower limit of range		–11	–12		V
		Upper limit of range		11	15		
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	25°C	25	100		V/mV
			Full range	15			
r_i	Input resistance	T_A = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 2 kΩ		70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See [3]		70	100		dB
I_{CC}	Supply current				8	11	mA

(1) Full range is 0°C to 70°C.
(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
(3) Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

6.6 Electrical Characteristics: LF347B

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	25°C		3	5	mV
			Full range[1]			7	
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			18		µV/°C
I_{IO}	Input offset current[2]	V_{IC} = 0	25°C		25	100	pA
			70°C			4	nA
I_{IB}	Input bias current[2]	V_{IC} = 0	25°C		50	200	pA
			70°C			8	nA
V_{ICR}	Common-mode input voltage	Lower limit of range		–11	–12		V
		Upper limit of range		11	15		
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	25°C	50	100		V/mV
			Full range	25			
r_i	Input resistance	$T_{A = 25°C}$			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_{S \le 2\ k\Omega}$		80	100		dB
k_{SVR}	Supply-voltage rejection ratio	See [3]		80	100		dB
I_{CC}	Supply current				8	11	mA

(1) Full range is 0°C to 70°C.
(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
(3) Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

6.7 Switching Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 5	8	13		V/μs
B_1	Unity-gain bandwidth				3		MHz
V_{O1} / V_{O2}	Crosstalk attenuation	f = 1 kHZ			120		dB
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01		pA/√Hz

6.8 Typical Characteristics

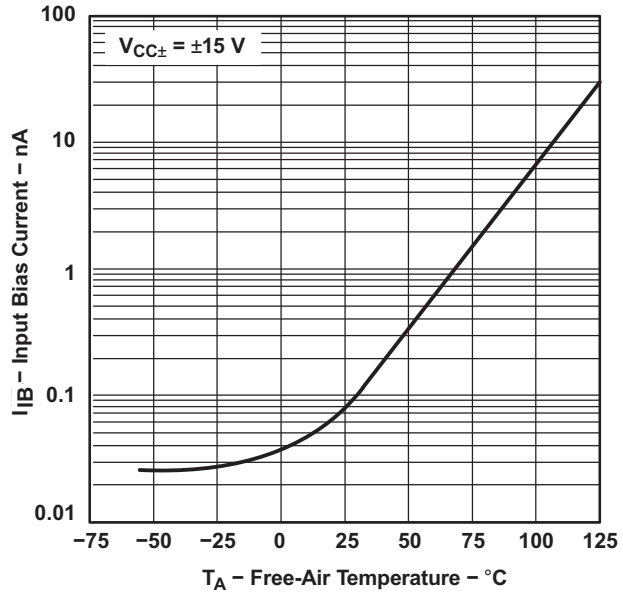


Figure 1. Input Bias Current vs Free-Air Temperature

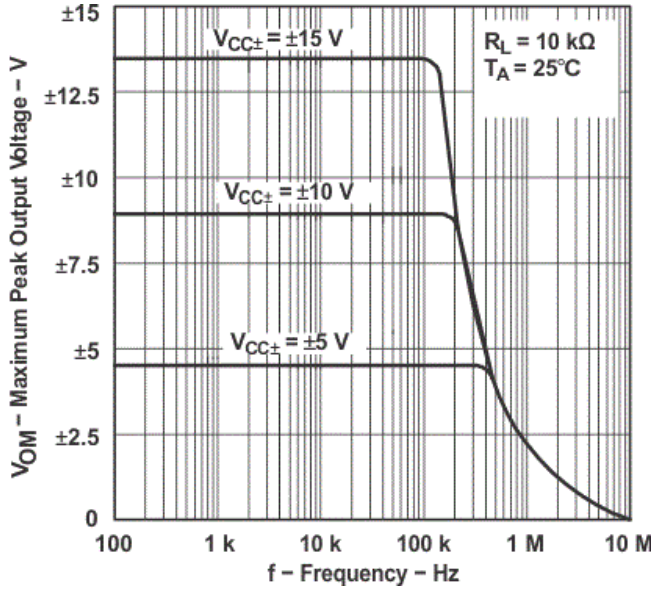


Figure 2. Maximum Peak Output Voltage vs Frequency

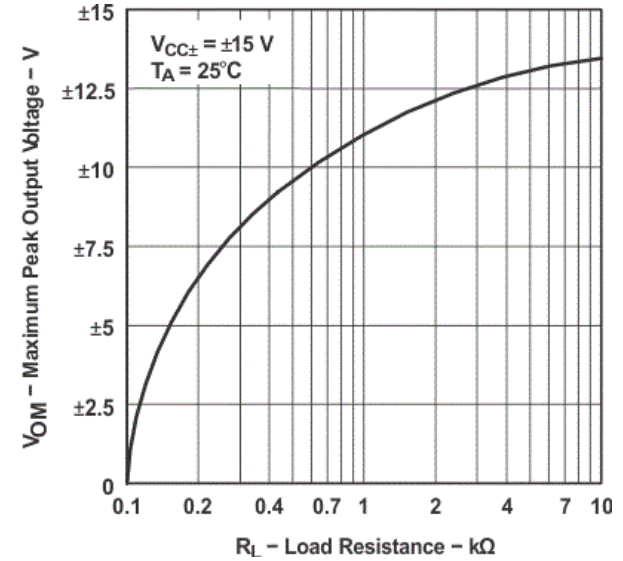


Figure 3. Maximum Peak Output Voltage vs Load Resistance

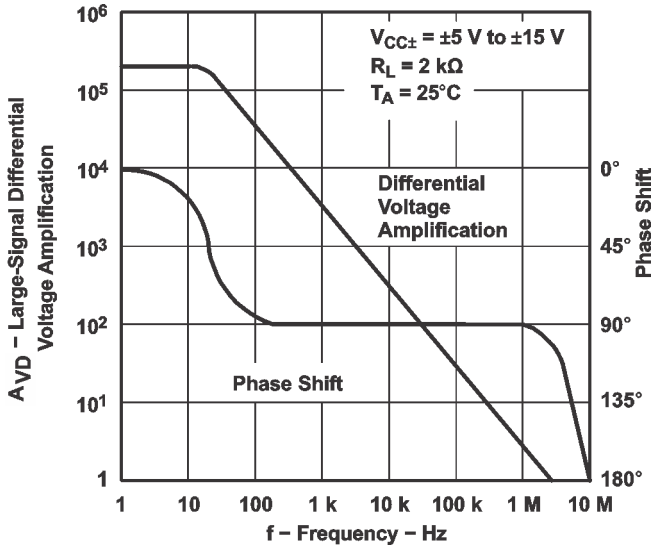


Figure 4. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

7 Parameter Measurement Information

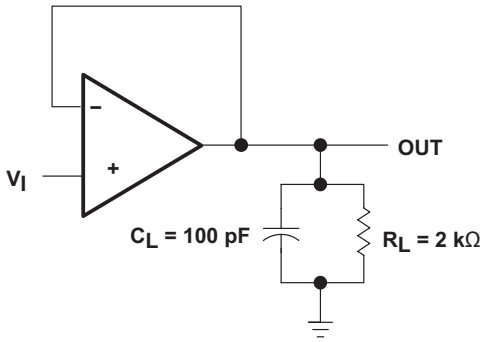


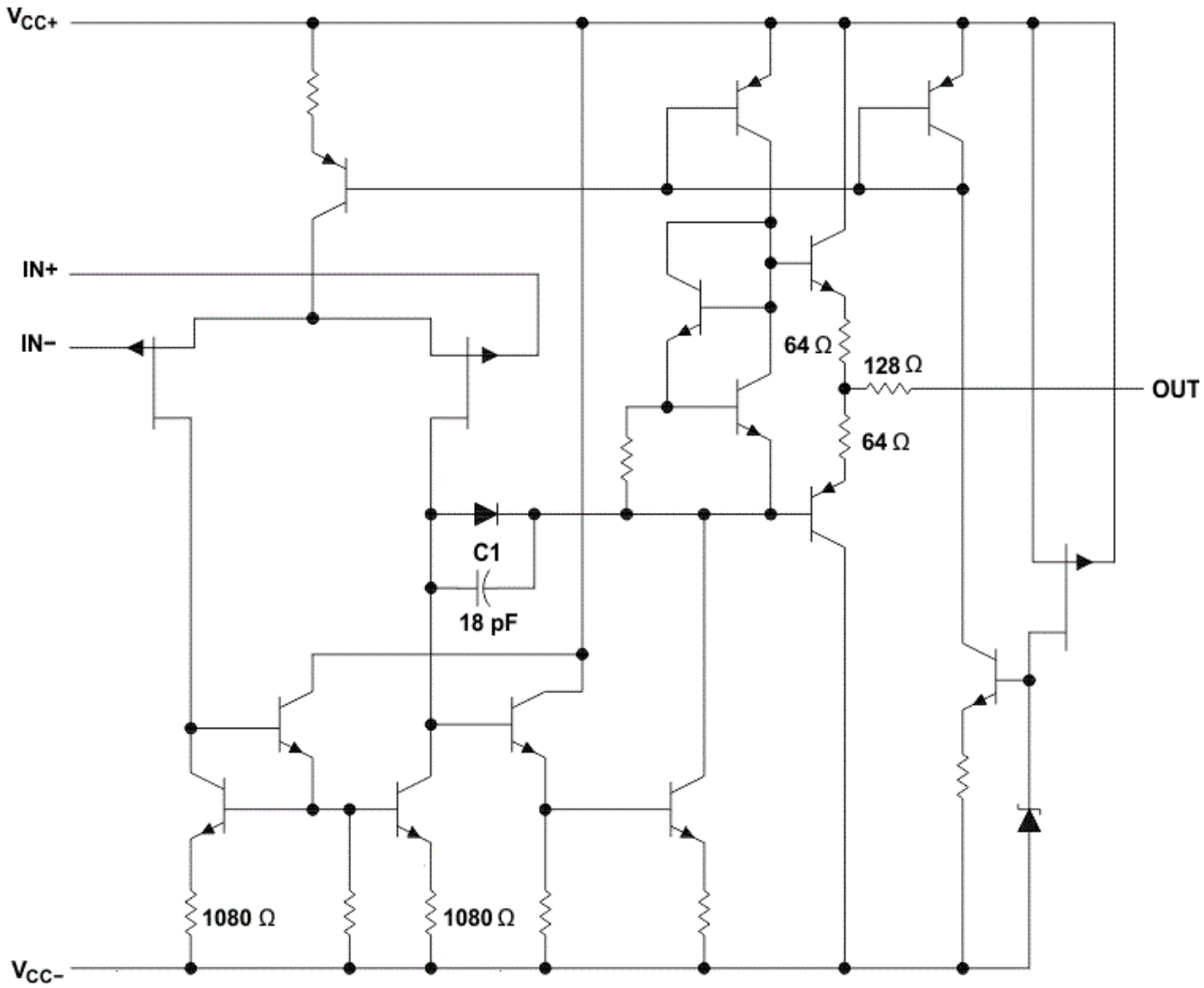
Figure 5. Unity-Gain Amplifier

8 Detailed Description

8.1 Overview

The LF347 is a JFET-input operational amplifier with low input bias and offset currents and fast slew rate. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip. The output is protected against shorts due to the resistive 200-Ω output impedance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/μs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LF347 has four independent amplifiers that have very low input bias current which allow using higher resistance resistors in the feedback network. The upper input common mode range typically goes to the positive supply rail. The lower common mode range does not include the negative supply rail; it must be at least 4-V greater. Output resistance is 200 Ω to protect the device from accidental shorts.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

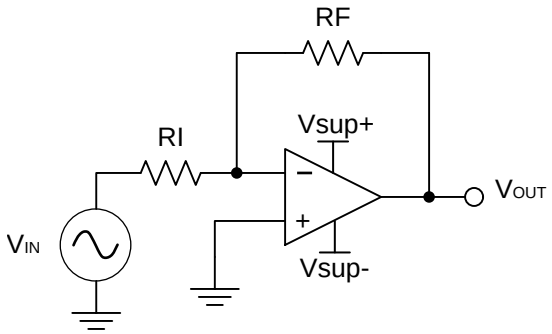


Figure 6. Inverting Amplifier

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

When the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit uses currents in the milliamp range. This ensures the part does not draw too much current. For this example, choose 10 kΩ for RI which means 36 kΩ is used for R, as determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

Typical Application (continued)

9.2.3 Application Curve

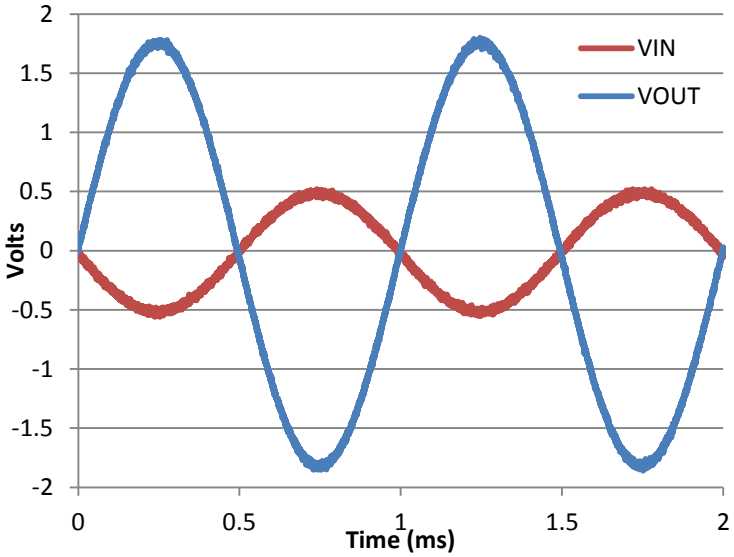


Figure 7. Input and Output Voltages of the Inverting Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see *Absolute Maximum Ratings*).

Place the 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Example*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see the chapter extract, *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting

Layout Guidelines (continued)

input minimizes parasitic capacitance, as shown in *Layout Example*.

- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

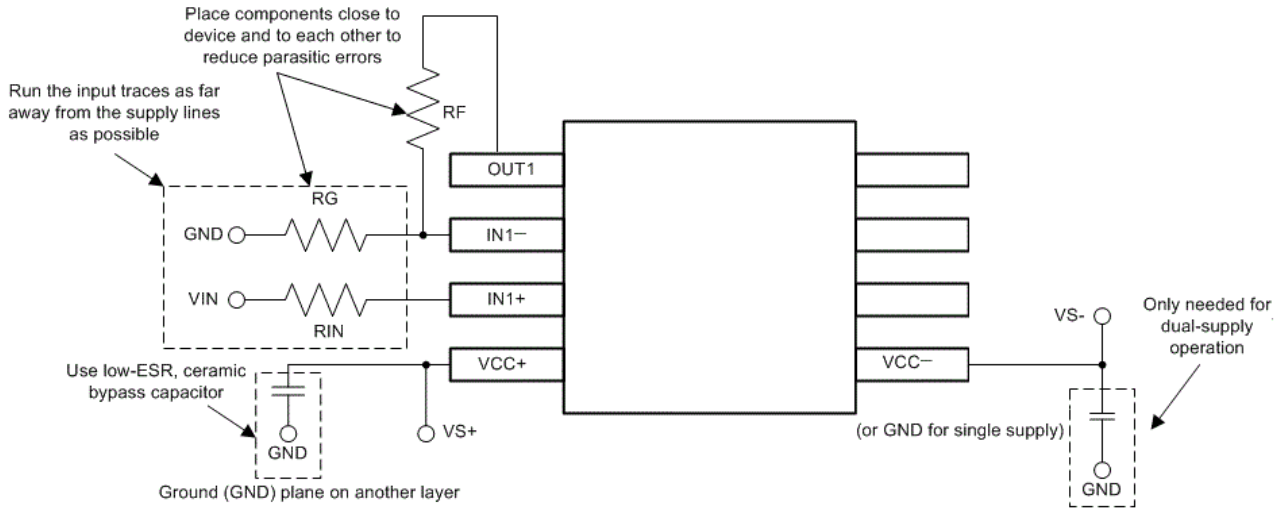


Figure 8. Operational Amplifier Board Layout for Noninverting Configuration

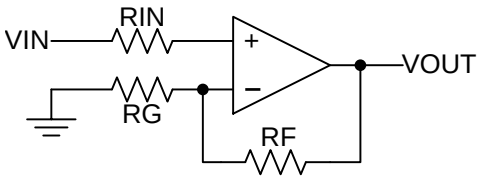


Figure 9. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following

Circuit Board Layout Techniques, SLOA089

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LF347	Click here	Click here	Click here	Click here	Click here
LF347B	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF347BD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LF347B
LF347BDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347B
LF347BDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347B
LF347BN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF347BN
LF347BN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF347BN
LF347D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LF347
LF347DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347
LF347DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347
LF347DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
LF347N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF347N
LF347N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF347N
LF347NE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

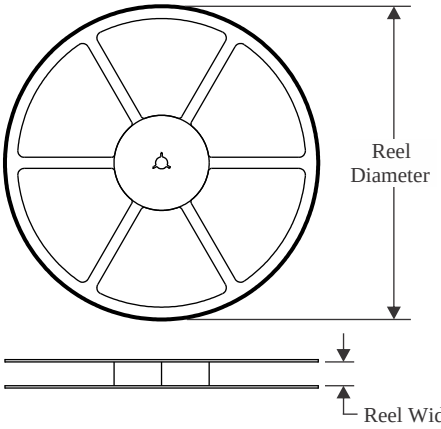
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

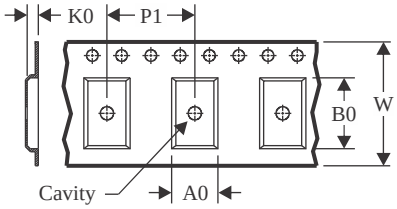
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

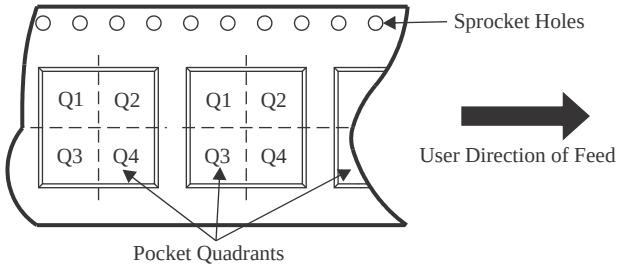


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

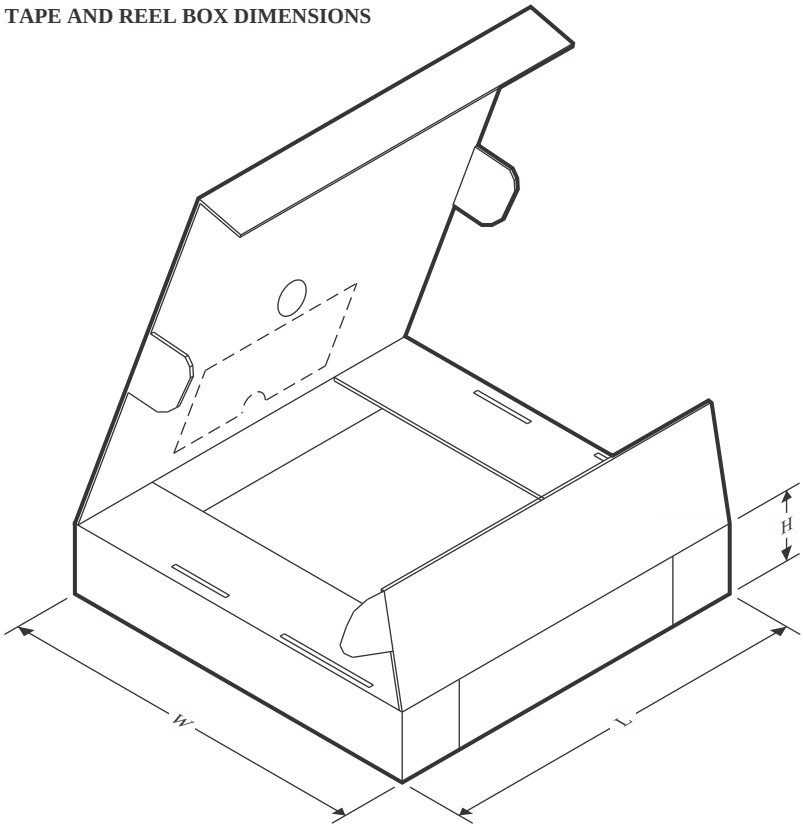
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF347BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LF347BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LF347DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LF347DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

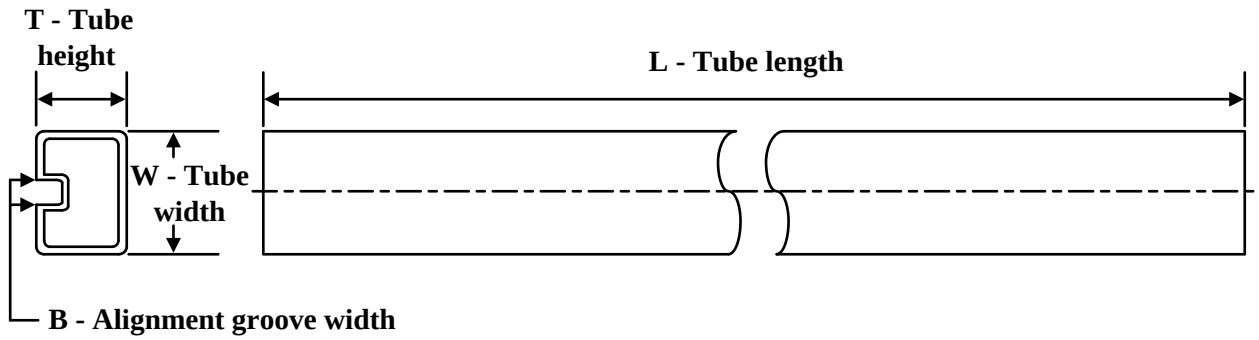
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

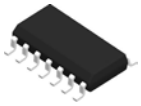
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF347BDR	SOIC	D	14	2500	340.5	336.1	32.0
LF347BDR	SOIC	D	14	2500	340.5	336.1	32.0
LF347DR	SOIC	D	14	2500	353.0	353.0	32.0
LF347DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF347BN	N	PDIP	14	25	506	13.97	11230	4.32
LF347BN	N	PDIP	14	25	506	13.97	11230	4.32
LF347BN.A	N	PDIP	14	25	506	13.97	11230	4.32
LF347BN.A	N	PDIP	14	25	506	13.97	11230	4.32
LF347N	N	PDIP	14	25	506	13.97	11230	4.32
LF347N	N	PDIP	14	25	506	13.97	11230	4.32
LF347N.A	N	PDIP	14	25	506	13.97	11230	4.32
LF347N.A	N	PDIP	14	25	506	13.97	11230	4.32

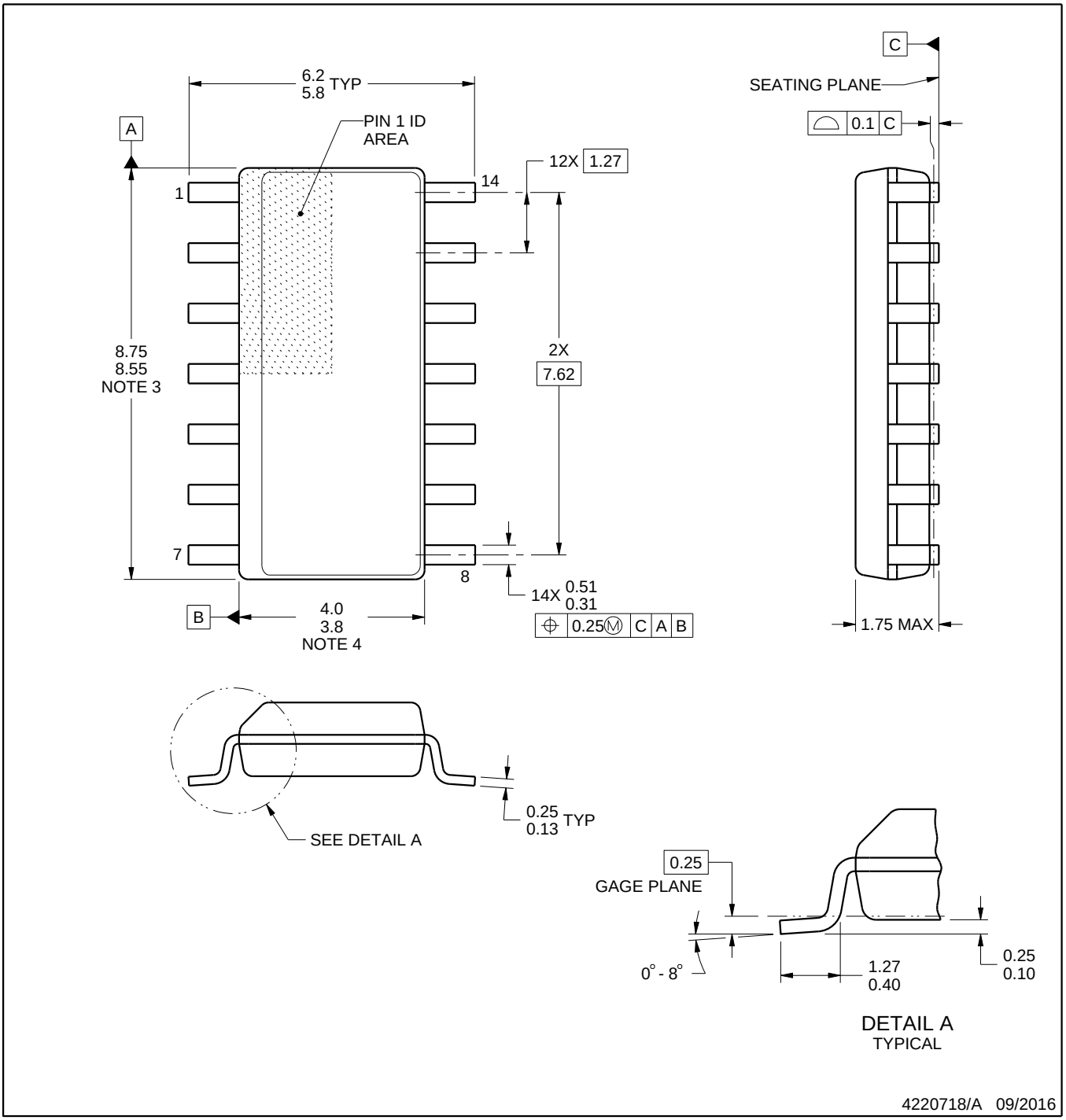


PACKAGE OUTLINE

D0014A

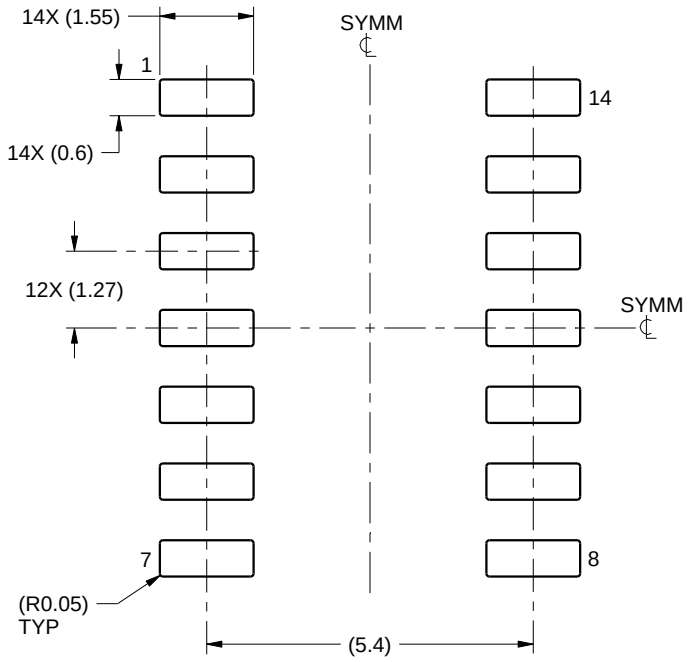
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

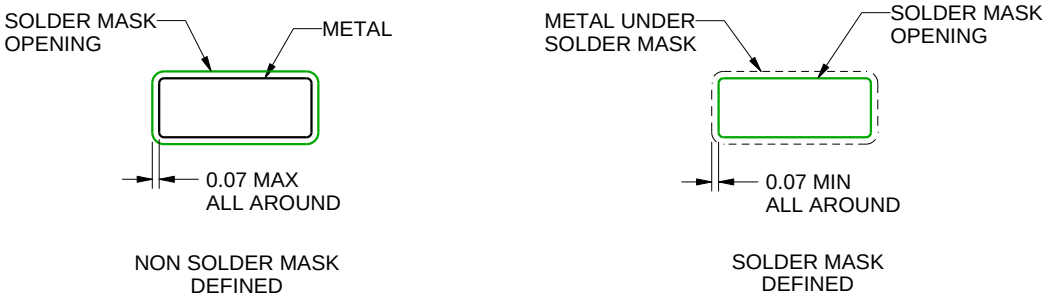


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

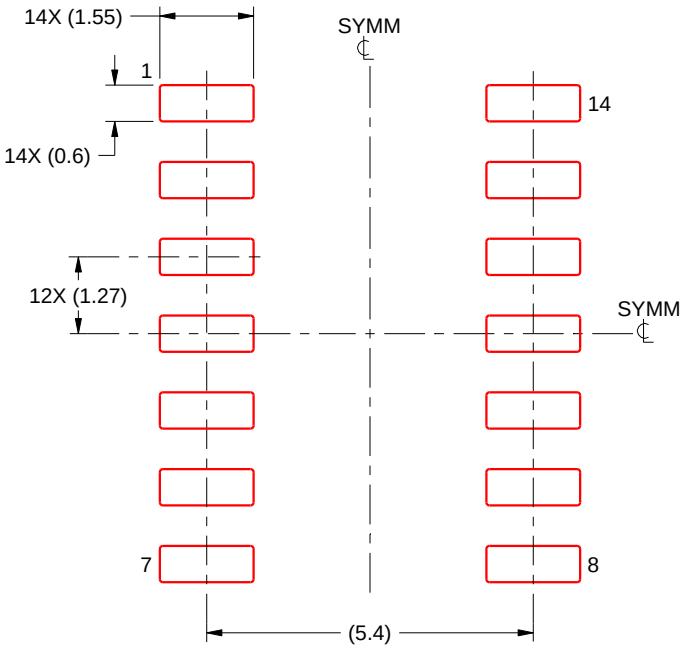
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

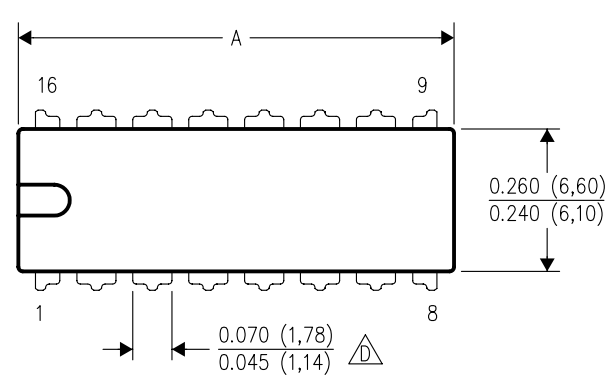
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

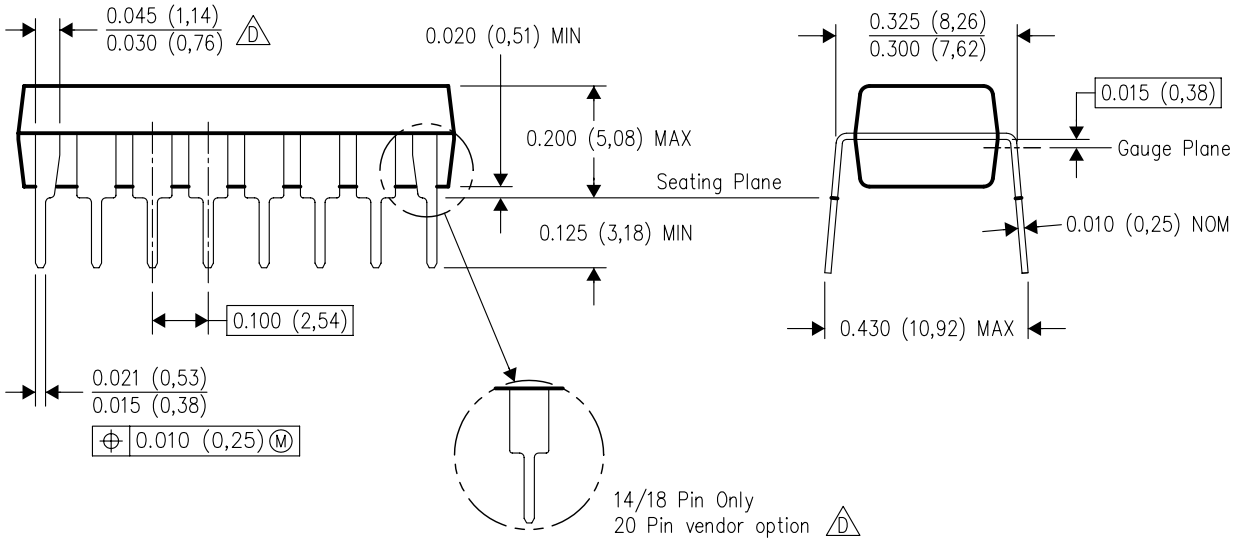
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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