LF442-MIL デュアル、低消費電力、JFET入力オペアンプ

1 特長

- LM1458の1/10の消費電流: 400μA (最大値)
- 低い入力バイアス電流: 50pA (最大値)
- 低い入力オフセット電圧: 1mV (最大値)
- 低い入力オフセット電圧ドリフト: 7μV/℃ (標準値)
- 高いゲイン帯域幅: 1MHz
- 高いスルー・レート: 1V/μs
- 低電力で低いノイズ電圧: 35nV/$\sqrt{Hz}$
- 低い入力ノイズ電流: 0.01pA/$\sqrt{Hz}$
- 高い入力インピーダンス: $10^{12}\Omega$
- 高いゲインV_O = ±10V、R_L = 10k: 50k (最小値)

2 アプリケーション

- 高速積分器
- 高速D/Aコンバータ
- サンプル・アンド・ホールド回路

3 概要

LF442-MILはデュアル低消費電力オペアンプで、業界標準のLM1458と同じAC特性の多くを保有しながら、LM1458よりもDC特性が大幅に向上しています。これらのアンプはLM1458と同じ帯域幅、スルー・レート、ゲイン(10kΩ負荷)を持ち、LM1458の1/10の電力しか消費しません。さらに、適切にマッチングされた高電圧JFET入力デバイスを搭載しているため、入力バイアス電流およびオフセット電流は、LM1458の10,000分の1に減少します。注意深いレイアウト設計と内部的なトリミングの組み合わせにより、非常に低い入力オフセット電圧と電圧ドリフトを保証できます。また、LF442-MILは低消費電力アンプとしては、等価入力ノイズ電圧が非常に低くなっています。

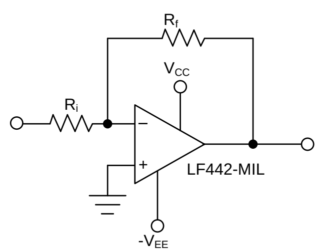
LF442-MILはLM1458とピン互換なので、多くのアプリケーションですぐに消費電力を1/10に削減できます。LF442-MILは、低消費電力と優れた電気的特性が主な考慮点である場合に使用します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LF442-MILACN	PDIP (8)	9.59mm×6.35mm
LF442-MILAMH	TO-99 (8)	直径8.96mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

反転アンプ



目次

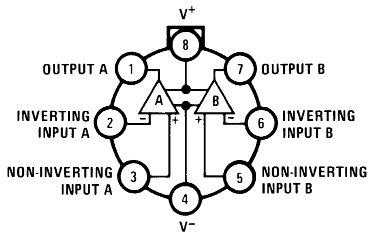
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年6月	*	初版

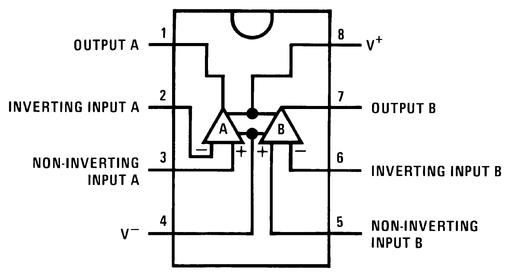
5 Pin Configuration and Functions

TO Package
8-Pin LMC
Top View



Pin 4 connected to case

P Package
8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Inverting input A	2	Input	Amplifier A inverting input
Inverting input B	6	Input	Amplifier B inverting input
Noninverting input A	3	Input	Amplifier A noninverting input
Noninverting input B	5	Input	Amplifier B noninverting Input
Output A	1	Output	Amplifier A output
Output B	7	Output	Amplifier B output
V+	8	Power	Positive supply
V-	4	Power	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

Supply voltage	±18 V
Differential input voltage	±30 V
Input voltage range(3)	±15 V
Output short circuit duration(4)	Continuous
Storage temperature, T_{stg}	–65 to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to RETS442X for LF442MH military specifications.
(3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(4) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

6.2 Absolute Maximum Ratings(1)(2)

	LMC0008C Package	P0008E Package
T_J max	150°C	115°C
Operating temperature range	See(3)(4)	See(3)(4)
Lead Temperature (Soldering, 10 sec.)	260°C	260°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to RETS442X for LF442MH military specifications.
(3) These devices are available in both the commercial temperature range 0°C ≤ T_A ≤ 70°C and the military temperature range −55°C ≤ T_A ≤ 125°C. The temperature range is designated by the position just before the package type in the device number. A “C” indicates the commercial temperature range and an “M” indicates the military temperature range. The military temperature range is available in “H” package only.
(4) The value given is in static air.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage			±15	V

6.4 Thermal Information

THERMAL METRIC(1)			LF442-MIL		UNIT
			LMC (TO)	P (PDIP)	
			8 PINS	8 PINS	
$R_{\theta JA}$ (Typical)	Junction-to-ambient thermal resistance	400 linear feet/min air flow	65	114	°C/W
		Static air	165	152	
$R_{\theta JC}$ (Typical)	Junction-to-case thermal resistance		21		°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics[1][2]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	R_S = 10 kΩ, T_A = 25°C			1	5	mV
		Over temperature				7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of input offset voltage	R_S = 10 kΩ			7		μV/°C
I_{OS}	Input offset voltage	V_S = ±15 V[1][3]	T_J = 25°C		5	50	pA
			T_J = 70°C			1.5	nA
			T_J = 125°C				nA
I_B	Input bias current	V_S = ±15 V[1][3]	T_J = 25°C		10	100	pA
			T_J = 70°C			3	nA
			T_J = 125°C				nA
R_{IN}	Input resistance	T_J = 25°C			10^{12}		Ω
A_{VOL}	Large signal voltage gain	V_S = ±15 V, V_O = ±10 V, R_L = 10 kΩ, T_A = 25°C		25	200		V/mV
		Over temperature		15	200		V/mV
V_O	Output voltage swing	V_S = ±15 V, R_L = 10 kΩ		±12	±13		V
V_{CM}	Input common-mode voltage range			±11	14		V
					−12		V
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		70	95		dB
PSRR	Supply voltage rejection ratio	See[4]		70	90		dB
I_S	Supply current				400	500	μA

(1) Unless otherwise specified, the specifications apply over the full temperature range of V_S = ±15 V for the LF442-MIL. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.
(2) Refer to RETS442X for LF442-MIL MH military specifications.
(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15 V to ±5 V for the LF442-MIL.

6.6 AC Electrical Characteristics[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Amplifier to amplifier coupling	T_A = 25°C, f = 1 Hz-20 kHz (Input referred)		−120		dB
SR	Slew rate	V_S = ±15 V, T_A = 25°C	0.6	1		V/μs
GBW	Gain-bandwidth product	V_S = ±15 V, T_A = 25°C	0.6	1		MHz
e_n	Equivalent input noise voltage	T_A = 25°C, R_S = 100 Ω, f = 1 kHz		35		nV/√Hz
i_n	Equivalent input noise current	T_A = 25°C, f = 1 kHz		0.01		pA/√Hz

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S = ±15 V for the LF442-MIL. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.
(2) Refer to RETS442X for LF442-MIL MH military specifications.

6.7 Typical Characteristics

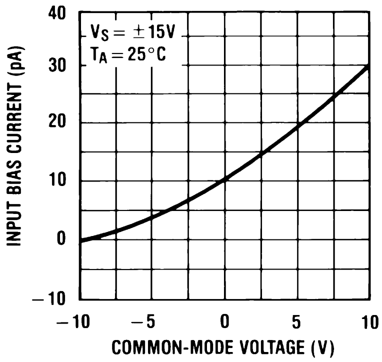


図 1. Input Bias Current

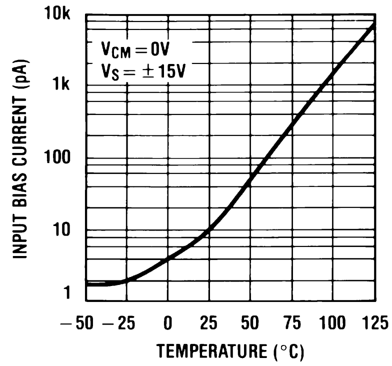


図 2. Input Bias Current

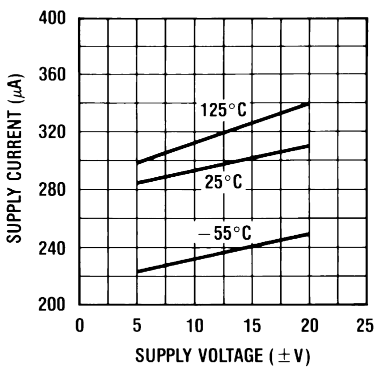


図 3. Supply Current

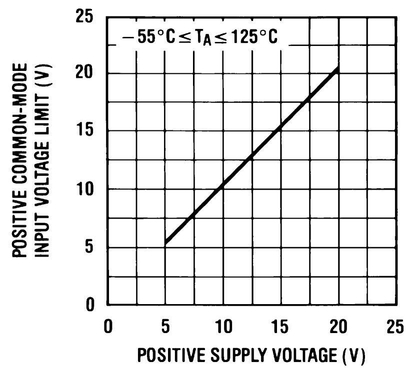


図 4. Positive Common-Mode Input Voltage Limit

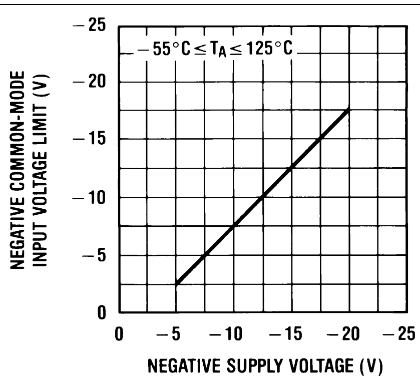


図 5. Negative Common-Mode Input Voltage Limit

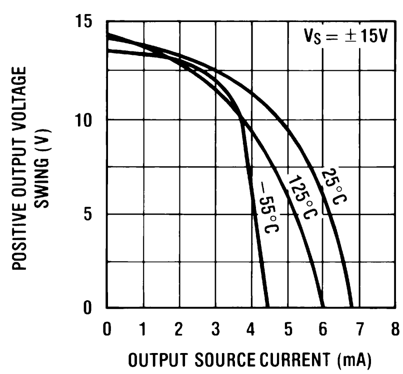


図 6. Positive Current Limit

Typical Characteristics (continued)

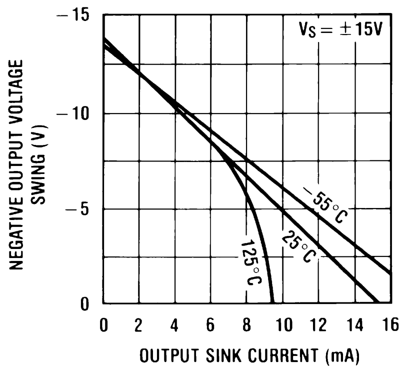


図 7. Negative Current Limit

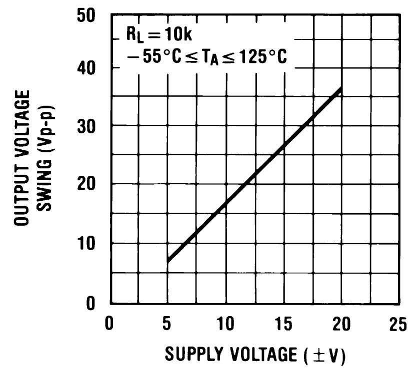


図 8. Output Voltage Swing

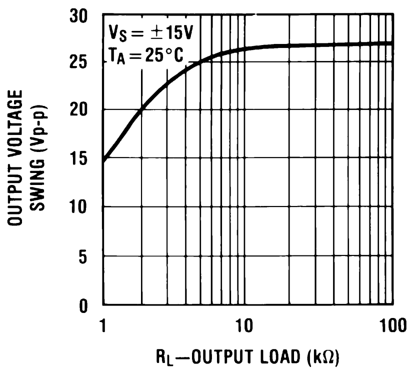


図 9. Output Voltage Swing

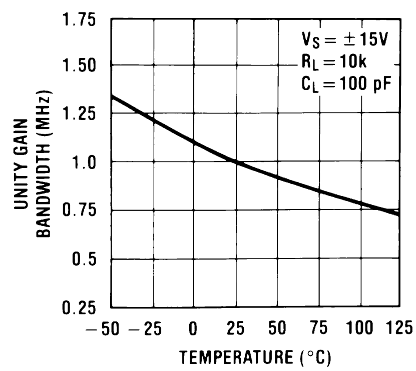


図 10. Gain Bandwidth

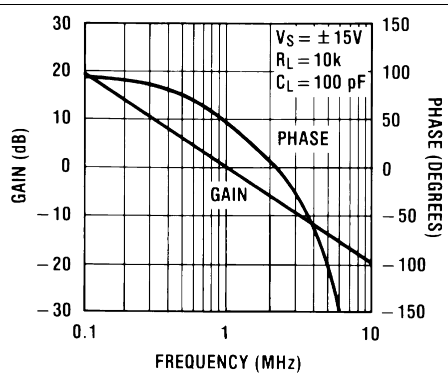


図 11. Bode Plot

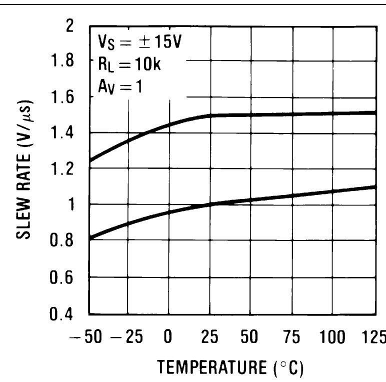


図 12. Slew Rate

Typical Characteristics (continued)

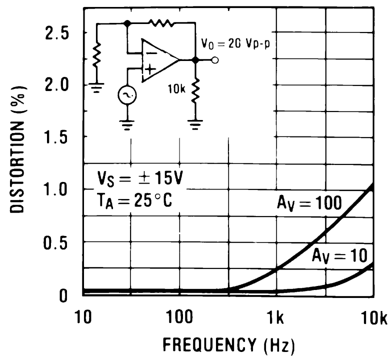


図 13. Distortion vs Frequency

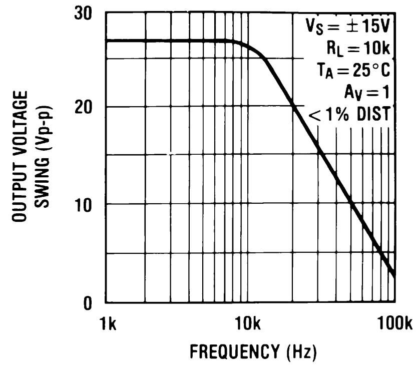


図 14. Undistorted Output Voltage Swing

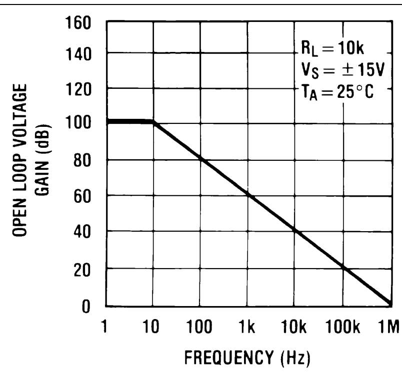


図 15. Open Loop Frequency Response

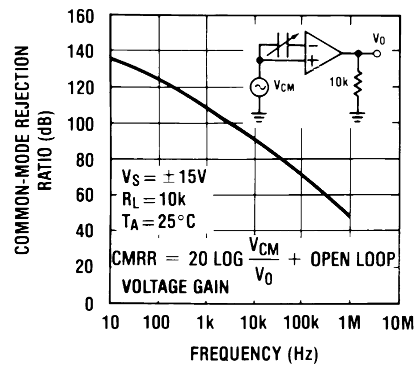


図 16. Common-Mode Rejection Ratio

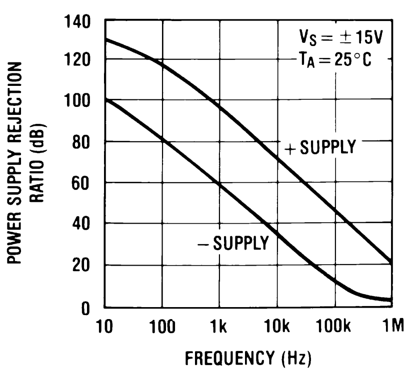


図 17. Power Supply Rejection Ratio

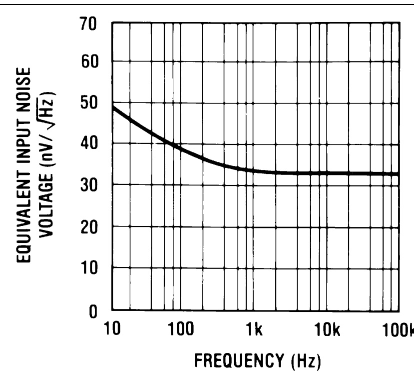


図 18. Equivalent Input Noise Voltage

Typical Characteristics (continued)

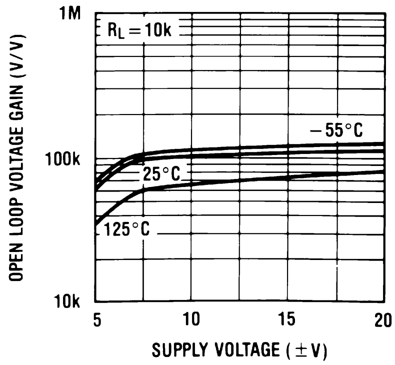


図 19. Open Loop Voltage Gain

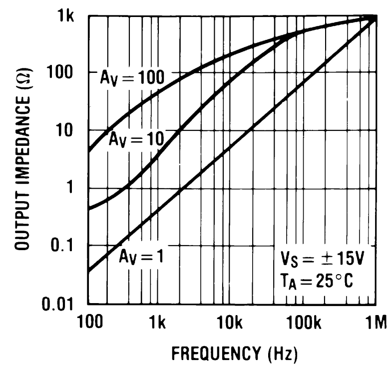


図 20. Output Impedance

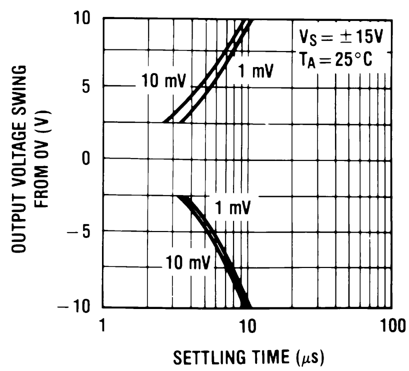


図 21. Inverter Settling Time

6.7.1 Pulse Response

R_L = 10 kΩ, C_L = 10 pF

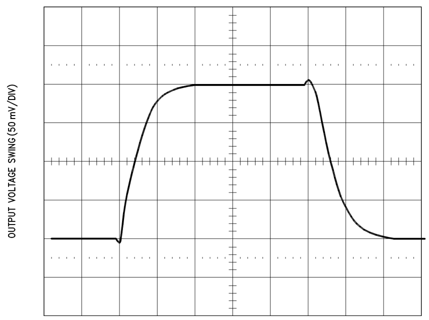


図 22. Small Signal Inverting

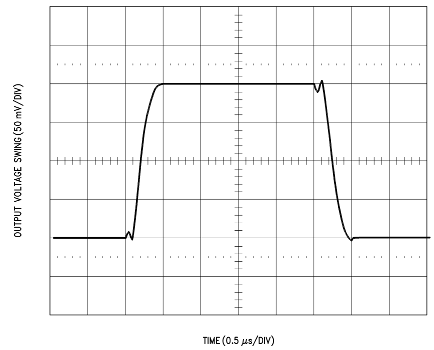


図 23. Small Signal Non-Inverting

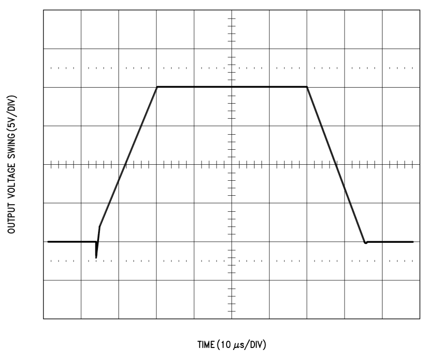


図 24. Large Signal Inverting

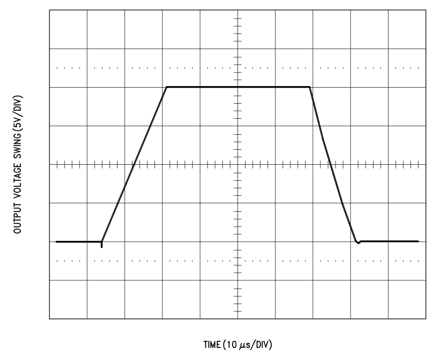


図 25. Large Signal Non-Inverting

7 Detailed Description

7.1 Overview

The LF442-MIL dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442-MIL reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming ensures very low input offset voltage and voltage drift. The LF442-MIL also has a very low equivalent input noise voltage for a low power amplifier.

The LF442-MIL is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442-MIL should be used where low power dissipation and good electrical characteristics are the major considerations.

7.2 Functional Block Diagram

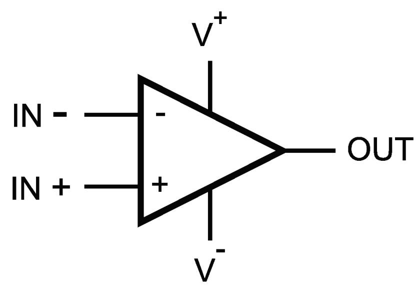


図 26. Each Amplifier

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (-IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by the equation $V_{OUT} = A_{OL}(IN+ - IN-)$.

7.4 Device Functional Modes

7.4.1 Input and Output Stage

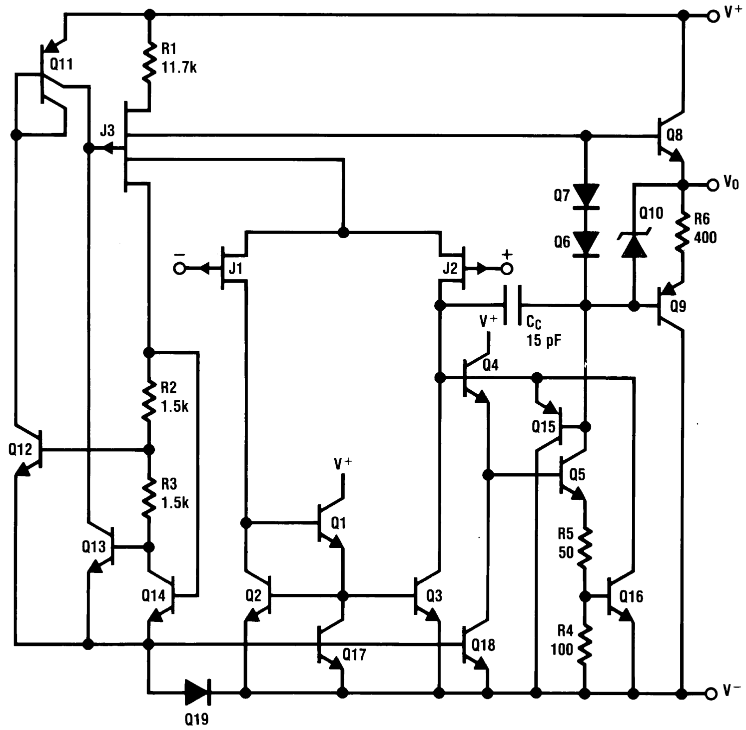


図 27. 1/2 Dual LF442-MIL

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LF442-MIL uses a combination of careful layout design and internal trimming to ensure very low input offset voltage and voltage drift. The LF442-MIL also has a very low equivalent input noise voltage for a low power amplifier. The LF442-MIL should be used where low power dissipation and good electrical characteristics are the major considerations.

8.2 Typical Applications

1. Battery Powered Strip Chart Preamplifier
2. "No FET" Low Power V to F Converter
3. High Efficiency Crystal Oven Controller
4. Conventional Log Amplifier
5. Unconvential Log Amplifier

8.2.1 Battery Powered Strip Chart Preamplifier

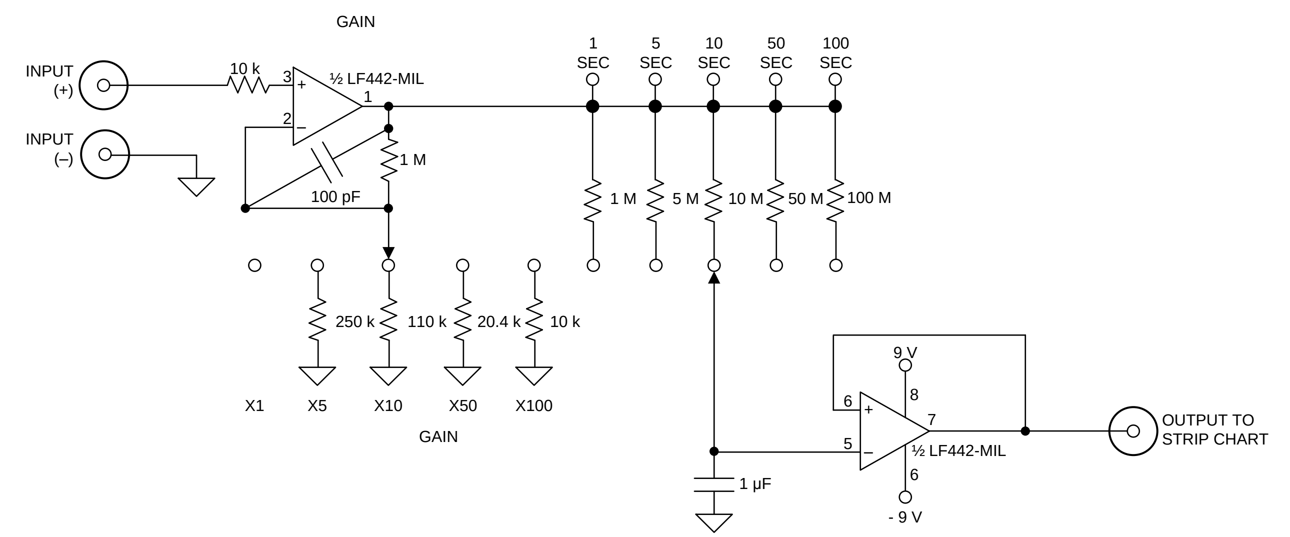


図 28. Battery Powered Strip Chart Preamplifier

8.2.1.1 Design Requirements

Runs from 9V batteries (±9V supplies).

Fully set gain and time constant.

Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

8.2.1.3 Application Curves

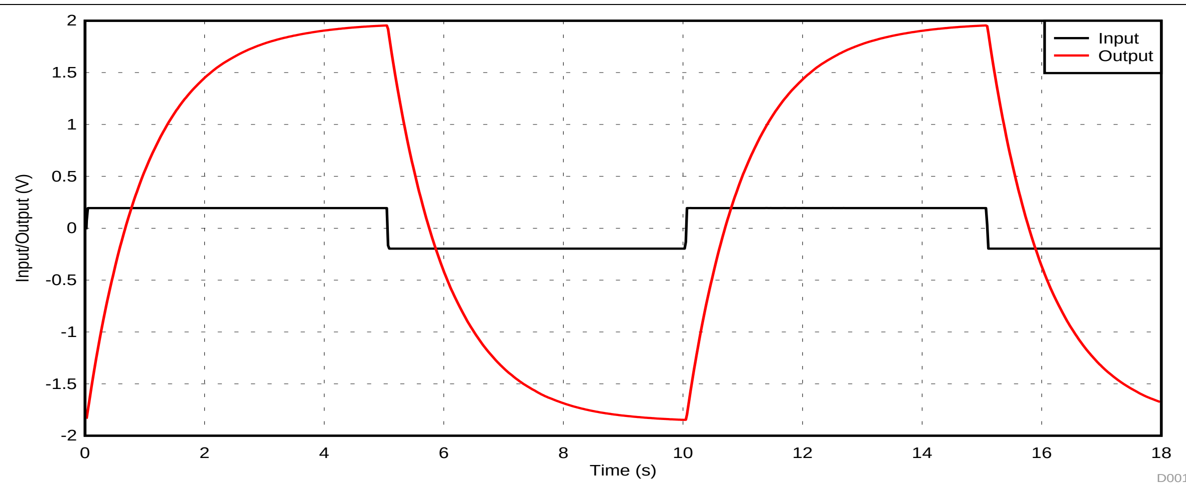


図 29. Input and Output Waveforms, Gain = 10, Time Constant = 1 Second

Typical Applications (continued)

8.2.2 "No FET" Low Power V to F Converter

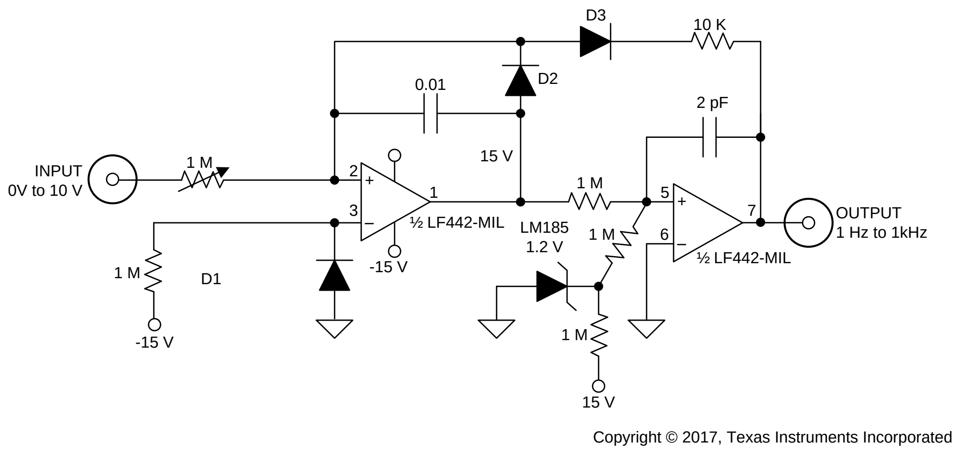


図 30. "No FET" Low Power V to F Converter

8.2.2.1 Design Requirements

1. Trim 1M pot for 1 kHz full-scale output.
2. 15 mW power drain.
3. No integrator reset FET required.
4. Mount D1 and D2 in close proximity.
5. 1% linearity to 1 kHz.

8.2.2.2 Detailed Design Procedure

See Section 8.2.1.2.

8.2.2.3 Application Curves

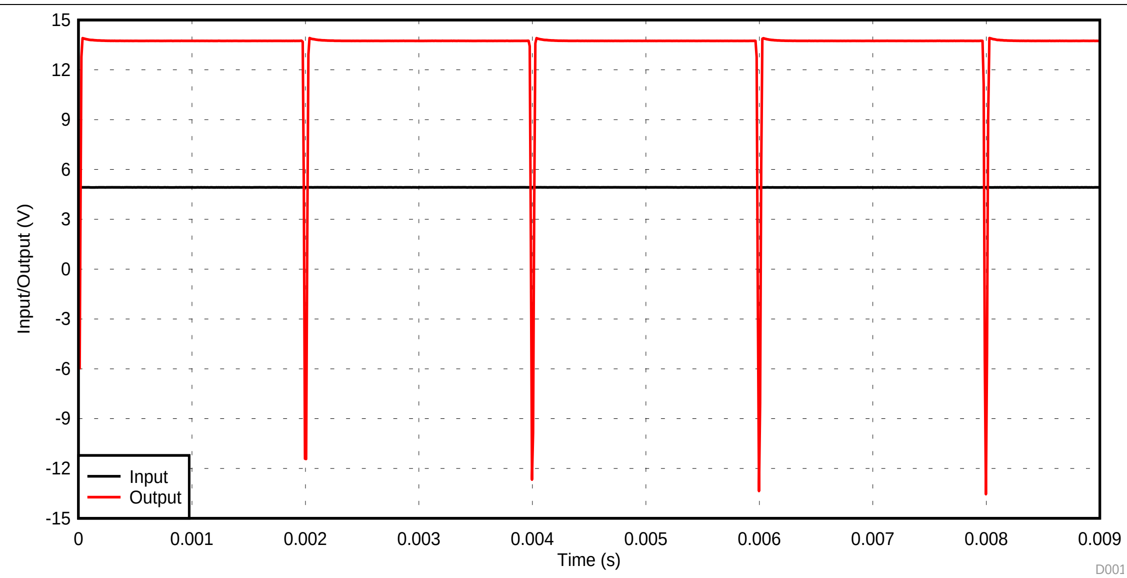


図 31. Input and Output Waveforms

Typical Applications (continued)

8.2.3 High Efficiency Crystal Oven Controller

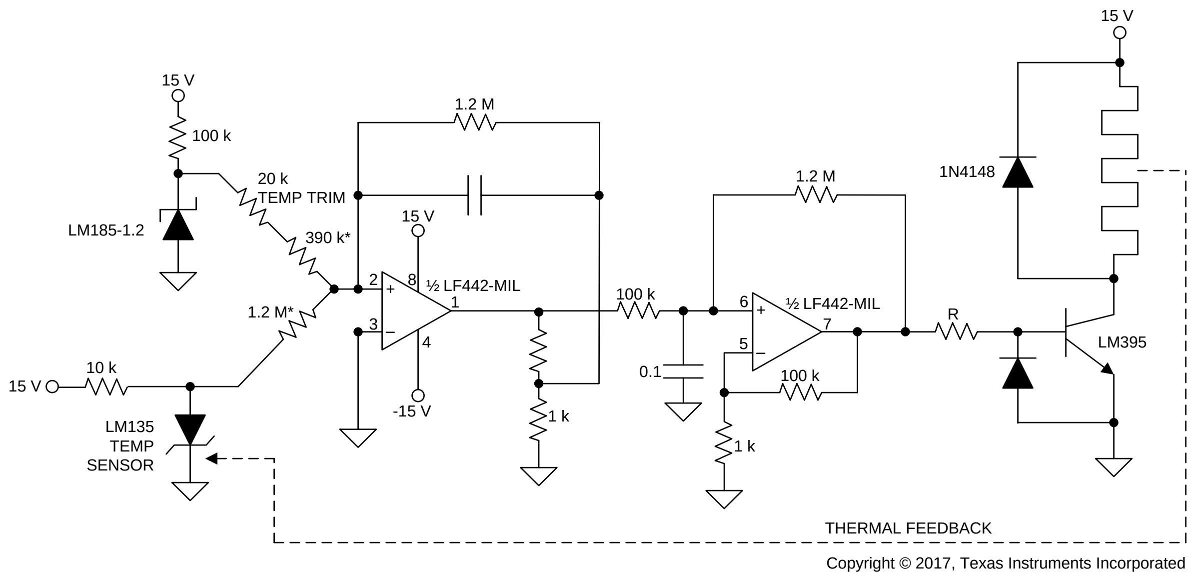


図 32. High Efficiency Crystal Oven Controller

8.2.3.1 Design Requirements

1. $T_{control}$= 75°C
2. A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature.
3. A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop.
4. Switched mode operation yields high efficiency.
5. 1% metal film resistor.

8.2.3.2 Detailed Design Procedure

See Section 8.2.1.2.

8.2.4 Conventional Log Amplifier

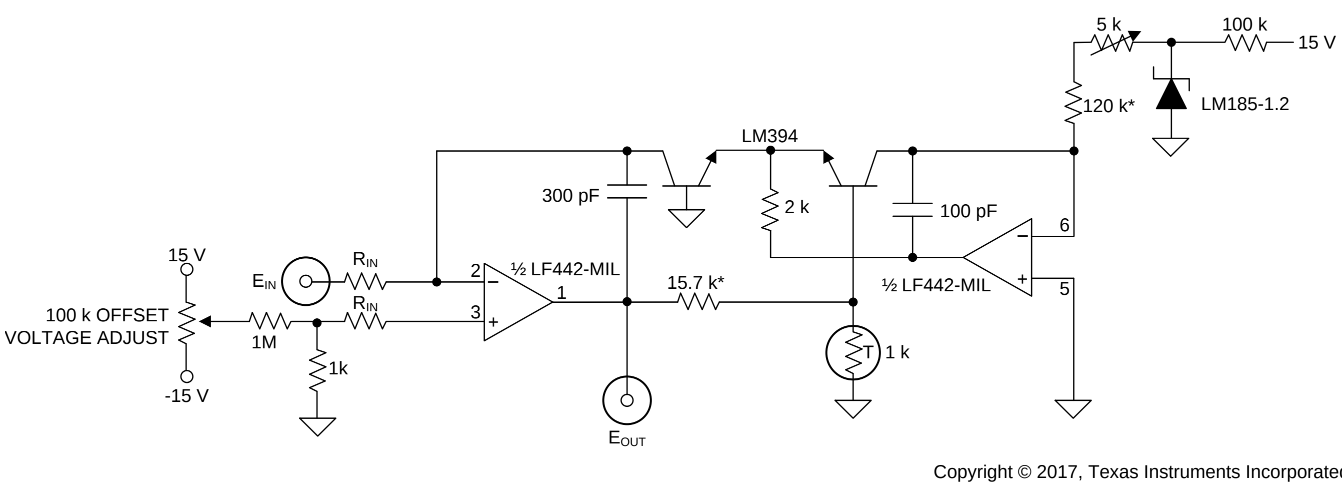


図 33. Conventional Log Amplifier

Typical Applications (continued)

$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

8.2.4.1 Design Requirements

1. R_T = Tel Labs type Q81.
2. Trim 5k for 10 μA through the 5k–120k combination.
3. *1% film resistor

8.2.4.2 Detailed Design Procedure

See Section 8.2.1.2.

8.2.5 Unconventional Log Amplifier

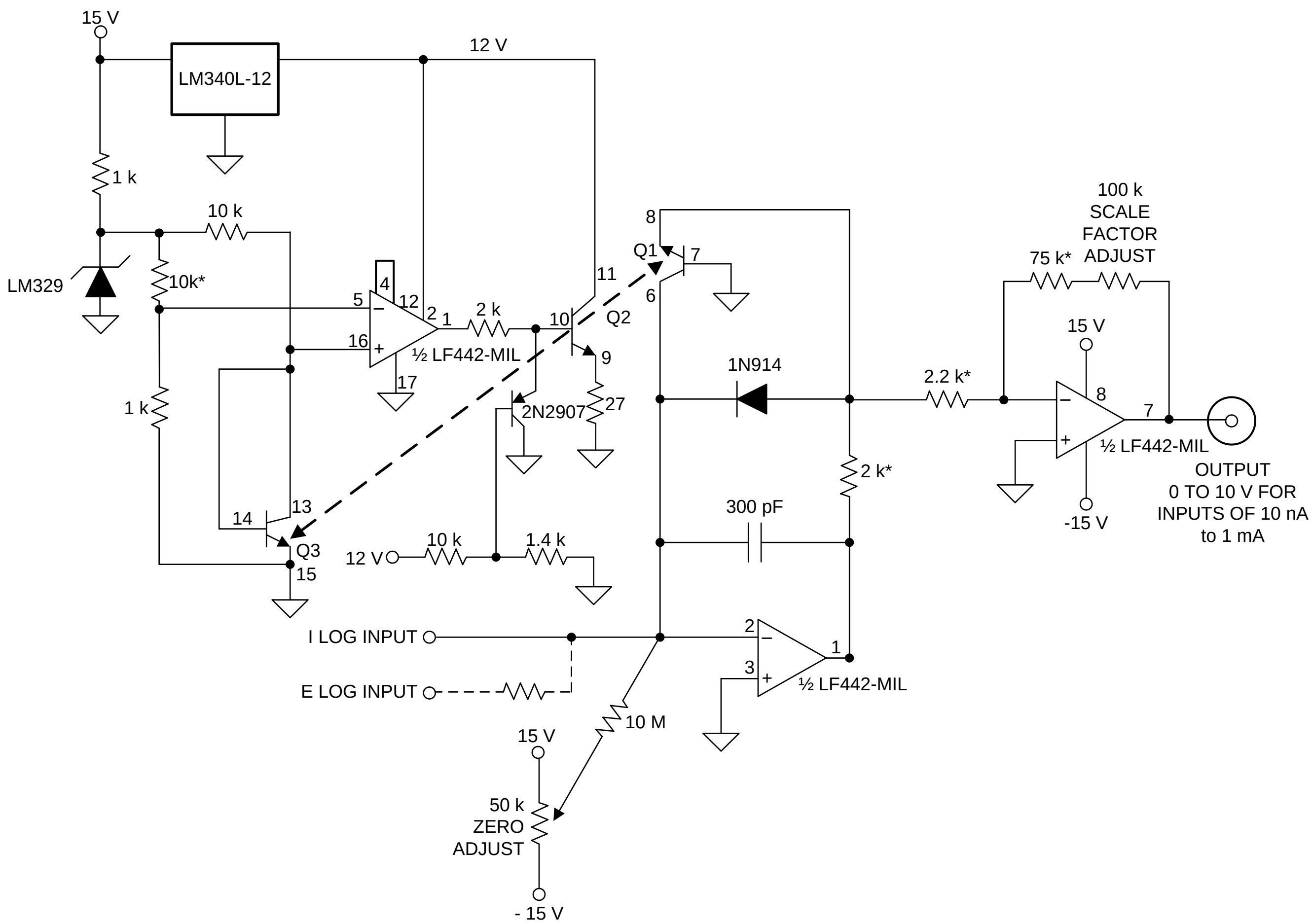


図 34. Unconventional Log Amplifier

8.2.5.1 Design Requirements

1. Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.
2. Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.

Typical Applications (continued)

8.2.5.2 Detailed Design Procedure

See Section 8.2.1.2.

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 0.1µF capacitors be placed as close as possible to the op amp power supply pins. The minimum power supply voltage is ±5V.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

10.2 Layout Example

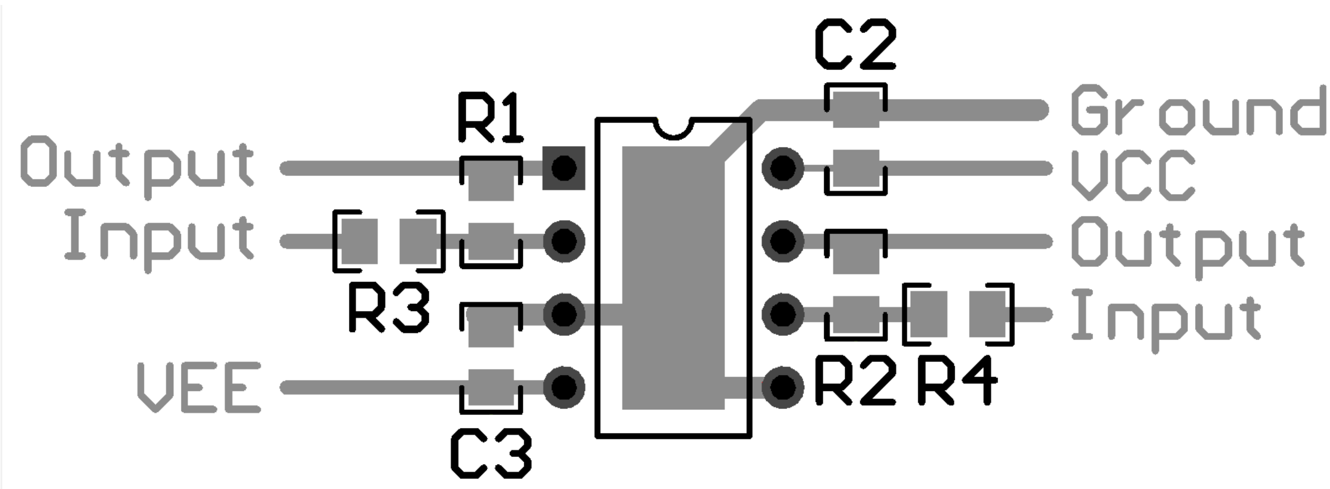


図 35. LF442-MIL Layout

11 デバイスおよびドキュメントのサポート

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF442-MWA	Active	Production	WAFERSALE (YS) | 0	1 | NOT REQUIRED	-	Call TI	Level-1-NA-UNLIM	-40 to 85	
LF442AMH	Active	Production	TO-99 (LMC) | 8	500 | TRAY NON-STD	No	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF442AMH, LF442A MH)
LF442AMH/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF442AMH, LF442A MH)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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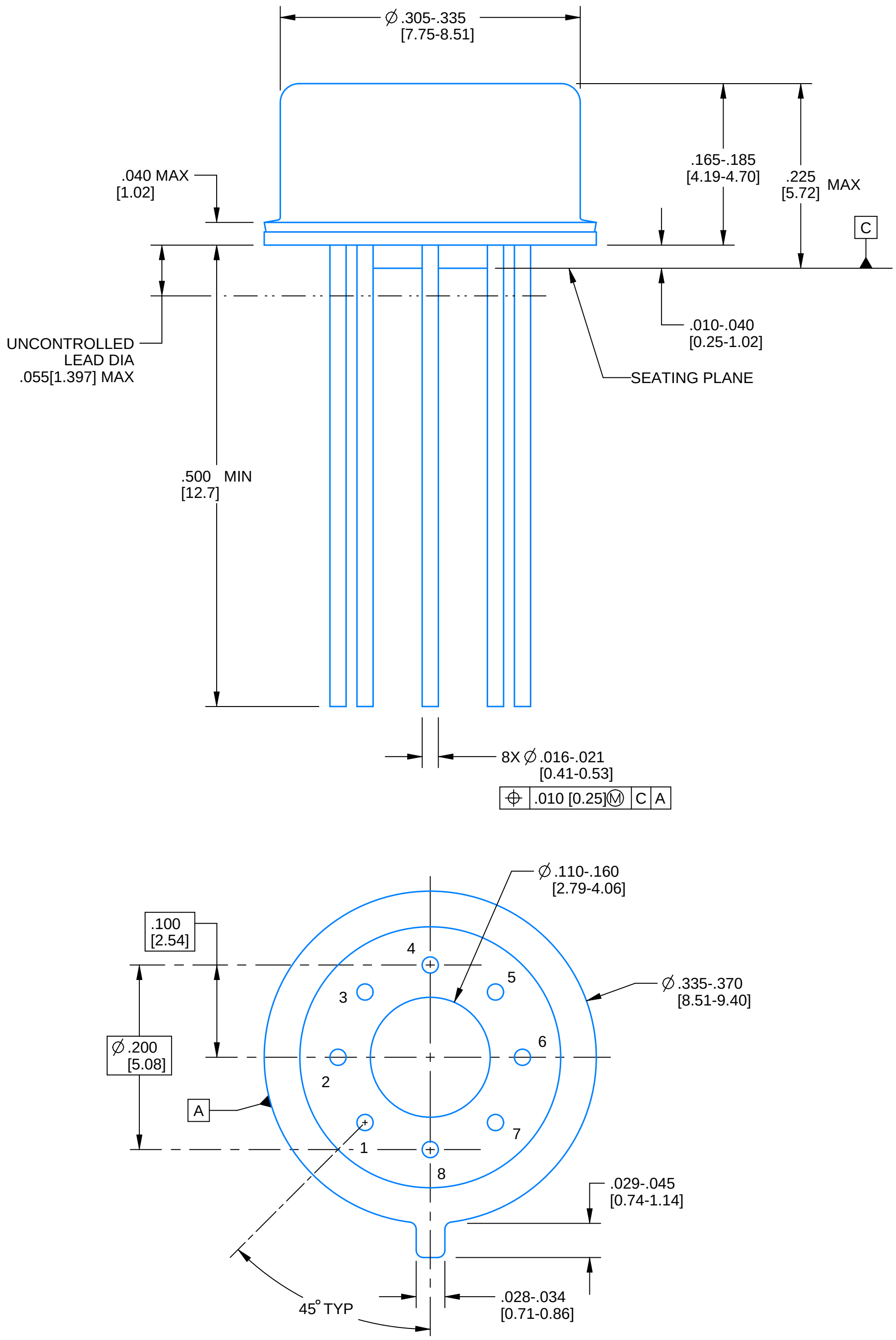
LMC0008A

TO-CAN - 5.72 mm max height

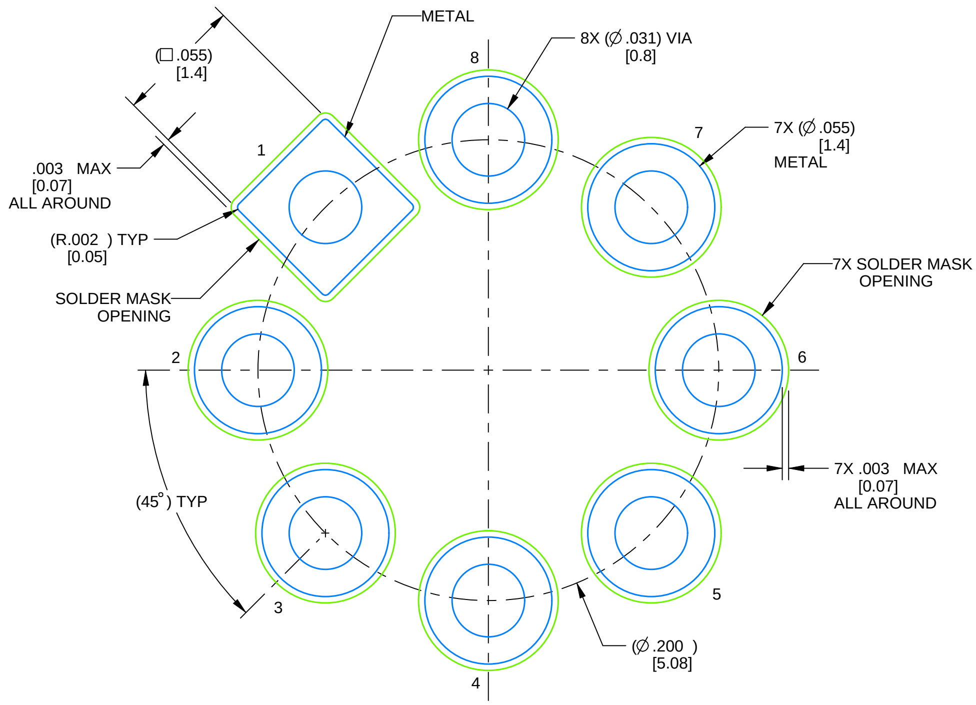
TRANSISTOR OUTLINE



4220610/B 09/2024

NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

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最終更新日：2025 年 10 月