LM4060 18ppm/°C Maximum Drift High Precision Shunt Voltage Reference

1 Features

- Low operating current:
  - 40μA typical
- Initial accuracy: ±0.05 % (maximum)
- Temperature coefficient:
  - 6ppm/°C typical for −40°C to 125°C
- Wide operating current range up to 50mA
- No output capacitor required
- Capable of driving capacitive loads up to 4.7μF
- Output voltages options:
  - 1.25V, 1.5V 1.6V 1.65V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V
- Low output noise:
  - 10Hz to 1kHz: 26ppm$_{\text{rms}}$
  - Output 1/f noise (0.1Hz to 10Hz): 9ppm$_{\text{P-P}}$
- Long-term stability: 40ppm at 1000 hours
- Specified temperature range −40°C to 125°C
- Small footprint 3-pin SOT−23 package
- Pin-to-pin compatible with LM4040, LM4040-N, TL4050, and LM4050-N

2 Applications

- Data-acquisition systems
- Instrumentation and test equipment
- Process control
- Energy management, metering
- Precision audio

3 Description

The LM4060 is a family of high-precision shunt voltage references. The LM4060 family offers low 18ppm/°C temperature coefficient and 0.05% high precision initial accuracy. The LM4060 design eliminates the need for an external stabilizing capacitor and provides stability with capacitive loads up to 4.7μF. The LM4060 is offered in several fixed reverse breakdown voltages: 1.25V, 1.5V, 1.6V, 1.65V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V. The flexible voltage options make the LM4060 a companion device for ADCs, DACs, and level shifting signal conditioning circuits.

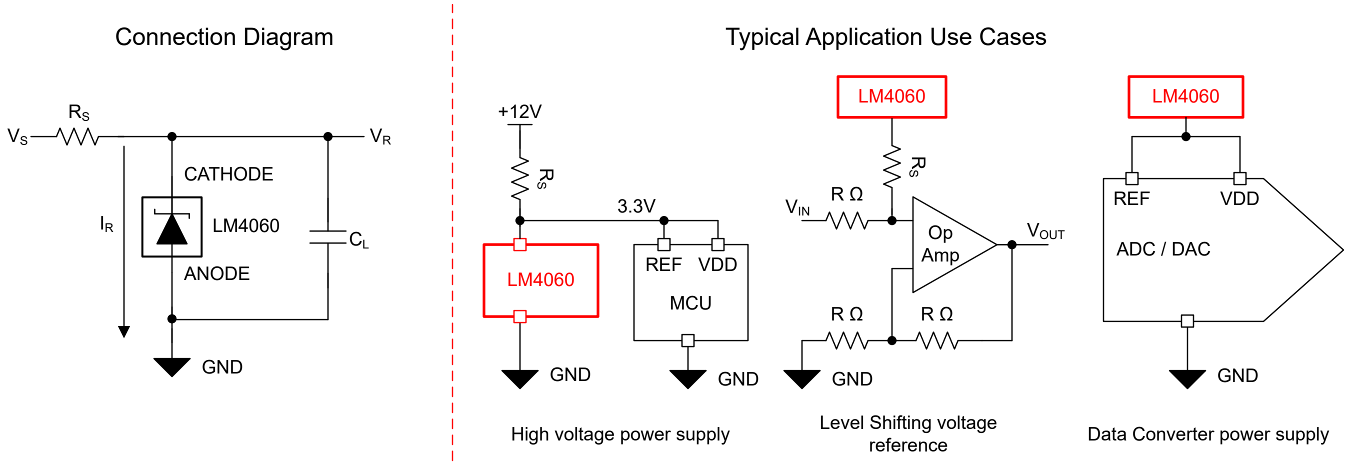
The LM4060 supports a maximum operating current up to 50mA to support a wide range of loads. The wide load current support allows for powering of ADCs, DACs, and MCUs while providing a stable voltage reference. The LM4060 functionality is similar to a Zener diode where the cathode voltage is constant above the minimum operating current. The LM4060 can be powered from a wide input supply voltage but an external resistor is required.

The LM4060 is specified for −40°C and 125°C, which enables operation across various industrial applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM4060	DBZ (SOT-23, 3)	2.92mm × 2.37mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



LM4060 Use Case

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4 Device Comparison Table

The LM4060 has multiple voltage options available. Use the following table as the part number decoding table for all devices. For devices marked preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options.

ORDERABLE PART NAME	V_R
LM4060A12EDBZR	1.25V
LM4060A15EDBZR (1)	1.5V
LM4060A16EDBZR (1)	1.6V
LM4060A165EDBZR (1)	1.65V
LM4060A18EDBZR (1)	1.8V
LM4060A20EDBZR	2.048V
LM4060A25EDBZR	2.5V
LM4060A30EDBZR	3.0V
LM4060A33EDBZR	3.3V
LM4060A41EDBZR (1)	4.096V
LM4060A50EDBZR	5.0V

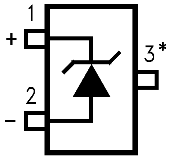
(1) Preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options

Table 4-1. Shunt Voltage Reference Summary Table

Specification	LM4060	LM4030	LM4050-N, TL4050 (2)	LM4051-N, TL4051 (2)	LM4040-N, LM4040 (2)	LM4041-N, LM4041 (2)	REF1112
V_R	1.25V, 1.5V(1), 1.6V(1), 1.65V(1), 1.8V(1), 2.048V, 2.5V, 3.0V, 3.3V, 4.096V, 5V	2.5V, 4.096V	2.048V, 2.5V, 4.096V, 5V, 8.192V, 10V	1.225V, Adjustable	2.048V, 2.5V, 3V, 4.096V, 5V, 8.192V, 10V	1.225V, Adjustable	1.25V
V_R Accuracy	0.05%	0.05%, 0.1%, 0.15%	0.1%, 0.2%, 0.5%	0.1%, 0.2%, 0.5%	0.1%, 0.2%, 0.5%, 1%, 2%	0.1%, 0.2%, 0.5%, 1%, 2%	0.2%
V_R Temp Co (Max)	18ppm/°C	20ppm/°C	50ppm/°C	50ppm/°C	100ppm/°C	100ppm/°C	50ppm/°C
$I_{R(MAX)}$	50mA	30mA	10mA	12mA	10mA	12mA	5mA
I_{RMIN}	50µA	120µA	65µA	65µA	65µA	65µA	1.2µA
Long Term Stability (t = 1000 hrs)	40ppm	40ppm	120ppm	120ppm	120ppm	120ppm	60ppm

(1) Preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options
(2) Refer to product data sheet for the most up to date product specifications and availability.

5 Pin Configuration and Functions



*This pin must be left floating or connected to pin 2.

Figure 5-1. DBZ Package
3-Pin SOT-23
Top View

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Cathode	1	I/O	Shunt current and input voltage
Anode	2	O	Common pin, normally connected to ground
DNC	3	—	This pin must be left floating or connected to pin 2.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
I_R	Reverse Current		55	mA
T_J	Maximum Junction Temperature		150	C
Tstg	Storage Temperature	–65	150	C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

6.3 Recommended Operating Conditions

conditions apply over the operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I_R	Continuous Cathode Current Range		I_{RMIN}	50	mA
T_J	Junction Temperature		–40	125	C

6.4 Thermal Information

THERMAL METRIC[1]		LM4060 DBZ (SOT-23) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229.8	C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.7	C/W
$R_{\theta JB}$	Junction-to-boardthermal resistance	99.4	C/W
Ψ_{JT}	Junction-to-top characterization resistance	16.5	C/W
Ψ_{JB}	Junction-to-board characterization resistance	98.6	C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

over recommended operating conditions, T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_R	Reverse breakdown voltage Accuracy	I_R = 100µA		–0.05		0.05	%
V_R	Output voltage temperature coefficient (1)	I_R = 100µA	T_J = –40°C to 125°C		6	18	ppm/°C
I_{RMIN}	Minimum cathode current		T_J = –40°C to 125°C		35	50	µA
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} < I_R <$ 50mA	T_J = –40°C to 125°C			50	ppm/mA
Z_R	Reverse Dynamic Impedance(2)	I_R = 1mA, F = 120Hz, I_{AC} = 0.1 I_R			0.55	1.5	Ω
e_{np-p}	Low frequency noise	I_R = 100µA, 0.1Hz ≤ f ≤ 10Hz			9		$µV_{p-p}$/V
e_N	Wideband Noise	I_R = 100µA, 10 Hz ≤ f ≤ 10kHz			27		ppm_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	V_R = 3.3V, I_R = 100µA	t = 1000hr, T_A = 35°C ±0.1C		40		ppm
ΔV_R	Reverse Breakdown Voltage Long Term Stability	V_R = 3.3V, I_R = 100µA	t = 2000hr, T_A = 35C ±0.1°C		55		ppm
V_{HYST}	Thermal Hysteresis	V_R = 3.3V	T_A = 25°C, –40°C, 125°C, 25°C (cycle 1)		130		ppm
V_{HYST}	Thermal Hysteresis	V_R = 3.3V	T_A = 25°C, –40°C, 125°C, 25°C (cycle 2)		20		ppm
C_L	Stable output capacitor range		T_J = –40°C to 125°C			4.7	µF
t_{ST}	Settling Time	I_R = 100µA, C_L = 0µF, 99% of V_R			2000		µS
t_{ST}	Settling Time	I_R = 1mA, C_L = 1µF, 99% of V_R			6		mS

(1) The temperature coefficient parameter for V_R is calculated using the box method which is the difference between the maximum and minimum values obtained over the rated temperature range. For more details on V_R and average temperature coefficient, see *Parameter Measurement Information* .

(2) The dynamic impedance is defined by $|Z_R| = \Delta V_R/\Delta I_R$. This parameter is established by design or characterization and is not tested in production.

6.6 Typical Characteristics

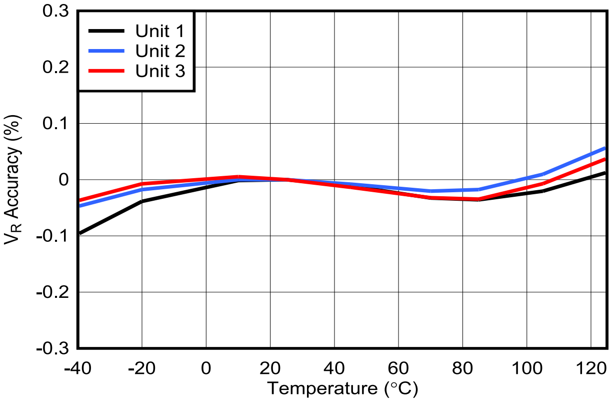


Figure 6-1. Temperature Drift

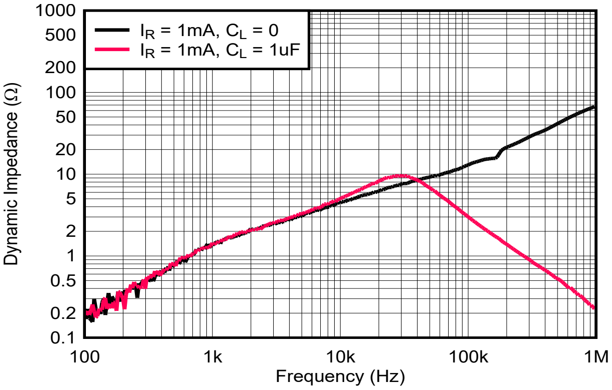


Figure 6-2. Output Impedance vs Frequency, V_R = 1.25V

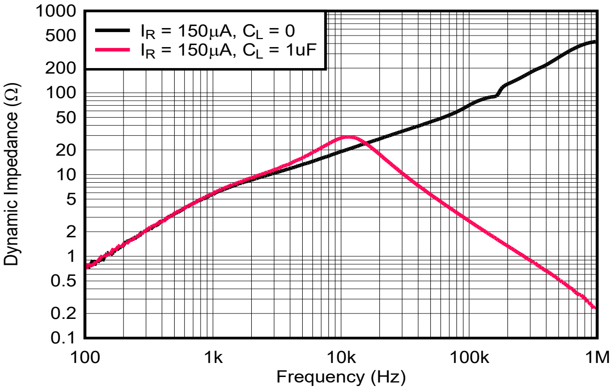


Figure 6-3. Output Impedance vs Frequency, V_R = 1.25V

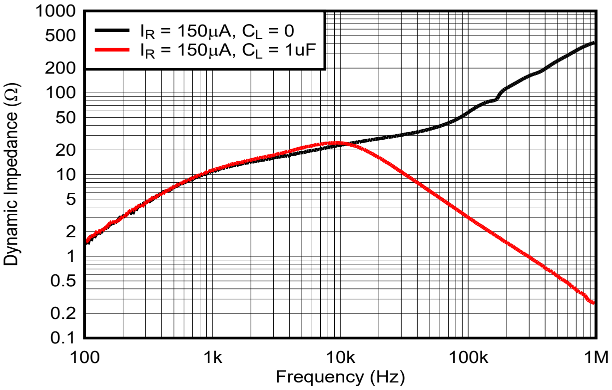


Figure 6-4. Output Impedance vs Frequency, V_R = 3.3V

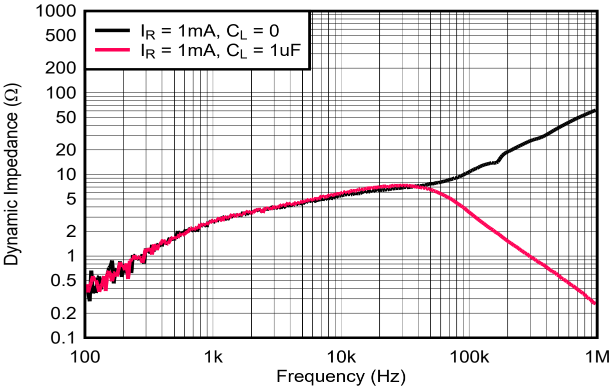


Figure 6-5. Output Impedance vs Frequency, V_R = 3.3V

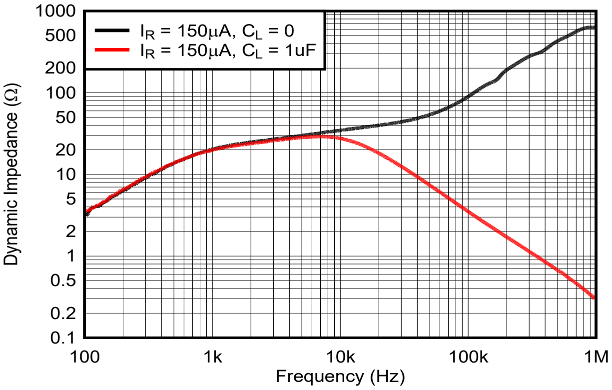


Figure 6-6. Output Impedance vs Frequency, V_R = 5V

6.6 Typical Characteristics (continued)

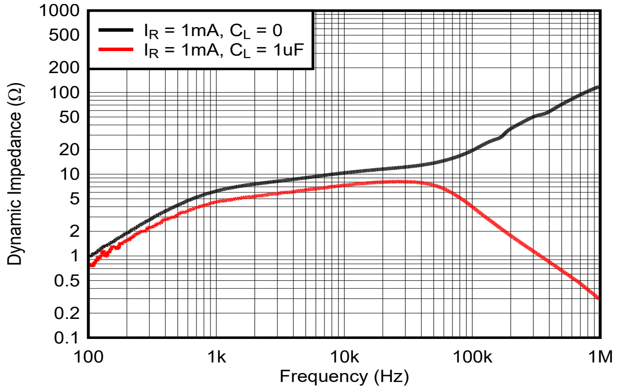


Figure 6-7. Output Impedance vs Frequency, V_R = 5V

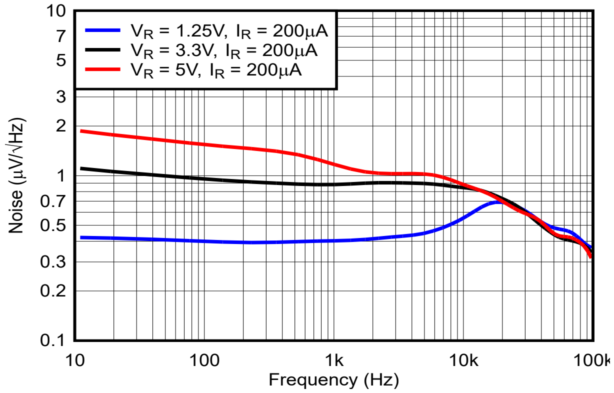


Figure 6-8. Noise Spectral Density

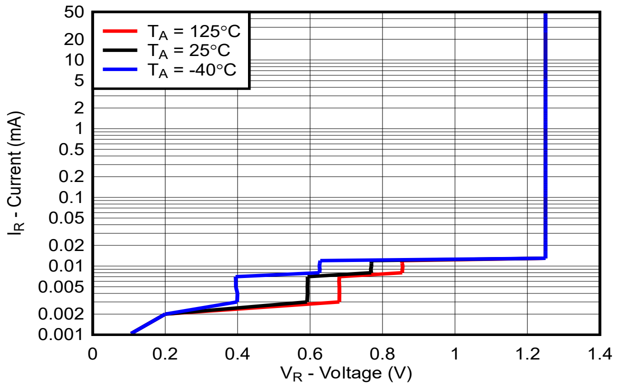


Figure 6-9. Minimun Operating Voltage, V_R = 1.25V

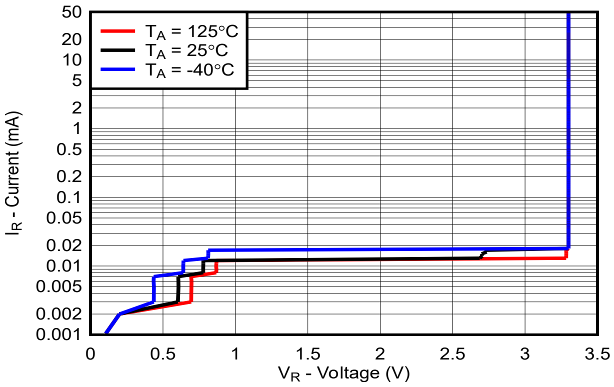


Figure 6-10. Minimun Operating Voltage, V_R = 3.3V

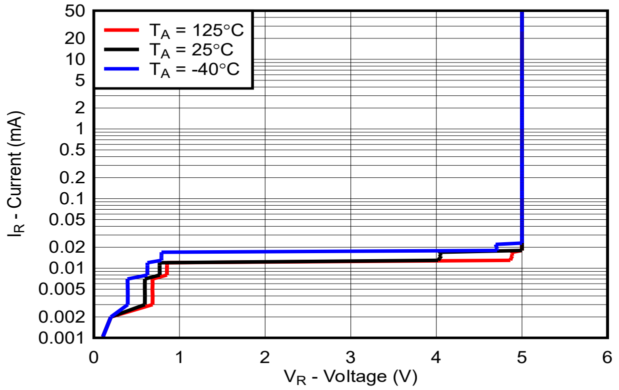


Figure 6-11. Minimun Operating Voltage, V_R = 5V

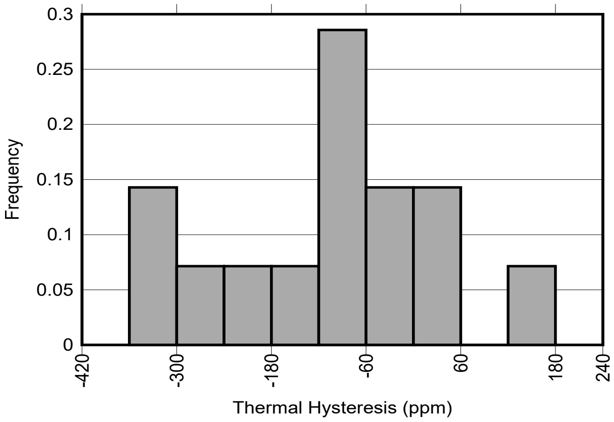


Figure 6-12. Thermal Hysteresis - Cycle 1

6.6 Typical Characteristics (continued)

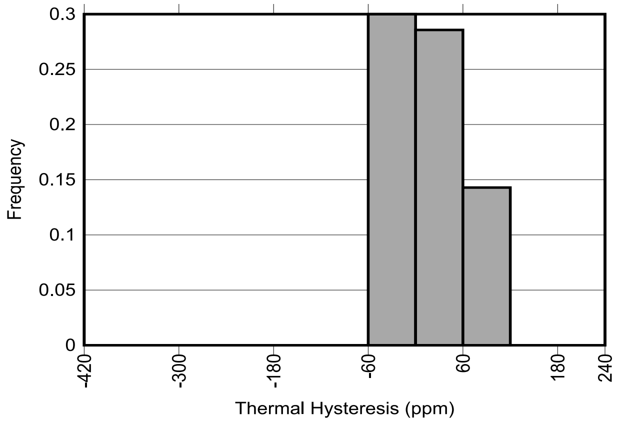


Figure 6-13. Thermal Hysteresis - Cycle 2

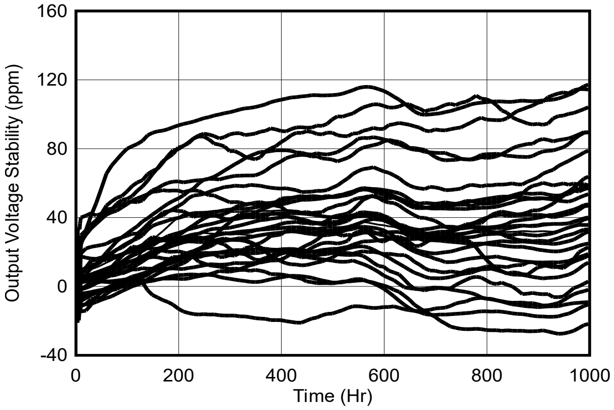


Figure 6-14. Long Term Stability - 1000 hours (V_R)

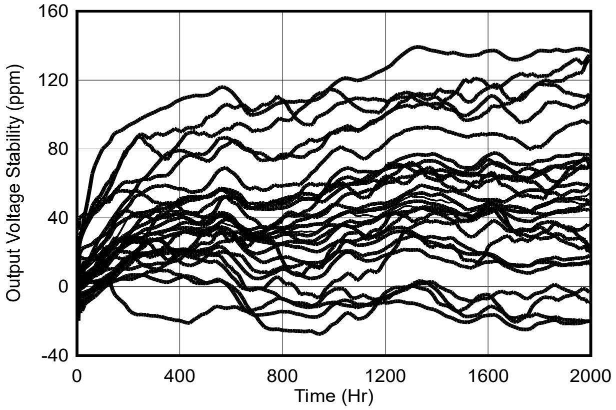


Figure 6-15. Long Term Stability - 2000 hours (V_R)

7 Parameter Measurement Information

7.1 Temperature Coefficient

The LM4060 temperature coefficient is calculated using the box method. The box method temperature coefficient of V_R is defined in Figure 7-1. The box method temperature coefficient is an average of the full operating temperature range and therefore any subsection of the rated operating temperature range can yield a value that is greater or less than the average. For more details on temperature coefficient, refer to the *Voltage Reference Selection Basics* white paper.

$$TC_{BOX} = 10^6\left(\frac{V_{R(MAX)} - V_{R(MIN)}}{V_{R(25°C)}}\right)\left(\frac{1}{T_{MAX} - T_{MIN}}\right) \quad (1)$$

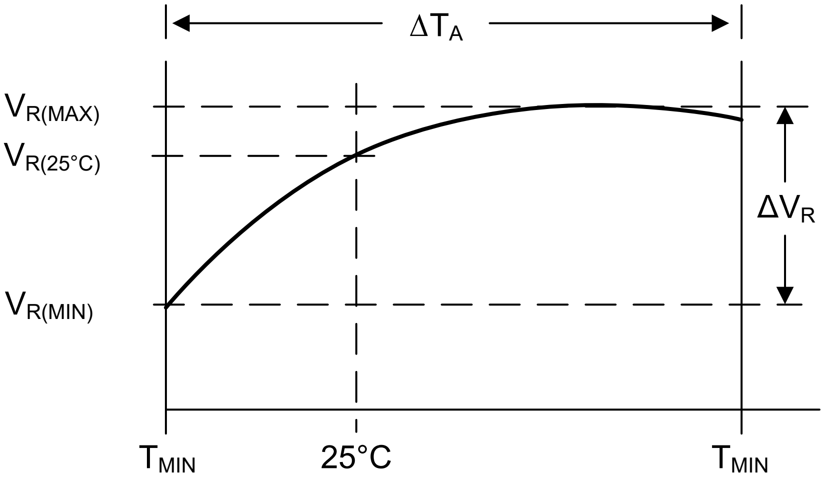


Figure 7-1. Temperature Coefficient

7.2 Solder Heat Shift

The materials used in the manufacturing of the LM4060 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 32 devices were soldered on one printed circuit board using lead-free solder paste and the paste manufacturer suggested reflow profile. Figure 7-2 shows the reflow profile. The printed circuit board is comprised of FR4 material. The board thickness is 1.66mm and the area is 174mm × 135mm.

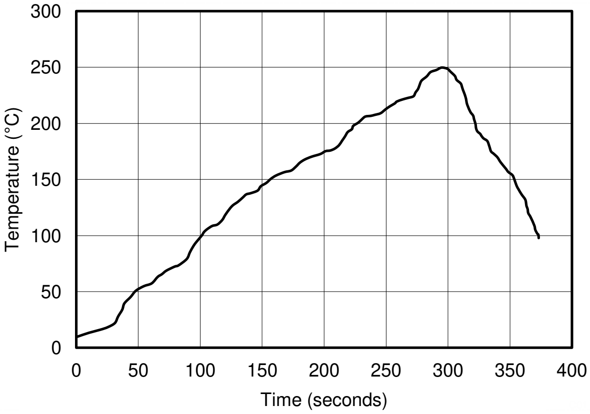


Figure 7-2. Reflow Profile

The reference output voltage is measured before and after the reflow process; Figure 7-3 shows the typical shift. Although all tested units exhibit very low shifts (< 0.04%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board (PCB). An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize the exposure to thermal stress.

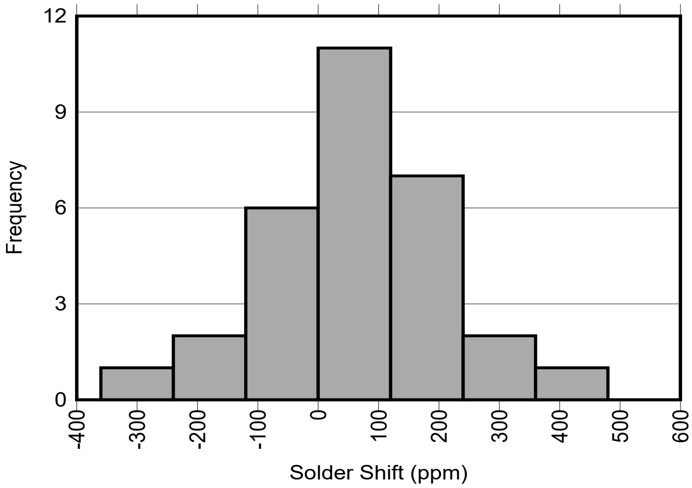


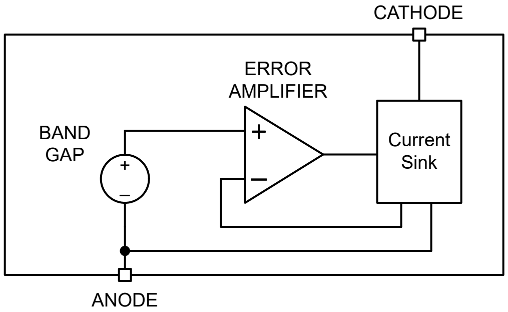
Figure 7-3. Solder Heat Shift Distribution, V_{REF} (%)

8 Detailed Description

8.1 Overview

The LM4060 is a family of high-precision shunt voltage references. The LM4060 family offers low 18ppm/°C temperature coefficient and 0.05% high precision initial accuracy. The LM4060 design eliminates the need for an external stabilizing capacitor and provides stability with capacitive loads up to 4.7µF.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Current (I_R)

In a conventional shunt regulator application (Figure 8-1) , an external series resistor (R_S) is connected between the supply voltage and the LM4060. R_S determines the current that flows through the load (I_L) and the LM4060 (I_R). Since load current and supply voltage varies, R_S has to be small enough to supply at least the maximum I_{RMIN} (spec. table) to the LM4060 even when the supply voltage is at the minimum and the load current is at the maximum value. When the supply voltage is at the maximum and I_L is at the minimum, R_S has to be large enough so that the current flowing through the LM4060 is less than 50mA.

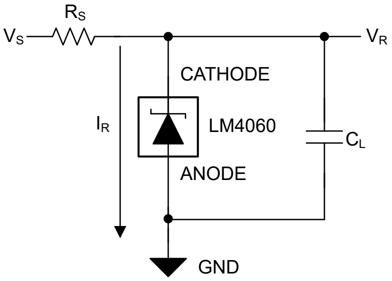


Figure 8-1. LM4060 Typical Diagram

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_R), and the LM4060 reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_R} \tag{2}$$

8.4 Device Functional Modes

The LM4060 operates in closed loop due to the fact that the feedback is internal to the device. Additionally, the output voltage cannot be adjusted for the same reason. The output voltage is regulated in a closed loop, provided the R_S (see Figure 8-1) resistor is sized to deliver the current to the cathode within the limits specified for operation.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM4060 shunt voltage reference with high accuracy and high sink current capabilities is suitable reference for multiple applications. The device can be used as a precision high accuracy low noise voltage reference for data converters or level shifting circuits for signal chains. With the LM4060 50mA capabilities, the device can be the voltage reference and the power supply to sensor or data converter instead of traditional LDO or DC/DC based power supply. As a shunt voltage reference, the LM4060 can be powered from any voltage rail greater than V_R with proper resistor sizing including 12V supply rails.

9.2 Typical Application

The following sections describe in detail how to properly use this device. As this device has many applications and setups, there are many situations that this data sheet cannot characterize in detail and vary from these applications depending on the requirements of the final application.

9.2.1 Design: LM4060 Precision Power Supply and Voltage Reference

The LM4060 combination of high-precision with high current sink can be the power supply and voltage reference to a MCU. In Figure 9-1, the device is able to support the load current required by both the MCU VDD pin and REF pin. The main design consideration is the R_S resistor that needs to be sized to reduce current draw but supply the load under all conditions.

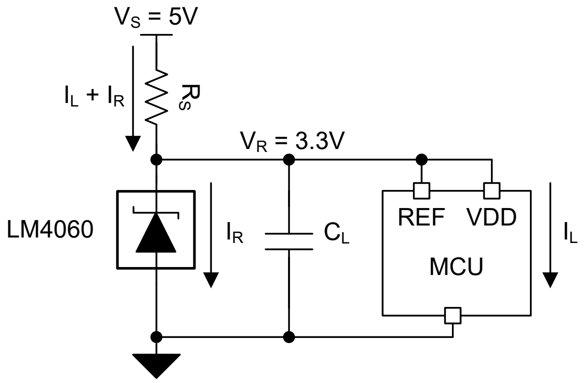


Figure 9-1. LM4060 Voltage Reference With MCU Load

9.2.1.1 Design Requirements

For this design the goal is to design R_S to minimize current consumption and function worst case conditions. Use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	4.8V to 5.2V
Input voltage typical	5V
Output voltage	3.3V
Minimum cathode current	60µA
Typical MCU VDD current	12mA

Table 9-1. Design Parameters (continued)

DESIGN PARAMETER	VALUE
Maximum MCU VDD current	20mA
Typical MCU REF current	130µA
Maximum MCU REF current	150µA

9.2.1.2 Detailed Design Procedure

R_S sets the cathode current of the shunt reference and is calculated using Equation 3. The resistor R_S must be selected such that current I_R remains in the operational region of the part for the entire V_S range and load current range I_L.

$$R_S = \frac{V_S - V_R}{I_L + I_R} \tag{3}$$

The two extremes to consider are V_S at the minimum, and the load at the maximum, where R_S must be small enough for I_R to remain above I_{RMIN}. For this design, design I_R with a small margin of current for a total of 0.1mA. This design makes the maximum R_S required to maintain operation at the worst case conditions to be 74Ω.

$$R_{SMAX} = \frac{V_{SMIN} - V_R}{I_{LMAX} + I_R} = \frac{4.8V - 3.3V}{20mA + 0.15mA + 0.1mA} = 74\Omega \tag{4}$$

The other extreme is V_S at the maximum, and the load at the minimum, where R_S must be large enough to maintain $I_R < I_{RMAX}$. For this design, the assumption is that the load is off. The calculated I_{RMAX} is 25.6mA, which is less than the maximum the device can support.

$$I_{RMAX} = \frac{V_{SMAX} - V_R}{R_S} - I_{LMIN} = \frac{5.2V - 3.3V}{74\Omega} = 25.6mA \tag{5}$$

The same equation above is used to find out the typical current the device sinks.

$$I_R = \frac{V_S - V_R}{R_S} - I_L = \frac{5V - 3.3V}{74\Omega} - 12mA - 0.13mA = 10.8mA \tag{6}$$

9.2.1.3 Application Curves

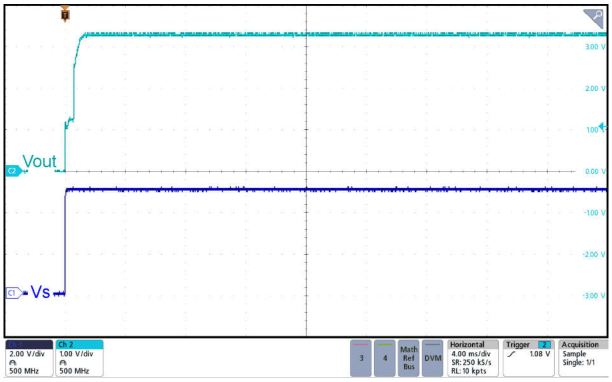


Figure 9-2. LM4060 Start-Up With C_L = Open, I_R = 0mA, Variant: LM4060A33EDBZR

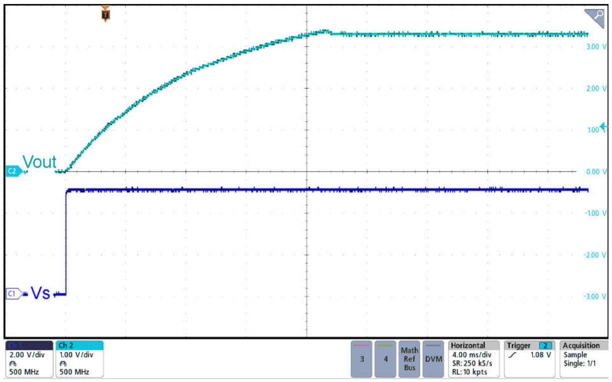


Figure 9-3. LM4060 Start-Up With C_L = 1µF, I_R = 0mA, Variant: LM4060A33EDBZR

9.3 Power Supply Recommendations

Noise on the power supply input to R_S can affect output noise performance. Noise performance can be reduced by using an optional bypass capacitor at the input side of R_S and Ground. TI recommends a 0.1µF ceramic capacitor or higher.

9.3.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

Use Equation 7 to calculate the maximum continuous allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \tag{7}$$

Equation 8 calculates the actual power being dissipated in the device:

$$P_D = V_R \times I_R \tag{8}$$

Equation 7 and Equation 8 establish the relationship between the maximum power dissipation allowed due to thermal consideration and the continuous current capability of the device. Use these two equations to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be increased.

In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part and package in the application ($R_{\theta JA}$), as given by Equation 9:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \tag{9}$$

9.4 Layout

9.4.1 Layout Guidelines

Place R_S as close to the cathode as possible. Place capacitor C_L as close to the cathode as possible.

9.4.2 Layout Example

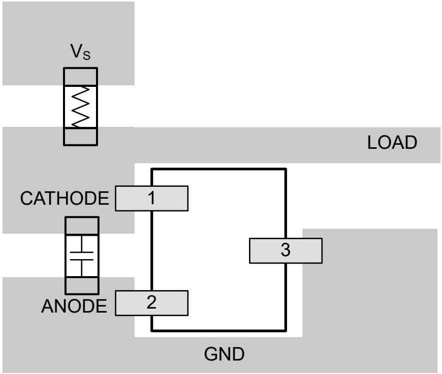


Figure 9-4. Layout Recommendation

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

Texas Instruments, *Voltage Reference Selection Basics* white paper

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from Revision * (November 2025) to Revision A (July 2026)	**Page**
• Updated document status to production data	1
• Changed temperature coefficient from 20ppm/C to 18ppm/C throughout the document	1
• Changed long-term stability time-frame from 500 hours to 1000 hours	1
• Added Shunt Voltage Reference Summary Table	3
• Changed maximum Output voltage temperature coefficient from 20ppm/°C to 18ppm/°C	6
• Added Reverse breakdown voltage long term stability for 1000 hours and 2000 hours	6
• Updated Temperature Drift typical graph	7
• Added Long-Term Stability typical graphs for 1000 hours and 2000 hours	7
• Changed temperature coefficient from 20ppm/C to 18ppm/C	12

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4060A12EDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P25C
LM4060A20EDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2P0XC
LM4060A25EDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2P5XC
LM4060A30EDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3P0XC
LM4060A33EDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3P3XC
LM4060A50EDBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5P0XC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM4060 :

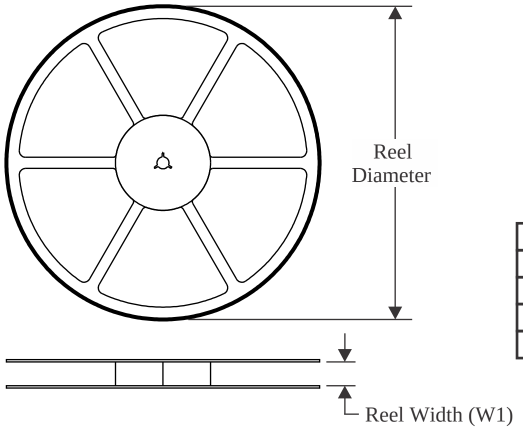
- Automotive : LM4060-Q1

NOTE: Qualified Version Definitions:

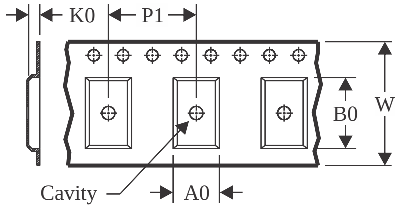
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

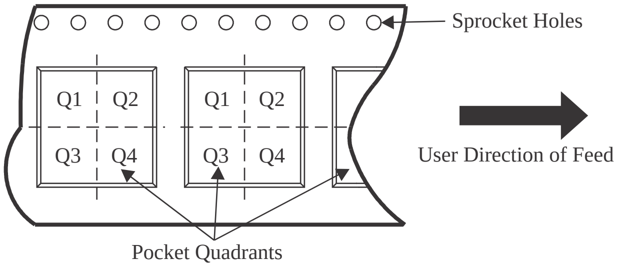


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

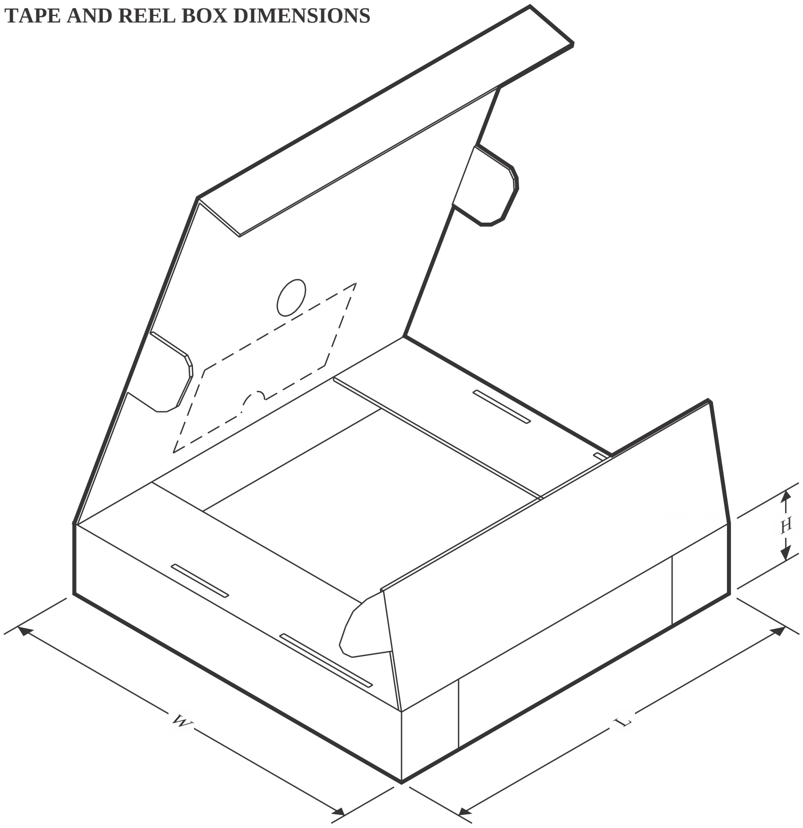
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4060A12EDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A20EDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A25EDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A30EDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A33EDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
LM4060A50EDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

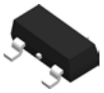
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4060A12EDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A20EDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A25EDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A30EDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A33EDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4060A50EDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

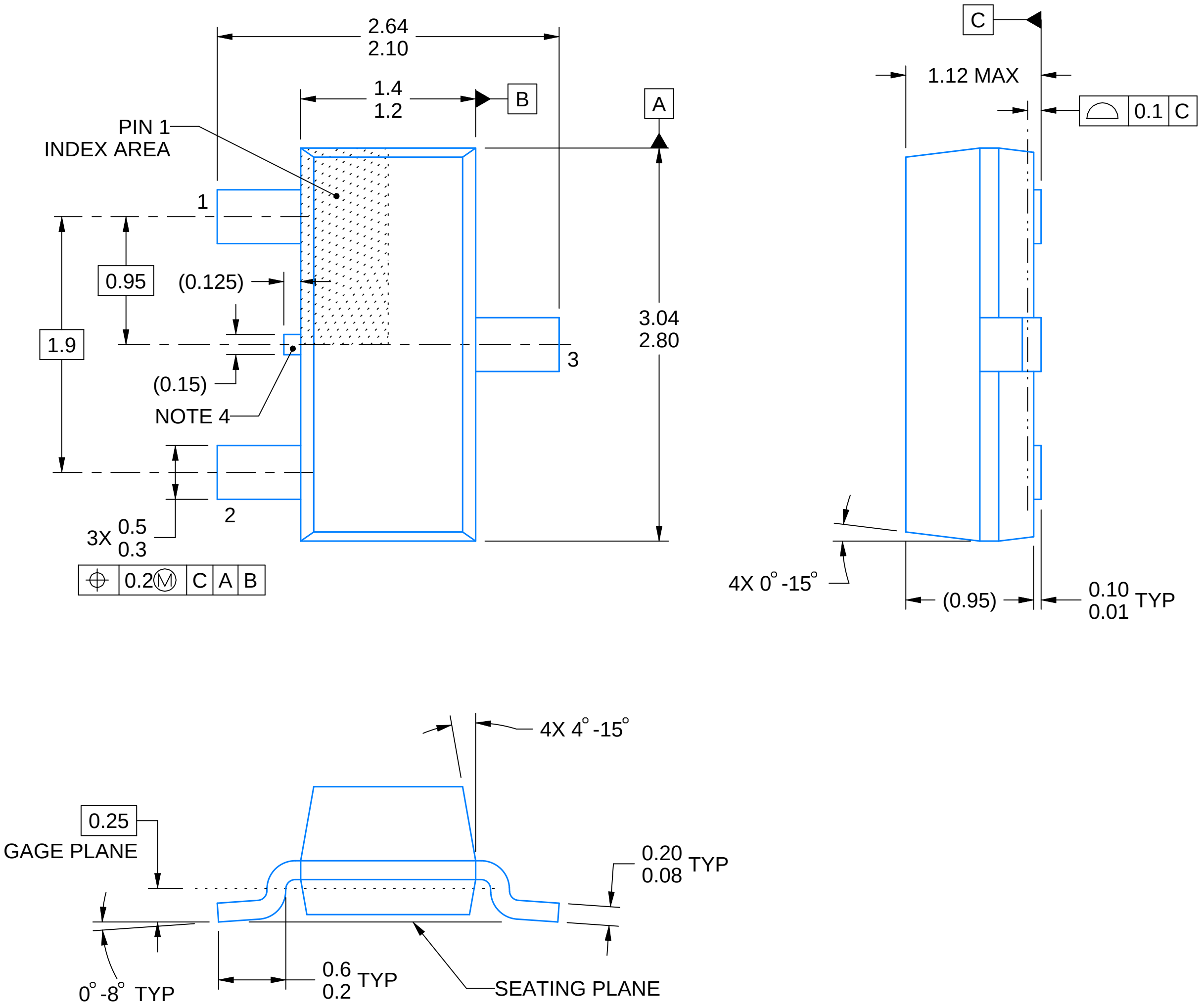
PACKAGE OUTLINE



DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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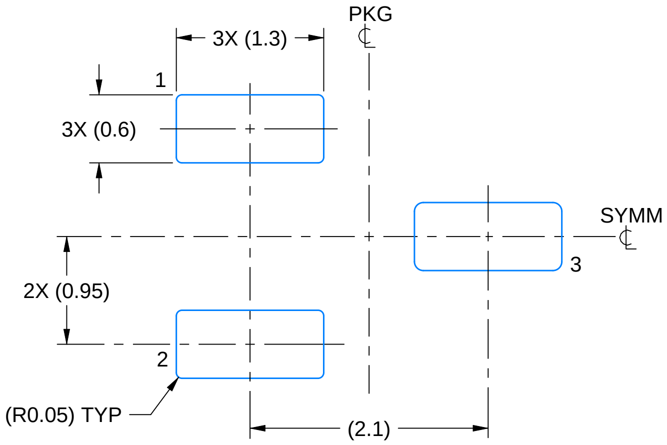
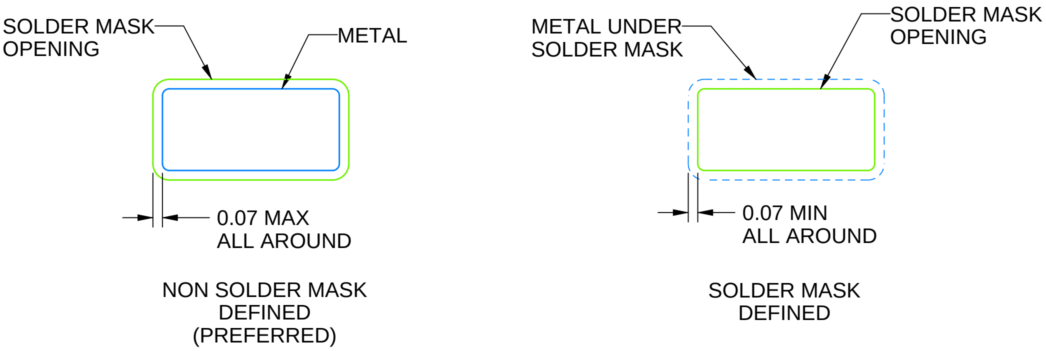
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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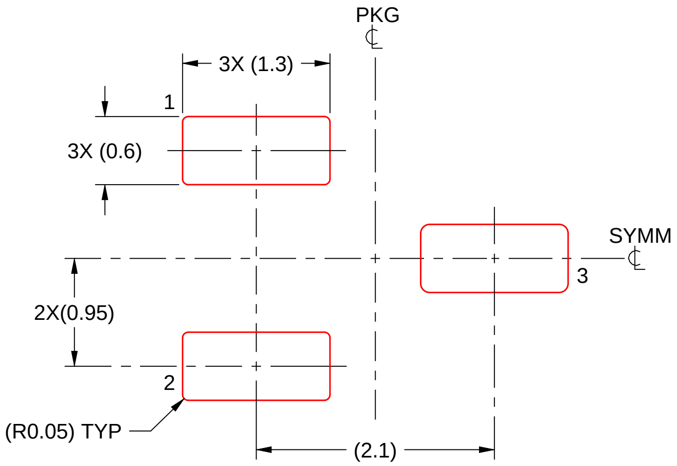
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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