LM48580 Boomer™ オーディオ パワー アンプ シリーズの高効率 Class-H、高電圧、ハプティクス ピエゾ アクチュエータ / セラミック スピーカ ドライバ

1 特長

- Class-H ドライバ
- 統合ブースト コンバータ
- ブリッジ接続負荷出力
- 差動入力
- 3 ピン プログラマブル ゲイン
- 低い電源電流
- 外付け部品が最小限
- マイクロパワー シャットダウン機能
- 過熱保護機能
- 省スペースの 12 バンプ DSBGA パッケージで供給

2 アプリケーション

- スマートフォンのタッチ画面
- タブレット PC
- 携帯電子機器
- MP3 プレーヤー
- 主な仕様:
  - 出力電圧 V_{DD} = 3.6V、
    R_L = 6μF + 10Ω、THD+N ≤ 1%
    •
  - $30V_{P-P}$ (標準値)
  - 3.6V での静止時消費電流
    - 2.7mA (標準値)
  - 25V $_{P-P}$ での消費電力
    - 800mW (標準値)
  - シャットダウン電流
    - 0.1μA (標準値)

3 概要

LM48580 は、携帯マルチメディア デバイスに使用されるピエゾ アクチュエータおよびセラミック スピーカー用の、完全差動の高電圧ドライバです。TI の Powerwise™ 製品ラインの一部である LM48580 Class-H アーキテクチャは、従来の Class-AB アンプと比較して消費電力を大幅に削減します。このデバイスは $30V_{P-P}$ の出力ドライブ能力があり、静止時消費電力はわずか 15mW です。

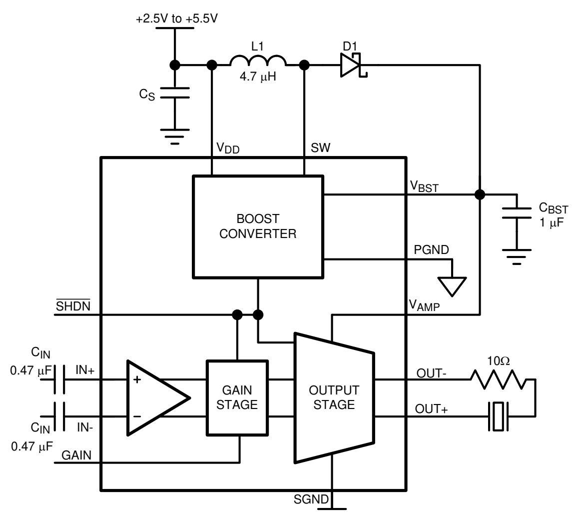
LM48580 は単一電源ドライバで、昇圧コンバータが内蔵されており、単一 3.6V 電源から 30V $_{P-P}$ を供給できます。

LM48580 には、ピンでプログラム可能な 3 つのゲイン設定と、低消費電力のシャットダウン モードがあり、静止電流を 0.1μA に減らすことができます。LM48580 は、超小型の 12 バンプ DSBGA パッケージで供給されます。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
LM48580	DSBGA	1.96 mm × 1.46mm

(1) 供給されているすべてのパッケージについては、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます



代表的なアプリケーション

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4 Pin Configuration and Functions

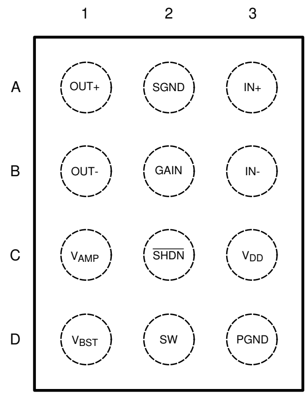


図 4-1. DSBGA Package YZR 12-Pin Top View

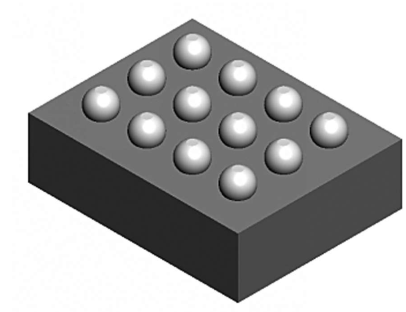


図 4-2. YZR0012 Package (Bumps Up) View

表 4-1. Pin Functions

Bump	Name	Description
A1	OUT+	Amplifier Non-Inverting Output
A2	SGND	Amplifier Ground
A3	IN+	Amplifier Non-Inverting Input
B1	OUT-	Amplifier Inverting Output
B2	GAIN	Gain Select: GAIN = float: A_V = 18dB GAIN = GND: A_V = 24dB GAIN = V_{DD}: A_V = 30dB
B3	IN-	Amplifier Inverting Input
C1	V_{AMP}	Amplifier Supply Voltage. Connect to V_{BST}
C2	$\overline{SHDN}$	Active Low Shutdown. Drive $\overline{SHDN}$ low to disable device. Connect $\overline{SHDN}$ to V_{DD} for normal operation.
C3	V_{DD}	Power Supply
D1	V_{BST}	Boost Converter Output
D2	SW	Boost Converter Switching Node
D3	PGND	Boost Converter Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

	MIN	MAX	UNIT
Supply Voltage		6	V
SW Voltage		25	V
VBST Voltage		21	V
V_{AMP}		17	V
Input Voltage	−0.3	V_{DD} + 0.3	V
Storage temperature, T_{stg}	−65	150	°C
Junction Temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature Range	−40	T_A	85	°C
Supply Voltage	2.5	V_{DD}	5.5	V

5.4 Thermal Information

THERMAL METRIC[(1)]		LM48580 YZR (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

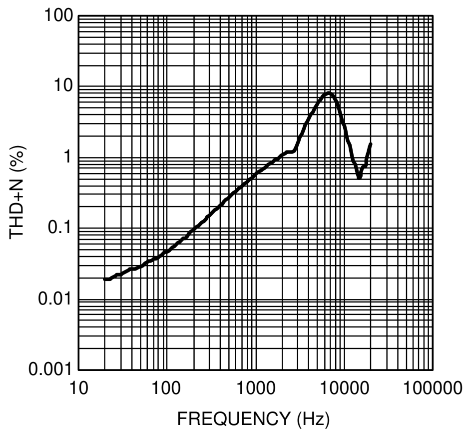
5.5 Electrical Characteristics: V_{DD} = 3.6 V (1)

The following specifications apply for R_L = 6 µF + 10Ω, C_{BST} = 1 µF, C_{IN} = 0.47 µF, A_V = 24 dB unless otherwise specified. Limits apply for T_A = 25°C.

PARAMETER		TEST CONDITIONS	Min (3)	Typ (2)	Max (3)	Unit
V_{DD}	Supply Voltage Range		2.5		5.5	V
I_{DD}	Quiescent Power Supply Current, V_{IN} = 0V, R_L = ∞	V_{DD} = 3.6V		2.7	4	mA
		V_{DD} = 3V		3		mA
P_D	Power Consumption V_{OUT} = 25_{P-P}, f = 200 Hz	V_{DD} = 3.6V		800		mW
		V_{DD} = 3V		830		mW
I_{SD}	Shutdown Current	Shutdown Enabled		0.5	2	µA
T_{WU}	Wake-up Time	From Shutdown	1	1.4	1.6	ms
V_{OS}	Differential Output Offset Voltage	V_{DD} = 3.6 V		63	360	mV
A_V	Gain	GAIN = FLOAT	17.5	18	18.5	dB
		GAIN = GND	23.5	24	24.5	dB
		GAIN = V_{DD}	29.5	30	30.5	dB
R_{IN}	Input Resistance		46	52	58	kΩ
R_{IN}	Gain Input Resistance	to GND			575	kΩ
		to V_{DD}			131	kΩ
V_{IN}	Maximum Input Voltage Range	A_V = 18dB			3	V_{P-P}
V_{OUT}	Output Voltage f = 200 Hz, THD+N = 1%	V_{DD} = 3.6 V	25	30.5		V_{P-P}
		V_{DD} = 3 V		30.5		V_{P-P}
	Output Voltage f = 2 kHz, THD+N = 5%	V_{DD} = 3.6 V		11		V_{P-P}
		V_{DD} = 3 V		8.5		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = $25V_{P-P}$, f = 200Hz		0.16%		
PSRR	Power Supply Rejection Ratio V_{DD} = 3.6 V + 200 mV_{p-p} sine, Inputs AC GND	f_{RIPPLE} = 217 Hz,		75		dB
		f_{RIPPLE} = 1 kHz		71		dB
CMRR	Common Mode Rejection Ratio V_{CM} = $200mV_{P-P}$ sine	f_{RIPPLE} = 217 Hz		56		dB
		f_{RIPPLE} = 1 kHz		55		dB
f_{SW}	Boost Converter Switching Frequency			2.1		MHz
I_{LIMIT}	Boost Converter Current Limit				1100	mA
V_{IH}	Logic High Input Threshold	$\overline{SHDN}$	1.2			V
V_{IL}	Logic Low Input Threshold	$\overline{SHDN}$			0.45	V
I_{IN}	Input Leakage Current	$\overline{SHDN}$		0.1	1	µA

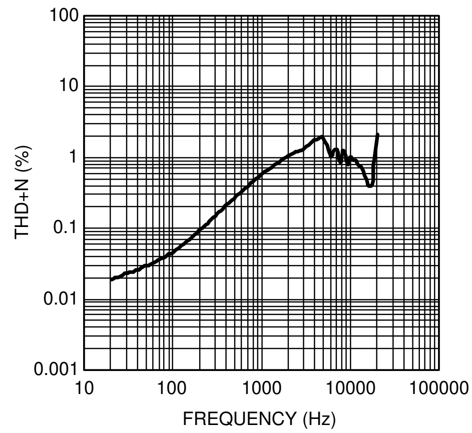
(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.
(3) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

5.6 Typical Performance Characteristics



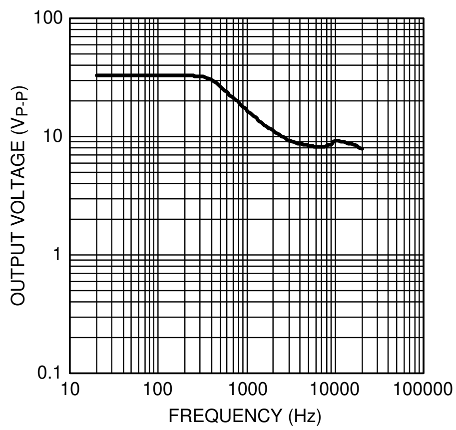
V_{DD} = 3.6 V V_{OUT} = 9 V_{P-P} R_L = 6 µF + 10 Ω

図 5-1. THD+N vs Frequency



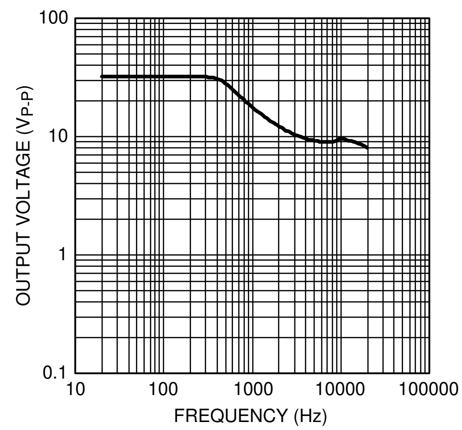
V_{DD} = 4.2 V V_{OUT} = 10 V_{P-P} R_L = 6 µF + 10 Ω

図 5-2. THD+N vs Frequency



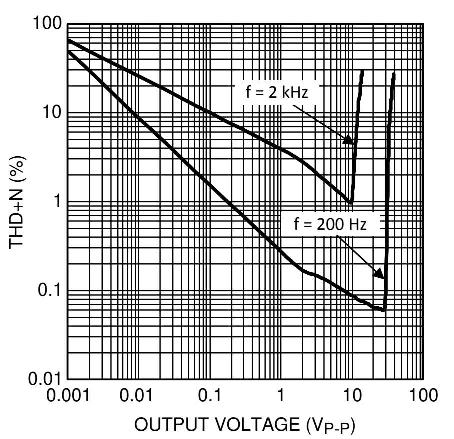
V_{DD} = 3.6 V   THD+N = 5% R_L = 6 µF + 10 Ω

図 5-3. Output Voltage vs Frequency



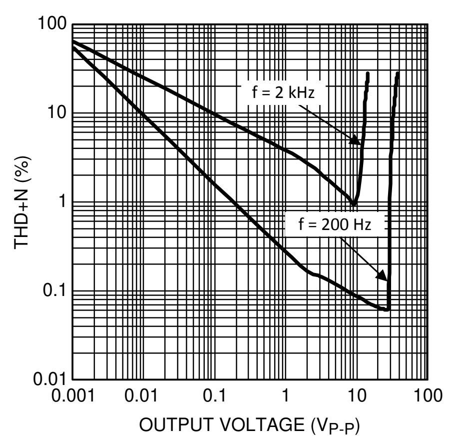
V_{DD} = 4.2 V   THD+N = 5% R_L = 6 µF + 10 Ω

図 5-4. Output Voltage vs Frequency



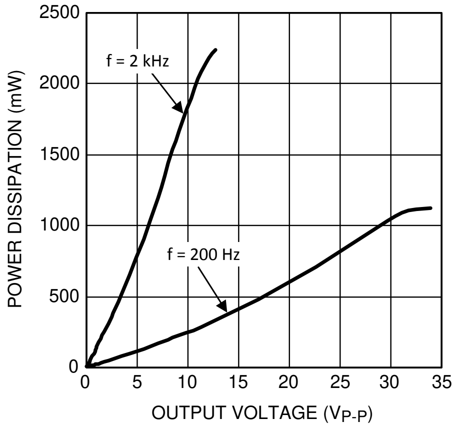
V_{DD} = 3.6 V R_L = 6 µF + 10 Ω

図 5-5. THD+N vs Output Voltage



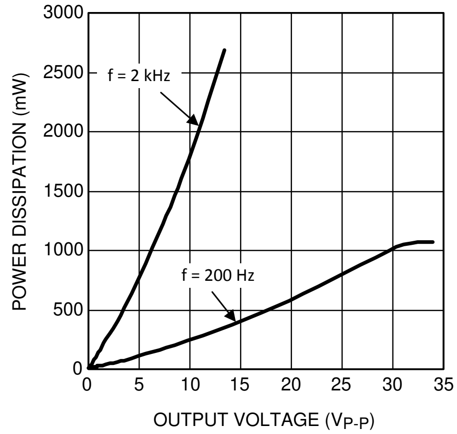
V_{DD} = 4.2 V R_L = 6 µF + 10 Ω

図 5-6. THD+N vs Output Voltage



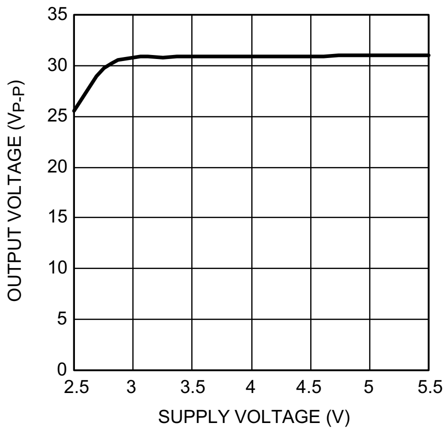
V_{DD} = 3.6 V R_L = 6 µF + 10 Ω

図 5-7. Power Consumption vs Output Voltage



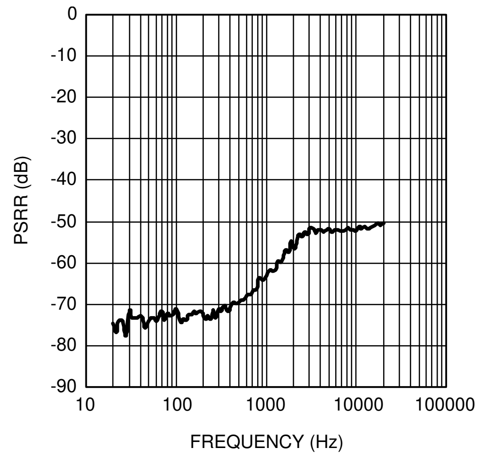
V_{DD} = 4.2 V R_L = 6 µF + 10 Ω

図 5-8. Power Consumption vs Output Voltage



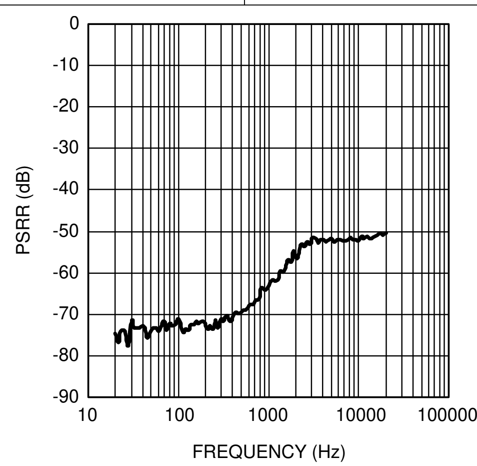
R_L = 6 µF + 10 Ω, f = 200 Hz

図 5-9. Output Voltage vs Supply Voltage



A. V_{DD} = 3.6 V f = 200 Hz R_L = 6 µF + 10 Ω, V_{RIPPLE} = 200 mV_{P-P}

図 5-10. PSRR vs Frequency



V_{DD} = 3.6 V V_{CM} = 1 V_{P-P} R_L = 6 µF + 10 Ω

図 5-11. CMRR vs Frequency

Parameter Measurement Information

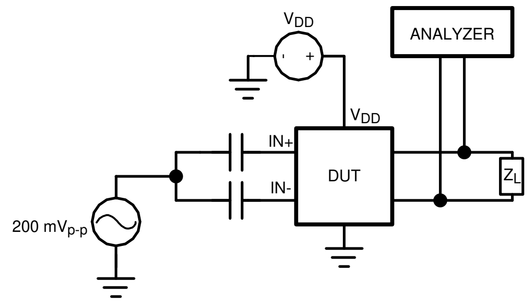


図 6-1. PSRR Test Circuit

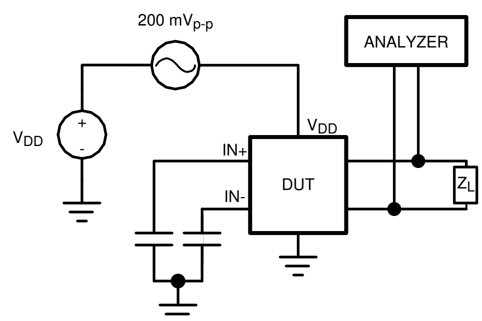


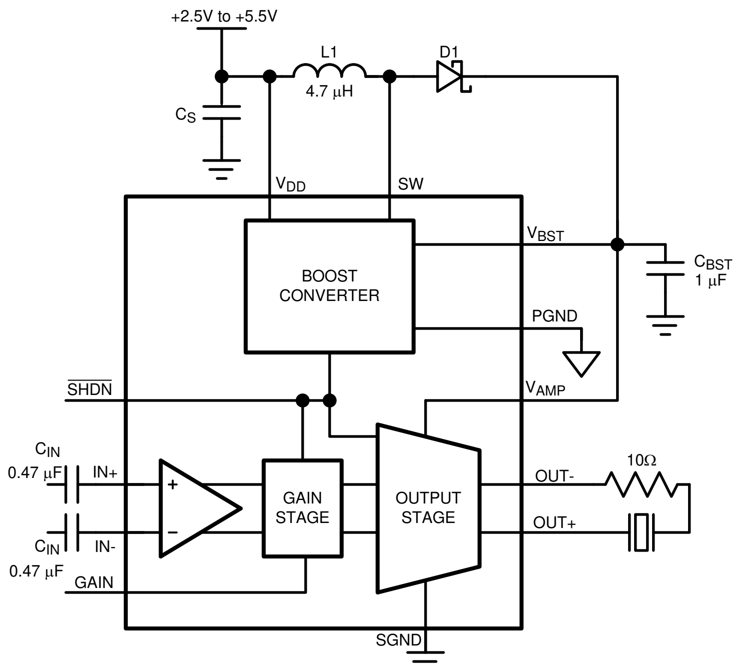
図 6-2. CMRR Test Circuit

6 Detailed Description

6.1 Overview

The LM48580 is a fully differential, Class H ceramic element driver for ceramic speakers and haptic actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier's supply voltage based on the output signal, increasing headroom and improving efficiency compared to a conventional Class AB driver. The fully differential amplifier takes advantage of the increased headroom and bridge-tied load (BTL) architecture, delivering significantly more voltage than a single-ended amplifier.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Class H Operation

Class H is a modification of another amplifier class (typically Class B or Class AB) to increase efficiency and reduce power dissipation. To decrease power dissipation, Class H uses a tracking power supply that monitors the output signal and adjusts the supply accordingly. When the amplifier output is below 3 V_{P-P}, the nominal boost voltage is 6 V. As the amplifier output increases above 3 V_{P-P}, the boost voltage tracks the amplifier output as shown in 図 6-1. When the amplifier output falls below 3 V_{P-P}, the boost converter returns to its nominal output voltage. Power dissipation is greatly reduced compared to conventional Class AB drivers.

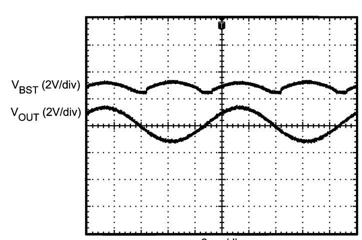


図 6-1. Class H Operation

6.3.2 Properties of Piezoelectric Elements

Piezoelectric elements such as ceramic speakers or piezoelectric haptic actuators are capacitive in nature. Due to their capacitive nature, piezoelectric elements appear as low impedance loads at high frequencies (typically above 5 kHz). A resistor in series with the piezoelectric element is required to ensure the amplifier does not see a short at high frequencies.

The value of the series resistor depends on the capacitance of the element, the frequency content of the output signal, and the desired frequency response. Higher valued resistors minimize power dissipation at high frequencies, but also impacts the frequency response. This configuration is suited for use with haptic actuators, where the majority of the signal content is typically below 2 kHz. Conversely, lower valued resistors maximize frequency response, while increasing power dissipation at high frequency. This configuration is ideal for ceramic speaker applications, where high frequency audio content needs to be reproduced. Resistor values are typically between 10 Ω and 20 Ω.

6.3.3 Differential Amplifier Explanation

The LM48580 features a fully differential amplifier. A differential amplifier amplifies the difference between the two input signals. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

6.3.4 Thermal Shutdown

The LM48580 features thermal shutdown that protects the device during thermal overload conditions. When the junction temperature exceeds +160°C, the device is disabled. The LM48580 remains disabled until the die temperature falls below the +160°C and $\overline{\text{SHDN}}$ is toggled.

6.3.5 Gain Setting

The LM48580 features three internally configured gain settings 18, 24, and 30 dB. The device gain is selected through a single pin (GAIN). The gain settings are shown in 表 6-1.

表 6-1. Gain Setting

Gain	Gain Setting
FLOAT	18 dB
GND	24 dB
VDD	30 dB

6.4 Device Functional Modes

6.4.1 Shutdown Function

The LM48580 features a low current shutdown mode. Set $\overline{\text{SD}}$ = GND to disable the amplifier and boost converter and reduce supply current to 0.01μA.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.2 Typical Application

The LM48580 is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. 図 7-1 shows the typical single-ended applications circuit.

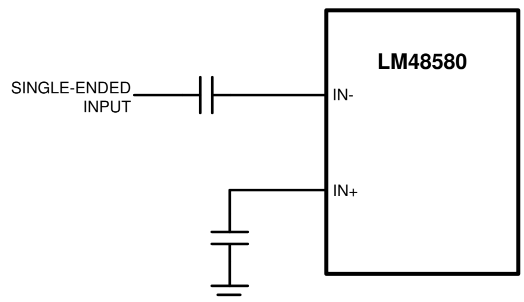


図 7-1. Single-Ended Configuration

7.2.1 Design Requirements

7.2.1.1 Proper Selection of External Components

7.2.1.1.1 Boost Converter Capacitor Selection

The LM48580 boost converter requires three external capacitors for proper operation: a 1 µF supply bypass capacitor, and 1 µF + 100 pF output reservoir capacitors. Place the supply bypass capacitor as close to V_{DD} as possible. Place the reservoir capacitors as close to VBST and VAMP as possible. Low ESR surface-mount multi-layer ceramic capacitors with X7R or X5R temperature characteristics are recommended. Select output capacitors with voltage rating of 25 V or higher. Tantalum, OS-CON and aluminum electrolytic capacitors are not recommended. See 表 7-1 for suggested capacitor manufacturers.

7.2.2 Detailed Design Procedure

7.2.2.1 Boost Converter Output Capacitor Selection

7.2.2.1.1 Inductor Selection

The LM48580 boost converter is designed for use with a 4.7 µH inductor. 表 7-1 lists various inductors and their manufacturers. Choose an inductor with a saturation current rating greater than the maximum operating peak current of the LM48580 (> 1 A). This ensures that the inductor does not saturate, preventing excess efficiency loss, over heating and possible damage to the inductor. Additionally, choose an inductor with the lowest possible DCR (series resistance) to further minimize efficiency losses.

表 7-1. Recommended Inductors (1)

MANUFACTURER	PART#	INDUCTANCE/ISAT
Taiyo Yuden	BRL3225T4R7M	4.7 µH/1.1 A
Coilcraft	LP3015	4.7 µH/1.1 A

(1) See *セクション 8.1.1*

7.2.2.1.2 Diode Selection

Use a Schottkey diode as shown in the *Functional Block Diagram*. A 20 V diode such as the NSR0520V2T1G from On Semiconductor is recommended. The NSR0520V2T1G is designed to handle a maximum average current of 500 mA.

7.2.2.2 Application Curves

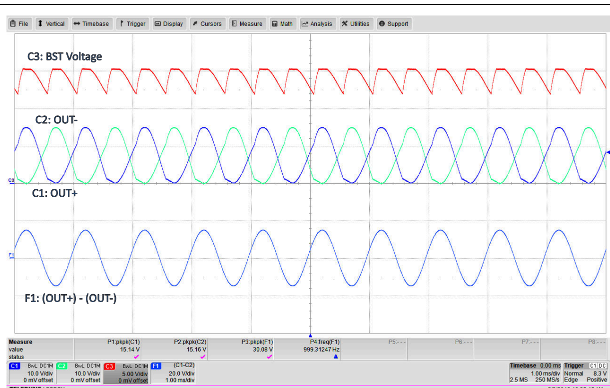


図 7-2. Full Scale Output 30 V_{PP} at 1 kHz

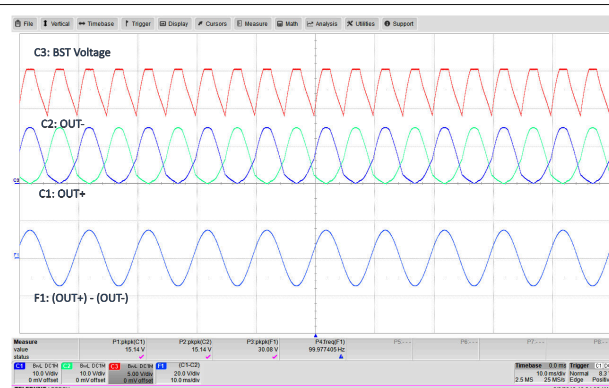


図 7-3. Full Scale Output 30 V_{PP} at 100 Hz

7.3 Power Supply Recommendations

The LM48580 device is designed be operate with a power supply between 2.5 V and 5.5 V. Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1-µF ceramic capacitor from VDD to GND. Additional bulk capacitance may be added as required

7.4 Layout

7.4.1 Layout Guidelines

- Minimize trace impedance of the power, ground and all output traces for optimum performance.
- Voltage loss due to trace resistance between the LM48580 and the load results in decreased output power and efficiency.
- Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power.
- Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device.

- Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal.
- Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

7.4.2 Layout Example

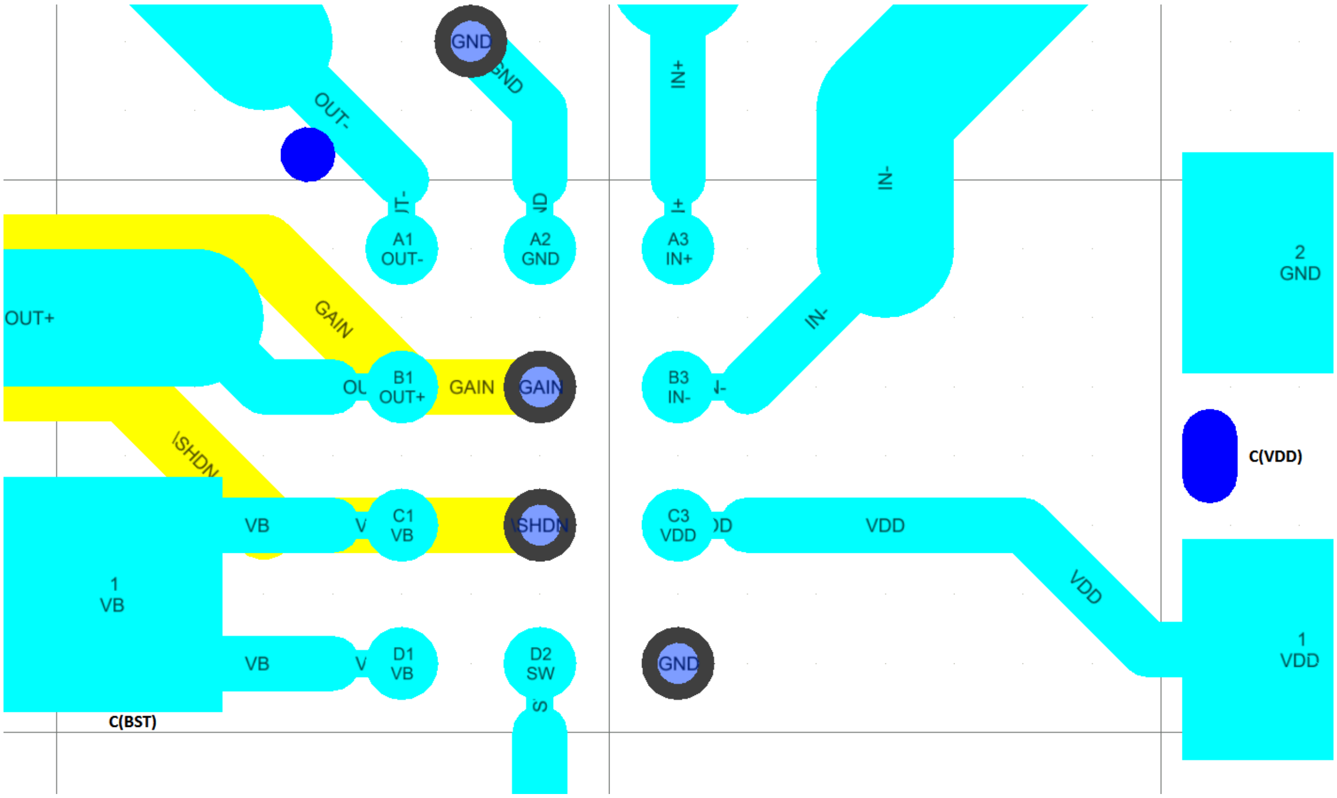


図 7-4. Example Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Community Resources

8.4 Trademarks

Boomer™ is a trademark of Texas Instruments.
Powerwise™ is a trademark of Texas Instruments.
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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (February 2018) to Revision C (January 2025)	Page
• 「製品情報」表を更新	1

Changes from Revision A (May 2013) to Revision B (February 2018)	Page
• 「製品情報」表、「ESD」表、「熱に関する情報」表、「パラメータ測定情報」、「詳細説明」、「デバイス機能モード」、「電源に関する推奨事項」、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」、および「メカニカル、パッケージ、および注文情報」を追加	1
• Deleted the *Demoboard Bill of Materials* section	12
• Deleted the *Demo Board Schematic* section	12

Changes from Revision * (February 2010) to Revision A (May 2013)	Page
• ナショナル セミコンダクターのデータシートのレイアウトを テキサス・インスツルメンツのフォーマットへ変更。	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM48580TL/NOPB	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GM3
LM48580TL/NOPB.A	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GM3
LM48580TLX/NOPB	Active	Production	DSBGA (YZR) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GM3
LM48580TLX/NOPB.A	Active	Production	DSBGA (YZR) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GM3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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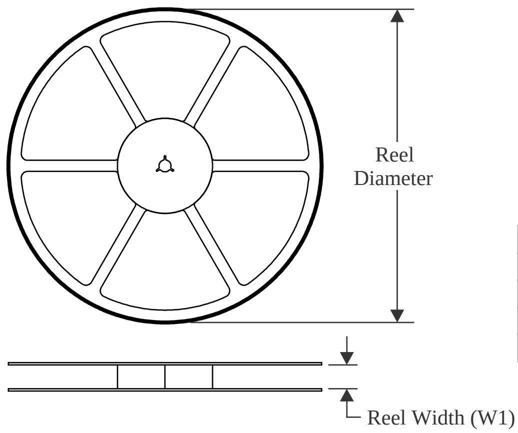
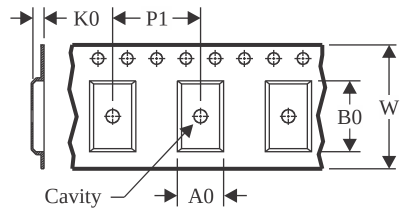
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

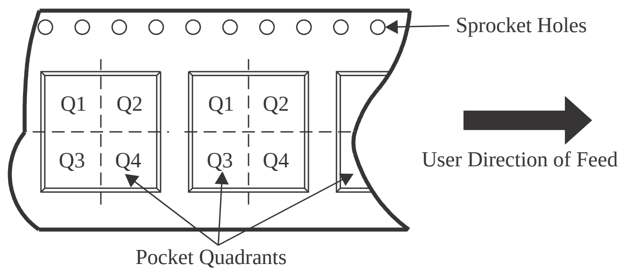


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

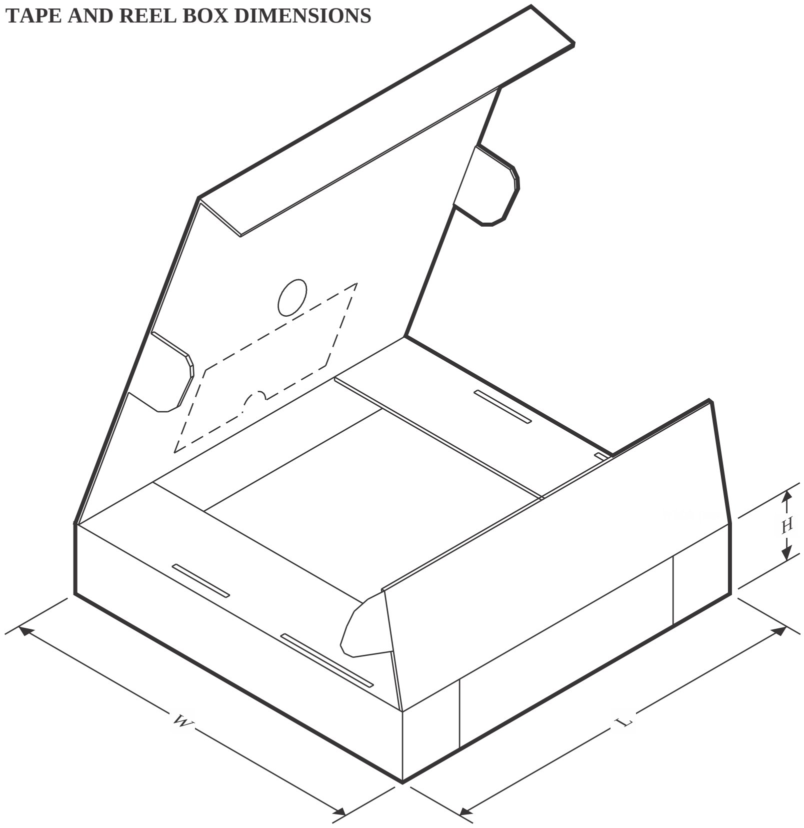
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

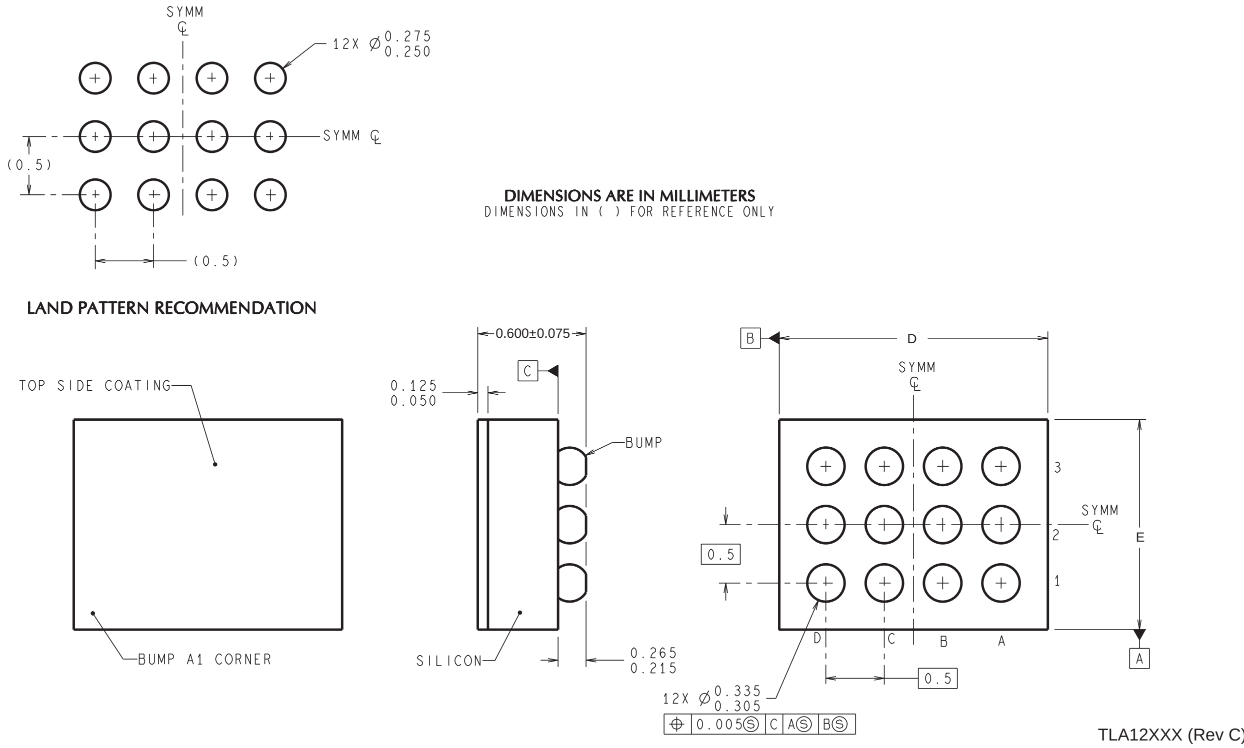
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48580TL/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
LM48580TLX/NOPB	DSBGA	YZR	12	3000	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48580TL/NOPB	DSBGA	YZR	12	250	208.0	191.0	35.0
LM48580TLX/NOPB	DSBGA	YZR	12	3000	208.0	191.0	35.0



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.49 mm, Min = 1.43 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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