

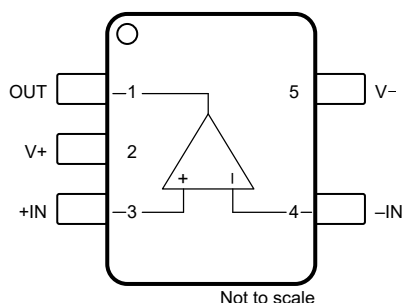
LMC7111 レール ツー レール入出力対応超小型 CMOS オペアンプ

1 特長

- 超小型 5 ピン SOT-23 パッケージにより基板面積を削減
- 非常に広い同相入力範囲
- 2.7V、5V、10V の仕様を規定
- 電源電流 (標準値): 5V で 25 μ A
- ゲイン帯域幅積: 5V で 50kHz
- 一般的な LMC6462 と類似
- 出力は、100k Ω 負荷時に電源レールから 20mV 以内
- 良好な容量性負荷駆動能力

2 アプリケーション

- モバイル通信
- ポータブル コンピュータ
- バッテリー チャージャ向け電流検出
- 電圧リファレンスバッファ
- センサ インターフェイス
- GaAs RF アンプの安定的なバイアス



DBV パッケージ、5 ピン SOT-23 (上面図)

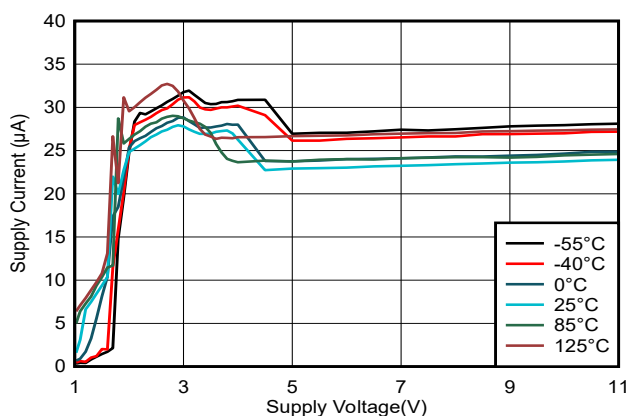
3 概要

LMC7111 は、省スペースの SOT-23 パッケージで提供される Micropower CMOS オペアンプです。このパッケージにより、LMC7111 はスペースと重量の制約が厳しい設計にも最適です。同相入力範囲が広いこと、V+ 電源より大きな信号を検出するバッテリー監視回路を設計できます。この超小型パッケージの主な利点は、携帯電話、ポケベル、ポータブルコンピュータなどの小型で携帯用電子機器において特に顕著に現れます。超小型アンプは必要に応じて基板に配置でき、基板レイアウトを簡素化できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
LM7111	DBV (SOT-23, 5)	2.9mm × 2.8mm

- 詳細については、[セクション 10](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



電源電流と電源電圧との関係



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4 Pin Configuration and Functions

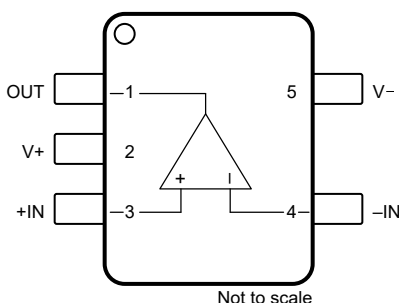


図 4-1. DBV Package, 5-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT	Output	Output
2	V+	Power	Positive supply
3	+IN	Input	Noninverting input
4	-IN	Input	Inverting input
5	V-	Power	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
	Differential input voltage		±Supply voltage	V
V _S	Supply voltage, V _S = (V+) – (V–)		11	V
	Voltage at input/output pin	(V–) – 0.3	(V+) + 0.3	V
	Current at input pin		±5	mA
I _{SC}	Output short circuit ⁽²⁾		±30	mA
	Supply pin current		30	mA
	Lead temperature (soldering, 10s)		260	°C
T _{stg}	Storage temperature	–65	150	°C
T _J	Junction temperature ⁽³⁾		150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
- (3) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A) / R_{θJA}. All numbers apply for packages soldered directly into a printed circuit board (PCB).

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	2.5		11	V
T _J	Junction temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMC7111	UNIT
		DBV (SOT-23)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	325	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics for $V_S = 2.7V$ or $\pm 1.35V$

at $T_A = +25^\circ C$, $V_+ = 2.7V$, $V_- = 0V$, $V_{CM} = V_O = V_+ / 2$, and $R_L > 1M\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage			±0.9		±7	mV
		T _J = −40°C to +85°C				±9	
dV _{OS} /dT	Input offset voltage drift			±10			μV/°C
PSRR	Power-supply rejection ratio	Positive 2.7V < V+ < 5V, V− = 0V		55	60	dB	
			T _J = −40°C to +85°C	50			
		Negative 2.7V < V+ < 5V, V+ = 0V		55	60		
			T _J = −40°C to +85°C	50			
INPUT BIAS CURRENT							
I _B	Input bias current ⁽¹⁾			±0.1		±1	pA
		T _J = −40°C to +85°C				±20	
I _{OS}	Input offset current ⁽¹⁾			±0.01		±0.5	pA
		T _J = −40°C to +85°C				±10	
INPUT VOLTAGE							
V _{CM}	Input common-mode voltage	To positive rail CMRR ≥ 47dB		2.7	2.8	V	
			T _J = −40°C to +85°C	2.25			
		To negative rail CMRR ≥ 41dB		−0.10			0.0
			T _J = −40°C to +85°C				0.40
		To positive rail CMRR ≥ 47dB, V+ = 3V		3.0	3.2		
			T _J = −40°C to +85°C	2.8			
		To negative rail, CMRR > 47dB, V+ = 3V		−0.25			0.0
		To positive rail CMRR ≥ 47dB, V+ = 3.3V		3.4	3.5		
			T _J = −40°C to +85°C	3.2			
		To negative rail CMRR ≥ 47dB, V+ = 3.3V		−0.25			−0.10
T _J = −40°C to +85°C			0.0				
INPUT IMPEDANCE							
R _{IN}	Input resistance			> 10			TΩ
C _{IN}	Input capacitance	Common mode		3			pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	Sourcing		400		V/mV	
		Sinking		150			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product			40			kHz
SR	Slew rate			0.015			V/μs
OUTPUT							
V _O	Voltage output swing	Positive rail R _L = 100kΩ		2.68	2.69	V	
			T _J = −40°C to +85°C	2.40			
		Negative rail R _L = 100kΩ		0.10			0.20
			T _J = −40°C to +85°C				0.08
		Positive rail R _L = 10kΩ		2.60	2.65		
			T _J = −40°C to +85°C	2.40			
Negative rail R _L = 10kΩ		0.03		0.10			
	T _J = −40°C to +85°C			0.3			
I _{SC}	Short-circuit current	Sourcing (V _O = 0V) and sinking (V _O = 2.7V)		1	7	mA	
		T _J = −40°C to +85°C		0.7			
POWER SUPPLY							
I _Q	Quiescent current per amplifier			20		50	μA
		T _J = −40°C to +85°C				65	

(1) Input bias current specified by design and processing.

5.6 Electrical Characteristics for $V_S = 5V$ or $\pm 2.5V$

at $T_A = +25^\circ\text{C}$, $V_+ = 5V$, $V_- = 0V$, $V_{CM} = V_O = V_S / 2$, and $R_L > 1M\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage			±0.9			mV
dV _{OS} /dT	Input offset voltage drift	T _J = −40°C to +85°C		2			μV/°C
PSRR	Power-supply rejection ratio	Positive, 5V < V+ < 10V, V− = 0V		60	85		dB
		Negative, −5V < V− < −10V, V+ = 0V		60	85		
INPUT BIAS CURRENT							
I _B	Input bias current ⁽¹⁾			±0.1		±1	pA
		T _J = −40°C to +85°C				±20	
I _{OS}	Input offset current ⁽¹⁾			±.01		±0.5	pA
		T _J = −40°C to +85°C				±10	
NOISE							
INPUT VOLTAGE							
V _{CM}	Common-mode voltage range	To positive rail CMRR ≥ 50dB		5.20	5.25		V
			T _J = −40°C to +85°C	5.0			
		To negative rail CMRR ≥ 50dB			−0.3	−0.2	
			T _J = −40°C to +85°C			0.0	
CMRR	Common-mode rejection ratio	0V < V _{CM} < 5V		60	85		dB
INPUT IMPEDANCE							
R _{IN}	Input resistance			>10			TΩ
C _{IN}	Common mode input capacitance			3			pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	Sourcing		500			V/mV
		Sinking		200			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product			50			kHz
SR	Slew rate	Voltage follower with 1V step input, R _L = 100kΩ to 1.5V, f = 1kHz, V _O = 1V _{PP}		0.010	0.027		V/μs
OUTPUT							
V _O	Voltage output swing	R _L = 100kΩ	Positive rail	4.98	4.99		V
			Negative rail		0.01	0.02	
		R _L = 10kΩ	Positive rail	4.9	4.98		
			Negative rail		0.02	0.1	
I _{SC}	Short-circuit current	Sourcing V _O = 0V		5	7		mA
			T _J = −40°C to +85°C	3.5			
		Sinking V _O = 3V		5	7		
			T _J = −40°C to +85°C	3.5			
POWER SUPPLY							
I _Q	Quiescent current per amplifier			25			μA

(1) Input bias current specified by design and processing.

5.7 Electrical Characteristics for $V_S = 10V$ or $\pm 5V$

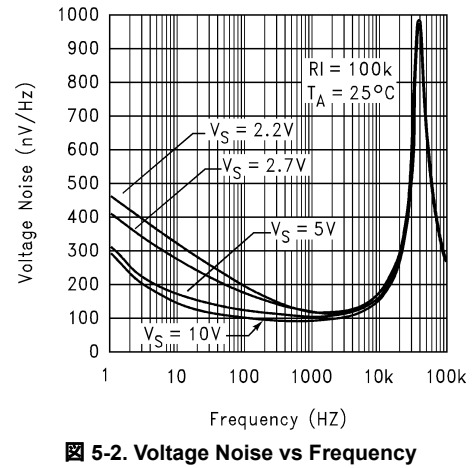
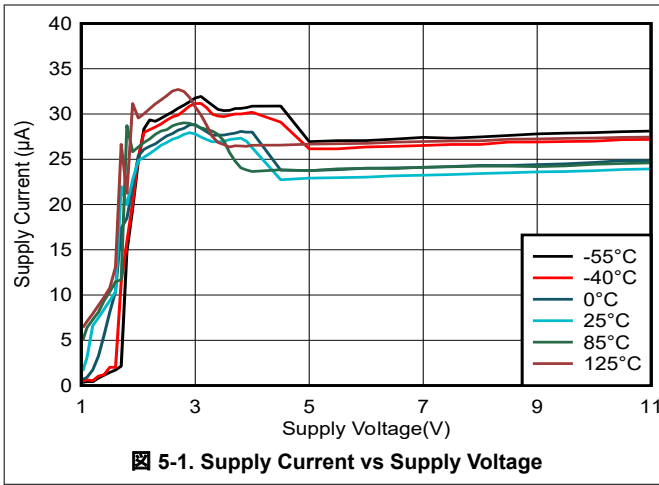
at $T_A = +25^\circ C$, $V_+ = 10V$, $V_- = 0V$, $V_{CM} = V_O = V_+ / 2$, and $R_L > 1M\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage			±0.9	±7	mV	
		T _J = −40°C to +85°C			±9		
dV _{OS} /dT	Input offset voltage drift	T _J = −40°C to +85°C		2		μV/°C	
PSRR	Power supply rejection ratio	Positive 5V < V _S < 10V, V _− = 0V, V _O = 2.5V		80		dB	
		Negative −5V < V _S < −10V, V ₊ = 0V, V _O = 2.5V		80			
INPUT BIAS CURRENT							
I _B	Input bias current ⁽¹⁾			±0.1	±1	pA	
		T _J = −40°C to +85°C			±20		
I _{OS}	Input offset current ⁽¹⁾			±0.01	±0.5	pA	
		T _J = −40°C to +85°C			±10		
NOISE							
e _n	Input voltage noise density	f = 1kHz, V _{CM} = 1V		110		nV/√Hz	
i _n	Input current noise density	f = 1kHz		0.03		pA/√Hz	
INPUT VOLTAGE							
V _{CM}	Common-mode voltage range	To positive rail CMRR ≥ 50dB		10.15	10.2	V	
			T _J = −40°C to +85°C		10.0		
		To negative rail CMRR ≥ 50dB		−0.2	−0.15		
			T _J = −40°C to +85°C				0.0
INPUT IMPEDANCE							
R _{IN}	Input resistance			>10		TΩ	
C _{IN}	Common mode input capacitance			3		pF	
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	R _L = 100kΩ	Sourcing	500		V/mV	
			Sinking	200			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product			50		kHz	
SR	Slew rate	Voltage follower with 1V step input, R _L = 100kΩ to 5V, f = 1kHz, V _O = 2V _{PP}		0.03		V/μs	
G _M	Gain margin			15		dB	
θ _m	Phase margin			50		°	
OUTPUT							
V _O	Voltage output swing	R _L = 100kΩ	Positive rail,	9.98	9.99	V	
			Negative rail		0.01		0.02
		R _L = 10kΩ	Positive rail	9.90	9.98		mA
			Negative rail		0.02		
I _{SC}	Short-circuit current	Sourcing V _O = 0V		25	20		
			T _J = −40°C to +85°C		7		
		Sinking V _O = 10V		30	20		
			T _J = −40°C to +85°C		7		
POWER SUPPLY							
I _Q	Quiescent current per amplifier			25	60	μA	
		T _J = −40°C to +85°C			75		

(1) Input bias current specified by design and processing.

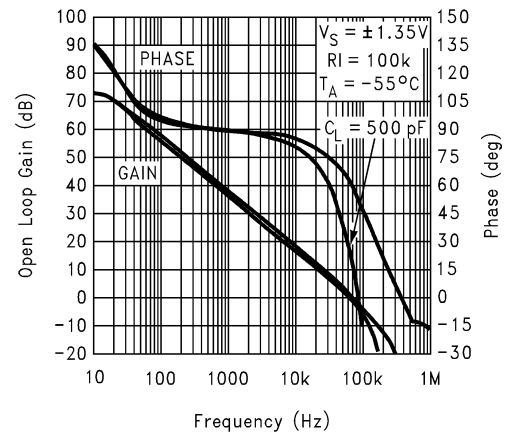
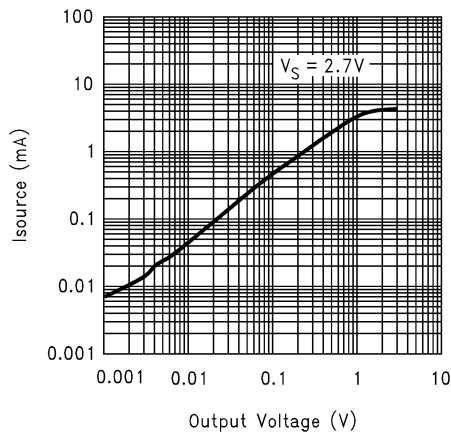
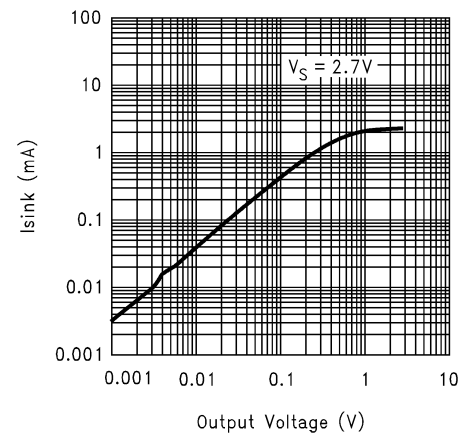
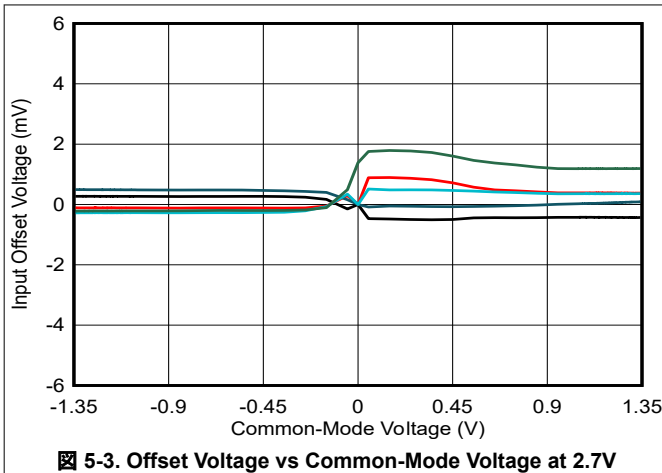
5.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)



5.9 Typical Characteristics: 2.7V

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)



5.9 Typical Characteristics: 2.7V (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)

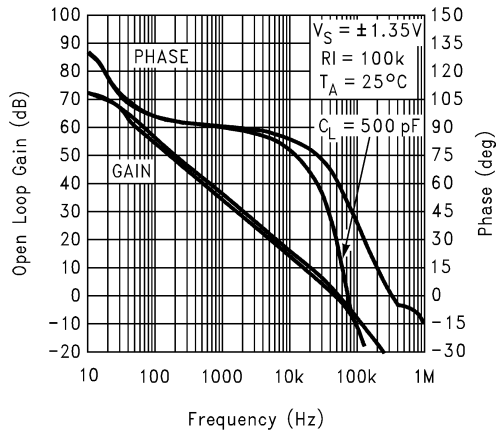


Figure 5-7. Gain and Phase vs Capacitive Load at 2.7V

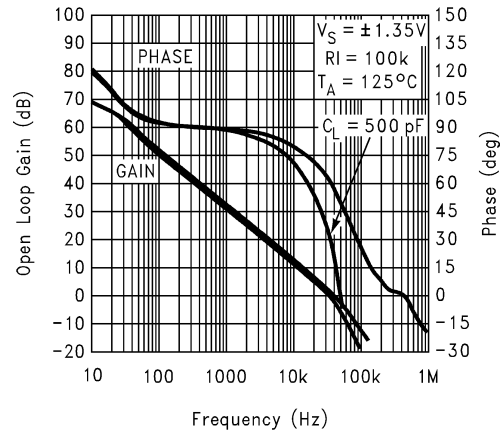


Figure 5-8. Gain and Phase vs Capacitive Load at 2.7V

5.10 Typical Characteristics: 3V

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)

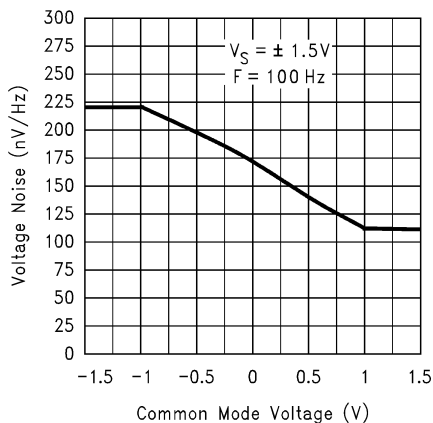


Figure 5-9. Voltage Noise vs Common-Mode Voltage at 3V

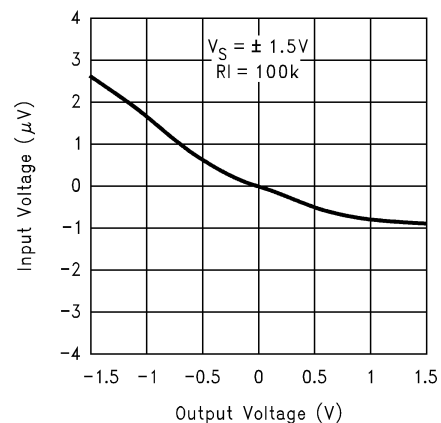


Figure 5-10. Output Voltage vs Input Voltage at 3V

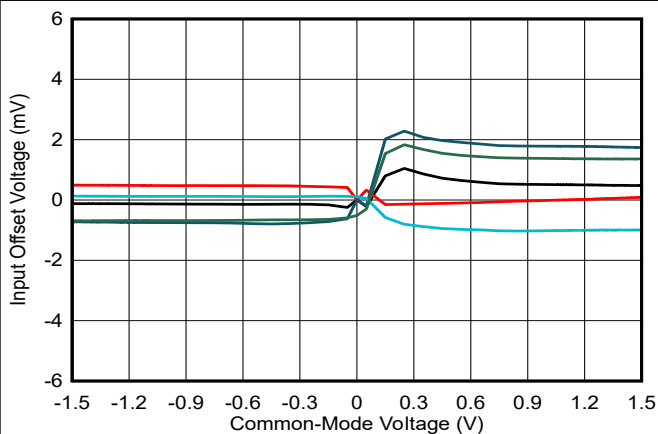


Figure 5-11. Offset Voltage vs Common-Mode Voltage at 3V

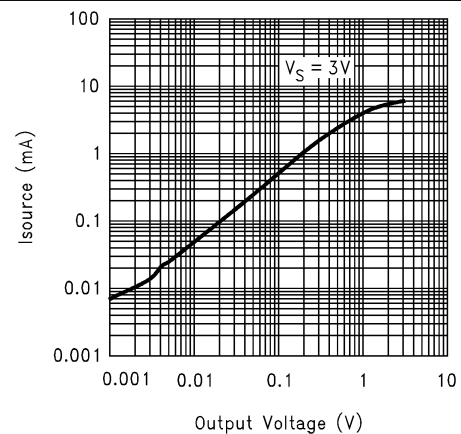
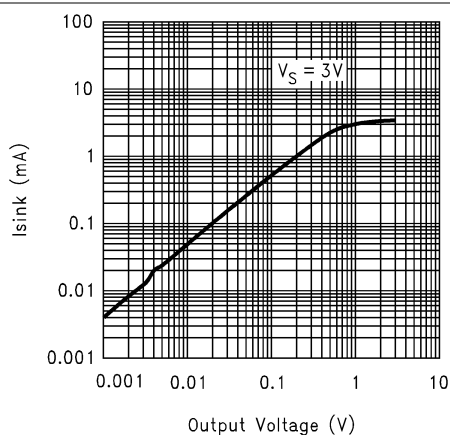


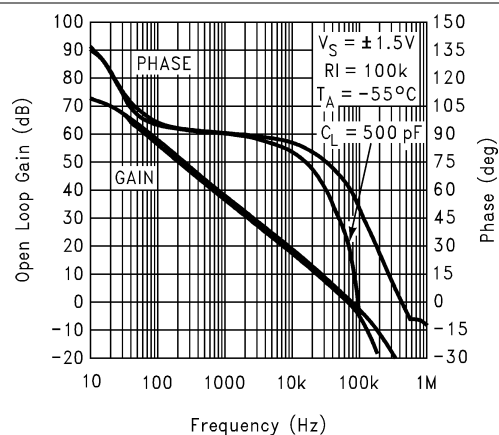
Figure 5-12. Sourcing Output vs Output Voltage

5.10 Typical Characteristics: 3V (continued)

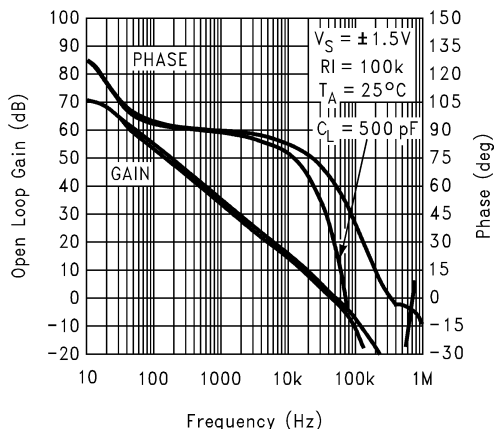
at $T_A = 25^\circ\text{C}$ (unless otherwise specified)



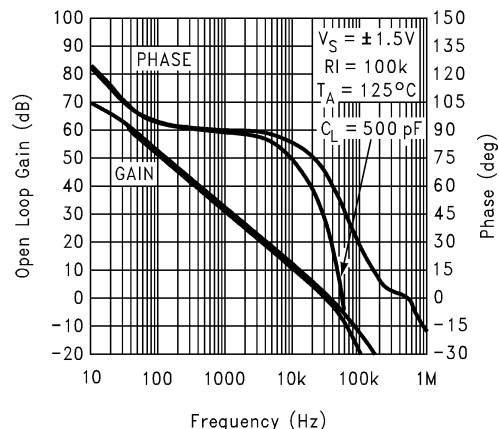
5-13. Sinking Output vs Output Voltage



5-14. Gain and Phase vs Capacitive Load at 3V



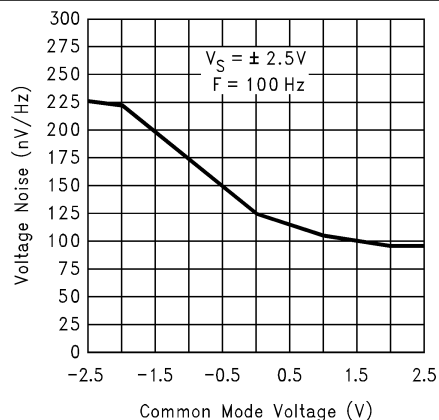
5-15. Gain and Phase vs Capacitive Load at 3V



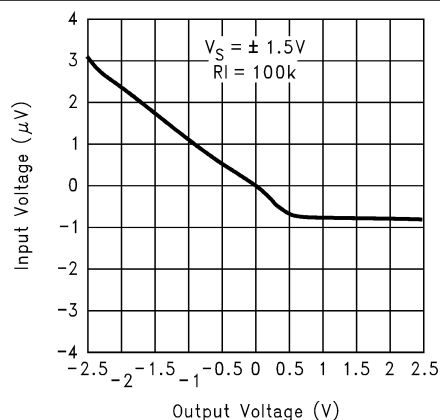
5-16. Gain and Phase vs Capacitive Load at 3V

5.11 Typical Characteristics: 5V

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)



5-17. Voltage Noise vs Common-Mode Voltage at 5V



5-18. Output Voltage vs Input Voltage at 5V

5.11 Typical Characteristics: 5V (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)

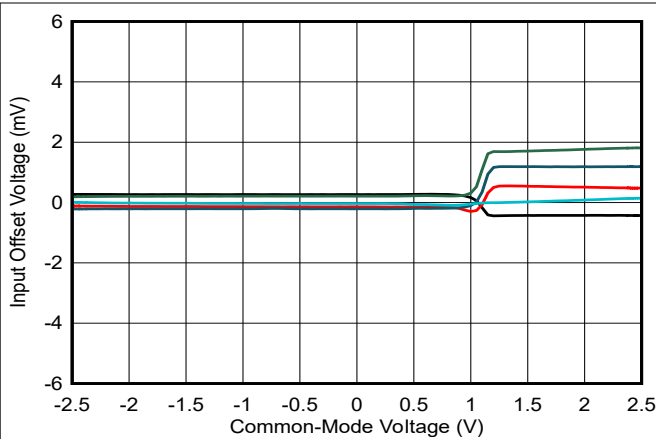


FIG 5-19. Offset Voltage vs Common-Mode Voltage at 5V

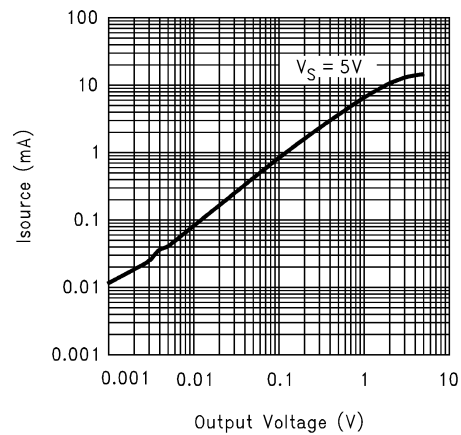


FIG 5-20. Sourcing Output vs Output Voltage

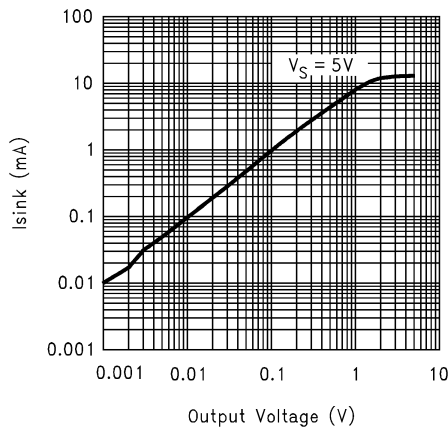


FIG 5-21. Sinking Output vs Output Voltage

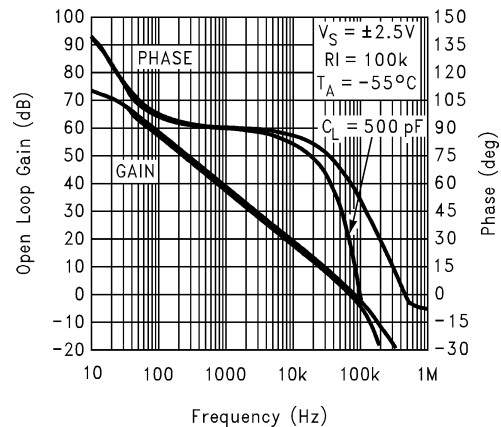


FIG 5-22. Gain and Phase vs Capacitive Load at 5V

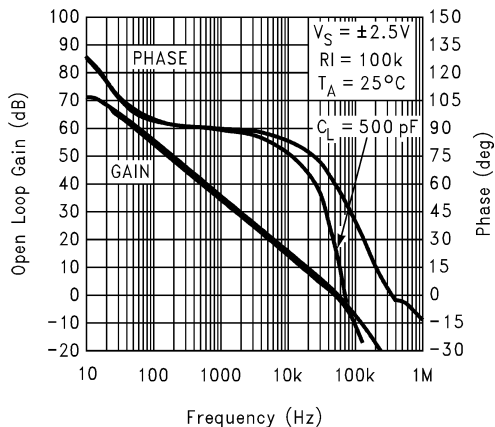


FIG 5-23. Gain and Phase vs Capacitive Load at 5V

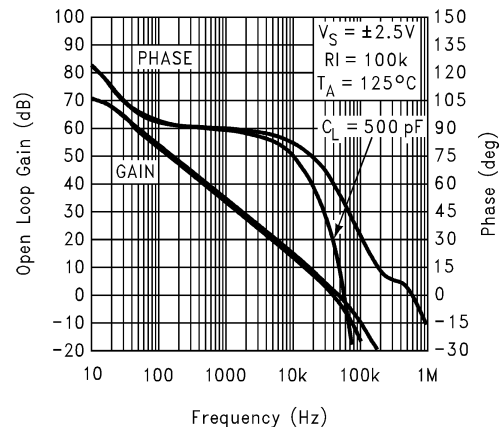


FIG 5-24. Gain and Phase vs Capacitive Load at 5V

5.11 Typical Characteristics: 5V (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)

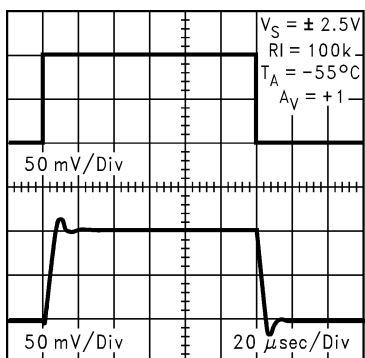


図 5-25. Noninverting Small-Signal Pulse Response at 5V

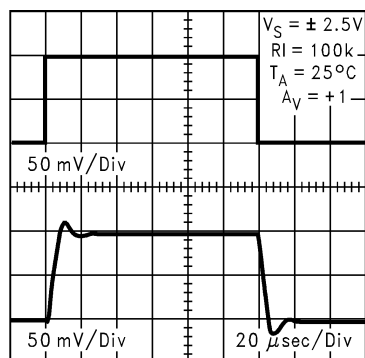


図 5-26. Noninverting Small-Signal Pulse Response at 5V

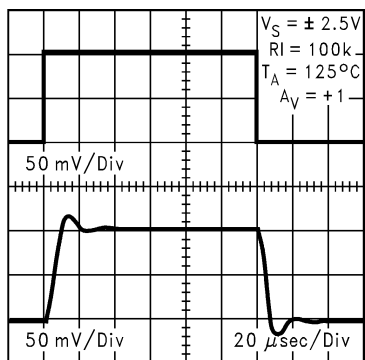


図 5-27. Noninverting Small-Signal Pulse Response at 5V

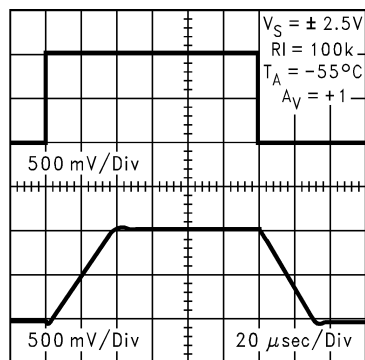


図 5-28. Noninverting Large-Signal Pulse Response at 5V

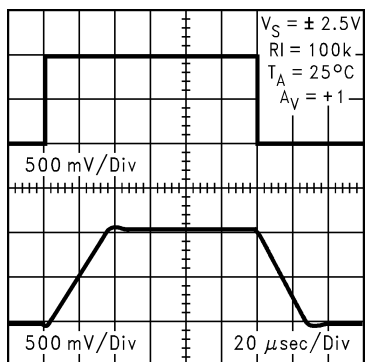


図 5-29. Noninverting Large-Signal Pulse Response at 5V

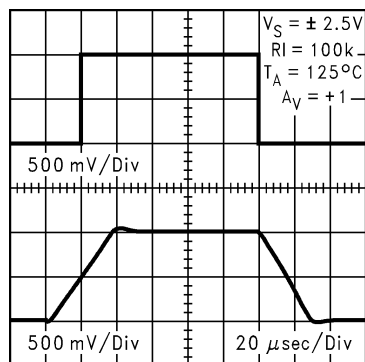
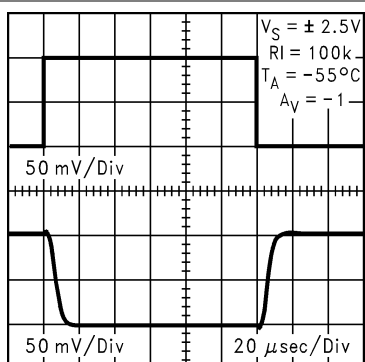


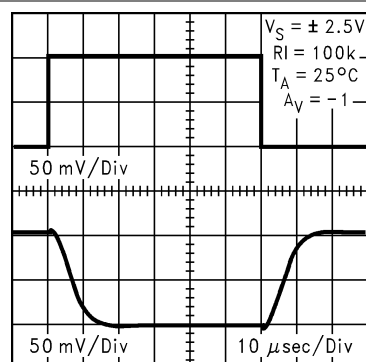
図 5-30. Noninverting Large-Signal Pulse Response at 5V

5.11 Typical Characteristics: 5V (continued)

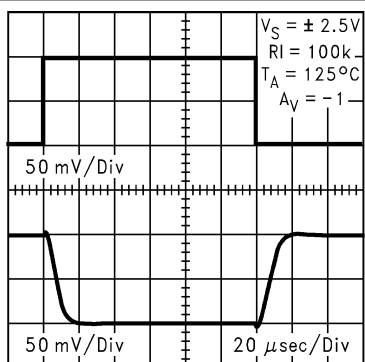
at $T_A = 25^\circ\text{C}$ (unless otherwise specified)



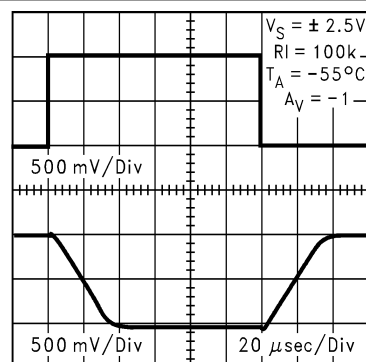
5-31. Inverting Small-Signal Pulse Response at 5V



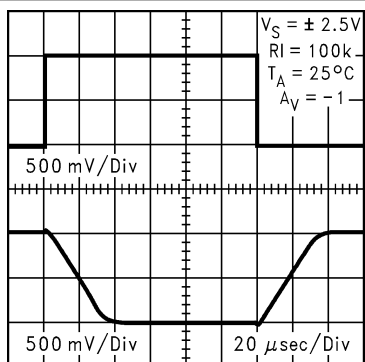
5-32. Inverting Small-Signal Pulse Response at 5V



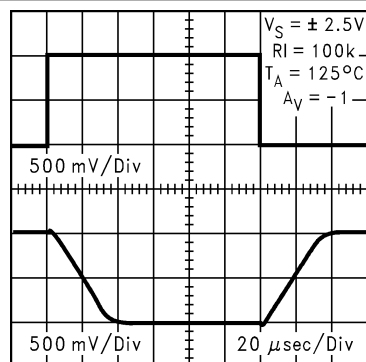
5-33. Inverting Small-Signal Pulse Response at 5V



5-34. Inverting Large-Signal Pulse Response at 5V



5-35. Inverting Large-Signal Pulse Response at 5V



5-36. Inverting Large-Signal Pulse Response at 5V

5.12 Typical Characteristics: 10V

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)

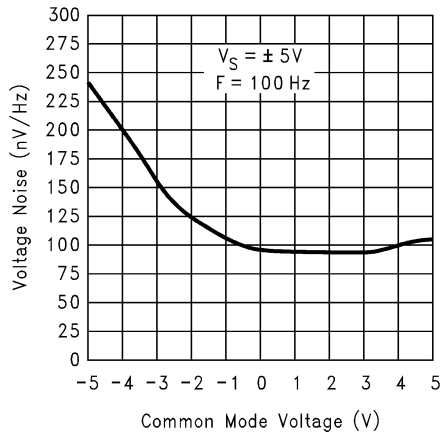


FIG 5-37. Voltage Noise vs Common-Mode Voltage at 10V

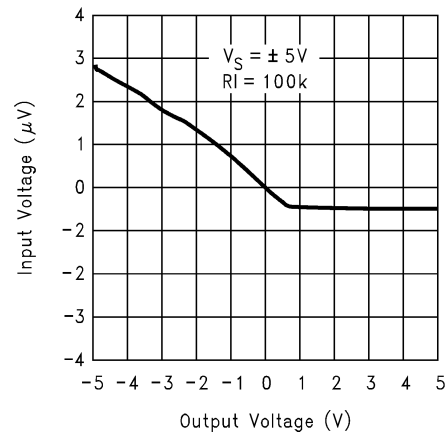


FIG 5-38. Output Voltage vs Input Voltage at 10V

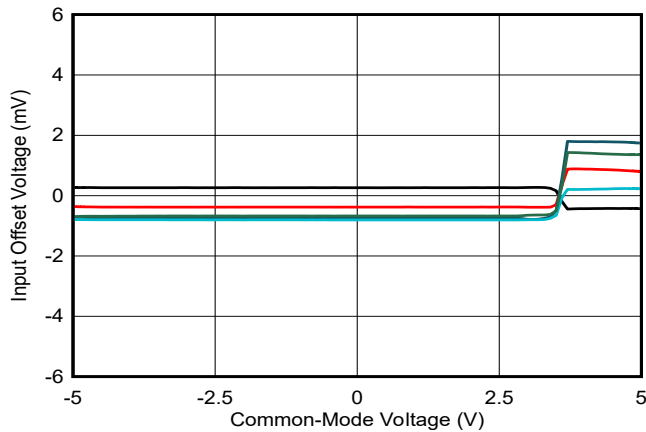


FIG 5-39. Offset Voltage vs Common-Mode Voltage at 10V

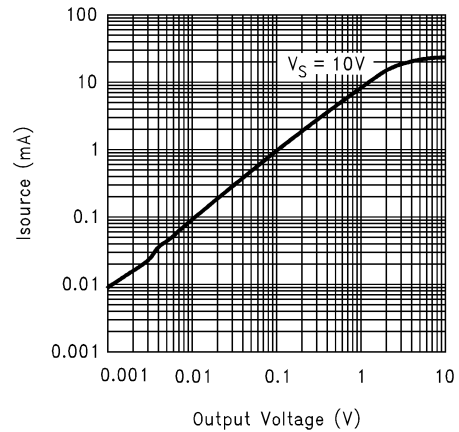


FIG 5-40. Sourcing Output vs Output Voltage

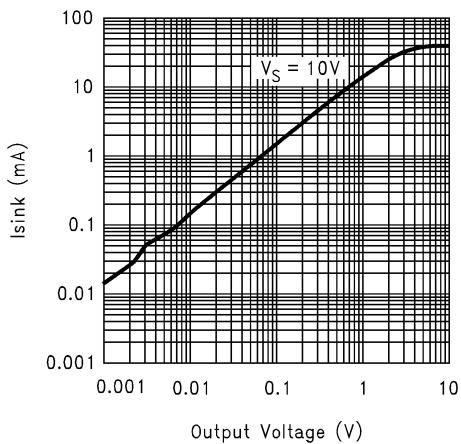


FIG 5-41. Sinking Output vs Output Voltage

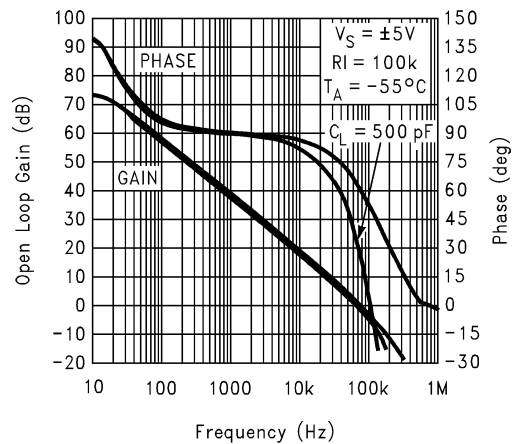


FIG 5-42. Gain and Phase vs Capacitive Load at 10V

5.12 Typical Characteristics: 10V (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise specified)

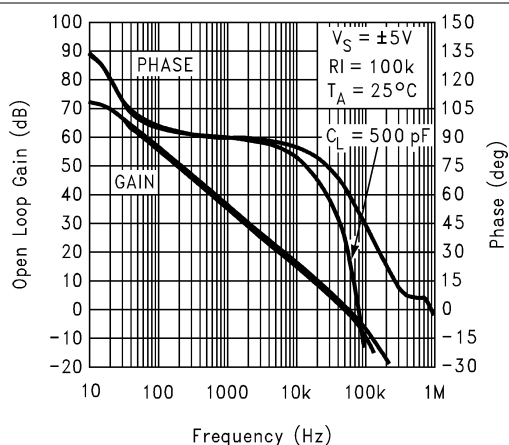


図 5-43. Gain and Phase vs Capacitive Load at 10V

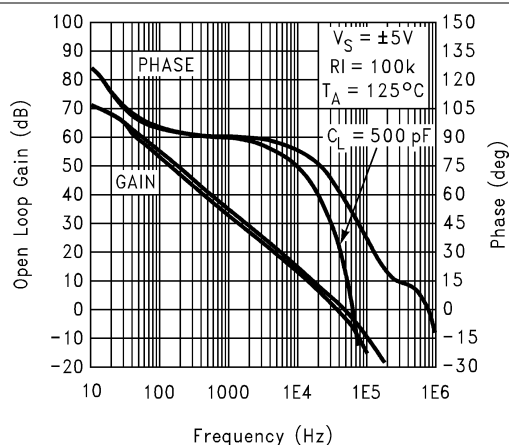


図 5-44. Gain and Phase vs Capacitive Load at 10V

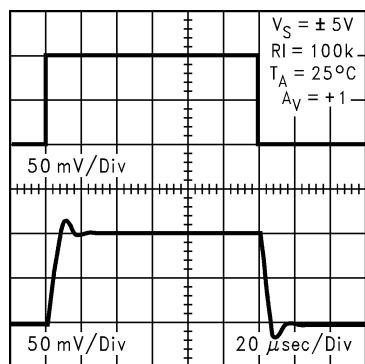


図 5-45. Noninverting Small-Signal Pulse Response at 10V

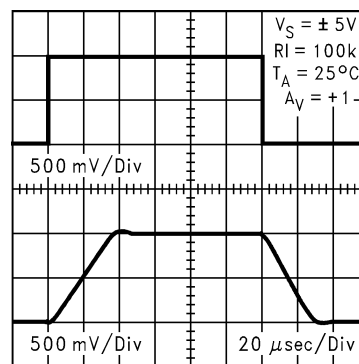


図 5-46. Noninverting Large-Signal Pulse Response at 10V

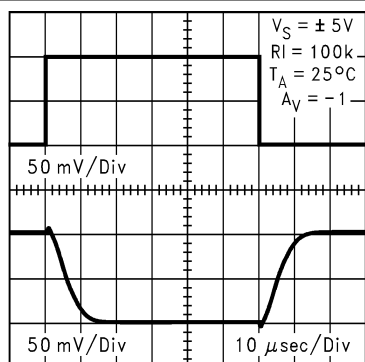


図 5-47. Inverting Small-Signal Pulse Response at 10V

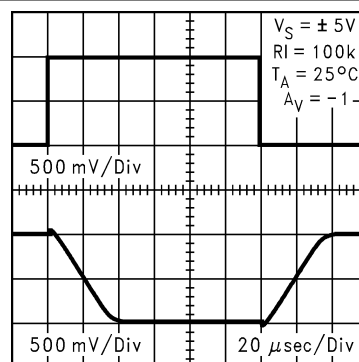


図 5-48. Inverting Large-Signal Pulse Response at 10V

6 Detailed Description

6.1 Feature Description

6.1.1 Benefits of the LMC7111 Tiny Amp

6.1.1.1 Size

The small footprint of the SOT-23-5 packaged tiny amplifier, (0.12in × 0.118in, 3.05mm × 3mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Many customers prefer smaller and lighter products because the designs can contribute to overall weight reduction in applications.

6.1.1.2 Height

The height (0.056 inches, 1.43mm) of the tiny amplifier makes the device an excellent choice for use in a wide range of circuit boards in which a thin profile is required.

6.1.1.3 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

6.1.1.4 Simplified Board Layout

The tiny amplifier can simplify board layout in several ways. Avoid long PCB traces by correctly placing amplifiers instead of routing signals to a dual or quad device. By using multiple tiny amplifiers instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

6.1.1.5 Low Supply Current

The typical 25μA supply current of the LMC7111 extends battery life in portable applications, and can allow for the reduction of battery size in some applications.

6.1.1.6 Wide Voltage Range

The LMC7111 is characterized at 2.7V, 3V, 3.3V, 5V and 10V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7111 a good choice for devices where the voltage can vary over the life of the batteries.

6.1.2 Input Common-Mode Voltage Range

The LMC7111 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage.

The absolute maximum input voltage is 300mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

Applications that exceed this rating must externally limit the maximum input current to ±5mA with an input resistor as shown in [Figure 6-1](#).

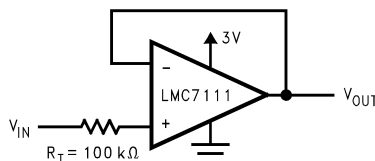


Figure 6-1. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

6.1.3 Output Swing

The LMC7111 output goes to within 100mV of either power supply rail for a 10kΩ load, and to 20mV of the rail for a 100kΩ load. This feature makes the LMC7111 useful to drive transistors connected to the same power supply. By going very close to the supply, the LMC7111 can turn the transistors all the way on or off.

7 Application and Implementation

注

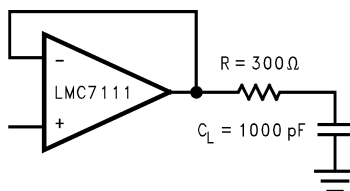
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7.1 Application Information

7.1.1 Capacitive Load Tolerance

The LMC7111 can typically directly drive a 300pF load with $V_S = 10V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in [図 7-1](#). This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.



**図 7-1. Resistive Isolation
of a 330pF Capacitive Load**

7.1.2 Compensating for Input Capacitance When Using Large-Value Feedback Resistors

When using very large value feedback resistors, (usually > 500kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in [Figure 7-2](#)), C_f is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance can be larger or smaller than that of a breadboard, so the actual optimum value for C_f can be different. Check C_f values on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

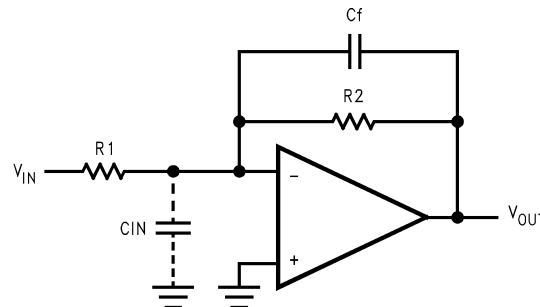


Figure 7-2. Canceling the Effect of Input Capacitance

7.1.3 Dual and Quad Devices With Similar Performance

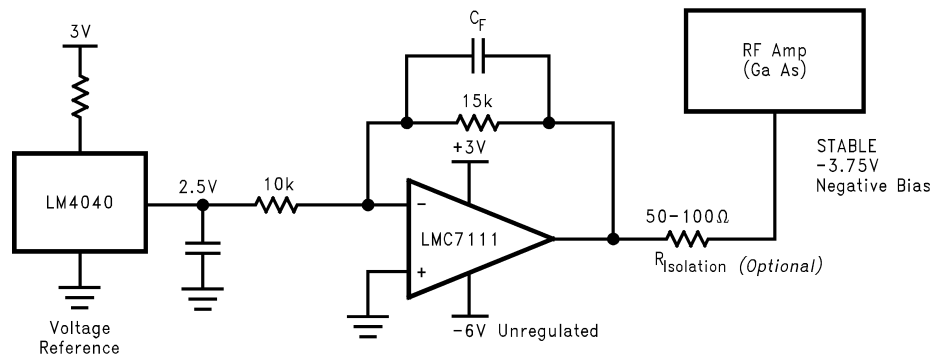
The dual LMC6462 and quad LMC6464 devices achieve performance similar to the LMC7111. Both devices are available in both conventional through-hole and surface-mount packaging. See also the [LMC646x data sheet](#) for details.

7.2 Typical Application

7.2.1 Biasing GaAs RF Amplifiers

The capacitive load capability, low current draw, and small size of the SOT-23 LMC7111 make this device a good choice for providing a stable negative bias to other integrated circuits.

The very small size of the LMC7111 and the LM4040 reference take up very little board space.



Note: C_F and $R_{isolation}$ prevent oscillations when driving capacitive loads.

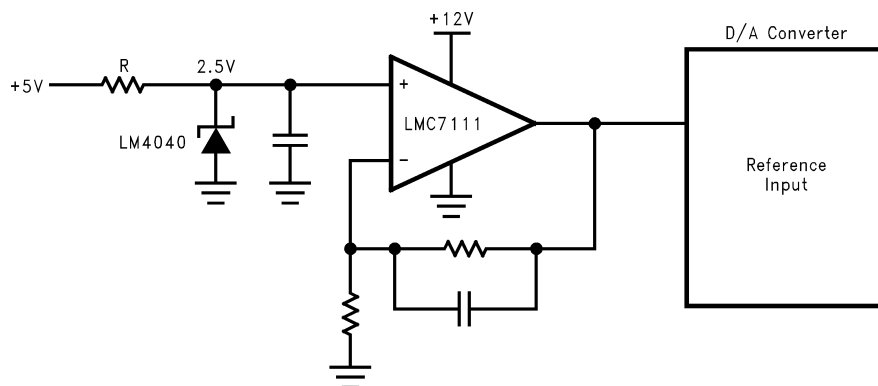
FIG 7-3. Stable Negative Bias

7.2.2 Reference Buffer for Analog-to-Digital Converters

The LMC7111 can be used as a voltage reference buffer for an analog-to-digital converter (ADC). This configuration works best for ADCs with the reference input is a static load, such as dual slope integrating ADCs. Converters with a reference input that is a dynamic load (the reference current changes with time) can require a faster device, such as the LMC7101 or the LMC7131.

The small size of the LMC7111 allows this device to be placed close to the reference input. The low supply current (25 μ A typical) saves power.

For ADC reference inputs that require higher accuracy and lower offset voltage, see the [LMC646x data sheet](#). The LMC6462 has performance similar to the LMC7111. The LMC6462 is available in two grades with reduced input voltage offset.



8 Device and Documentation Support

8.1 Device Support

8.1.1 Spice Macromodel

A SPICE macromodel is available for the LMC7111. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Visit the LMC7111 product page on <http://www.ti.com> for the spice model.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (March 2013) to Revision F (January 2025)	Page
• Updated pin diagram for SOT-23 and pin names in <i>Pin Configurations and Functions</i>	2
• Deleted PDIP package information in <i>Pin Configuration and Functions</i>	2
• Updated parameter names and table format in all <i>Electrical Characteristics</i>	4
• Deleted reference to AI version in all <i>Electrical Characteristics</i>	4
• Updated dV_{OS}/dT from $2\mu V/^{\circ}C$ to $10\mu V/^{\circ}C$	4
• Changed V_{CM} test condition from $CMRR \geq 50dB$ to $CMRR \geq 47dB$	4
• Changed V_{CM} test condition for negative rail for $V_S = 2.7V$ from $CMRR \geq 50dB$ to $CMRR \geq 41dB$	4
• Changed I_{SC} MIN from 30mA to 25mA.....	6

Changes from Revision D (March 2013) to Revision E (March 2013)**Page**

- ナショナル セミコンダクター データシートのレイアウトをテキサス・インスツルメンツ形式に変更 [1](#)

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC7111BIM5/NOPB	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 85	A01B
LMC7111BIM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A01B
LMC7111BIM5X/NOPB.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A01B
LMC7111BIM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A01B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

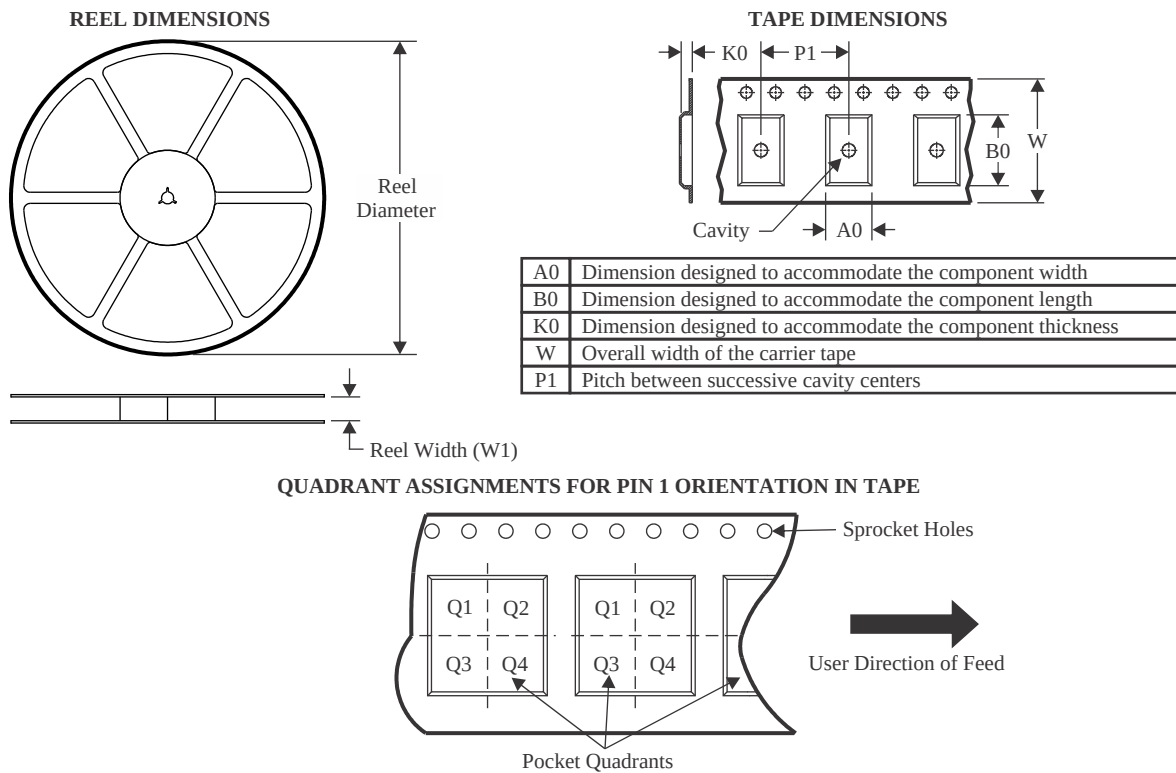
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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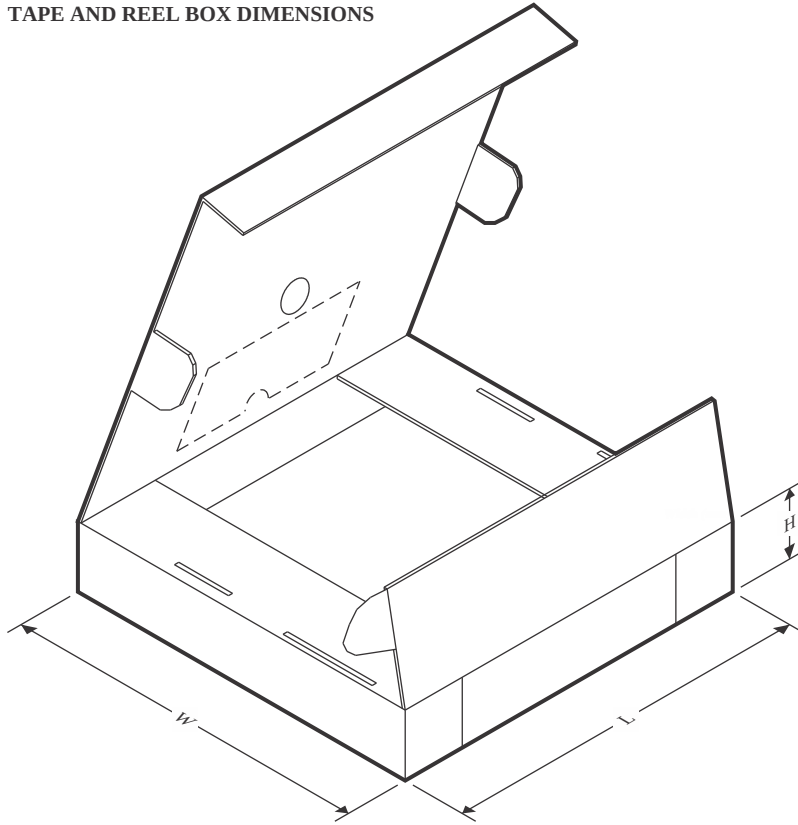
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7111BIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

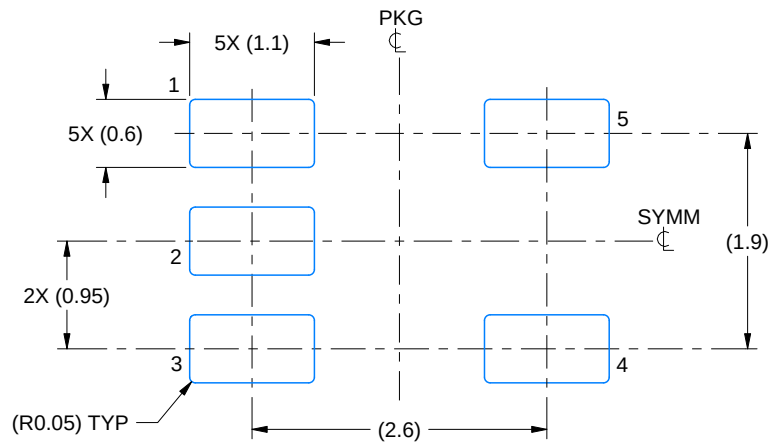
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7111BIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

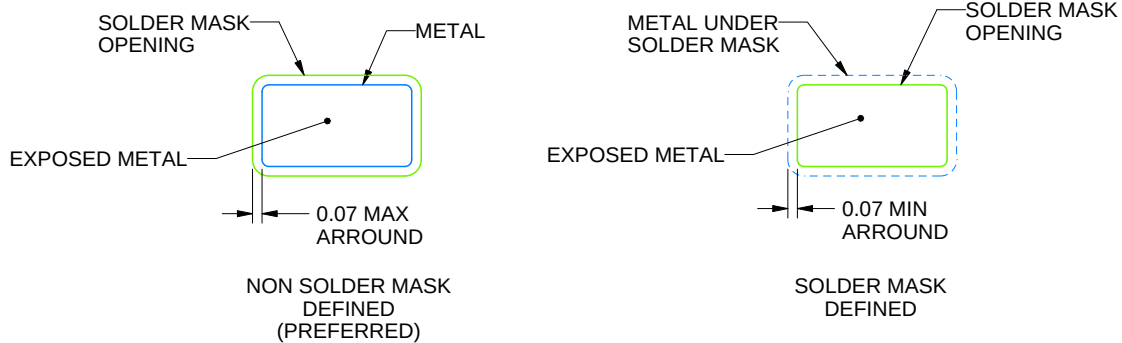
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

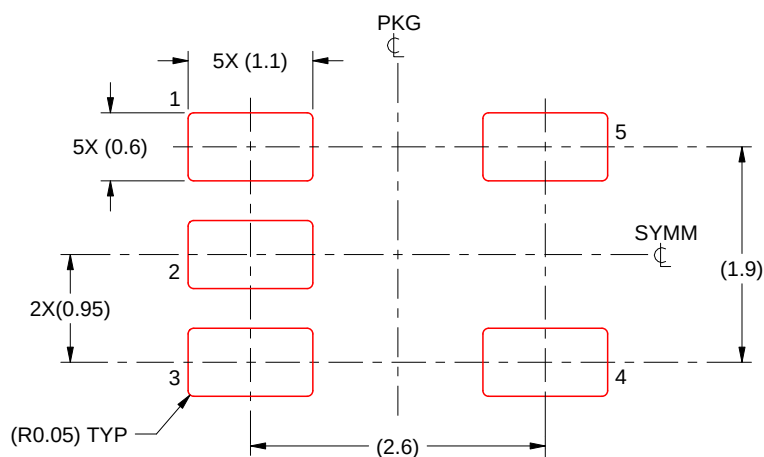
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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