LMG5200 80V、10A GaNハーフ・ブリッジ電力ステージ

1 特長

- 15mΩ GaN FETおよびドライバを内蔵
- 電圧定格: 連続80V、パルス100V
- PCBレイアウトが簡単になるようパッケージを最適化、アンダーフィル、クリーページ、クリアランスの要件を撤廃
- 共通ソース・インダクタンスが非常に低いため、ハード・スイッチングのトポロジで過剰なリンギングなしに高いスルー・レートのスイッチングを保証
- 絶縁および非絶縁アプリケーションに最適
- ゲート・ドライバは最高10MHzのスイッチングが可能
- 内部的なブートストラップ電源電圧クランピングにより、GaN FETオーバードライブを防止
- 電源レールの低電圧誤動作防止保護
- 非常に優れた伝搬遅延(標準値29.5ns)およびマッチング(標準値2ns)
- 低消費電力

2 アプリケーション

- 広いV_{IN}のマルチMHz同期整流降圧コンバータ
- オーディオ用Class-Dアンプ
- テレコム、産業、エンタープライズ・コンピューティング用の、48Vのポイント・オブ・ロード(POL)コンバータ
- 電力密度の高い単相および三相モータ・ドライブ

3 概要

LMG5200デバイスは80V、10Aのドライバに GaNハーフ・ブリッジ電力ステージを加えたもので、エンハンスメント・モードの窒化ガリウム(GaN) FETを使用する統合電力ステージ・ソリューションに使用できます。このデバイスは2つの80V GaN FETで構成され、1つの高周波数GaN FETドライバによりハーフ・ブリッジ構成で駆動されます。

GaN FETは逆方向回復時間がほぼゼロで、入力容量C_{ISS}が非常に小さいため、電力変換において大きな利点があります。すべてのデバイスはボンド・ワイヤを一切使用しないパッケージ・プラットフォームに取り付けられ、パッケージの寄生要素は最小限に抑えられます。LMG5200デバイスは、6mm×8mm×2mmの鉛フリー・パッケージで供給され、簡単にPCBへ取り付けできます。

TTLロジック互換の入力は、VCC電圧にかかわらず最高12Vの入力電圧に耐えられます。独自のブートストラップ電圧クランピング技法により、エンハンスメント・モードGaN FETのゲート電圧が安全な動作範囲内であることが保証されます。

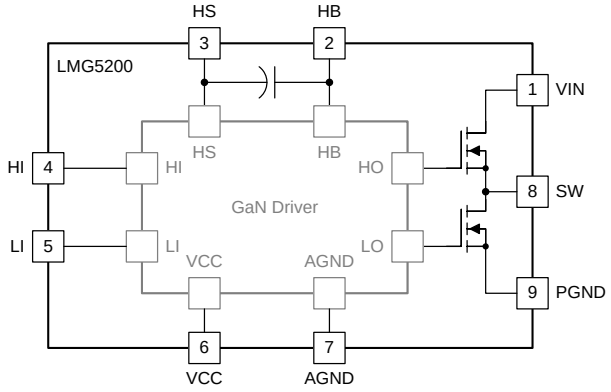
このデバイスは、ディスクリートGaN FETに対して、より使いやすいインターフェイスを提供し、その利点を拡大します。小さなフォーム・ファクタで高周波数、高効率の動作が必要なアプリケーションに理想的なソリューションです。LMG5200をTPS53632Gコントローラとともに使用すると、48Vからポイント・オブ・ロード電圧(0.5～1.5V)への直接変換が可能です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMG5200	QFM (9)	6.00mm×8.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ブロック概略図



目次

4 改訂履歴

Revision C (December 2016) から **Revision D** に変更 **Page**

- 全般的な編集およびSDSの更新 ... 1
- Changed *Thermal Information* table ... 5

Revision B (January 2016) から **Revision C** に変更 **Page**

- GaNテクノロジのプレビューから量産データへ 変更 ... 1
- 追加 Device Functional Modes Section ... 12
- 追加 Typical Application Section ... 12
- Updated Power Supply Recommendations Section ... 15
- 追加 開発サポート・セクションへのリンク ... 20

Revision A (March 2015) から **Revision B** に変更 **Page**

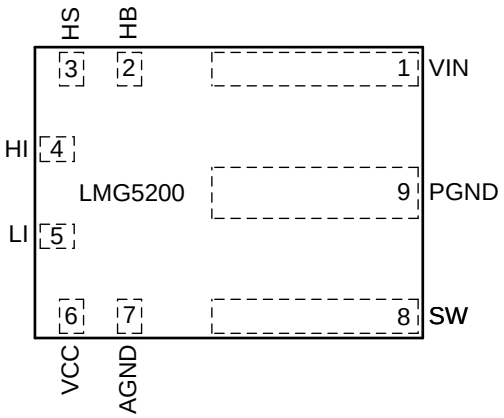
- 変更 part number typographical error in 図 14 ... 16

2015年3月発行のものから更新 **Page**

- ブロック概略図の誤字を修正 ... 1
- Corrected typographical error in 図 5 ... 8
- Corrected typographical error in 図 10 ... 10
- Corrected typographical error in 図 11 ... 12

5 Pin Configuration and Functions

MOF Package
9-Pin QFM
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	7	G	Analog ground. Ground of driver device.
HB	2	P	High-side gate driver bootstrap rail.
HI	4	I	High-side gate driver control input
HS	3	P	High-side GaN FET source connection
LI	5	I	Low-side driver control input
PGND	9	G	Power ground. Low-side GaN FET source. Electrically shorted to AGND pin.
SW	8	P	Switching node. Electrically shorted to HS pin. Ensure low capacitance at this node on PCB.
VCC	6	P	5-V positive gate drive supply
VIN	1	P	Input voltage pin. Electrically connected to high-side GaN FET drain.

(1) I = Input, O = Output, G = Ground, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	MIN	MAX	UNIT
VIN to PGND	0	80	V
VIN to PGND (pulsed, 100-ms maximum duration)(2)		100	V
HB to AGND	–0.3	86	V
HS to AGND	–5	80	V
HI to AGND	–0.3	12	V
LI to AGND	–0.3	12	V
VCC to AGND	–0.3	6	V
HB to HS	–0.3	6	V
HB to VCC	0	80	V
SW to PGND	–5	80	V
IOUT from SW pin		10	A
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device can withstand 1000 pulses up to 100 V of 100-ms duration and less than 1% duty cycle over its lifetime.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VCC	4.75	5	5.25	V
LI or HI Input	0		12	V
VIN	0		80	V
HS, SW	–5		80	V
HB	V_{HS} + 4		V_{HS} + 5.25	V
HS, SW slew rate(1)			50	V/ns
Junction temperature, T_J	–40		125	°C

(1) This parameter is ensured by design. Not tested in production.

6.4 Thermal Information

THERMAL METRIC (1) (2)		LMG5200 MOF (QFM) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator* .

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{CC}	VCC quiescent current	LI = HI = 0 V, VCC = 5 V, HB-HS = 4.6 V		0.08	0.125	mA
I_{CCO}	Total VCC operating current	f = 500 kHz		3	5	mA
I_{HB}	HB quiescent current	LI = HI = 0 V, VCC = 5 V, HB-HS = 4.6 V		0.09	0.15	mA
I_{HBO}	HB operating current	f = 500 kHz, 50% Duty cycle, V_{DD} = 5 V		1.5	2.5	mA
INPUT PINS						
V_{IH}	High-level input voltage threshold	Rising edge	1.87	2.06	2.22	V
V_{IL}	Low-level input voltage threshold	Falling edge	1.48	1.66	1.76	V
V_{HYS}	Hysteresis between rising and falling threshold			400		mV
R_I	Input pulldown resistance		100	200	300	kΩ
UNDERVOLTAGE PROTECTION						
V_{CCR}	V_{CC} Rising edge threshold	Rising	3.2	3.8	4.5	V
$V_{CC(hyst)}$	V_{CC} UVLO threshold hysteresis			200		mV
V_{HBR}	HB Rising edge threshold	Rising	2.5	3.2	3.9	V
$V_{HB(hyst)}$	HB UVLO threshold hysteresis			200		mV
BOOTSTRAP DIODE						
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 100 µA		0.45	0.65	V
V_{DH}	High current forward voltage	I_{VDD-HB} = 100 mA		0.9	1.0	V
R_D	Dynamic resistance	I_{VDD-HB} = 100 mA		1.85	2.8	Ω
	HB-HS clamp	Regulation Voltage	4.65	5	5.2	V
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, IR = 100 mA		40		ns
Q_{RR}	Bootstrap diode reverse recovery charge	V_{VIN} = 50 V		2		nC

(1) Parameters that show only a typical value are ensured by design and may not be tested in production.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1)

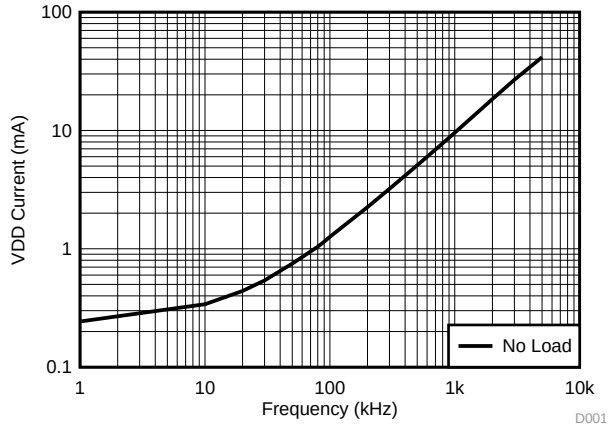
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER STAGE						
$R_{DS(ON)HS}$	High-side GaN FET on-resistance	LI = 0 V, HI = VCC=5 V, HB-HS = 5 V, VIN-SW = 10 A, T_J = 25℃		15	20	mΩ
$R_{DS(ON)LS}$	Low-side GaN FET on-resistance	LI = VCC = 5V, HI = 0 V, HB-HS = 5 V, SW-PGND = 10 A, T_J = 25℃		15	20	mΩ
V_{SD}	GaN 3rd quadrant conduction drop	I_{SD} = 500 mA, V_{IN} floating, V_{VCC} = 5 V, HI = LI = 0 V		2		V
$I_{L-VIN-SW}$	Leakage from VIN to SW when the high-side GaN FET and low-side GaN FET are off	VIN = 80 V, HI = LI = 0 V, V_{VCC} = 5 V, T_J= 25℃		25	150	µA
$I_{L-SW-GND}$	Leakage from SW to GND when the high-side GaN FET and low-side GaN FET are off	SW = 80 V, HI = LI = 0 V, V_{VCC} = 5V, T_J = 25℃		25	150	µA
C_{OSS}	Output capacitance of high-side GaN FET and low-side GaN FET	V_{DS}=40 V, V_{GS}= 0V (HI = LI = 0 V)		266		pF
Q_G	Total gate charge	V_{DS}=40 V, I_D= 10A, V_{GS}= 5 V		3.8		nC
Q_{OSS}	Output charge	V_{DS}=40 V, I_D= 10 A		21		nC
Q_{RR}	Source-to-drain reverse recovery charge	Not including internal driver bootstrap diode		0		nC
t_{HIPLH}	Propagation delay: HI rising(2)	LI = 0 V, VCC = 5 V, HB-HS = 5 V, VIN = 30 V		29.5	50	ns
t_{HIPHL}	Propagation delay: HI falling(2)	LI = 0 V, VCC = 5 V, HB-HS = 5 V, VIN = 30 V		29.5	50	ns
t_{LPLH}	Propagation delay: LI rising(2)	HI = 0 V, VCC = 5 V, HB-HS = 5 V, VIN = 30 V		29.5	50	ns
t_{LPHL}	Propagation delay: LI falling(2)	HI = 0 V, VCC = 5 V, HB-HS = 5 V, VIN = 30 V		29.5	50	ns
t_{MON}	Delay matching: LI high and HI low(2)			2	8	ns
t_{MOFF}	Delay matching: LI low and HI high(2)			2	8	ns
t_{PW}	Minimum input pulse width that changes the output			10		ns

(2) See *Propagation Delay and Mismatch Measurement*.

6.6 Typical Characteristics

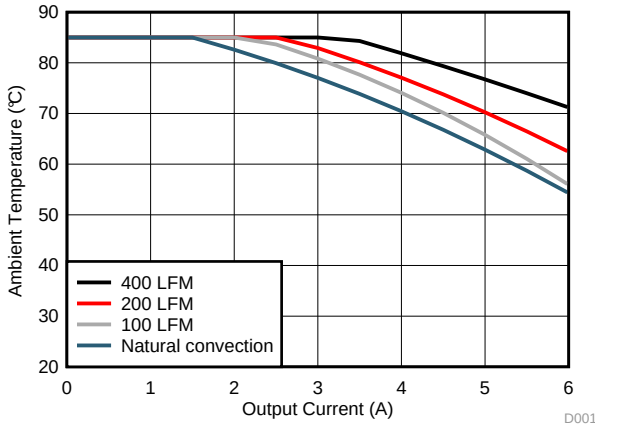
All the curves are based on measurements made on a PCB design with dimensions of 3.2 inches (W) × 2.7 inches (L) × 0.062 inch (T) and 4 layers of 2 oz copper.

The safe operating area (SOA) curves displays the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. A buck converter is used for measuring the SOA. 図 2 outlines the temperature and airflow conditions required for a given load current. The area under the curve dictates the SOA for different airflow conditions.



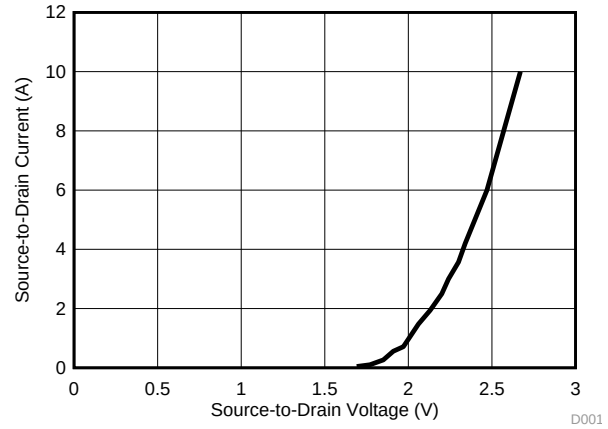
V_{DD} = 5 V

図 1. V_{DD} Supply Current vs Switching Frequency



V_{IN} = 48 V V_{OUT} = 5 V f_{SW} = 1 MHz

図 2. Safe Operating Area



GaN third quadrant conduction.

図 3. Source-to-Drain Current vs Source-to-Drain Voltage

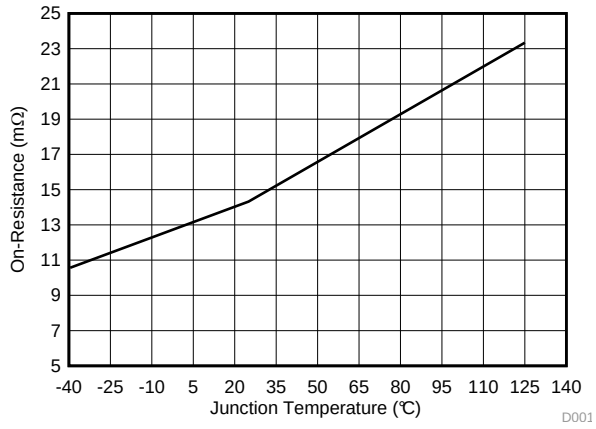


図 4. GaN FET On-Resistance vs Junction Temperature

7 Parameter Measurement Information

7.1 Propagation Delay and Mismatch Measurement

図 5 shows the typical test setup used to measure the propagation mismatch. As the gate drives are not accessible, pullup and pulldown resistors in this test circuit are used to indicate when the low-side GaN FET turns ON and the high-side GaN FET turns OFF and vice versa to measure the t_{MON} and t_{MOFF} parameters. Resistance values used in this circuit for the pullup and pulldown resistors are in the order of 1 kΩ; the current sources used are 2 A.

図 6 through 図 9 show propagation delay measurement waveforms. For turnon propagation delay measurements, the current sources are not used. For turnoff time measurements, the current sources are set to 2 A, and a voltage clamp limit is also set, referred to as $VIN_{(CLAMP)}$. When measuring the high-side component turnoff delay, the current source across the high-side FET is turned on, the current source across the low-side FET is off, HI transitions from high-to-low, and output voltage transitions from V_{IN} to $V_{IN(CLAMP)}$. Similarly, for low-side component turnoff propagation delay measurements, the high-side component current source is turned off, and the low-side component current source is turned on, LI transitions from high to low and the output transitions from GND potential to $V_{IN(CLAMP)}$. The time between the transition of LI and the output change is the propagation delay time.

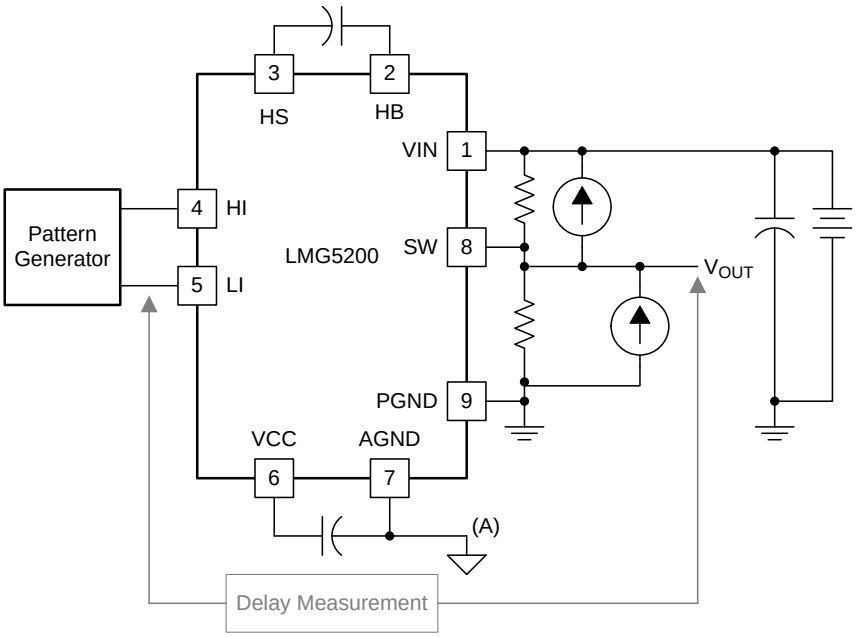


図 5. Propagation Delay and Propagation Mismatch Measurement

Propagation Delay and Mismatch Measurement (continued)

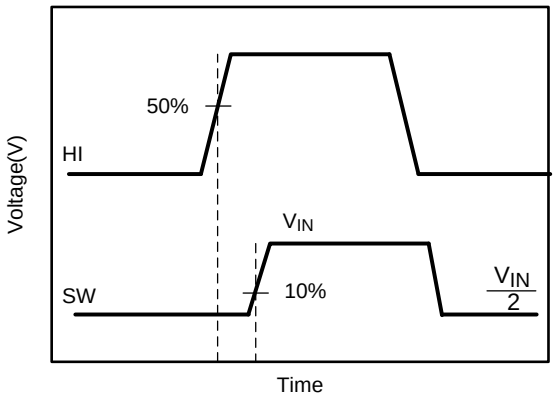


図 6. High-Side Gate Driver Turnon

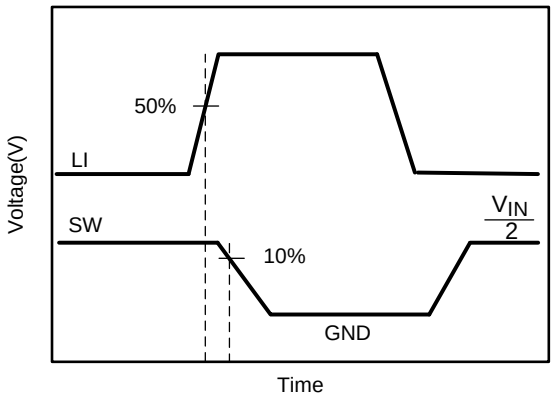


図 7. Low-Side Gate Driver Turnon

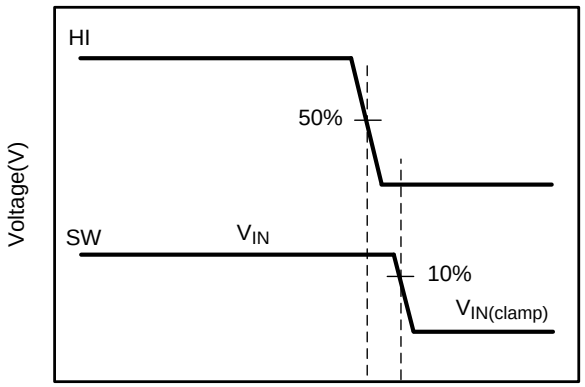


図 8. High-Side Gate Driver Turnoff

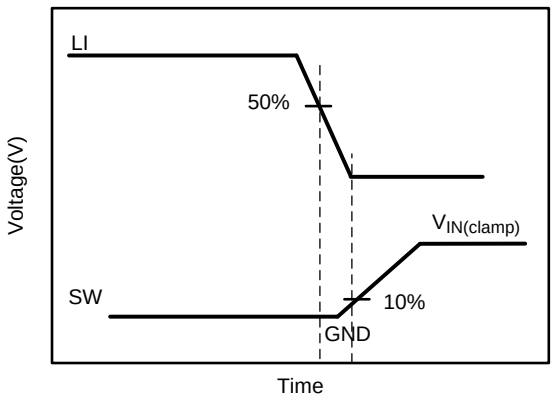


図 9. Low-Side Gate Driver Turnoff

8 Detailed Description

8.1 Overview

図 10 shows the LMG5200, half-bridge, GaN power stage with highly integrated high-side and low-side gate drivers, which includes built-in UVLO protection circuitry and an overvoltage clamp circuitry. The clamp circuitry limits the bootstrap refresh operation to ensure that the high-side gate driver overdrive does not exceed 5.4 V. The device integrates two, 15-mΩ GaN FETs in a half-bridge configuration. The device can be used in many isolated and non-isolated topologies allowing very simple integration. The package is designed to minimize the loop inductance while keeping the PCB design simple. The drive strengths for turnon and turnoff are optimized to ensure high voltage slew rates without causing any excessive ringing on the gate or power loop.

8.2 Functional Block Diagram

図 10 shows the functional block diagram of the LMG5200 device with integrated high-side and low-side GaN FETs.

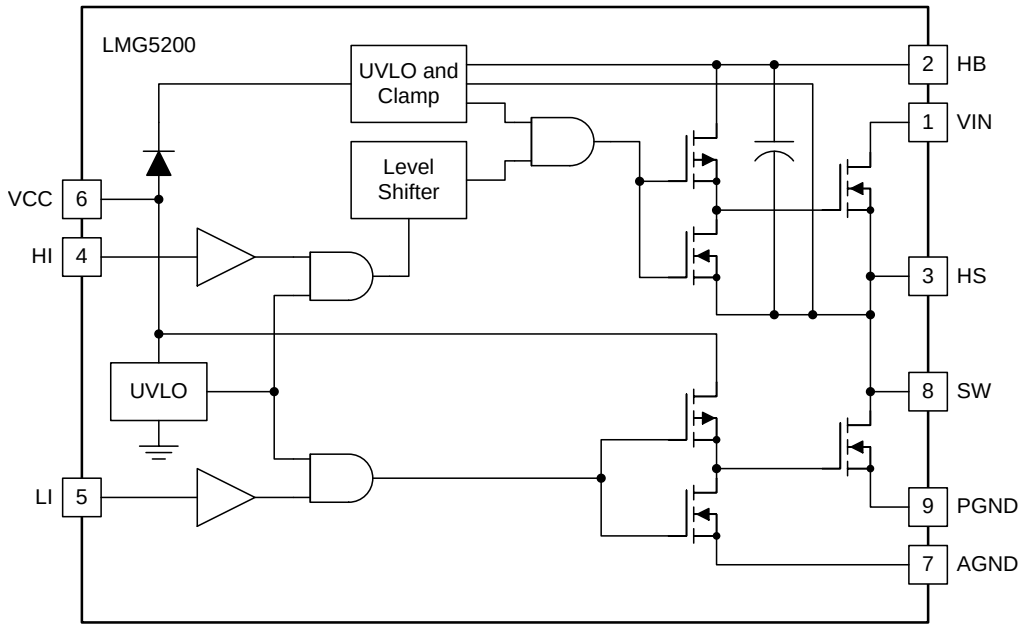


図 10. Functional Block Diagram

8.3 Feature Description

The LMG5200 device brings ease of designing high power density boards without the need for underfill while maintaining creepage and clearance requirements. The propagation delays between the high-side gate driver and low-side gate driver are matched to allow very tight control of dead time. Controlling the dead time is critical in GaN-based applications to maintain high efficiency. HI and LI can be independently controlled to minimize the third quadrant conduction of the low-side FET for hard switched buck converters. A very small propagation mismatch between the HI and LI to the drivers for both the falling and rising thresholds ensures dead times of < 10 ns. Co-packaging the GaN FET half-bridge with the driver ensures minimized common source inductance. This minimized inductance has a significant performance impact on hard-switched topologies.

The built-in bootstrap circuit with clamp prevents the high-side gate drive from exceeding the GaN FETs maximum gate-to-source voltage (Vgs) without any additional external circuitry. The built-in driver has an undervoltage lockout (UVLO) on the VDD and bootstrap (HB-HS) rails. When the voltage is below the UVLO threshold voltage, the device ignores both the HI and LI signals to prevent the GaN FETs from being partially turned on. Below UVLO, if there is sufficient voltage (V_{VCC} > 2.5 V), the driver actively pulls the high-side and low-side gate driver output low. The UVLO threshold hysteresis of 200 mV prevents chattering and unwanted turnon due to voltage spikes. Use an external VCC bypass capacitor with a value of 0.1 µF or higher. TI recommends a size of 0402 to minimize trace length to the pin. Place the bypass and bootstrap capacitors as close as possible to the device to minimize parasitic inductance.

8.3.1 Control Inputs

The LMG5200's inputs pins are independently controlled with TTL input thresholds and can withstand voltages up to 12V regardless of the VDD voltage. This allows the inputs to be directly connected to the outputs of an analog PWM controller with up to 12V power supply, eliminating the need for a buffer stage.

In order to allow flexibility to optimize deadtime according to design needs, the LMG5200 does not implement an overlap protection functionality. If both HI and LI are asserted, both the high-side and low-side GaN FETs are turned on. Careful consideration must be applied to the control inputs in order to avoid a shoot-through condition.

Feature Description (continued)

8.3.2 Start-up and UVLO

The LMG5200 has an UVLO on both the V_{CC} and HB (bootstrap) supplies. When the V_{CC} voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also, if there is insufficient V_{CC} voltage, the UVLO actively pulls the high- and low-side GaN FET gates low. When the HB to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only the high-side GaN FET gate is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

表 1. V_{CC} UVLO Feature Logic Operation

CONDITION (V_{HB-HS} > V_{HBR} for all cases below)	HI	LI	SW
V_{CC} - V_{SS} < V_{CCR} during device start-up	H	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	L	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	H	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	L	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	H	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	L	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	H	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	L	L	Hi-Z

表 2. V_{HB-HS} UVLO Feature Logic Operation

CONDITION (V_{CC} > V_{CCR} for all cases below)	HI	LI	SW
V_{HB-HS} < V_{HBR} during device start-up	H	L	Hi-Z
V_{HB-HS} < V_{HBR} during device start-up	L	H	PGND
V_{HB-HS} < V_{HBR} during device start-up	H	H	PGND
V_{HB-HS} < V_{HBR} during device start-up	L	L	Hi-Z
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	H	L	Hi-Z
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	L	H	PGND
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	H	H	PGND
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	L	L	Hi-Z

8.3.3 Bootstrap Supply Voltage Clamping

The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5 V (typical). This clamp prevents the gate voltage from exceeding the maximum gate-source voltage rating of the enhancement-mode GaN FETs.

8.3.4 Level Shift

The level-shift circuit is the interface from the high-side input HI to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the high-side GaN FET gate driver output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

8.4 Device Functional Modes

The LMG5200 operates in normal mode and UVLO mode. See *Start-up and UVLO* for information on UVLO operation mode. In the normal mode, the output state is dependent on the states of the HI and LI pins. 表 3 lists the output states for different input pin combinations. Note that when both HI and LI are asserted, both GaN FETs in the power stage are turned on. Careful consideration must be applied to the control inputs in order to avoid this state, as it will result in a shoot-through condition, which can permanently damage the device.

表 3. Truth Table

HI	LI	HIGH-SIDE GaN FET	LOW-SIDE GaN FET	SW
L	L	OFF	OFF	Hi-Z
L	H	OFF	ON	PGND
H	L	ON	OFF	VIN
H	H	ON	ON	- - -

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMG5200 GaN power stage is a versatile building block for various types of high-frequency, switch-mode power applications. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the GaN FETs. The device design is highly optimized for synchronous buck converters and other half-bridge configurations.

9.2 Typical Application

図 11 shows a synchronous buck converter application with V_{CC} connected to a 5-V supply. It is critical to optimize the power loop (loop impedance from VIN capacitor to PGND). Having a high power loop inductance causes significant ringing in the SW node and also causes the associated power loss. Refer to the *Layout Guidelines* section for information on how to minimize this power loop.

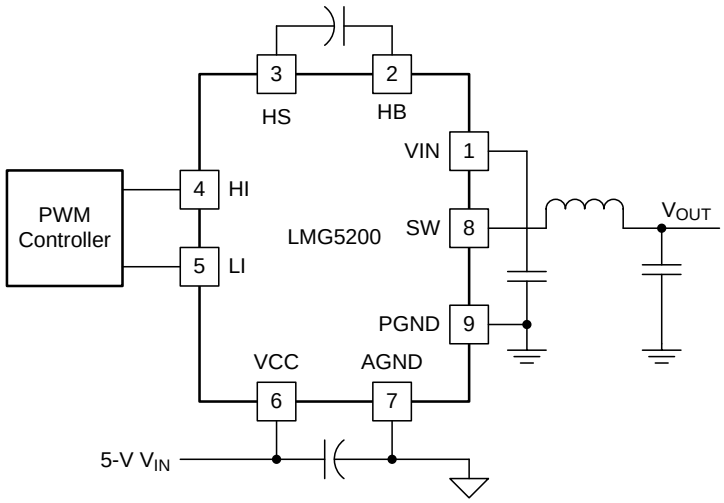


図 11. Typical Connection Diagram For a Synchronous Buck Converter

Typical Application (continued)

9.2.1 Design Requirements

When designing a synchronous buck converter application that incorporates the LMG5200 power stage, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are the input voltages, passive components, operating frequency, and controller selection. 表 4 shows some sample values for a typical application. See *Power Supply Recommendations*, *Layout*, and *Power Dissipation* for other key design considerations for the LMG5200.

表 4. Design Parameters

PARAMETER	SAMPLE VALUE
Half-bridge input supply voltage, V_{IN}	48 V
Output voltage, V_{OUT}	12 V
Output current	8 A
V_{HB-HS} bootstrap capacitor	0.1 uF, X5R
Switching frequency	1 MHz
Dead time	8 ns
Inductor	4.7 µH
Controller	TPS40400

9.2.2 Detailed Design Procedure

This procedure outlines the design considerations of LMG5200 in a synchronous buck converter. For additional design help, see 関連資料 .

9.2.2.1 V_{CC} Bypass Capacitor

The V_{CC} bypass capacitor provides the gate charge for the low-side and high-side transistors and to absorb the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with 式 1.

$$C_{VCC} = (Q_{gH} + Q_{gL} + Q_{rr}) / \Delta V \quad (1)$$

Q_{gH} and Q_{gL} are the gate charge of the high-side and low-side transistors, respectively. Q_{rr} is the reverse recovery charge of the bootstrap diode. ΔV is the maximum allowable voltage drop across the bypass capacitor. A 0.1-µF or larger value, good-quality, ceramic capacitor is recommended. Place the bypass capacitor as close as possible to the V_{CC} and AGND pins of the device to minimize the parasitic inductance.

9.2.2.2 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side gate drive, dc bias power for HB UVLO circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated using 式 2.

$$C_{BST} = (Q_{gH} + Q_{rr} + I_{HB} * t_{ON(max)}) / \Delta V$$

where

- I_{HB} is the quiescent current of the high-side gate driver (150 µA, maximum)
- t_{ON}(maximum) is the maximum on-time period of the high-side gate driver
- Q_{rr} is the reverse recovery charge of the bootstrap diode
- Q_{gH} is the gate charge of the high-side GaN FET
- ΔV is the permissible ripple in the bootstrap capacitor (< 100 mV, typical) (2)

A 0.1-µF, 16-V, 0402 ceramic capacitor is suitable for most applications. Place the bootstrap capacitor as close as possible to the HB and HS pins.

9.2.2.3 Power Dissipation

Ensure that the power loss in the driver and the GaN FETs is maintained below the maximum power dissipation limit of the package at the operating temperature. The smaller the power loss in the driver and the GaN FETs, the higher the maximum operating frequency that can be achieved in the application. The total power dissipation of the LMG5200 device is the sum of the gate driver losses, the bootstrap diode power loss and the switching and conduction losses in the FETs.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated using 式 3.

$$P = (2 \times Q_g) \times V_{DD} \times f_{SW} \quad (3)$$

where

- Q_g is the gate charge
- V_{DD} is the bias supply
- f_{SW} is the switching frequency

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the outputs. 図 1 shows the measured gate driver power dissipation versus frequency and load capacitance. Use this graph to approximate the power losses due to the gate drivers.

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Because each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

The power losses due to the GaN FETs can be divided into conduction losses and switching losses. Conduction losses are resistive losses and can be calculated using 式 4.

$$P_{COND} = \left[(I_{RMS(HS)})^2 \times RDS_{(on)HS}\right] + \left[(I_{RMS(LS)})^2 \times RDS_{(on)LS}\right] \quad (4)$$

where

- $R_{DS(on)HS}$ is the high-side GaN FET on-resistance
- $R_{DS(on)LS}$ is the low-side GaN FET on-resistance
- $I_{RMS(HS)}$ is the high-side GaN FET RMS current
- $I_{RMS(LS)}$ and low-side GaN FET RMS current

The switching losses can be computed to a first order using 式 5.

$$P_{SW} = V_{IN} \times I_{OUT} \times f_{SW} \times t_{TR} \quad (5)$$

where

- t_{TR} is the switch transition time from ON to OFF and from OFF to ON

Note that the low-side FET does not suffer from this loss. The third quadrant loss in the low-side device is ignored in this first order loss calculation.

As described previously, switching frequency has a direct effect on device power dissipation. Although the gate driver of the LMG5200 device is capable of driving the GaN FETs at frequencies up to 10 MHz, careful consideration must be applied to ensure that the running conditions for the device meet the recommended operating temperature specification. Specifically, hard-switched topologies tend to generate more losses and self-heating than soft-switched applications.

The sum of the driver loss, the bootstrap diode loss, and the switching and conduction losses in the GaN FETs is the total power loss of the device. Careful board layout with an adequate amount of thermal vias close to the power pads (VIN and PGND) allows optimum power dissipation from the package. A top-side mounted heat sink with airflow can also improve the package power dissipation.

9.2.3 Application Curves

図 12. SW Node Behavior Showing the Dead Time

図 13. Zoom-In Showing the Dead Time of 7.7 ns and the Overshoot of the SW Node

10 Power Supply Recommendations

The recommended bias supply voltage range for LMG5200 is from 4.75 V to 5.25 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the V_{CC} supply circuit. The upper end of this range is driven by the 6 V absolute maximum voltage rating of V_{CC}. Note that the gate voltage of the low-side GaN FET is not clamped internally. Hence, it is important to keep the V_{CC} bias supply within the recommended operating range to prevent exceeding the low-side GaN transistor gate breakdown voltage.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{CC} voltage drops, the device continues to operate in normal mode as far as the voltage drop does not exceeds the hysteresis specification, $V_{CC(hyst)}$. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LMG5200 to avoid triggering device-shutdown.

Place a local bypass capacitor between the VDD and VSS pins. This capacitor must be located as close as possible to the device. A low ESR, ceramic surface-mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

11 Layout

11.1 Layout Guidelines

To maximize the efficiency benefits of fast switching, it is extremely important to optimize the board layout such that the power loop impedance is minimal. When using a multilayer board (more than 2 layers), power loop parasitic impedance is minimized by having the return path to the input capacitor (between VIN and PGND), small and directly underneath the first layer as shown in 図 14 and 図 15. Loop inductance is reduced due to flux cancellation as the return current is directly underneath and flowing in the opposite direction. It is also critical that the VCC capacitors and the bootstrap capacitors are as close as possible to the device and in the first layer. Carefully consider the AGND connection of LMG5200 device. It must NOT be directly connected to PGND so that PGND noise does not directly shift AGND and cause spurious switching events due to noise injected in HI and LI signals.

11.2 Layout Examples

Placements shown in 図 14 and in the cross section of 図 15 show the suggested placement of the device with respect to sensitive passive components, such as VIN, bootstrap capacitors (HS and HB) and VSS capacitors. Use appropriate spacing in the layout to reduce creepage and maintain clearance requirements in accordance with the application pollution level. Inner layers if present can be more closely spaced due to negligible pollution.

The layout must be designed to minimize the capacitance at the SW node. Use as small an area of copper as possible to connect the device SW pin to the inductor, or transformer, or other output load. Furthermore, ensure that the ground plane or any other copper plane has a cutout so that there is no overlap with the SW node, as this would effectively form a capacitor on the printed circuit board. Additional capacitance on this node reduces the advantages of the advanced packaging approach of the LMG5200 and may result in reduced performance. 図 16, 図 17, 図 18, and 図 19 show an example of how to design for minimal SW node capacitance on a four-layer board. In these figures, U1 is the LMG5200 device.

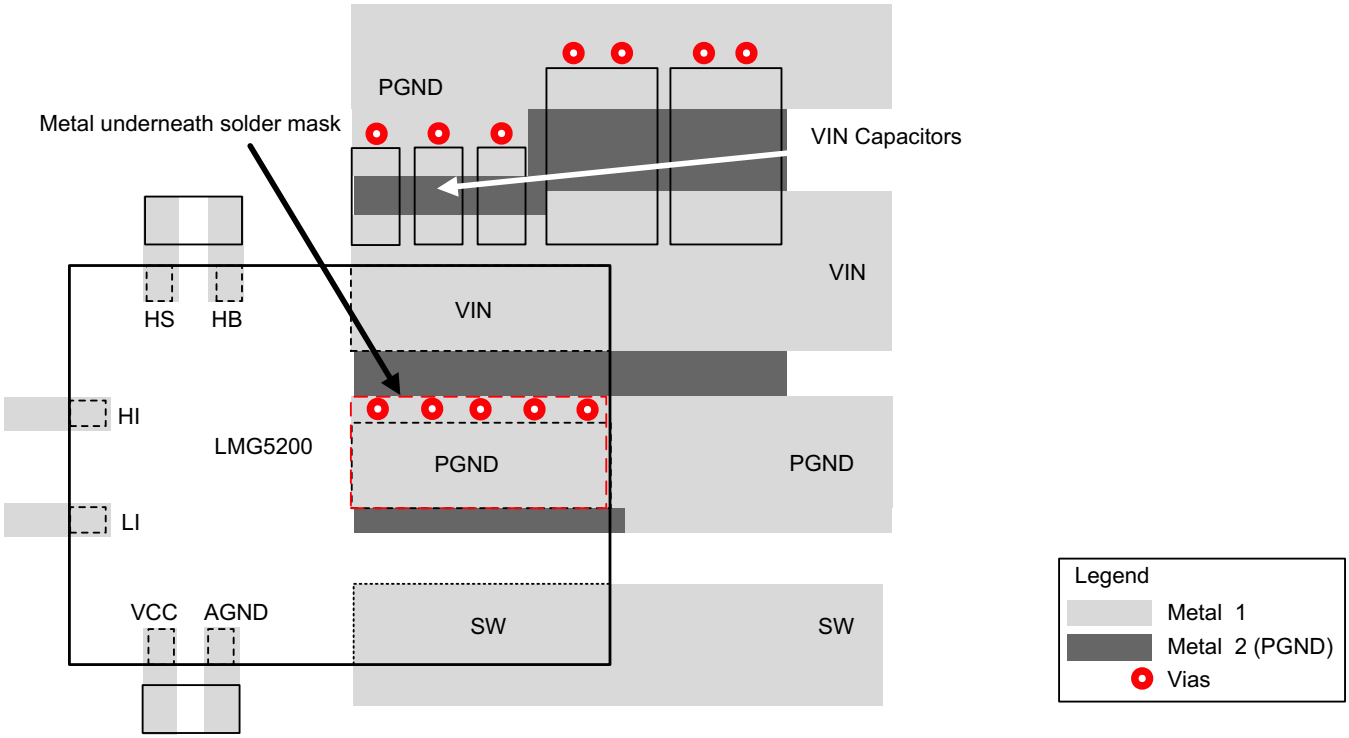


図 14. External Component Placement (Single Layer)

Layout Examples (continued)

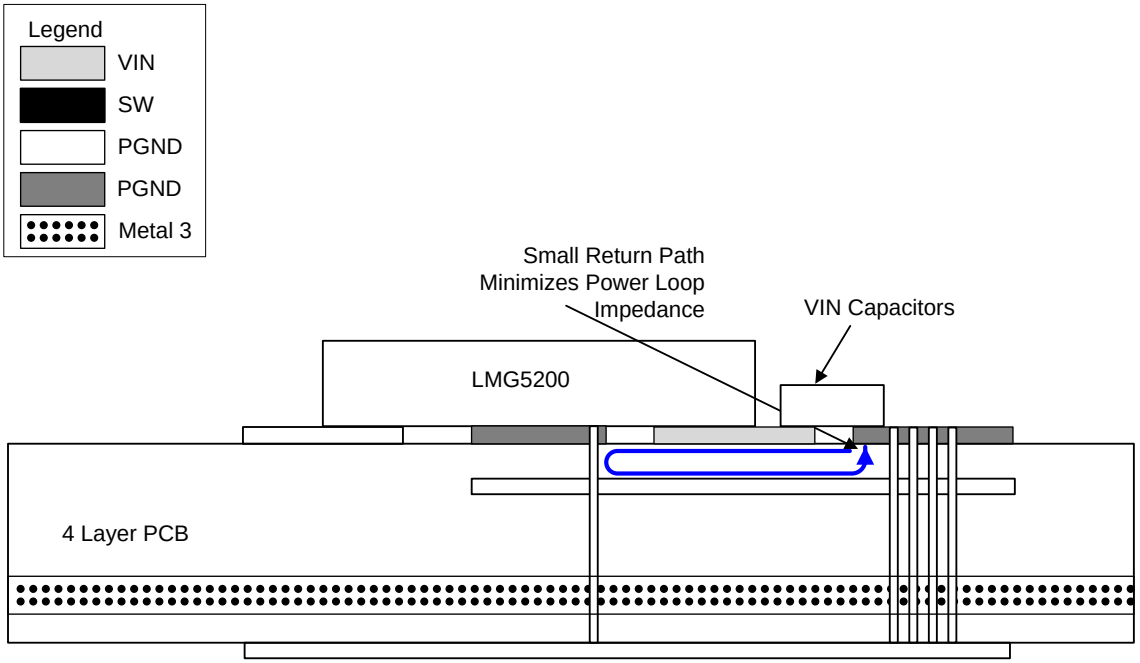


図 15. Four-Layer Board Cross Section With Return Path Directly Underneath for Power Loop

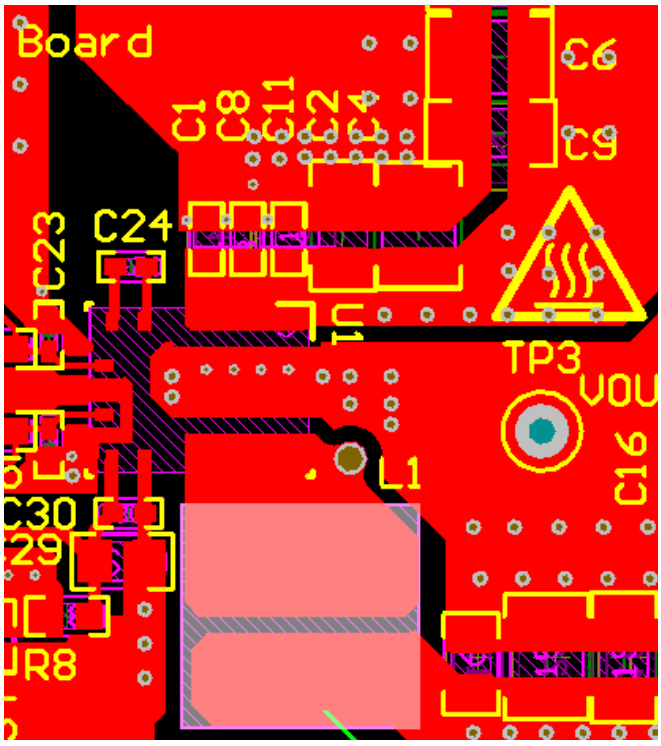


図 16. Top Layer

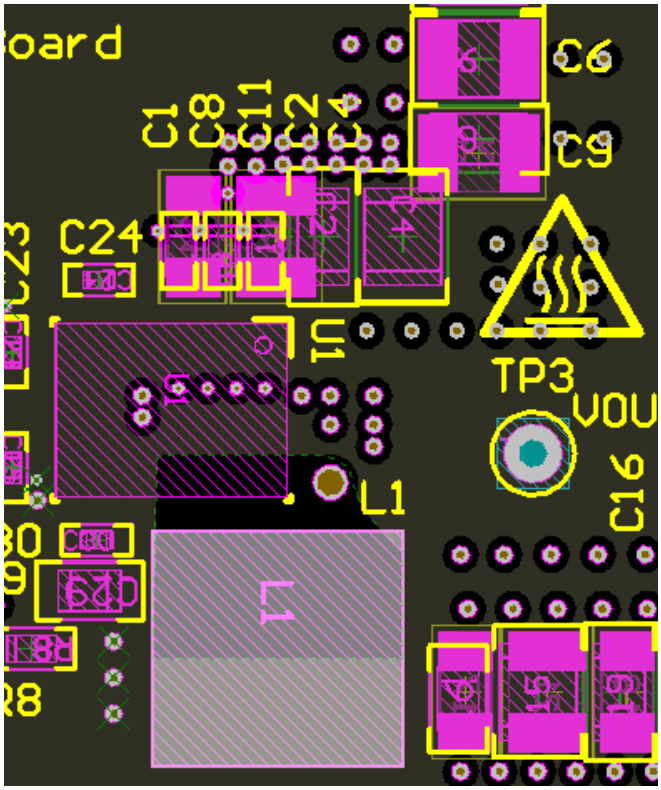


図 17. Ground Plane

Layout Examples (continued)

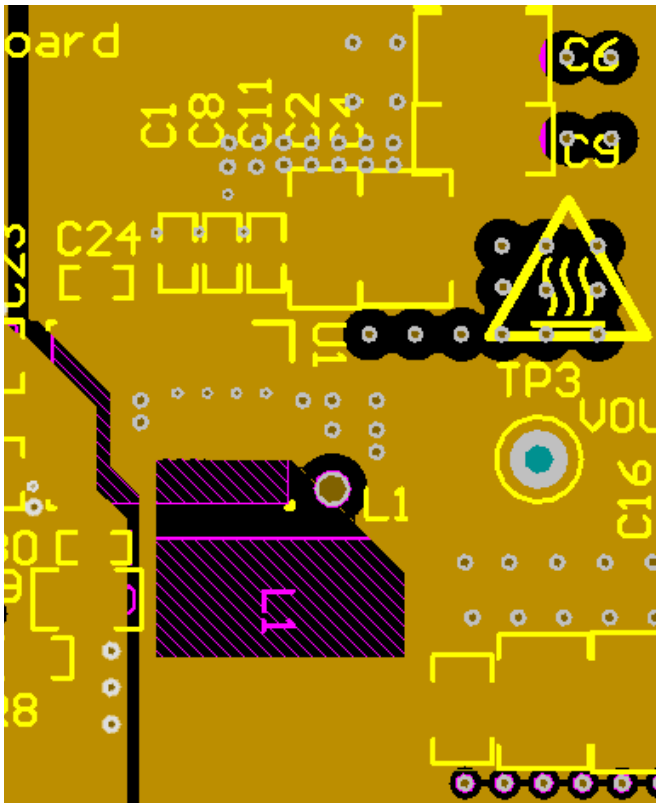


図 18. Middle Layer

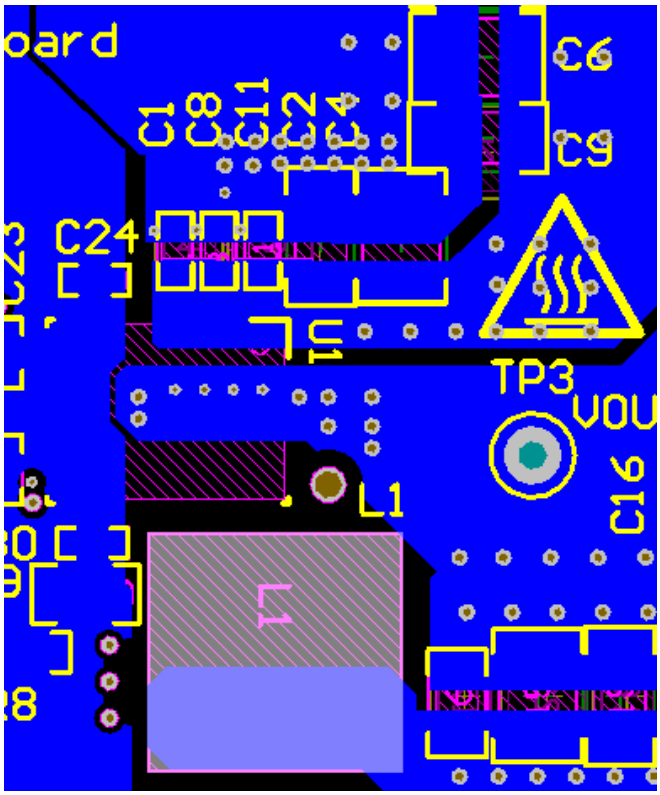


図 19. Bottom Layer

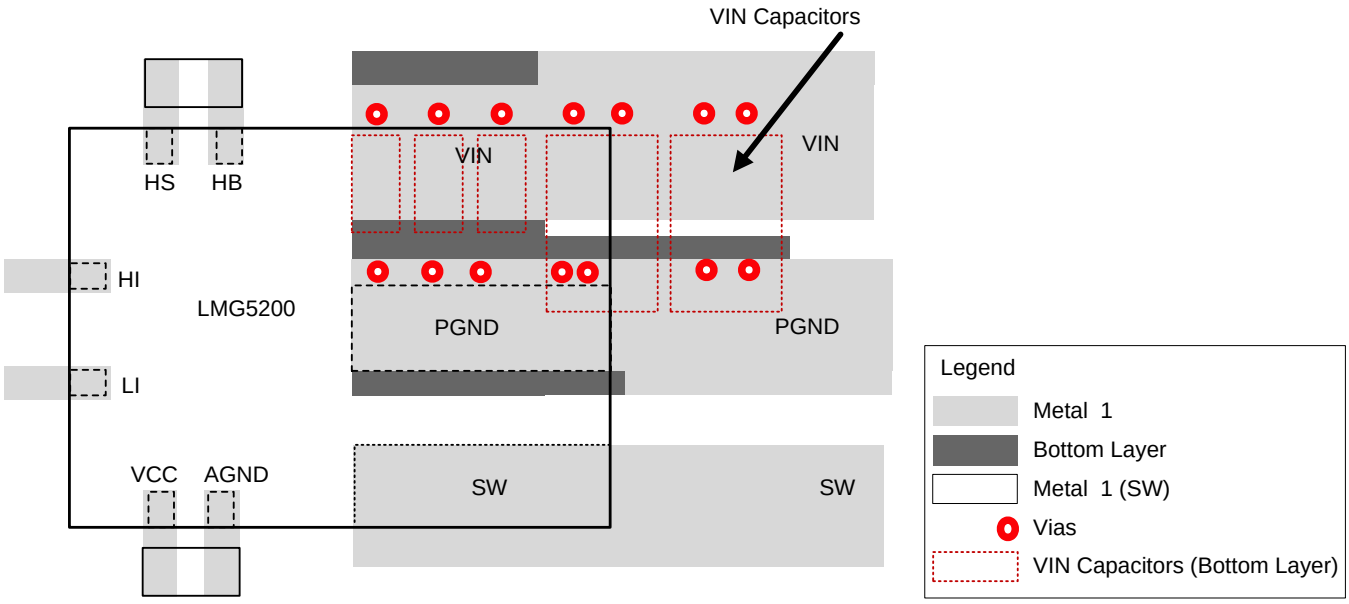


図 20. External Component Placement (Double Layer PCB)

Layout Examples (continued)

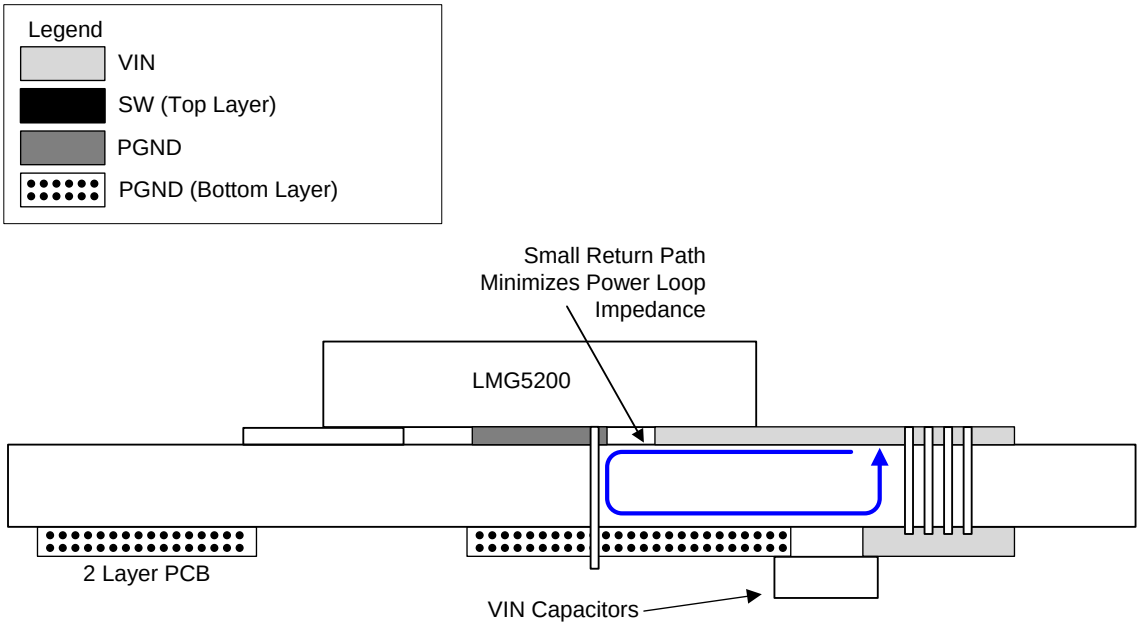


図 21. Two-Layer Board Cross Section With Return Path

Two-layer boards are not recommended for use with LMG5200 device due to the larger power loop inductance. However, if design considerations allow only two board layers, place the input decoupling capacitors immediately behind the device on the back-side of the board to minimize loop inductance. 図 20 and 図 21 show a layout example for two-layer boards.

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

LMG5200 PSpiceトランジェント・モデル

LMG5200 TINA-TIトランジェント・リファレンス・デザイン

LMG5200 TINA-TIトランジェントSpiceモデル

12.2 ドキュメントのサポート

12.2.1 関連資料

『LMG5200 GaN電力ステージ・モジュールのレイアウト・ガイドライン』

『LMG5200の使用法: GaNハーフ・ブリッジ電力モジュール評価モジュール』

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

13.1 パッケージ情報

LMG5200デバイスのパッケージはMSL3パッケージ(湿度感受性レベル3)に分類されています。MSL3パッケージに固有の取り扱いおよび処理の推奨事項については、*『AN-2029　取り扱いおよび処理の推奨事項』*アプリケーション・レポートを参照してください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG5200MOFR	Active	Production	QFM (MOF) | 9	2000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	LMG5200 513B
LMG5200MOFR.A	Active	Production	QFM (MOF) | 9	2000 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	LMG5200 513B
LMG5200MOFT	Active	Production	QFM (MOF) | 9	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	LMG5200 513B
LMG5200MOFT.A	Active	Production	QFM (MOF) | 9	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 125	LMG5200 513B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

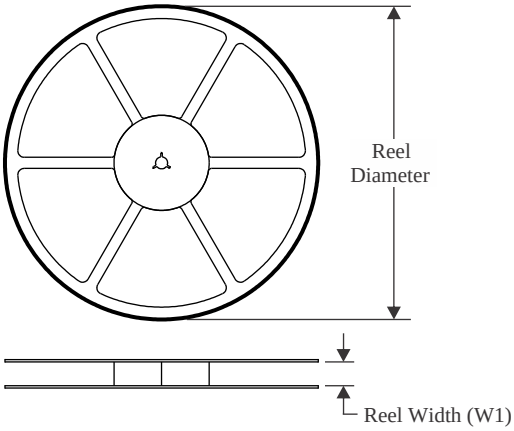
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

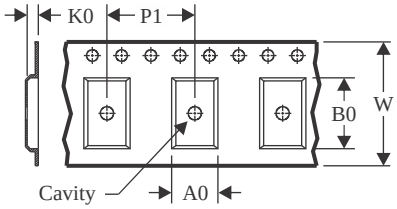
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

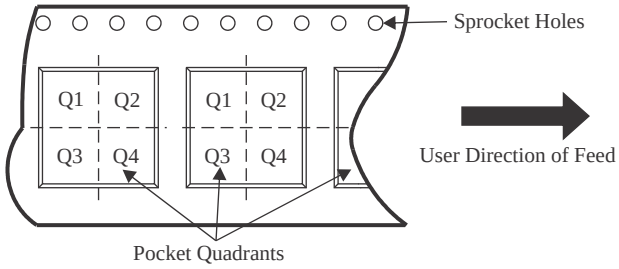


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

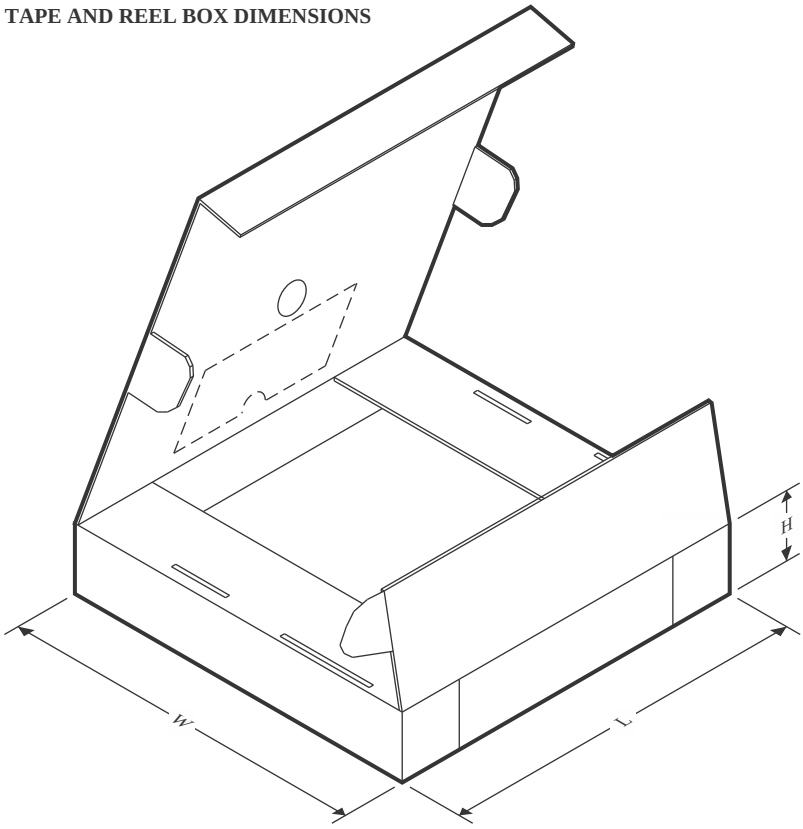
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG5200MOFR	QFM	MOF	9	2000	330.0	16.4	6.3	8.3	2.2	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

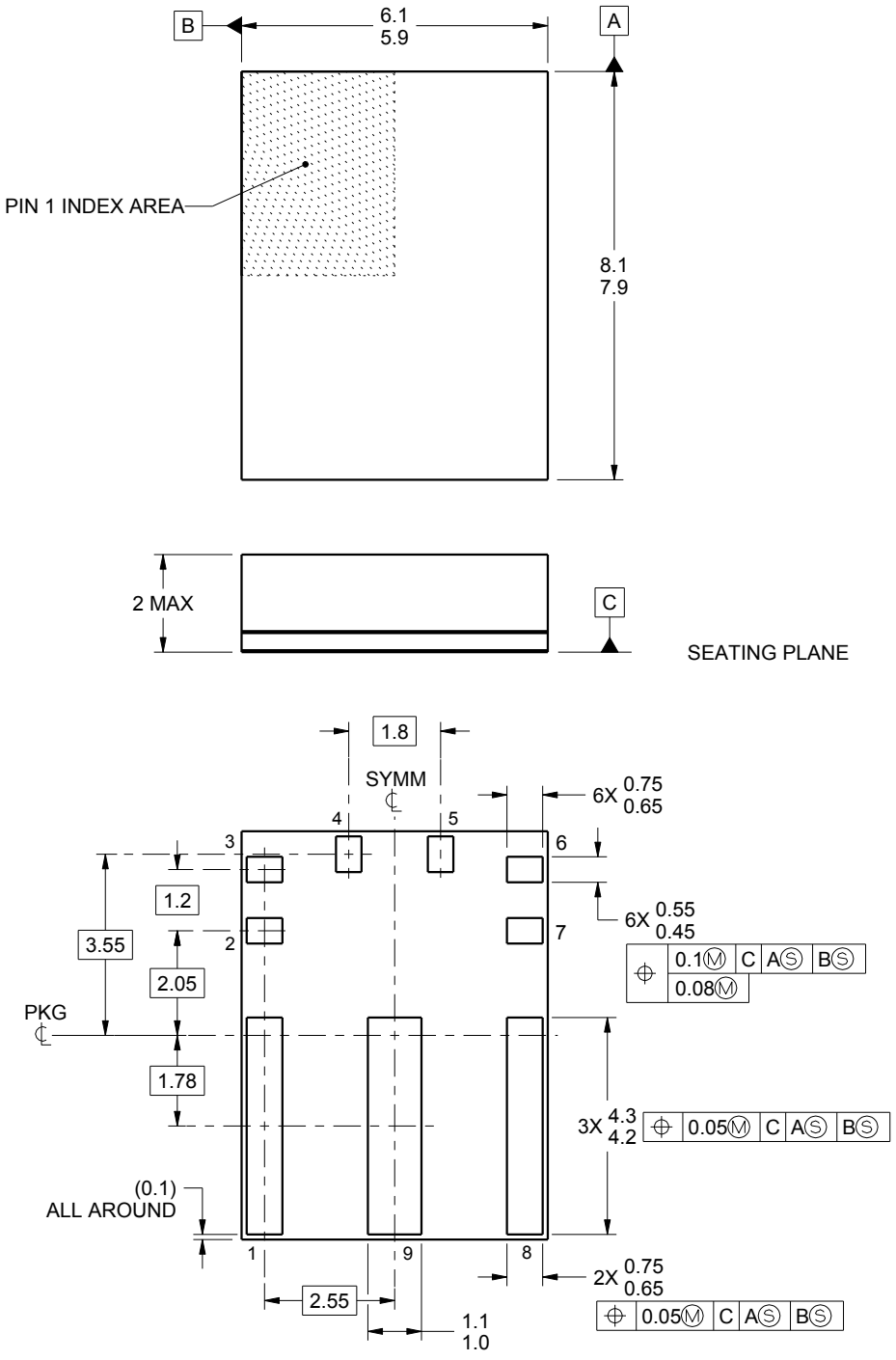
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG5200MOFR	QFM	MOF	9	2000	350.0	350.0	43.0

PACKAGE OUTLINE

MOF0009A

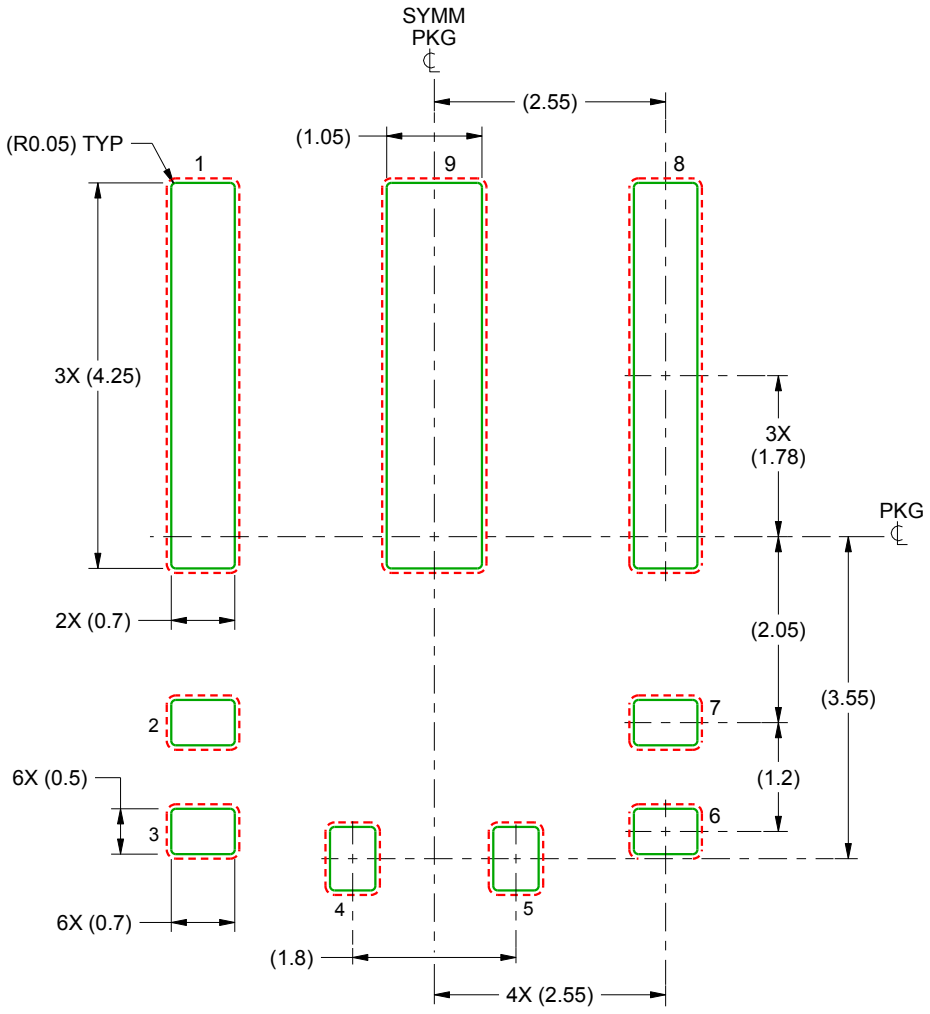
QFM - 2 mm max height

QUAD FLAT MODULE

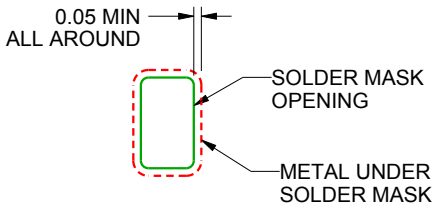


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:12X

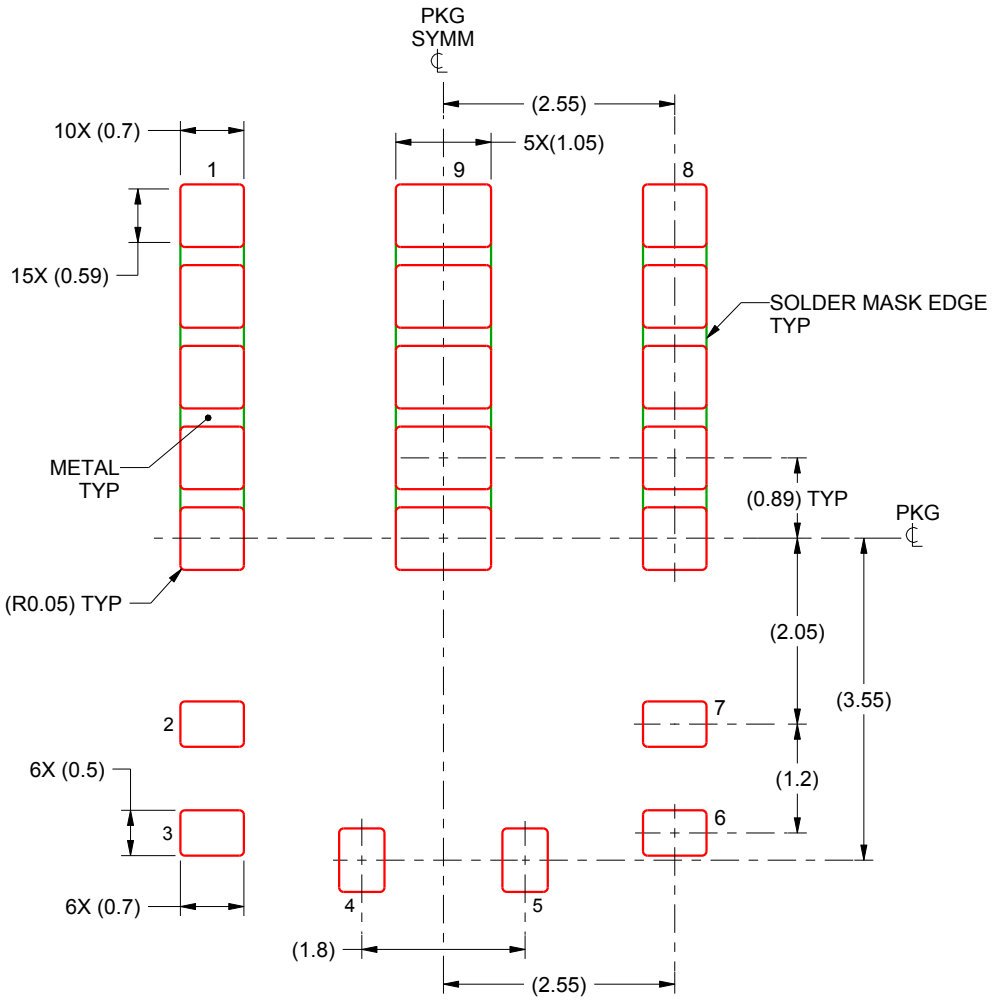


SOLDER MASK DEFINED
ALL PADS

4221487/B 06/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PADS 1, 8 & 9
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4221487/B 06/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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