LMH6321 調整可能な電流制限機能搭載、300mA、高速バッファ

1 特長

- 高いスルーレート:1800V/µs
- 広い帯域幅:110MHz
- 連続出力電流:±300mA
- 出力電流制限値の許容誤差:±5mA、±5%
- 広い電源電圧範囲:5V～±15V
- 広い温度範囲:−40℃～+125℃
- 調整可能な電流制限
- 大きな容量性負荷を駆動可能
- サーマル・シャットダウン・エラー・フラグ

2 アプリケーション

- ライン・ドライバ
- ピン・ドライバ
- ソナー・ドライバ
- モーター制御

3 概要

LMH6321 は、1800V/µs のスルーレートで出力を駆動でき、50Ω 負荷駆動時の小信号帯域幅が 110MHz である高速ユニティ・ゲイン・バッファです。±300mA を連続的に駆動でき、大きな容量性負荷を駆動しても発振しません。

LMH6321 は調整可能な電流制限機能を備えています。電流制限値は、±5mA、±5% の精度で 10mA から 300mA まで連続的に調整できます。この電流制限値は、外部リファレンス電流を抵抗で調整することで設定します。必要に応じて DAC に抵抗を接続して基準電流を作ることで、基準電流を簡単かつ即座に調整できます。ソース電流とシンク電流には同じ電流制限値が適用されます。

LMH6321 は省スペースの 8 ピン SO PowerPAD または 7 ピン DDPAK パワー・パッケージで供給されます。放熱性能を高めるため、SO PowerPAD™ パッケージはパッケージ下面に露出パッドを備えています。LMH6321 は、オペアンプの帰還ループ内で使用して電流出力を増加させることも、スタンドアローンのバッファとして使用することもできます。

表 3-1. 製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LMH6231	SO PowerPAD (8)	1.7mm × 1.27mm
	DDPAK (7)	4.65mm × 1.27mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

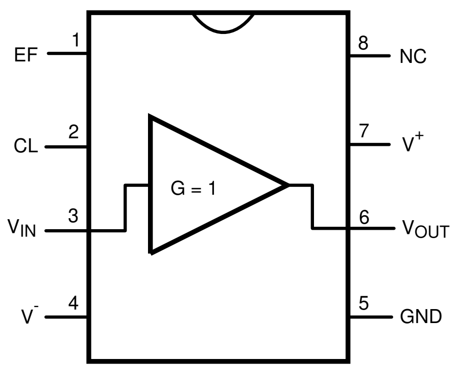
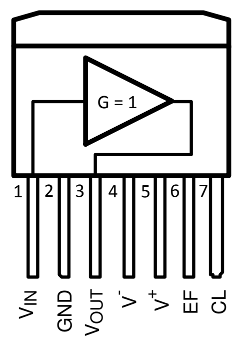


図 3-1. 接続図:8 ピン SO PowerPAD



A. V− ピンは各パッケージの下面のタブに接続されています。

図 3-2. 接続図:7 ピン DDPAK(A)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (March 2013) to Revision D (September 2021) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 1
- 製品情報の表を追加 1
- Removed the Thermal Resistance (θ_{JA}), (θ_{JC}), and SO PowerPAD Package details from the *Operating Ratings* table 3
- Added the *Thermal Information* section 3
- Added the *Device and Documentation Support* sections 24
- Added the *Mechanical, Packaging, and Orderable Information* section 24

Changes from Revision B (March 2013) to Revision C (March 2013) **Page**

- Changed layout of National Data Sheet to TI format 22

5 Specifications

5.1 Absolute Maximum Ratings

See (1) (2)

ESD Tolerance (3)	Human Body Model	2.5 kV
	Machine Model	250 V
Supply Voltage		36 V (±18 V)
Input to Output Voltage (4)		±5 V
Input Voltage		$\pm V_{SUPPLY}$
Output Short-Circuit to GND (5)		Continuous
Storage Temperature Range		−65°C to +150°C
Junction Temperature (T_{JMAX})		+150°C
Lead Temperature (Soldering, 10 seconds)		260°C
Power Dissipation		(6)
C_L Pin to GND Voltage		±1.2 V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics Table.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0 Ω in series with 200 pF.
(4) If the input-output voltage differential exceeds ±5 V, internal clamping diodes will turn on. The current through these diodes should be limited to 5 mA max. Thus for an input voltage of ±15 V and the output shorted to ground, a minimum of 2 kΩ should be placed in series with the input.
(5) The maximum continuous current must be limited to 300 mA. See セクション 6 for more details.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = T_{J(MAX)} – T_A)/\theta_{JA}$. See セクション 6.8 of セクション 6.

5.2 Operating Ratings

Operating Temperature Range	−40°C to +125°C
Operating Supply Range	5 V to ±16 V

5.3 Thermal Information

THERMAL METRIC[1]		LMH6321 DDA SO Power Pad 8 Pins	LMH6321 DDAPAK 7 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.8	21.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.7	6.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.5	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.7	6.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	1.1	°C/W

5.4 ±15 V Electrical Characteristics

The following specifications apply for Supply Voltage = ±15 V, V_{CM} = 0, R_L ≥ 100 kΩ and R_S = 50 Ω, C_L open, unless otherwise noted. *Italicized* limits apply for T_A = T_J = T_{MIN} to T_{MAX}; all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A_V	Voltage Gain	R_L = 1 kΩ, V_{IN} = ±10 V		0.99 *0.98*	0.995		V/V
		R_L = 50 Ω, V_{IN} = ±10 V		0.86 *0.84*	0.92		V/V
V_{OS}	Input Offset Voltage	R_L = 1 kΩ, R_S = 0 V			±4	±35 *±52*	mV
I_B	Input Bias Current	V_{IN} = 0 V, R_L = 1 kΩ, R_S = 0 V			±2	±15 *±17*	µA
$R._{IN}$	Input Resistance	$R._L$ = 50 Ω			250		kΩ
C_{IN}	Input Capacitance				3.5		pF
R_O	Output Resistance	I_O = ±10 mA			5		Ω
I_S	Power Supply Current	R_L = ∞, V_{IN} = 0			11	14.5 *16.5*	mA
			750 µA into C_L Pin		14.9	18.5 *20.5*	
V_O1	Positive Output Swing	I_O = 300 mA, R_S = 0 V, V_{IN} = ±V_S		11.2 *10.8*	11.9		V
	Negative Output Swing	I_O = 300 mA, R_S = 0 V, V_{IN} = ±V_S			−11.3	−10.3 *−9.8*	
V_O2	Positive Output Swing	R_L = 1 kΩ, R_S = 0 V, V_{IN} = ±V_S		13.1 *12.9*	13.4		V
	Negative Output Swing	R_L = 1 kΩ, R_S = 0 V, V_{IN} = ±V_S			−13.4	−12.9 *−12.6*	
V_O3	Positive Output Swing	R_L = 50 Ω, R_S = 0 V, V_{IN} = ±V_S		11.6 *11.2*	12.2		V
	Negative Output Swing	R_L = 50 Ω, R_S = 0 V, V_{IN} = ±V_S			−11.9	−10.9 *−10.6*	
V_{EF}	Error Flag Output Voltage	R_L = ∞, V_{IN} = 0, EF pulled up with 5 kΩ to +5 V	Normal		5.00		V
			During Thermal Shutdown		0.25		
T_{SH}	Thermal Shutdown Temperature	Measure Quantity is Die (Junction) Temperature			168		°C
		Hysteresis			10		
I_{SH}	Supply Current at Thermal Shutdown	EF pulled up with 5 kΩ to +5 V			3		mA
PSSR	Power Supply Rejection Ratio	R_L = 1 kΩ, V_{IN} = 0 V, V_S = ±5 V to ±15 V	Positive	58 *54*	66		dB
			Negative	58 *54*	64		
SR	Slew Rate	V_{IN} = ±11 V, R_L = 1 kΩ			2900		V/µs
		V_{IN} = ±11 V, R_L = 50 Ω			1800		
BW	−3 dB Bandwidth	V_{IN} = ±20 mV_{PP}, R_L = 50 Ω			110		MHz
LSBW	Large Signal Bandwidth	V_{IN} = 2 V_{PP}, R_L = 50 Ω			48		MHz
HD2	2^{nd} Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz	R_L = 50 Ω		−59		dBc
			R_L = 100 Ω		−70		
		V_O = 2 V_{PP}, f = 1 MHz	R_L = 50 Ω		−57		
			R_L = 100 Ω		−68		

5.4 ±15 V Electrical Characteristics (continued)

The following specifications apply for Supply Voltage = ±15 V, V_{CM} = 0, R_L ≥ 100 kΩ and R_S = 50 Ω, C_L open, unless otherwise noted. *Italicized* limits apply for T_A = T_J = T_{MIN} to T_{MAX}; all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
HD3	3rd Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz	R_L = 50 Ω		−59		dBc
			R_L = 100 Ω		−70		
		V_O = 2 V_{PP}, f = 1 MHz	R_L = 50 Ω		−62		
			R_L = 100 Ω		−73		
e_n	Input Voltage Noise	f ≥ 10 kHz			2.8		nV/√Hz
i_n	Input Current Noise	f ≥ 10 kHz			2.4		pA/√Hz
$I_{SC}1$	Output Short Circuit Current Source [(1)]	V_O = 0 V, Program Current into C_L = 25 µA	Sourcing V_{IN} = +3 V	4.5 *4.5*	10	15.5 *15.5*	mA
			Sinking V_{IN} = −3 V	4.5 *4.5*	10	15.5 *15.5*	
		V_O = 0 V Program Current into C_L = 750 µA	Sourcing V_{IN} = +3 V	280 *273*	295	308 *325*	mA
			Sinking V_{IN} = −3 V	280 *275*	295	310 *325*	
$I_{SC}2$	Output Short Circuit Current Source	R_S = 0 V, V_{IN} = +3 V[(1)] [(2)]		320 *300*	570	750 *920*	mA
	Output Short Circuit Current Sink	R_S = 0 V, V_{IN} = −3 V[(1)] [(2)]		300 *305*	515	750 *910*	
V/I Section							
CLV_{OS}	Current Limit Input Offset Voltage	R_L = 1 kΩ, GND = 0 V			±0.5	±4.0 *±8.0*	mV
CLI_B	Current Limit Input Bias Current	R_L = 1 kΩ		−0.5 *−0.8*	−0.2		µA
CL CMRR	Current Limit Common Mode Rejection Ratio	R_L = 1 kΩ, GND = −13 to +14 V		60 *56*	69		dB

(1) V_{IN} = + or −4 V at T_J = −40°C.
(2) For the condition where the C_L pin is left open the output current should not be continuous, but instead, should be limited to low duty cycle pulse mode such that the RMS output current is less than or equal to 300 mA.

5.5 ±5 V Electrical Characteristics

The following specifications apply for Supply Voltage = ±5 V, V_{CM} = 0, R_L ≥ 100 kΩ and R_S = 50 Ω, C_L Open, unless otherwise noted. *Italicized* limits apply for T_A = T_J = T_{MIN} to T_{MAX}; all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A_V	Voltage Gain	R_L = 1 kΩ, V_{IN} = ±3 V		0.99 *0.98*	0.994		V/V
		R_L = 50 Ω, V_{IN} = ±3 V		0.86 *0.84*	0.92		
V_{OS}	Offset Voltage	R_L = 1 kΩ, R_S = 0 V			±2.5	±35 *±50*	mV
I_B	Input Bias Current	V_{IN} = 0 V, R_L = 1 kΩ, R_S = 0 V			±2	±15 *±17*	µA
R_{IN}	Input Resistance	R_L = 50 Ω			250		kΩ
C_{IN}	Input Capacitance				3.5		pF
R_O	Output Resistance	I_{OUT} = ±10 mA			5		Ω
I_S	Power Supply Current	R_L = ∞, V_{IN} = 0 V			10	13.5 *14.7*	mA
			750 µA into CL Pin		14	17.5 *19.5*	

5.5 ±5 V Electrical Characteristics (continued)

The following specifications apply for Supply Voltage = ±5 V, V_{CM} = 0, R_L ≥ 100 kΩ and R_S = 50 Ω, C_L Open, unless otherwise noted. *Italicized* limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_O1	Positive Output Swing	I_O = 300 mA, R_S = 0 V, V_{IN} = ±V_S		1.3 *0.9*	1.9		V
	Negative Output Swing	I_O = 300 mA, R_S = 0 V, V_{IN} = ±V_S			−1.3	−0.5 *−0.1*	
V_O2	Positive Output Swing	R_L = 1 kΩ, R_S = 0 V, V_{IN} = ±V_S		3.2 *2.9*	3.5		V
	Negative Output Swing	R_L = 1 kΩ, R_S = 0 V, V_{IN} = ±V_S			−3.5	−3.1 *−2.9*	V
V_O3	Positive Output Swing	R_L = 50 Ω, R_S = 0 V, V_{IN} = ±V_S		2.8 *2.5*	3.1		V
	Negative Output Swing	R_L = 50 Ω, R_S = 0 V, V_{IN} = ±V_S			−3.0	−2.6 *−2.4*	V
PSSR	Power Supply Rejection Ratio	R_L = 1 kΩ, V_{IN} = 0, V_S = ±5 V to ±15 V	Positive	58 *54*	66		dB
			Negative	58 *54*	64		
$I_{SC}1$	Output Short Circuit Current	V_O = 0 V, Program Current into C_L = 25 µA	Sourcing V_{IN} = +3 V	4.5 *4.5*	9	14.0 *15.5*	mA
			Sinking V_{IN} = −3 V	4.5 *4.5*	9	14.0 *15.5*	
		V_O = 0 V, Program Current into C_L = 750 µA	Sourcing V_{IN} = +3 V	275 *270*	290	305 *320*	
			Sinking V_{IN} = −3 V	275 *270*	290	310 *320*	
$I_{SC}2$	Output Short Circuit Current Source	R_S = 0 V, V_{IN} = +3 V [1] [2]		300	470		mA
	Output Short Circuit Current Sink	R_S = 0 V, V_{IN} = −3 V [1] [2]		300	400		
SR	Slew Rate	V_{IN} = ±2 V_{PP}, R_L = 1 kΩ			450		V/µs
		V_{IN} = ±2 V_{PP}, R_L = 50 Ω			210		
BW	−3 dB Bandwidth	V_{IN} = ±20 mV_{PP}, R_L = 50 Ω			90		MHz
LSBW	Large Signal Bandwidth	V_{IN} = 2 V_{PP}, R_L = 50 Ω			39		MHz
T_{SD}	Thermal Shutdown	Temperature			170		°C
		Hysteresis			10		
V/I Section							
CLV_{OS}	Current Limit Input Offset Voltage	R_L = 1 kΩ, GND = 0 V			2.7	+5 *±5.0*	mV
CLI_B	Current Limit Input Bias Current	R_L = 1 kΩ, C_L = 0 V		−0.5 *−0.6*	−0.2		µA
CL CMRR	Current Limit Common Mode Rejection Ratio	R_L = 1 kΩ, GND = −3 V to +4 V		60 *56*	65		dB

1. V_{IN} = + or −4 V at T_J = −40°C.
2. For the condition where the C_L pin is left open the output current should not be continuous, but instead, should be limited to low duty cycle pulse mode such that the RMS output current is less than or equal to 300 mA.

5.6 Typical Characteristics

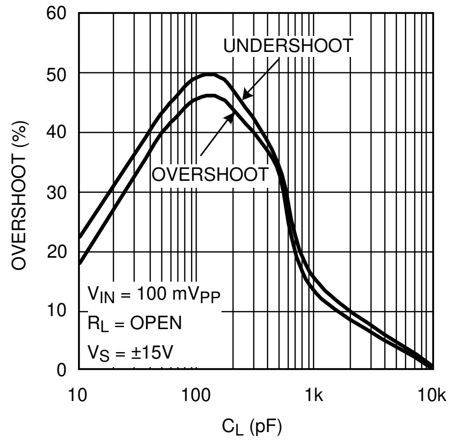


図 5-1. Overshoot vs. Capacitive Load

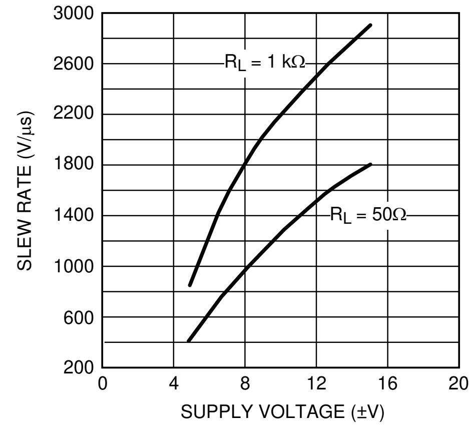


図 5-2. Slew Rate

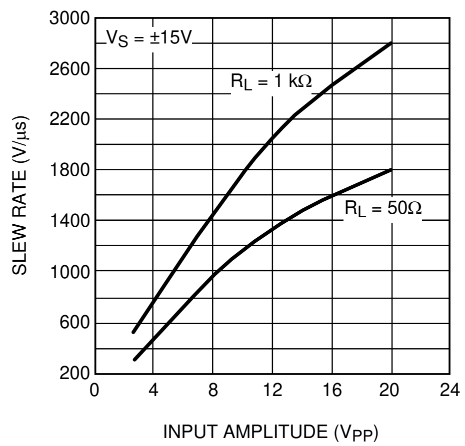


図 5-3. Slew Rate

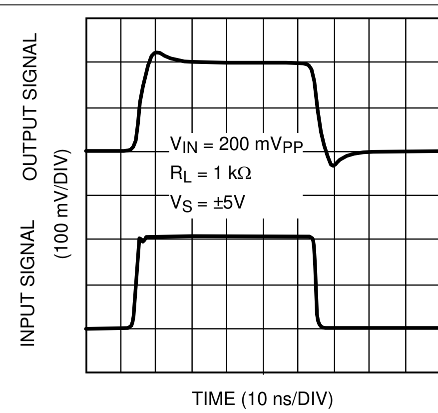


図 5-4. Small Signal Step Response

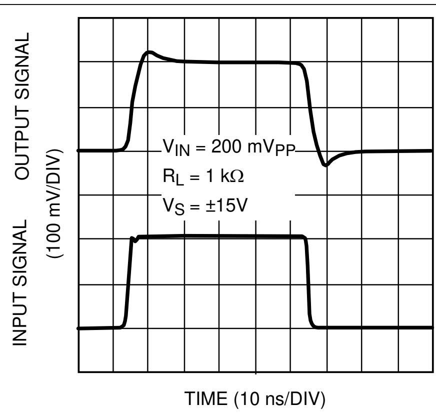


図 5-5. Small Signal Step Response

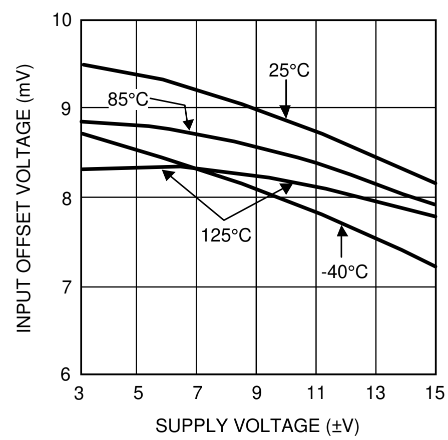


図 5-6. Input Offset Voltage of Amplifier vs. Supply Voltage

5.6 Typical Characteristics (continued)

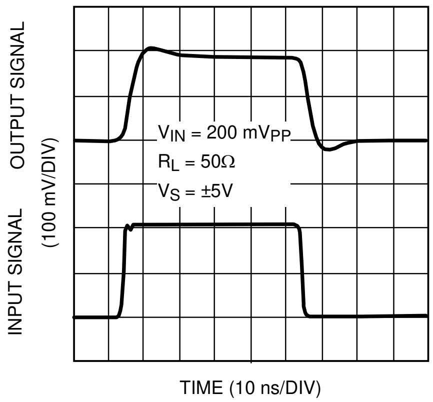


図 5-7. Small Signal Step Response

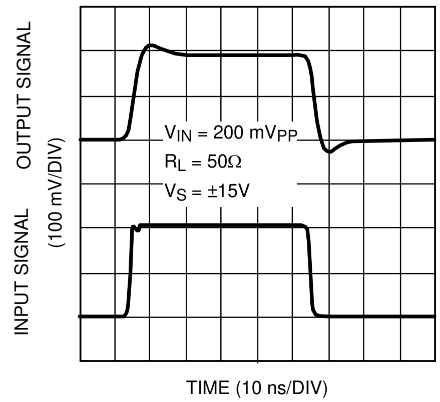


図 5-8. Small Signal Step Response

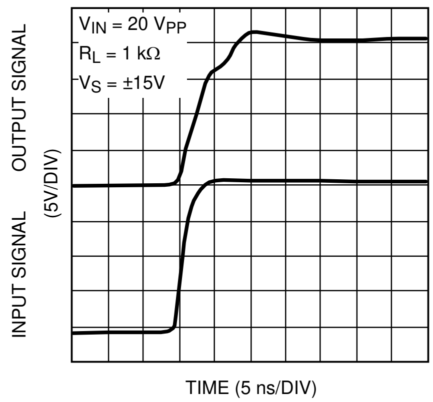


図 5-9. Large Signal Step Response—Leading Edge

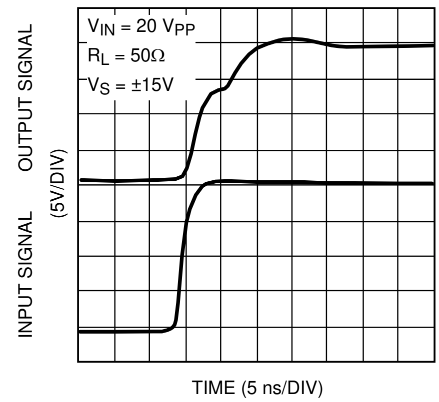


図 5-10. Large Signal Step Response — Leading Edge

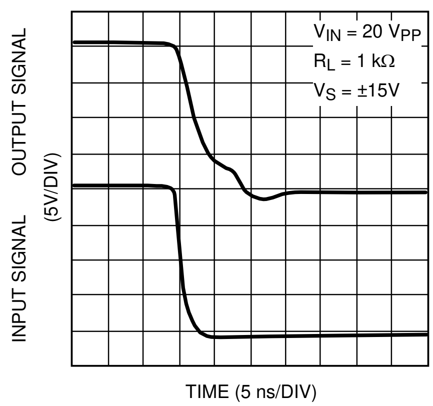


図 5-11. Large Signal Step Response — Trailing Edge

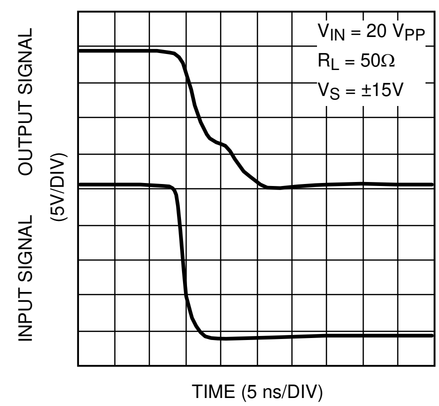


図 5-12. Large Signal Step Response — Trailing Edge

5.6 Typical Characteristics (continued)

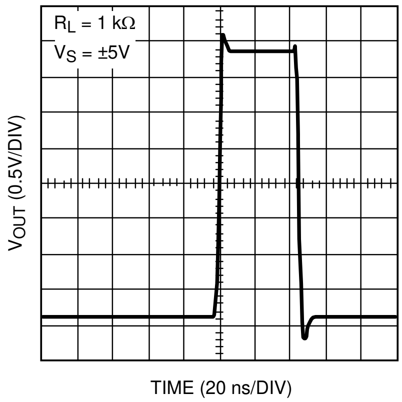


図 5-13. Large Signal Step Response

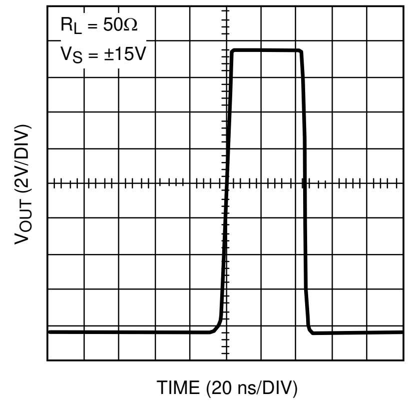


図 5-14. Large Signal Step Response

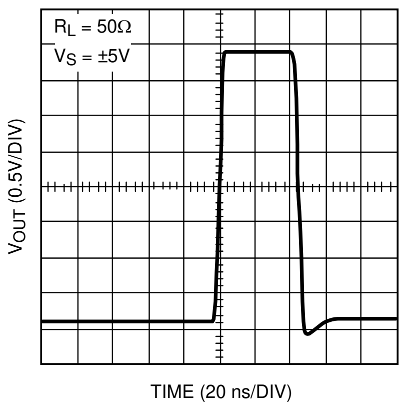


図 5-15. Large Signal Step Response

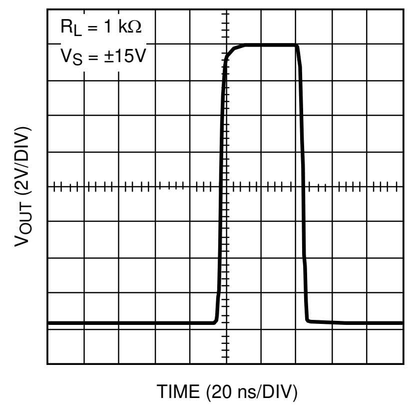


図 5-16. Large Signal Step Response

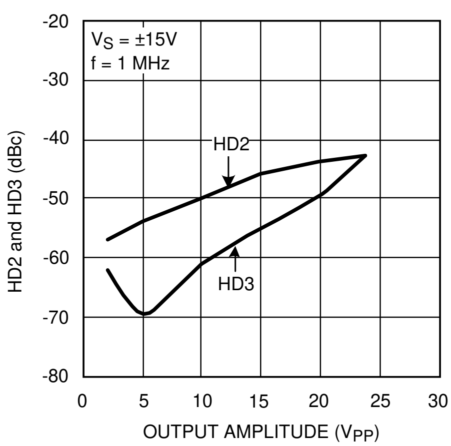


図 5-17. Harmonic Distortion with 50 Ω Load

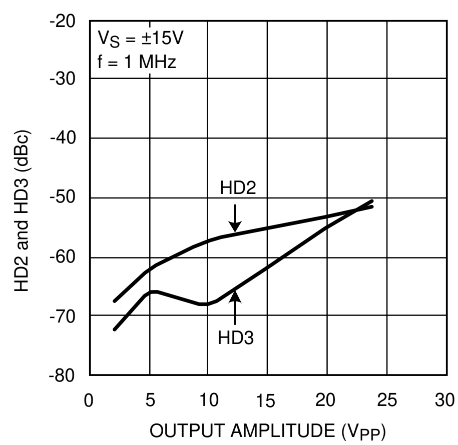


図 5-18. Harmonic Distortion with 100 Ω Load

5.6 Typical Characteristics (continued)

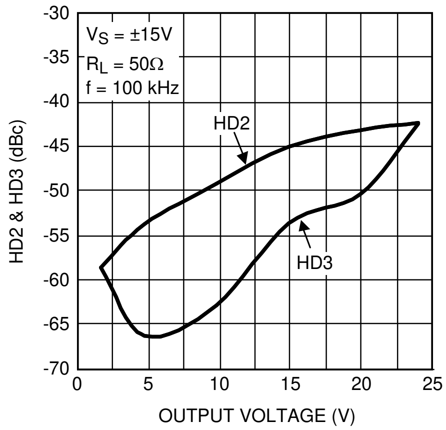


図 5-19. Harmonic Distortion with 50 Ω Load

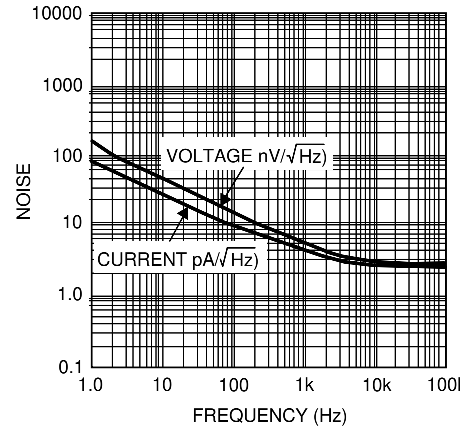


図 5-20. Noise vs. Frequency

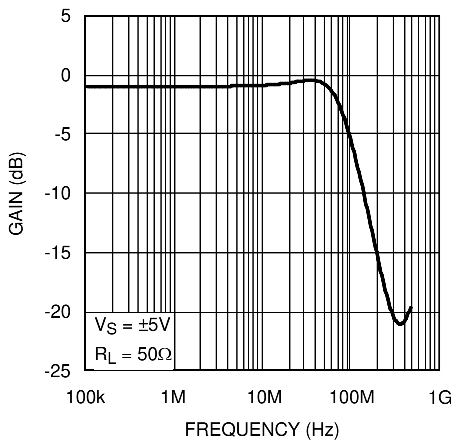


図 5-21. Gain vs. Frequency

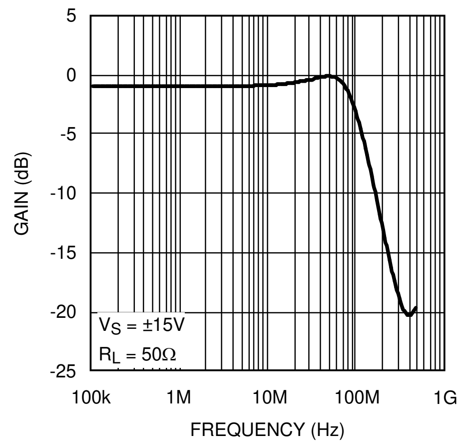


図 5-22. Gain vs. Frequency

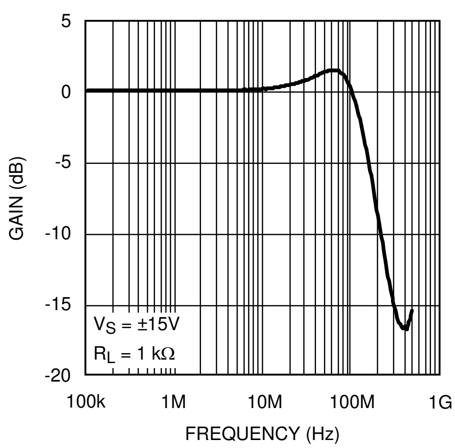


図 5-23. Gain vs. Frequency

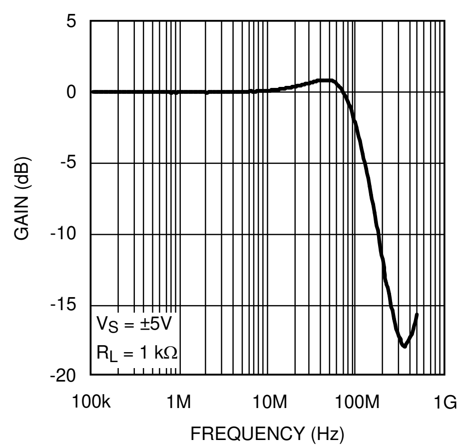


図 5-24. Gain vs. Frequency

5.6 Typical Characteristics (continued)

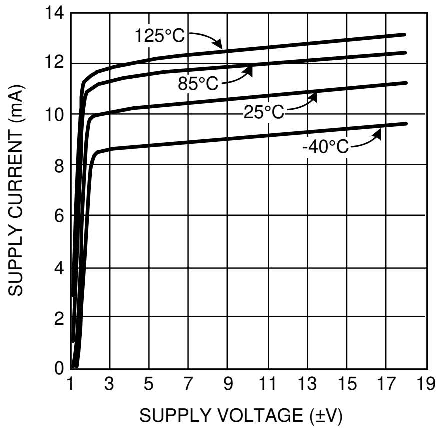


図 5-25. Supply Current vs. Supply Voltage

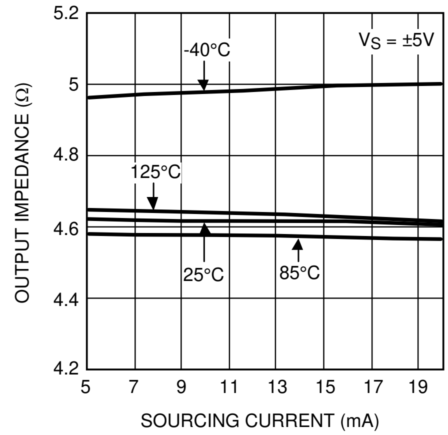


図 5-26. Output Impedance vs. Sourcing Current

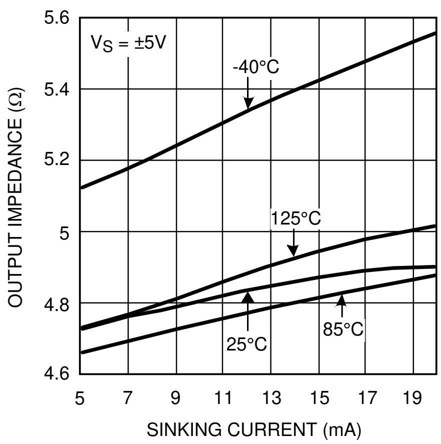


図 5-27. Output Impedance vs. Sinking Current

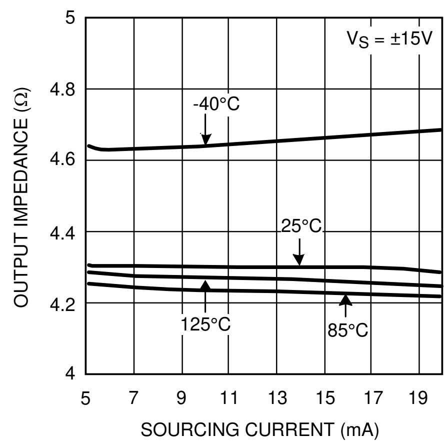


図 5-28. Output Impedance vs. Sourcing Current

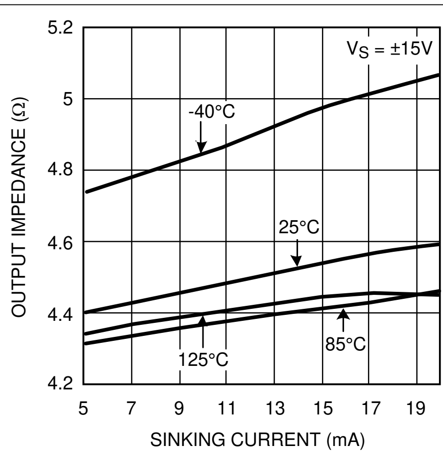


図 5-29. Output Impedance vs. Sinking Current

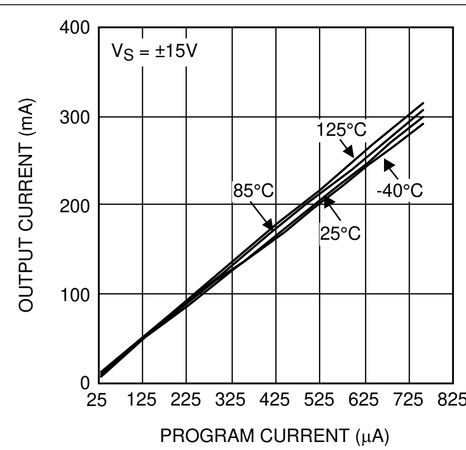


図 5-30. Output Short Circuit Current — Sourcing vs. Program Current

5.6 Typical Characteristics (continued)

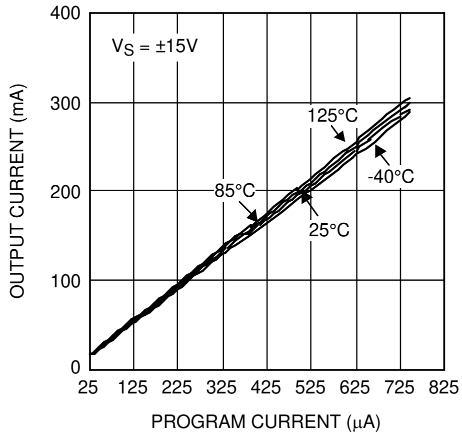


図 5-31. Output Short Circuit Current — Sinking vs. Program Current

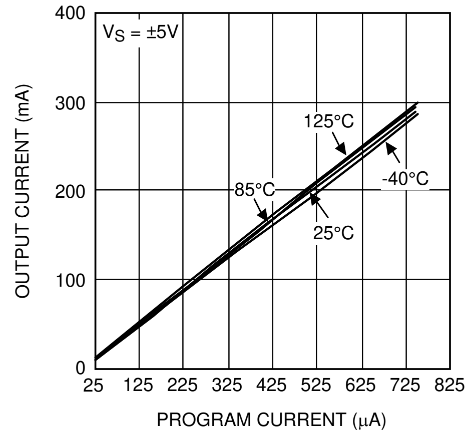


図 5-32. Output Short Circuit Current — Sourcing vs. Program Current

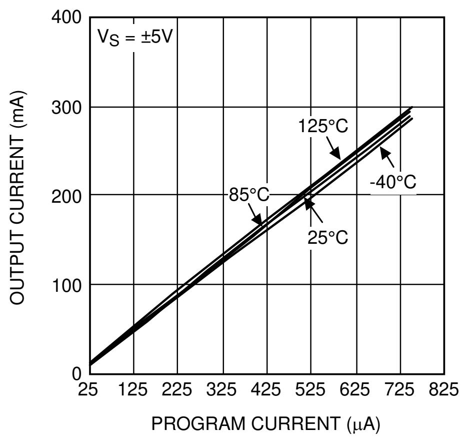


図 5-33. Output Short Circuit Current — Sinking vs. Program Current

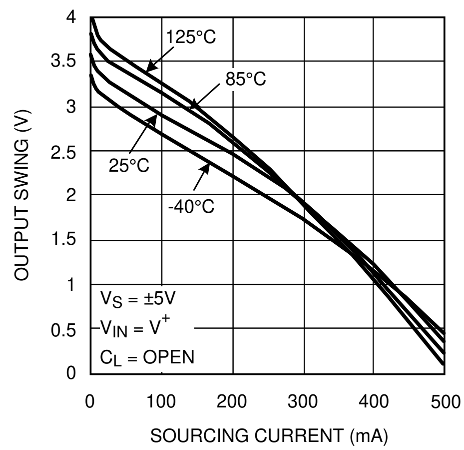


図 5-34. Positive Output Swing vs. Sourcing Current

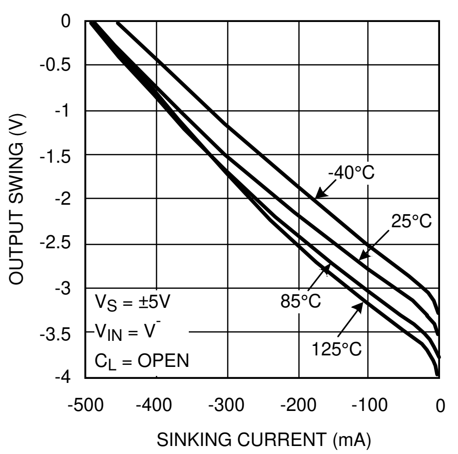


図 5-35. Negative Output Swing vs. Sinking Current

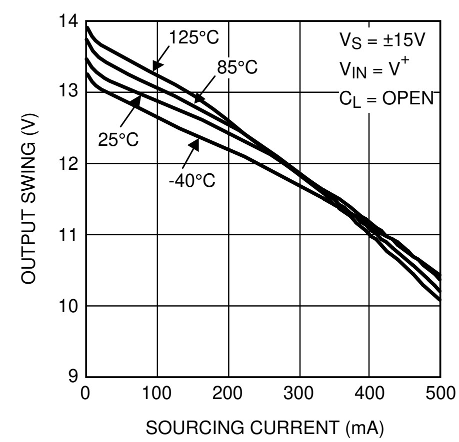


図 5-36. Positive Output Swing vs. Sourcing Current

5.6 Typical Characteristics (continued)

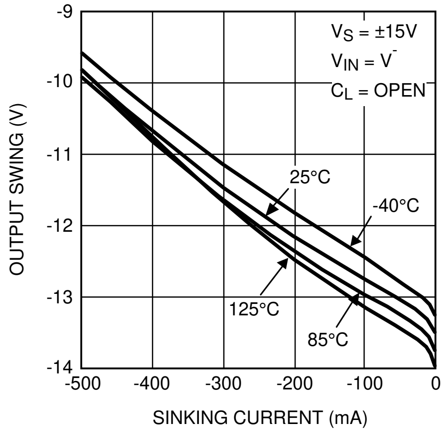


図 5-37. Negative Output Swing vs. Sinking Current

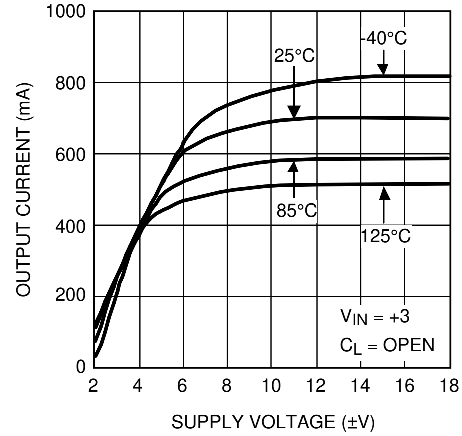


図 5-38. Output Short Circuit Current — Sourcing vs. Supply Voltage

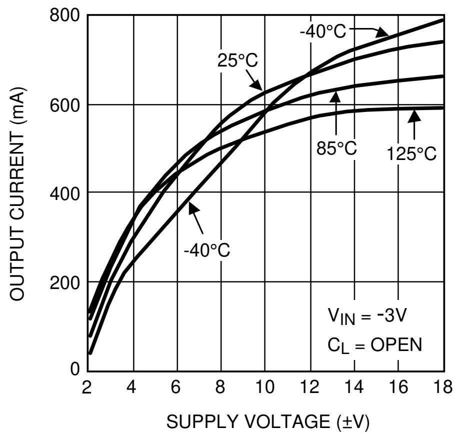


図 5-39. Output Short Circuit Current — Sinking vs. Supply Voltage

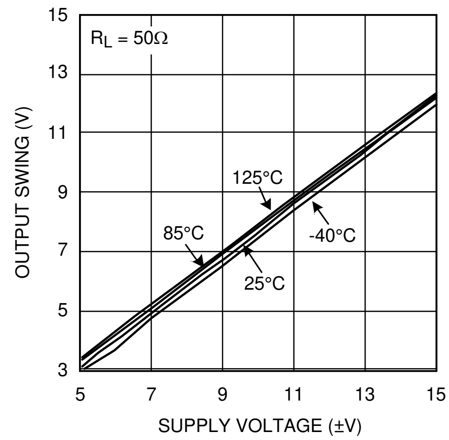


図 5-40. Positive Output Swing vs. Supply Voltage

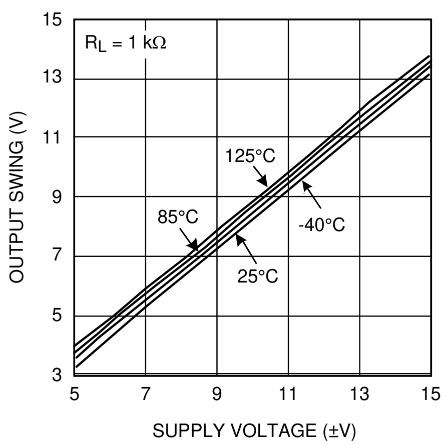


図 5-41. Positive Output Swing vs. Supply Voltage

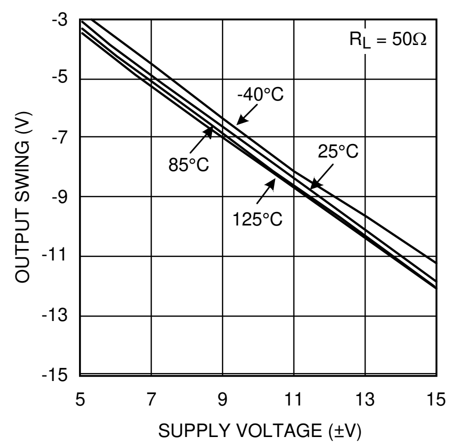


図 5-42. Negative Output Swing vs. Supply Voltage

5.6 Typical Characteristics (continued)

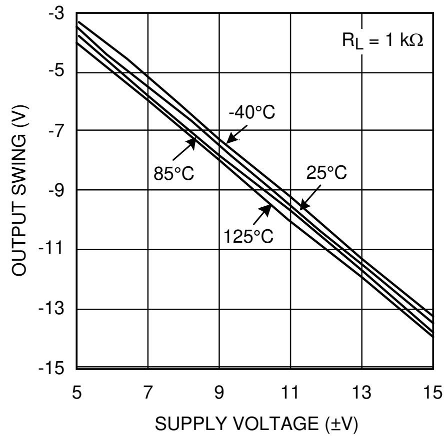


図 5-43. Negative Output Swing vs. Supply Voltage

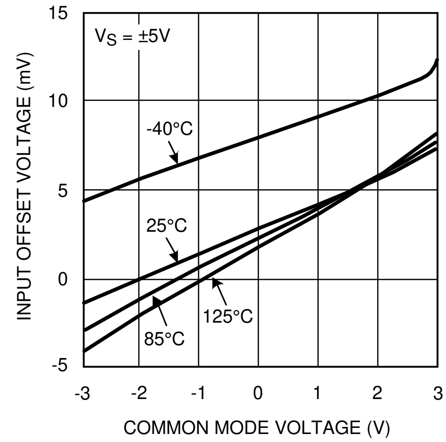


図 5-44. Input Offset Voltage of Amplifier vs. Common Mode Voltage

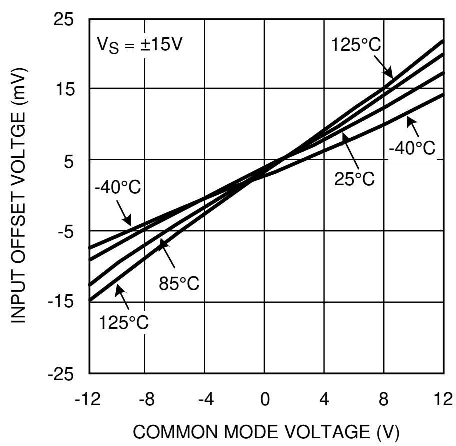


図 5-45. Input Offset Voltage of Amplifier vs. Common Mode Voltage

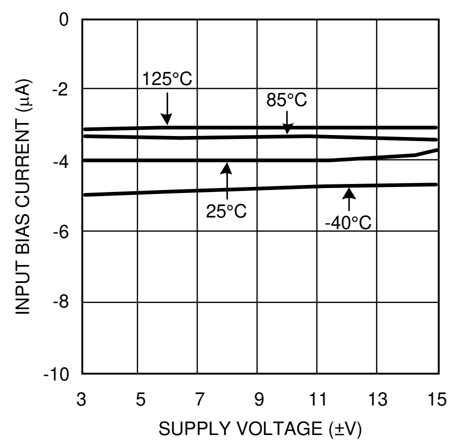


図 5-46. Input Bias Current of Amplifier vs. Supply Voltage

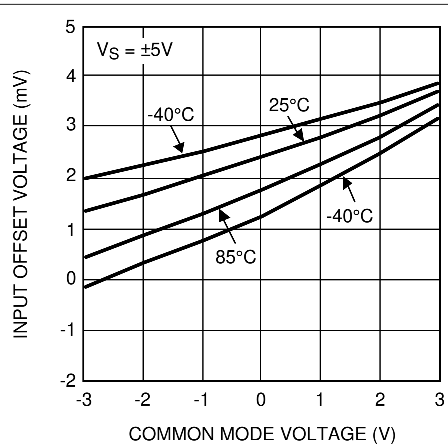


図 5-47. Input Offset Voltage of V/I Section vs. Common Mode Voltage

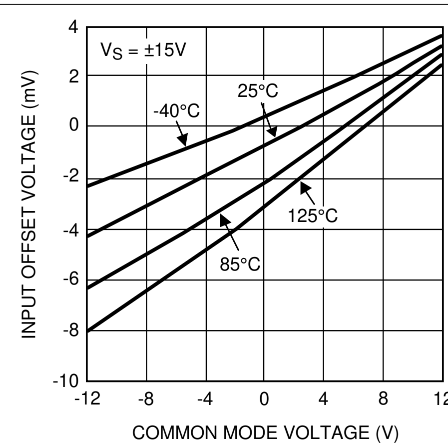


図 5-48. Input Offset Voltage of V/I Section vs. Common Mode Voltage

6 Application Hints

6.1 Buffers

Buffers are often called voltage followers because they have largely unity voltage gain, thus the name has generally come to mean a device that supplies current gain but no voltage gain. Buffers serve in applications requiring isolation of source and load, for example, high input impedance and low output impedance (high output current drive). In addition, they offer gain flatness and wide bandwidth.

Most operational amplifiers that meet the other given requirements in a particular application can be configured as buffers, though they are generally more complex and are, for the most part, not optimized for unity gain operation. The commercial buffer is a cost effective substitute for an op amp. Buffers serve several useful functions, either in tandem with op amps or in standalone applications. As mentioned, their primary function is to isolate a high impedance source from a low impedance load, since a high Z source cannott supply the needed current to the load. For example, in the case where the signal source to an analog to digital converter is a sensor, it is recommended that the sensor be isolated from the A/D converter. The use of a buffer ensures a low output impedance and delivery of a stable output to the converter. In A/D converter applications buffers need to drive varying and complex reactive loads.

Buffers come in two flavors: Open Loop and Closed Loop. While sacrificing the precision of some DC characteristics, and generally displaying poorer gain linearity, open loop buffers offer lower cost and increased bandwidth, along with less phase shift and propagation delay than do closed loop buffers. The LMH6321 is of the open loop variety.

図 6-1 shows a simplified diagram of the LMH6321 topology, revealing the open loop complementary follower design approach. 図 6-2 shows the LMH6321 in a typical application, in this case, a 50 Ω coaxial cable driver.

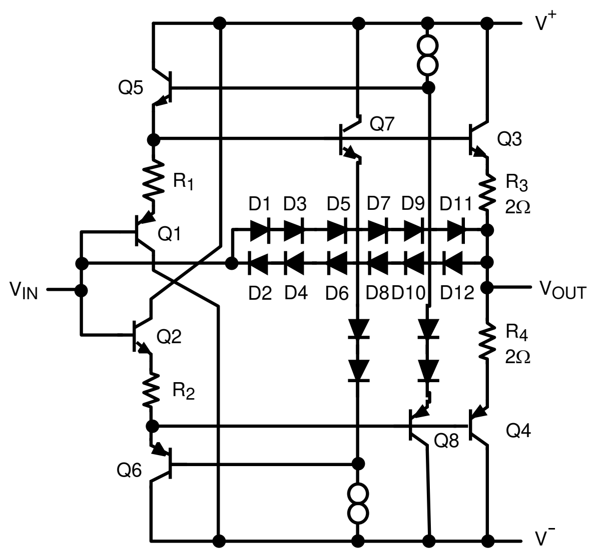


図 6-1. Simplified Schematic

6.2 Supply Bypassing

The method of supply bypassing is not critical for frequency stability of the buffer, and, for light loads, capacitor values in the neighborhood of 1 nF to 10 nF are adequate. However, under fast slewing and large loads, large transient currents are demanded of the power supplies, and when combined with any significant wiring inductance, these currents can produce voltage transients. For example, the LMH6321 can slew typically at 1000 V/µs. Therefore, under a 50 Ω load condition the load can demand current at a rate, di/dt, of 20 A/µs. This current flowing in an inductance of 50 nH (approximately 1.5” of 22 gauge wire) will produce a 1 V transient. Thus, it is recommended that solid tantalum capacitors of 5 µF to 10 µF, in parallel with a ceramic 0.1 µF capacitor be added as close as possible to the device supply pins.

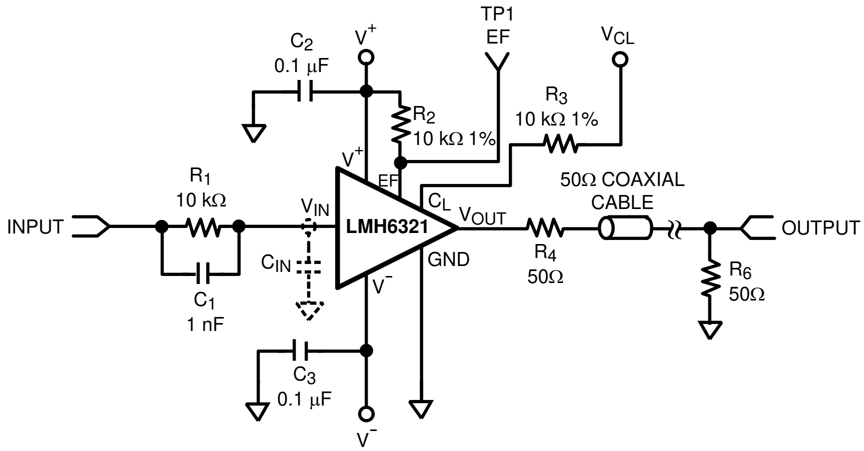


図 6-2. 50 Ω Coaxial Cable Driver with Dual Supplies

For values of capacitors in the 10 µF to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of their very low ESR (typically less than 10 MΩ) and low ESL.

6.3 Load Impedence

The LMH6321 is stable under any capacitive load when driven by a 50 Ω source. As shown by 図 5-1 in セクション 5.6, worst case overshoot is for a purely capacitive load of about 1 nF. Shunting the load capacitance with a resistor will reduce the overshoot.

6.4 Source Inductance

Like any high frequency buffer, the LMH6321 can oscillate with high values of source inductance. The worst case condition occurs with no input resistor, and a purely capacitive load of 50 pF, where up to 100 nH of source inductance can be tolerated. With a 50 Ω load, this goes up to 200 nH. However, a 100 Ω resistor placed in series with the buffer input will ensure stability with a source inductances up to 400 nH with any load.

6.5 Overvoltage Protection

(Refer to the simplified schematic in 図 6-1).

If the input-to-output differential voltage were allowed to exceed the Absolute Maximum Rating of 5 V, an internal diode clamp would turn on and divert the current around the compound emitter followers of Q1/Q3 (D1 – D11 for positive input), or around Q2/Q4 (D2 – D12 for negative inputs). Without this clamp, the input transistors Q1 – Q4 would zener, thereby damaging the buffer.

To limit the current through this clamp, a series resistor should be added to the buffer input (see R_1 in 図 6-2). Although the allowed current in the clamp can be as high as 5 mA, which would suggest a 2 kΩ resistor from a 15 V source, it is recommended that the current be limited to about 1 mA, hence the 10 kΩ shown.

The reason for this larger resistor is explained in the following: One way that the input or output voltage differential can exceed the Absolute Maximum value is under a short circuit condition to ground while driving the input with up to ±15 V. However, in the LMH6321 the maximum output current is set by the programmable Current Limit pin (C_L). The value set by this pin is specified to be accurate to 5 mA ±5%. If the input/output differential exceeds 5 V while the output is trying to supply the maximum set current to a shorted condition or to a very low resistance load, a portion of that current will flow through the clamp diodes, thus creating an error in the total load current. If the input resistor is too low, the error current can exceed the 5 mA ±5% budget.

6.6 Bandwidth and Stability

As can be seen in the schematic of 図 6-2, a small capacitor is inserted in parallel with the series input resistors. The reason for this is to compensate for the natural band-limiting effect of the 1st order filter formed by this resistor and the input capacitance of the buffer. With a typical C_{IN} of 3.5 pF (図 6-2), a pole is created at

$$fp2 = 1/(2\pi R_1 C_{IN}) = 4.5\ \text{MHz} \quad (1)$$

This will band-limit the buffer and produce further phase lag. If used in an op amp-loop application with an amplifier that has the same order of magnitude of unity gain crossing as fp2, this additional phase lag will produce oscillation.

The solution is to add a small feed-forward capacitor (phase lead) around the input resistor, as shown in 図 6-2. The value of this capacitor is not critical but should be such that the time constant formed by it and the input resistor that it is in parallel with (R_{IN}) be at least five times the time constant of $R_{IN}C_{IN}$. Therefore,

$$C_1 = (5R_{IN}/R_1)(C_{IN}) \quad (2)$$

from セクション 5.4, R_{IN} is 250 kΩ.

In the case of the example in 図 6-2, $R_{IN}C_{IN}$ produces a time-constant of 870 ns, so C_1 should be chosen to be a minimum of 4.4 µs, or 438 pF. The value of C_1 (1000 pF) shown in 図 6-2 gives 10 µs.

6.7 Output Current and Short Circuit Protection

The LMH6321 is designed to deliver a maximum continuous output current of 300 mA. However, the maximum available current, set by internal circuitry, is about 700 mA at room temperature. The output current is programmable up to 300 mA by a single external resistor and voltage source.

The LMH6321 is not designed to safely output 700 mA continuously and should not be used this way. However, the available maximum continuous current will likely be limited by the particular application and by the package type chosen, which together set the thermal conditions for the buffer (see セクション 6.8) and could require less than 300 mA.

The programming of both the sourcing and sinking currents into the load is accomplished with a single resistor. Figure 6-3 shows a simplified diagram of the V to I converter and I_{SC} protection circuitry that, together, perform this task.

Referring to Figure 6-3, the two simplified functional blocks, labeled V/I Converter and Short Circuit Protection, comprise the circuitry of the Current Limit Control.

The V/I converter consists of error amplifier A1 driving two PNP transistors in a Darlington configuration. The two input connections to this amplifier are V_{CL} (inverting input) and GND (non-inverting input). If GND is connected to zero volts, then the high open loop gain of A1, as well as the feedback through the Darlington, will force C_L, and thus one end R_{EXT} to be at zero volts also. Therefore, as shown in 式 3 a voltage applied to the other end of R_{EXT} will force a current into this pin.

$$I_{EXT} = V_{PROG}/R_{EXT} \quad (3)$$

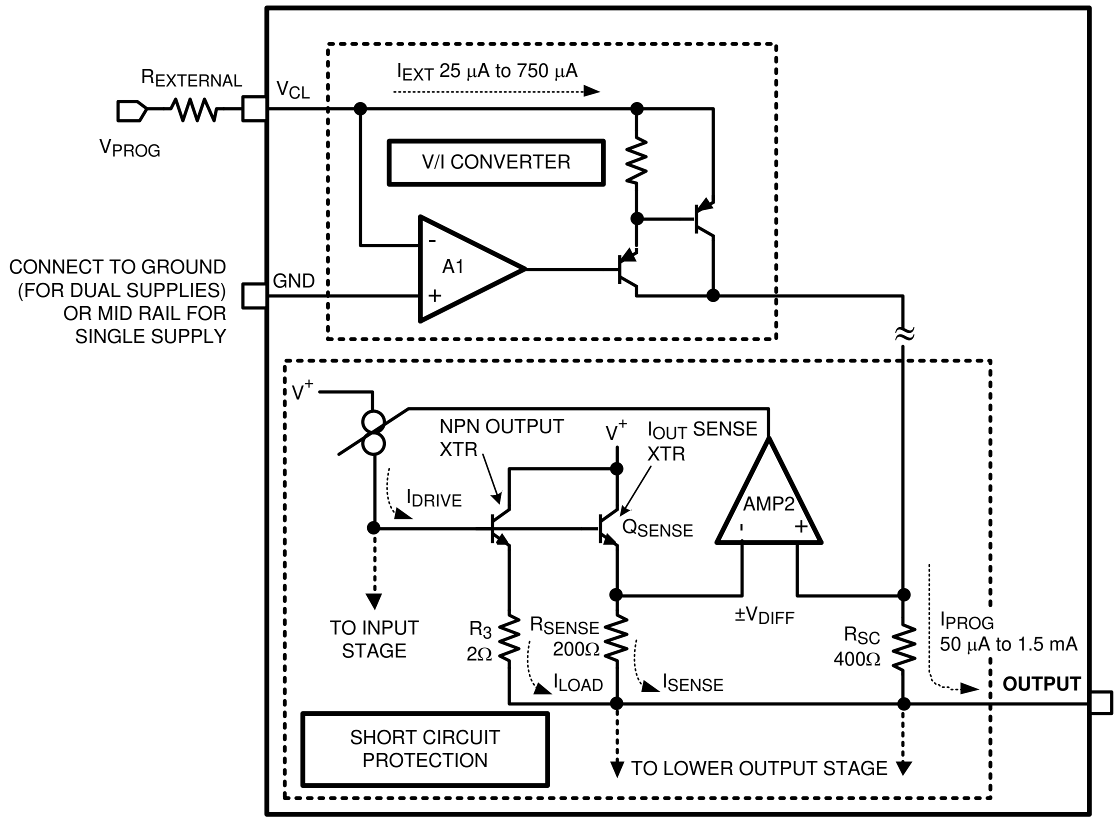
Through the VCL pin, I_{OUT} is programmable from 10 mA to 300 mA by setting I_{EXT} from 25 µA to 750 µA by means of a fixed R_{EXT} of 10 kΩ and making V_{PROG} variable from 0.25 V to 7.5 V. Thus, an input voltage V_{PROG} is converted to a current I_{EXT}. This current is the output from the V/I converter. It is gained up by a factor of two and sent to the Short Circuit Protection block as I_{PROG}. I_{PROG} sets a voltage drop across R_{SC} which is applied to the non-inverting input of error amp A2. The other input is across R_{SENSE}. The current through R_{SENSE}, and hence the voltage drop across it, is proportional to the load current, through the current sense transistor Q_{SENSE}. The output of A2 controls the drive (I_{DRIVE}) to the base of the NPN output transistor, Q3 which is, proportional to the amount and polarity of the voltage differential (V_{DIFF}) between AMP2 inputs, that is, how much the voltage across R_{SENSE} is greater than or less than the voltage across R_{SC}. This loop gains I_{EXT} up by another 200, thus

$$I_{SC} = 2 \times 200\ (I_{EXT}) = 400\ I_{EXT} \quad (4)$$

Therefore, combining 式 3 and 式 4, and solving for R_{EXT}, we get

$$R_{EXT} = 400\ V_{PROG}/I_{SC} \quad (5)$$

If the V_{CL} pin is left open, the output short circuit current will default to about 700 mA. At elevated temperatures this current will decrease.



Only the NPN output I_{SC} protection is shown. Depending on the polarity of V_{DIFF}, AMP2 will turn I_{DRIVE} either on or off.

図 6-3. Simplified Diagram of Current Limit Control

6.8 Thermal Management

6.8.1 Heatsinking

For some applications, a heat sink may be required with the LMH6321. This depends on the maximum power dissipation and maximum ambient temperature of the application. To accomplish heat sinking, the tabs on DDPAK and SO PowerPAD package may be soldered to the copper plane of a PCB for heatsinking (note that these tabs are electrically connected to the most negative point in the circuit, for example,V^-).

Heat escapes from the device in all directions, mainly through the mechanisms of convection to the air above it and conduction to the circuit board below it and then from the board to the air. Natural convection depends on the amount of surface area that is in contact with the air. If a conductive plate serving as a heatsink is thick enough to ensure perfect thermal conduction (heat spreading) into the far recesses of the plate, the temperature rise would be simply inversely proportional to the total exposed area. PCB copper planes are, in that sense, an aid to convection, the difference being that they are not thick enough to ensure perfect conduction. Therefore, eventually we will reach a point of diminishing returns (as seen in 図 6-5). Very large increases in the copper area will produce smaller and smaller improvement in thermal resistance. This occurs, roughly, for a 1 inch square of 1 oz copper board. Some improvement continues until about 3 square inches, especially for 2 oz boards and better, but beyond that, external heatsinks are required. Ultimately, a reasonable practical value attainable for the junction to ambient thermal resistance is about 30 °C/W under zero air flow.

A copper plane of appropriate size may be placed directly beneath the tab or on the other side of the board. If the conductive plane is placed on the back side of the PCB, it is recommended that thermal vias be used per JEDEC Standard JESD51-5.

6.8.2 Determining Copper Area

One can determine the required copper area by following a few basic guidelines:

1. Determine the value of the circuit's power dissipation, P_D
2. Specify a maximum operating ambient temperature, $T_{A(MAX)}$. Note that when specifying this parameter, it must be kept in mind that, because of internal temperature rise due to power dissipation, the die temperature, T_J, will be higher than T_A by an amount that is dependent on the thermal resistance from junction to ambient, θ_{JA}. Therefore, T_A must be specified such that T_J does not exceed the absolute maximum die temperature of 150°C.
3. Specify a maximum allowable junction temperature, $T_{J(MAX)}$, which is the temperature of the chip at maximum operating current. Although no strict rules exist, typically one should design for a maximum continuous junction temperature of 100°C to 130°C, but no higher than 150°C which is the absolute maximum rating for the part.
4. Calculate the value of junction to ambient thermal resistance, θ_{JA}
5. Choose a copper area that will ensure the specified $T_{J(MAX)}$ for the calculated θ_{JA}. θ_{JA} as a function of copper area in square inches is shown in 図 6-4.

The maximum value of thermal resistance, junction to ambient θ_{JA}, is defined as:

$$\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)})/ P_{D(MAX)} \quad (6)$$

where

- $T_{J(MAX)}$ = the maximum recommended junction temperature
- $T_{A(MAX)}$ = the maximum ambient temperature in the user's environment
- $P_{D(MAX)}$ = the maximum recommended power dissipation

Note

The allowable thermal resistance is determined by the maximum allowable heat rise , $T_{RISE} = T_{J(MAX)} - T_{A(MAX)} = (\theta_{JA}) (P_{D(MAX)})$. Thus, if ambient temperature extremes force T_{RISE} to exceed the design maximum, the part must be de-rated by either decreasing P_D to a safe level, reducing θ_{JA}, further, or, if available, using a larger copper area.

6.8.3 Procedure

1. First determine the maximum power dissipated by the buffer, $P_{D(MAX)}$. For the simple case of the buffer driving a resistive load, and assuming equal supplies, $P_{D(MAX)}$ is given by:

   $$P_{D(MAX)} = I_S (2V^+) + V^{+2}/4R_L \quad (7)$$

   where

   - I_S = quiescent supply current
2. Determine the maximum allowable die temperature rise,

   $$T_{R(MAX)} = T_{J(MAX)}-T_{A(MAX)} = P_{D(MAX)}\theta_{JA} \quad (8)$$
3. Using the calculated value of $T_{R(MAX)}$ and $P_{D(MAX)}$ the required value for junction to ambient thermal resistance can be found:

   $$\theta_{JA} = T_{R(MAX)}/P_{D(MAX)} \quad (9)$$
4. Finally, using this value for θ_{JA} choose the minimum value of copper area from 図 6-4.

6.8.4 Example

Assume the following conditions:

$V^+ = V^- = 15$ V, $R_L = 50\ \Omega$, $I_S = 15$ mA $T_{J(MAX)} = 125°C$, $T_{A(MAX)} = 85°C$.

1. From 式 7
   - $P_{D(MAX)} = I_S\ (2\ V^+) + V^{+2}/4R_L = (15\ mA)(30\ V) + 15\ V^2/200\ \Omega = 1.58\ W$
2. From 式 8
   - $T_{R(MAX)} = 125°C - 85°C = 40°C$
3. From 式 9
   - $\theta_{JA} = 40°C/1.58\ W = 25.3°C/W$

Examining 図 6-4, we see that we cannot attain this low of a thermal resistance for one layer of 1 oz copper. It will be necessary to derate the part by decreasing either the ambient temperature or the power dissipation. Other solutions are to use two layers of 1 oz foil, or use 2 oz copper (see 表 6-1), or to provide forced air flow. One should allow about an extra 15% heat sinking capability for safety margin.

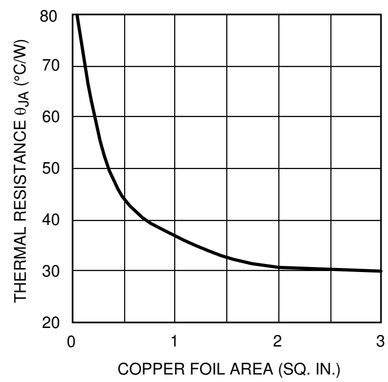


図 6-4. Thermal Resistance (Typical) for 7-L DDPAK Package Mounted on 1 oz. (0.036 mm) PC Board Foil

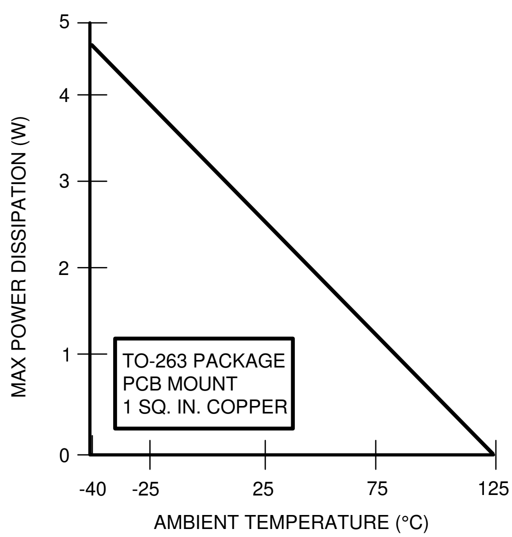


図 6-5. Derating Curve for DDPAK package. No Air Flow

表 6-1. $θ_{JA}$ vs. Copper Area and P_D for DDPAK. 1.0 oz cu Board. No Air Flow. Ambient Temperature = 24°C

Copper Area	θJA at 1.0W (°C/W)	θJA at 2.0W (°C/W)
1 Layer = 1”x2” cu Bottom	62.4	54.7
2 Layer = 1”x2” cu Top and Bottom	36.4	32.1
2 Layer = 2”x2” cu Top and Bottom	23.5	22.0
2 Layer = 2”x4” cu Top and Bottom	19.8	17.2

As seen in the previous example, buffer dissipation in DC circuit applications is easily computed. However, in AC circuits, signal wave shapes and the nature of the load (reactive, non-reactive) determine dissipation. Peak dissipation can be several times the average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

A selection of thermal data for the SO PowerPAD package is shown in 表 6-2. The table summarizes $θ_{JA}$ for both 0.5 watts and 0.75 watts. Note that the thermal resistance, for both the DDPAK and the SO PowerPAD package is lower for the higher power dissipation levels. This phenomenon is a result of the principle of Newtons Law of Cooling. Restated in term of heatsink cooling, this principle says that the rate of cooling and hence the thermal conduction, is proportional to the temperature difference between the junction and the outside environment (ambient). This difference increases with increasing power levels, thereby producing higher die temperatures with more rapid cooling.

表 6-2. $θ_{JA}$ vs. Copper Area and P_D for SO PowerPAD. 1.0 oz cu Board. No Airflow. Ambient Temperature = 22°C

Copper Area/Vias	θJA at 0.5W (°C/W)	θJA at 0.75W (°C/W)
1 Layer = 0.05 sq. in. (Bottom) + 3 Via Pads	141.4	138.2
1 Layer = 0.1 sq. in. (Bottom) + 3 Via Pads	134.4	131.2
1 Layer = 0.25 sq. in. (Bottom) + 3 Via Pads	115.4	113.9
1 Layer = 0.5 sq. in. (Bottom) + 3 Via Pads	105.4	104.7
1 Layer = 1.0 sq. in. (Bottom) + 3 Via Pads	100.5	100.2
2 Layer = 0.5 sq. in. (Top)/ 0.5 sq. in. (Bottom) + 33 Via Pads	93.7	92.5
2 Layer = 1.0 sq. in. (Top)/ 1.0 sq. in. (Bottom) + 53 Via Pads	82.7	82.2

6.9 Error Flag Operation

The LMH6321 provides an open collector output at the EF pin that produces a low voltage when the Thermal Shutdown Protection is engaged, due to a fault condition. Under normal operation, the Error Flag pin is pulled up to V^+ by an external resistor. When a fault occurs, the EF pin drops to a low voltage and then returns to V^+ when the fault disappears. This voltage change can be used as a diagnostic signal to alert a microprocessor of a system fault condition. If the function is not used, the EF pin can be either tied to ground or left open. If this function is used, a 10 kΩ, or larger, pull-up resistor (R_2 in 図 6-2) is recommended. The larger the resistor the lower the voltage will be at this pin under thermal shutdown. 表 6-3 shows some typical values of V_{EF} for 10 kΩ and 100 kΩ.

表 6-3. V_{EF} vs. R_2

R_2 (in 図 6-2)	At V^+ = 5 V	At V^+ = 15 V
10 kΩ	0.24 V	0.55 V
100 KΩ	0.036 V	0.072 V

6.10 Single Supply Operation

If dual supplies are used, then the GND pin can be connected to a hard ground (0 V) (as shown in 図 6-2). However, if only a single supply is used, this pin must be set to a voltage of one V_{BE} (≈0.7 V) or greater, or more commonly, mid rail, by a stiff, low impedance source. This precludes applying a resistive voltage divider to the GND pin for this purpose. 図 6-6 shows one way that this can be done.

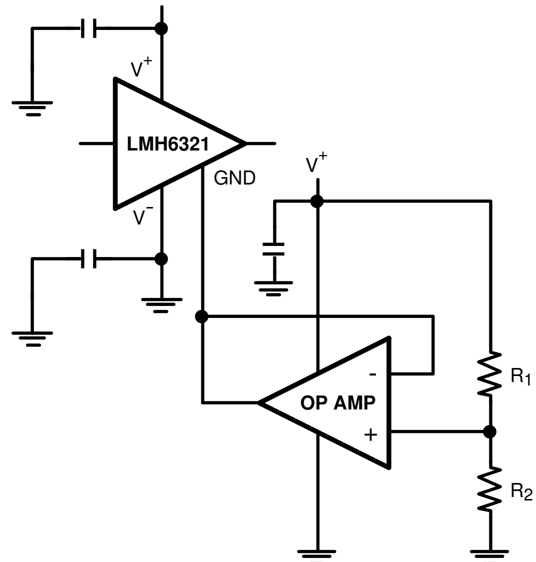


図 6-6. Using an Op Amp to Bias the GND Pin to ½ V⁺ for Single Supply Operation

In 図 6-6, the op amp circuit pre-biases the GND pin of the buffer for single supply operation.

The GND pin can be driven by an op amp configured as a constant voltage source, with the output voltage set by the resistor voltage divider, R_1 and R_2. It is recommended that These resistors be chosen so as to set the GND pin to $V^+/2$, for maximum common mode range.

6.11 Slew Rate

Slew rate is the rate of change of output voltage for large-signal step input changes. For resistive load, slew rate is limited by internal circuit capacitance and operating current (in general, the higher the operating current for a given internal capacitance, the faster is the slew rate). 図 6-7 shows the slew capabilities of the LMH6321 under large signal input conditions, using a resistive load.

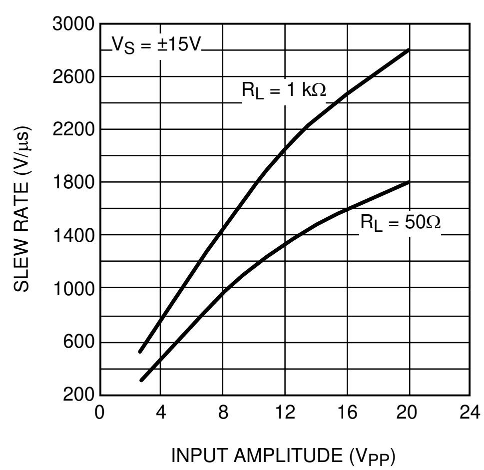


図 6-7. Slew Rate vs. Peak-to-Peak Input Voltage

However, when driving capacitive loads, the slew rate may be limited by the available peak output current according to the following expression.

$$dv/dt = I_{PK}/C_L \quad (10)$$

and rapidly changing output voltages will require large output load currents. For example if the part is required to slew at 1000 V/µs with a load capacitance of 1 nF the current demand from the LMH6321 would be 1A. Therefore, fast slew rate is incompatible with large C_L. Also, since C_L is in parallel with the load, the peak current available to the load decreases as C_L increases.

図 6-8 illustrates the effect of the load capacitance on slew rate. Slew rate tests are specified for resistive loads and/or very small capacitive loads, otherwise the slew rate test would be a measure of the available output current. For the highest slew rate, it is obvious that stray load capacitance should be minimized. Peak output current should be kept below 500 mA. This translates to a maximum stray capacitance of 500 pF for a slew rate of 1000 V/µs.

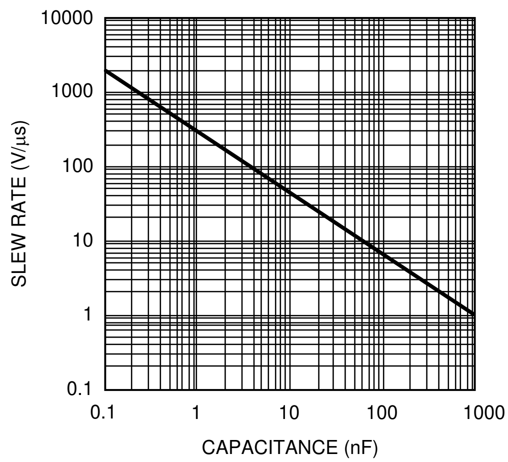


図 6-8. Slew Rate vs. Load Capacitance

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 サポート・リソース

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TI E2E™ is a trademark of Texas Instruments.
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7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6321MR/NOPB	Obsolete	Production	SO PowerPAD (DDA) | 8	-	-	Call TI	Call TI	-40 to 125	LMH63 21MR
LMH6321MRX/NOPB	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMH63 21MR
LMH6321MRX/NOPB.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LMH63 21MR
LMH6321TS/NOPB	Obsolete	Production	DDPAK/TO-263 (KTW) | 7	-	-	Call TI	Call TI	-40 to 125	LMH6321TS
LMH6321TSX/NOPB	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LMH6321TS
LMH6321TSX/NOPB.A	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LMH6321TS
LMH6321TSX/NOPB.B	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LMH6321TS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

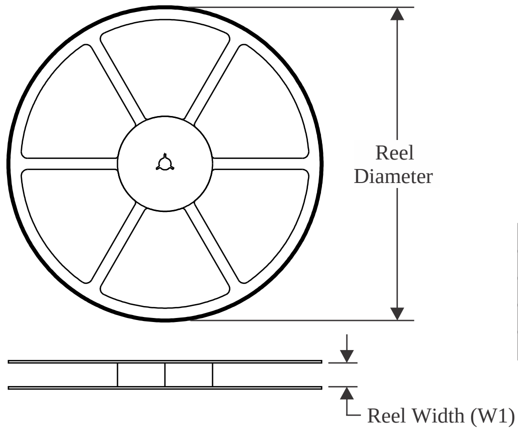
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

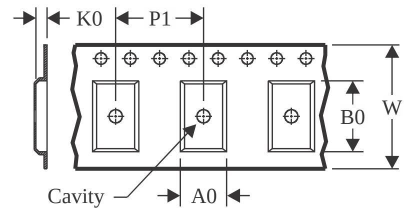
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

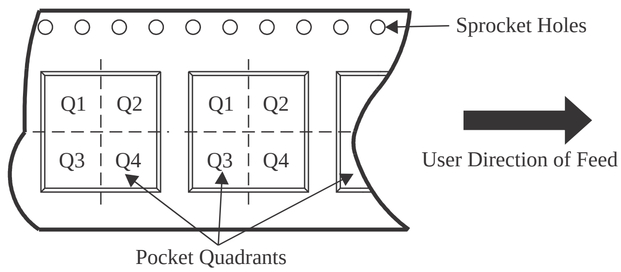


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

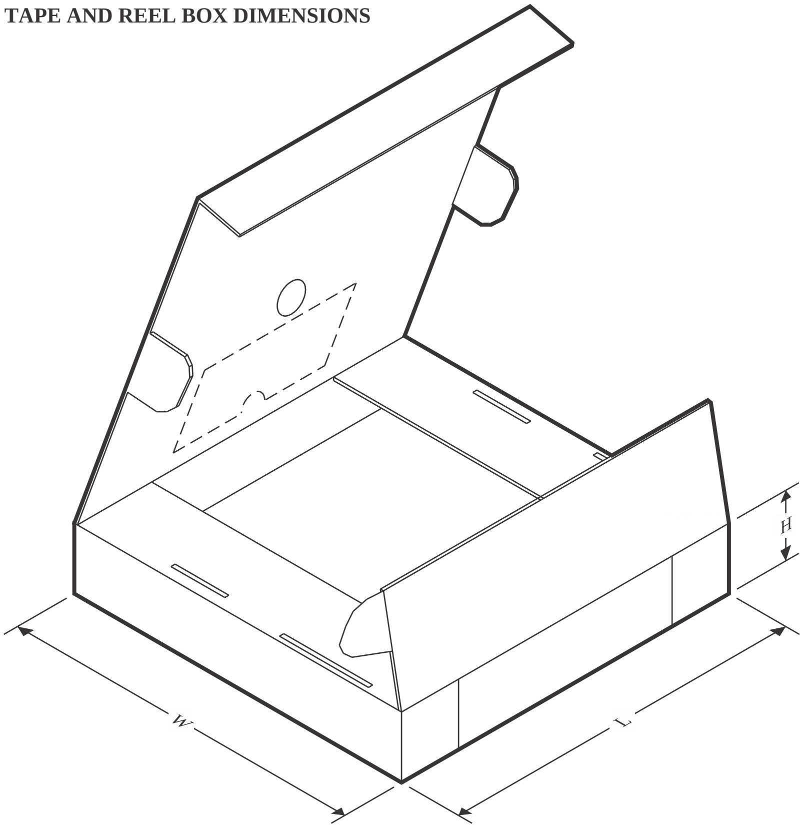
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

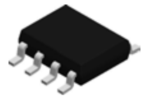
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6321MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LMH6321TSX/NOPB	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

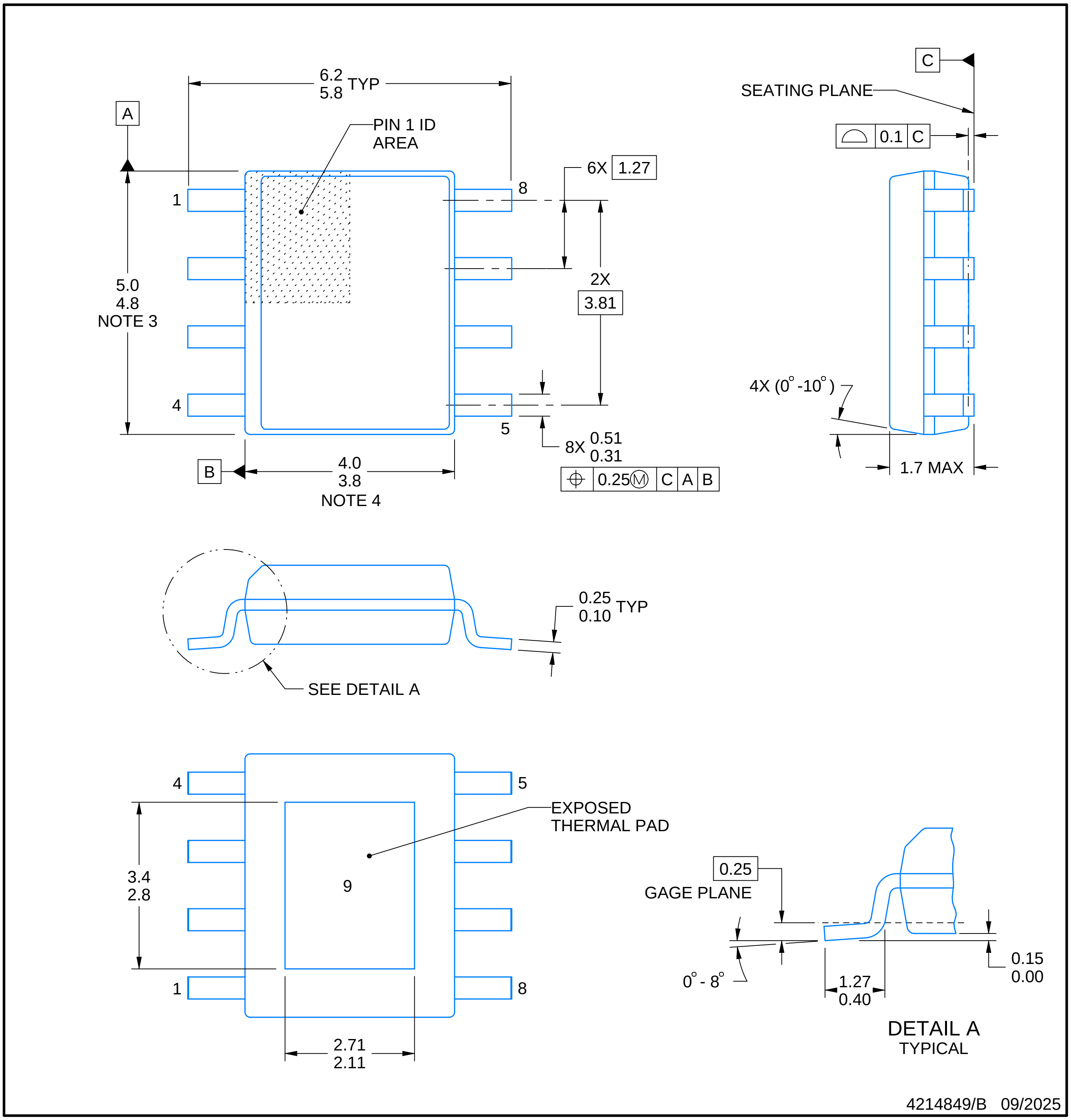
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6321MRX/NOPB	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
LMH6321TSX/NOPB	DDPAK/TO-263	KTW	7	500	356.0	356.0	45.0



PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE

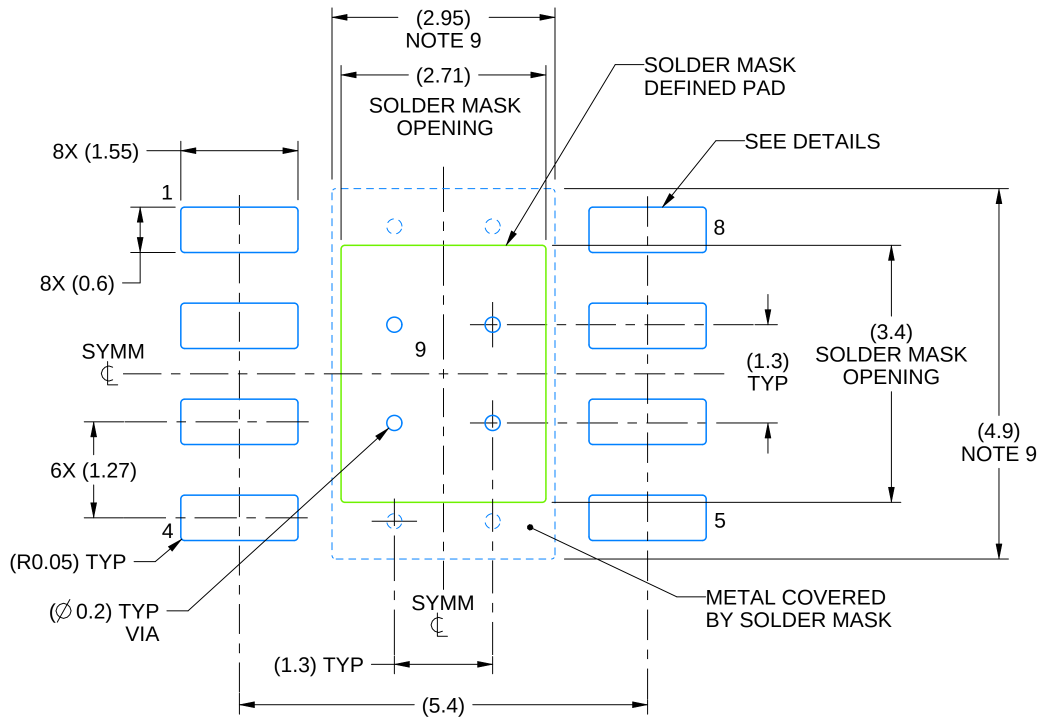


4214849/B 09/2025

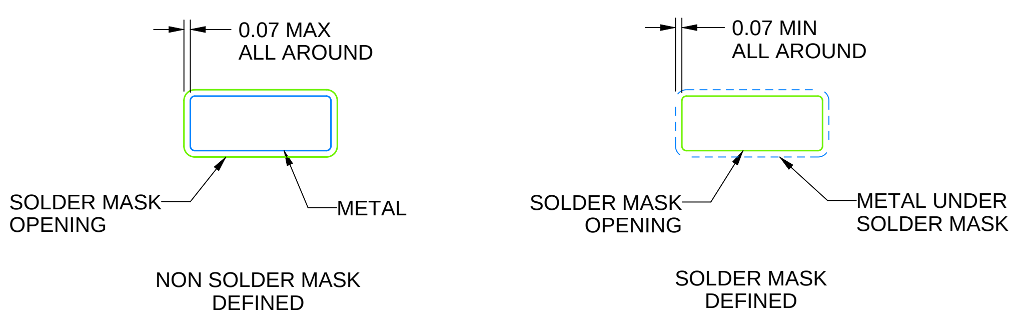
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

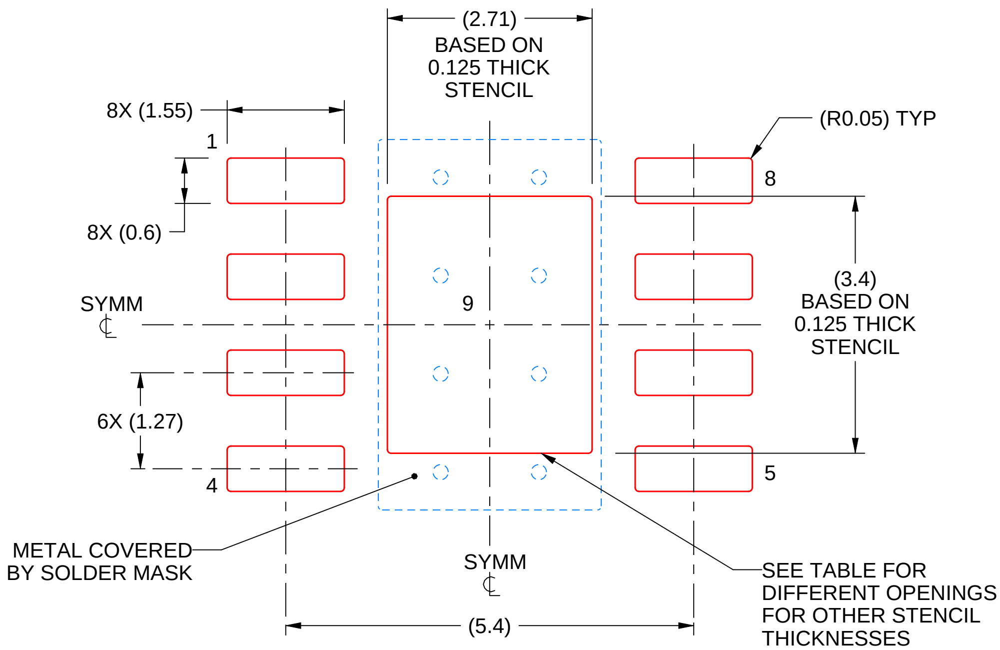


SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



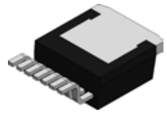
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

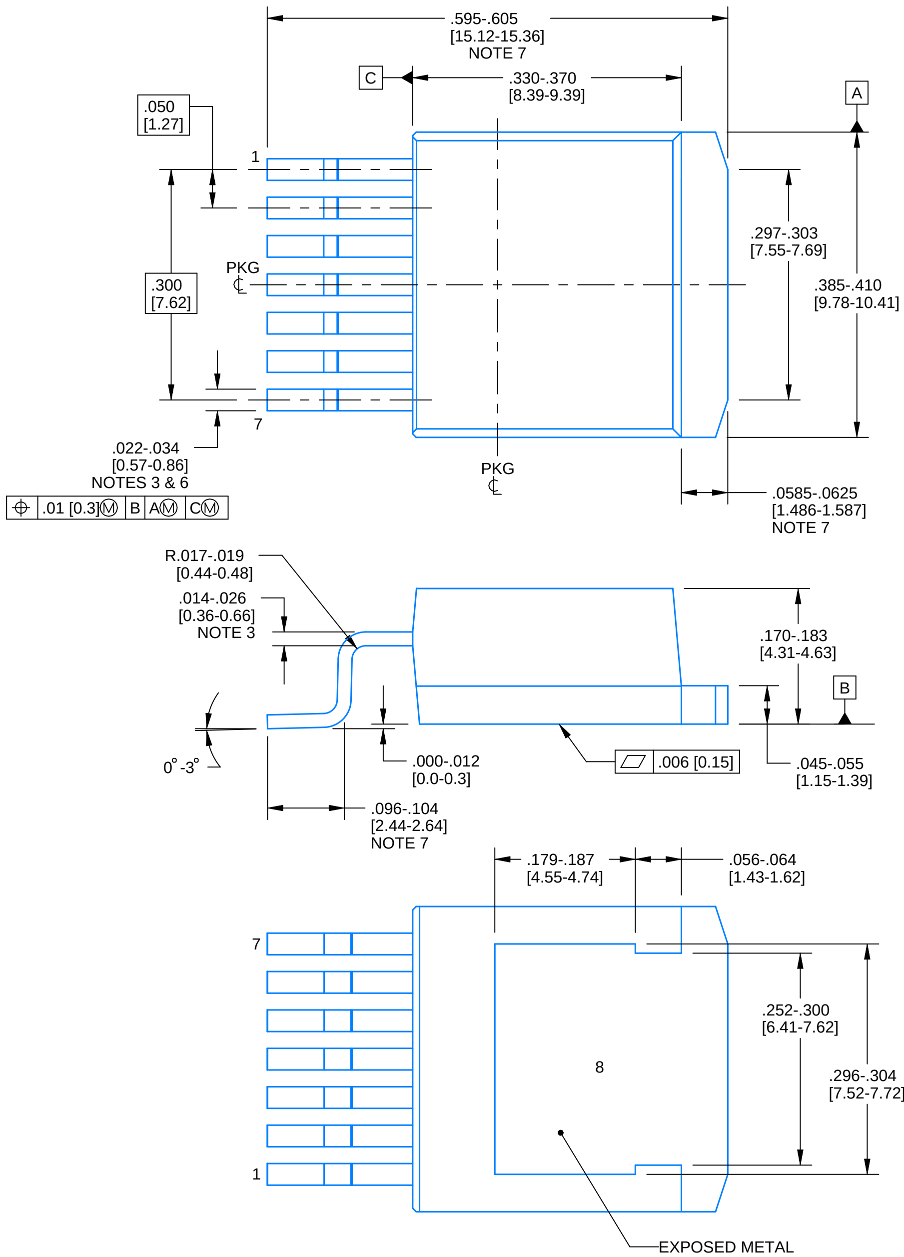


PACKAGE OUTLINE

KTW0007A

TO-263 - 5 mm max height

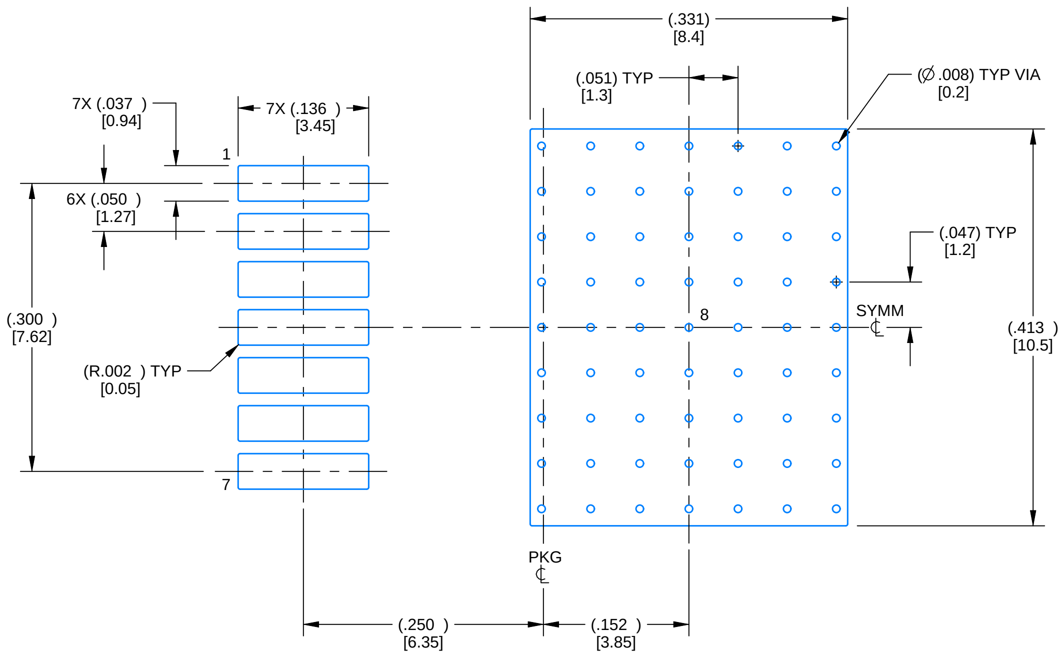
TRANSISTOR OUTLINE



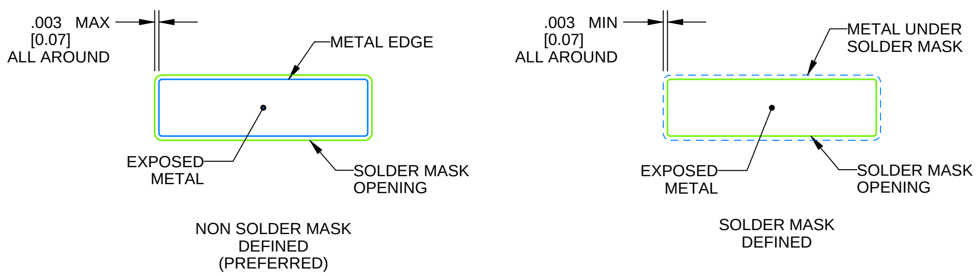
4232469/A 11/2025

NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead width and height dimensions apply to the plated lead.
4. Leads are not allowed above the Datum B.
5. Stand–off height is measured from lead tip with reference to Datum B.
6. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum bdimension by more than 0.003”.
7. Falls within JEDEC MO–169 with the exception of the dimensions indicated.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 5X

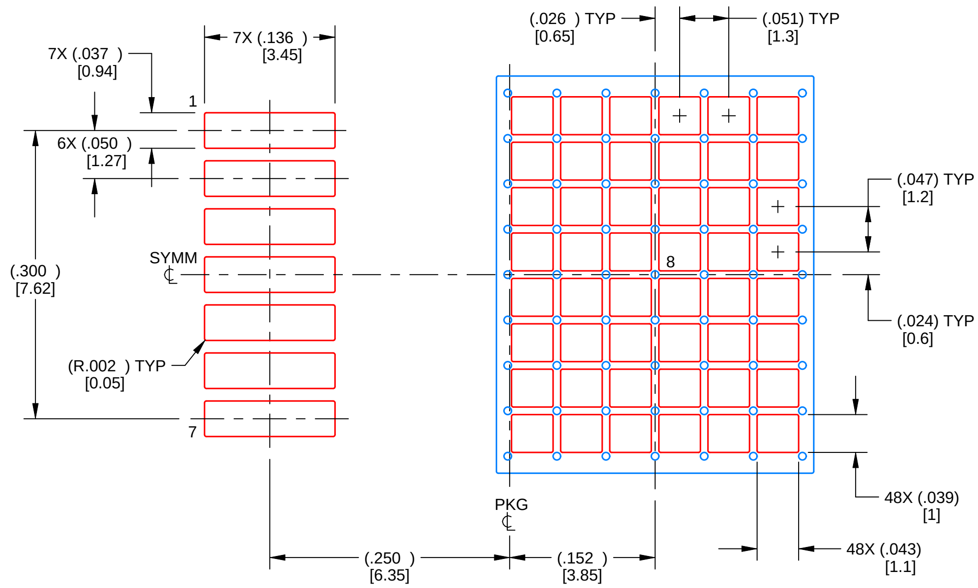


SOLDER MASK DETAILS

4232469/A 11/2025

NOTES: (continued)

8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 5X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 8: 60%

4232469/A 11/2025

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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