LMK00338 8 出力 PCIe Gen1/Gen2/Gen3/Gen4/Gen5 クロック・バッファ / レベル・トランスレータ

1 特長

- 3:1 入力マルチプレクサ
  - 2 つの汎用入力は最高 400MHz で動作し、LVPECL、LVDS、CML、SSTL、HSTL、HCSL、シングルエンド・クロックに対応
  - 1 つの水晶振動子入力で、10MHz～40MHz の水晶振動子またはシングルエンド・クロックに対応
- 2 バンクで、それぞれに 4 つの差動出力
  - HCSL または Hi-Z (バンクごとに選択可能)
  - 100MHz の PCIe Gen5 用の付加 RMS 位相ジッタ
    - 15 fs RMS (標準値)
- -72dBc (156.25 MHz)
- 同期イネーブル入力付きの LVCMOS 出力
- 構成をピンで制御可能
- V_{CC} コア電源:3.3V ± 5%
- 3 つの独立した V_{CCO} 出力電源:3.3V / 2.5V ± 5%
- 産業用温度範囲:-40℃～+85℃
- 40 リードの WQFN (6 mm×6 mm)

2 アプリケーション

- ADC、DAC、マルチ・ギガビット・イーサネット、XAUI、Fibre Channel、SATA/SAS、SONET/SDH、CPRI、高周波数バックプレーン用のクロック分配およびレベル変換
- スイッチ、ルータ、ライン・カード、タイミング・カード
- サーバ、コンピュータ、PCI Express (PCIe 3.0、4.0、5.0)
- リモート無線ユニットおよびベースバンド・ユニット

3 概要

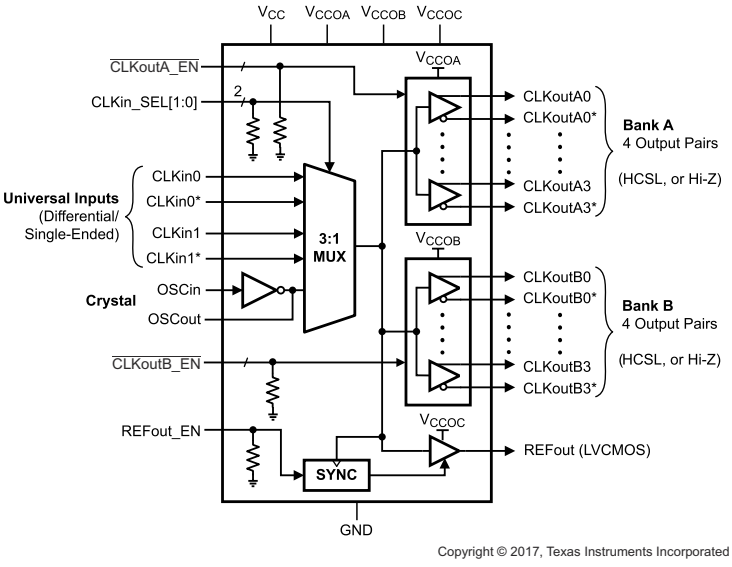
LMK00338 デバイスは、高周波数、低ジッタ クロック、データ分配、レベル変換を目的とした 8 出力 PCIe Gen1/Gen2/Gen3/Gen4/Gen5 ファンアウト・バッファです。入力クロックは 2 つの汎用入力、または 1 つの水晶振動子入力から選択できます。選択された入力クロックは 4 HCSL 出力の 2 バンクと、1 LVCMOS 出力に分配されます。LVCMOS 出力には同期イネーブル入力があり、イネーブルまたはディセーブル時にラント (微小) パルスなしの動作を実現できます。LMK00338 は 3.3V のコア電源、および 3 つの独立した 3.3V または 2.5V の出力電源で動作します。

LMK00338 は高性能、多用途、優れた電力効率から、固定出力のバッファ・デバイスの代替品として理想的で、システムのタイミング・マージンを拡大できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
LMK00338	WQFN（40）	6.00mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



LMK00338 機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2017) to Revision C (July 2021) — **Page**

- データシートのタイトルを *LMK00338 8 出力差動クロック・バッファ / レベル・トランスレータ* : *LMK00338 8 出力 PCIe Gen1/Gen2/Gen3/Gen4/Gen5 クロック・バッファ / レベル・トランスレータ* ... 1
- *目的アプリケーションを変更* 2 番目および 3 番目の箇条書き項目にアプリケーションを追加し、最初の項目から High-Speed と Serial の各インターフェイスを削除。 ... 1
- データシートに PCIe Gen5 を追加 ... 1
- Added PCIe 4.0 compliance data ... 6
- Added additive RMS phase jitter for PCIe 4.0 and PCIe 5.0 to the *Electrical Characteristics* table ... 6
- Removed the *LVPECL Phase Noise at 100 MHz* graph ... 11
- Changed the third paragraph in *Driving the Clock Inputs* section to include CLKin* and LVCMOS text. Revised to better correspond with information in the *Electrical Characteristics* table ... 17
- Changed the bypass cap text to signal attenuation text of the fourth paragraph in *Driving the Clock Inputs* section ... 17
- Changed the *Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing* image with revised graphic ... 17

Changes from Revision A (October 2014) to Revision B (June 2017) — **Page**

- データシート全体を通して、CLKoutA_EN ピンと CLKoutB_EN ピンを $\overline{\text{CLKoutA\_EN}}$ および $\overline{\text{CLKoutB\_EN}}$ に変更 ... 1

Changes from Revision * (December 2013) to Revision A (October 2014) — **Page**

- 次のセクションを追加、更新、または名称変更:「製品情報」表、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション ... 1
- Added PCIE Gen4 additive jitter to the *Electrical Characteristics* table ... 6
- Changed 1 MHz to 12 kHz ... 6
- Added 図 10-1 ... 25

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5 Pin Configuration and Functions

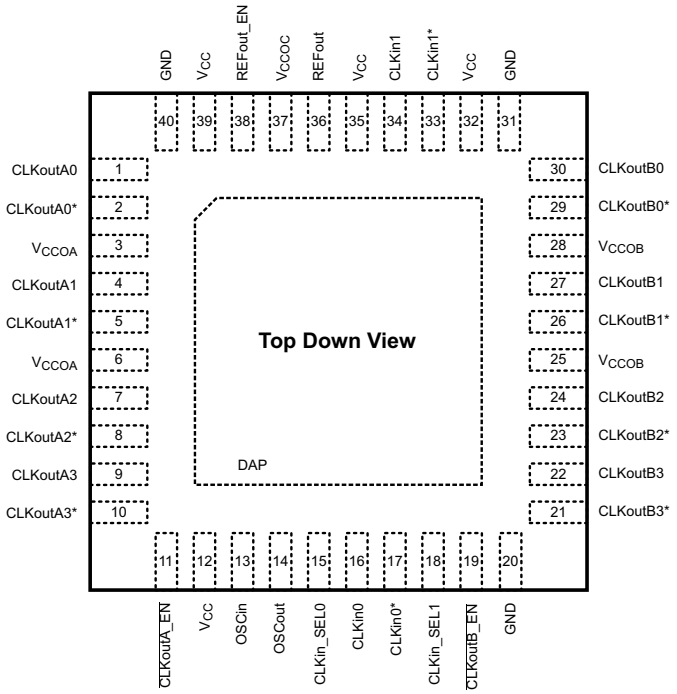

図 5-1. RTA Package 40-Pin WQFN Top View

表 5-1. Pin Functions(3)

PIN		TYPE	DESCRIPTION
NAME	NO.		
DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
CLKin0	16	I	Universal clock input 0 (differential/single-ended)
CLKin0*	17	I	Universal clock input 0 (differential/single-ended)
CLKin1	34	I	Universal clock input 1 (differential/single-ended)
CLKin1*	33	I	Universal clock input 1 (differential/single-ended)
$\overline{\text{CLKoutA\_EN}}$	11	I	Bank A low active output buffer enable(2)
CLKoutA0	1	O	Differential clock output A0.
CLKoutA0*	2	O	Differential clock output A0.
CLKoutA1	4	O	Differential clock output A1.
CLKoutA1*	5	O	Differential clock output A1.
CLKoutA2	7	O	Differential clock output A2.
CLKoutA2*	8	O	Differential clock output A2.
CLKoutA3	9	O	Differential clock output A3.
CLKoutA3*	10	O	Differential clock output A3.
$\overline{\text{CLKoutB\_EN}}$	19	I	Bank B low active output buffer enable(2)
CLKoutB1	27	O	Differential clock output B1.
CLKoutB1*	26	O	Differential clock output B1.
CLKoutB0	30	O	Differential clock output B0.
CLKoutB0*	29	O	Differential clock output B0.
CLKoutB2	24	O	Differential clock output B2.
CLKoutB2*	23	O	Differential clock output B2.
CLKoutB3	22	O	Differential clock output B3.

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表 5-1. Pin Functions(3) (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLKoutB3*	21	O	Differential clock output B3.
CLKin_SEL0	15	I	Clock input selection pins (2)
CLKin_SEL1	18	I	Clock input selection pins (2)
GND	20, 31, 40	GND	Ground
OSCin	13	I	Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock.
OSCout	14	O	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.
REFout	36	O	LVCMOS reference output. Enable output by pulling REFout_EN pin high.
REFout_EN	38	I	REFout enable input. Enable signal is internally synchronized to selected clock input.(2)
V_{CC}	12, 32, 35, 39	PWR	Power supply for Core and Input buffer blocks. The V_{CC} supply operates from 3.3 V. Bypass with a 0.1-µF low-ESR capacitor placed very close to each V_{CC} pin.
V_{CCOA}	3, 6	PWR	Power supply for Bank A Output buffers. V_{CCOA} can operate from 3.3 V or 2.5 V. The V_{CCOA} pins are internally tied together. Bypass with a 0.1-µF low-ESR capacitor placed very close to each V_{CCO} pin. (1)
V_{CCOB}	25, 28	PWR	Power supply for Bank B Output buffers. V_{CCOB} can operate from 3.3 V or 2.5 V. The V_{CCOB} pins are internally tied together. Bypass with a 0.1-µF low-ESR capacitor placed very close to each V_{CCO} pin. (1)
V_{CCOC}	37	PWR	Power supply for REFout Output buffer. V_{CCOC} can operate from 3.3 V or 2.5 V. Bypass with a 0.1-µF low-ESR capacitor placed very close to each V_{CCO} pin.(1)

(1) The output supply voltages/pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) is referred to generally as V_{CCO} when no distinction is needed, or when the output supply can be inferred by the output bank/type.
(2) CMOS control input with internal pull-down resistor.
(3) Any unused output pins should be left floating with minimum copper length (see note in *Clock Outputs*), or properly terminated if connected to a transmission line, or disabled/Hi-Z if possible. See *Clock Outputs* for output configuration or *Termination and Use of Clock Drivers* output interface and termination techniques.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{CC}, V_{CCO}	Supply voltages	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	(V_{CC} + 0.3)	V
T_L	Lead temperature (solder 4 s)		260	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	
		Machine model (MM)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
T_A	Ambient temperature		–40	25	85	°C
T_J	Junction temperature				125	°C
V_{CC}	Core supply voltage		3.15	3.3	3.45	V
V_{CCO}	Output supply voltage(1) (2)	3.3-V range	3.3 – 5%	3.3	3.3 + 5%	V
		2.5-V range	2.5 – 5%	2.5	2.5 + 5%	

(1) The output supply voltages/pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be referred to generally as V_{CCO} when no distinction is needed, or when the output supply can be inferred by the output bank/type.
(2) V_{CCO} should be less than or equal to V_{CC} ($V_{CCO} \le V_{CC}$).

6.4 Thermal Information

THERMAL METRIC(1)		LMK00338 RTA (WQFN) 40 PINS(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.2 (DAP)	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.
(2) Specification assumes 9 thermal vias connect the die attach pad (DAP) to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the package. TI recommends using the maximum number of vias in the board layout.

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6.5 Electrical Characteristics

Unless otherwise specified: V_{CC} = 3.3 V ± 5%, V_{CCO} = 3.3 V ± 5%, 2.5 V ± 5%, –40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.(1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION (3)							
ICC_CORE	Core supply current, all outputs disabled	CLKinX selected			8.5	10.5	mA
		OSCin selected			10	13.5	mA
ICC_HCSL					31	38.5	mA
ICC_CMOS					3.5	5.5	mA
ICCO_HCSL	Additive output supply current, HCSL banks enabled	Includes Output Bank Bias and Load Currents for both banks, R_T = 50 Ω on all outputs in bank			68	84	mA
ICCO_CMOS	Additive output supply current, LVCMOS output enabled	200 MHz, C_L = 5 pF	V_{CCO} = 3.3 V ±5%		9	10	mA
			V_{CCO} = 2.5V ± 5%		7	8	mA
POWER SUPPLY RIPPLE REJECTION (PSRR)							
$PSRR_{HCSL}$	Ripple-induced phase spur level(4) Differential HCSL output	156.25 MHz			–72		dBc
		312.5 MHz			–63		
CMOS CONTROL INPUTS (CLKin_SELn, CLKout_TYPEn, REFout_EN)							
V_{IH}	High-level input voltage			1.6		Vcc	V
V_{IL}	Low-level input voltage			GND		0.4	V
I_{IH}	High-level input current	V_{IH} = V_{CC}, internal pulldown resistor				50	µA
I_{IL}	Low-level input current	V_{IL} = 0 V, internal pulldown resistor		–5	0.1		µA
CLOCK INPUTS (CLKin0/CLKin0*, CLKin1/CLKin1*)							
f_{CLKin}	Input frequency range(10)	Functional up to 400 MHz Output frequency range and timing specified per output type (refer to HCSL, LVCMOS output specifications)		DC		400	MHz
V_{IHD}	Differential input high voltage	CLKin driven differentially				V_{CC}	V
V_{ILD}	Differential input low voltage			GND			V
V_{ID}	Differential input voltage swing(5)			0.15		1.3	V
V_{CMD}	Differential input CMD common-mode voltage	V_{ID} = 150 mV		0.25		V_{CC} – 1.2	V
		V_{ID} = 350 mV		0.25		V_{CC} – 1.1	
		V_{ID} = 800 mV		0.25		V_{CC} – 0.9	
V_{IH}	Single-ended input IH high voltage	CLKinX driven single-ended (AC- or DC-coupled), CLKinX* AC-coupled to GND or externally biased within V_{CM} range				VCC	V
V_{IL}	Single-ended input IL low voltage			GND			V
V_{I_SE}	Single-ended input voltage swing(14)			0.3		2	Vpp
V_{CM}	Single-ended input CM common-mode voltage			0.25		V_{CC} – 1.2	V

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Unless otherwise specified: V_{CC} = 3.3 V ± 5%, V_{CCO} = 3.3 V ± 5%, 2.5 V ± 5%, –40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.(1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO_{MUX}	Mux isolation, CLKin0 to CLKin1	f_{OFFSET} > 50 kHz, P_{CLKinX} = 0 dBm	f_{CLKin0} = 100 MHz		–84		dBc

Unless otherwise specified: V_{CC} = 3.3 V ± 5%, V_{CCO} = 3.3 V ± 5%, 2.5 V ± 5%, –40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.(1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
			f_{CLKin0} = 200 MHz		–82		
			f_{CLKin0} = 500 MHz		–71		
			f_{CLKin0} = 1000 MHz		–65		
CRYSTAL INTERFACE (OSCin, OSCout)							
F_{CLK}	External clock frequency range(10)	OSCin driven single-ended, OSCout floating				250	MHz
F_{XTAL}	Crystal frequency range	Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz)(6)		10		40	MHz
C_{IN}	OSCin input capacitance				1		pF
HCSL OUTPUTS (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout}	Output frequency range(10)	R_L = 50 Ω to GND, C_L ≤ 5 pF		DC		400	MHz
$Jitter_{ADD\_PCIe}$	Additive RMS phase jitter for PCIe 5.0(10)	PCIe Gen 5 filter	CLKin: 100 MHz, Slew rate ≥ 0.5 V/ns		0.015	0.03	ps
$Jitter_{ADD\_PCIe}$	Additive RMS phase jitter for PCIe 4.0(10)	PCIe Gen 4, PLL BW = 2–5 MHz, CDR = 10 MHz	CLKin: 100 MHz, Slew rate ≥ 1.8 V/ns		0.03	0.05	ps
$Jitter_{ADD\_PCIe}$	Additive RMS phase jitter for PCIe 3.0(10)	PCIe Gen 3, PLL BW = 2–5 MHz, CDR = 10 MHz	CLKin: 100 MHz, Slew rate ≥ 0.6 V/ns		0.03	0.15	ps
$Jitter_{ADD}$	Additive RMS jitter integration bandwidth to 20 MHz(8) (9)	V_{CCO} = 3.3 V, R_T = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		77		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		86		
Noise Floor	Noise floor f_{OFFSET} ≥ 10 MHz(8) (9)	V_{CCO} = 3.3 V, R_T = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		–161.3		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		–156.3		
DUTY	Duty cycle(10)	50% input clock duty cycle		45%		55%	
V_{OH}	Output high voltage	T_A = 25°C, DC measurement, R_T = 50 Ω to GND		520	810	920	mV
V_{OL}	Output low voltage			–150	0.5	150	mV
V_{CROSS}	Absolute crossing voltage(10) (11)	R_L = 50 Ω to GND, C_L ≤ 5 pF		160	350	460	mV
ΔV_{CROSS}	Total variation of V_{CROSS}					140	mV
t_R	Output rise time 20% to 80%(11) (14)	250 MHz, uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R_L = 50 Ω to GND, C_L ≤ 5 pF			300	500	ps
t_F	Output fall time 80% to 20%(11) (14)				300	500	ps

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Unless otherwise specified: V_{CC} = 3.3 V ± 5%, V_{CCO} = 3.3 V ± 5%, 2.5 V ± 5%, –40°C ≤ T_A ≤ 85°C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.(1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS OUTPUT (REFout)							
f_{CLKout}	Output frequency range(10)	C_L ≤ 5 pF		DC		250	MHz
$Jitter_{ADD}$	Additive RMS jitter integration bandwidth 1 MHz to 20 MHz(7)	V_{CCO} = 3.3 V, C_L ≤ 5 pF	100 MHz, Input slew rate ≥ 3 V/ns		95		fs
Noise Floor	Noise floor f_{OFFSET} ≥ 10 MHz(8) (9)	V_{CCO} = 3.3 V, C_L ≤ 5 pF	100 MHz, Input slew rate ≥ 3 V/ns		–159.3		dBc/Hz
DUTY	Duty cycle(10)	50% input clock duty cycle		45%		55%	
V_{OH}	Output high voltage	1-mA load		V_{CCO} – 0.1			V
V_{OL}	Output low voltage					0.1	V
I_{OH}	Output high current (source)	V_O = V_{CCO} / 2	V_{CCO} = 3.3 V		28		mA
I_{OL}	Output low current (sink)		V_{CCO} = 2.5 V		20		
			V_{CCO} = 3.3 V		28		mA
			V_{CCO} = 2.5 V		20		
t_R	Output rise time 20% to 80%(11) (14)	250 MHz, uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R_L = 50 Ω to GND, C_L ≤ 5 pF			225	400	ps
t_F	Output fall time 80% to 20%(11) (14)				225	400	ps
t_{EN}	Output enable time(12)	C_L ≤ 5 pF				3	cycles
t_{DIS}	Output disable time(12)					3	cycles
PROPAGATION DELAY and OUTPUT SKEW							
t_{PD_HCSL}	Propagation delay CLKin-to-HCSL(11) (14)	R_T = 50 Ω to GND, C_L ≤ 5 pF		295	590	885	ps
t_{PD_CMOS}	Propagation delay CLKin-to-LVCMOS(11) (14)	C_L ≤ 5 pF	V_{CCO} = 3.3 V	900	1475	2300	ps
			V_{CCO} = 2.5 V	1000	1550	2700	
$t_{SK(O)}$	Output skew(10) (11) (13)	Skew specified between any two CLKouts. Load conditions are the same as propagation delay specifications.			30	50	ps
$t_{SK(PP)}$	Part-to-part output skew HCSL(11) (14) (13)				80	120	ps

(1) The output supply voltages/pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be referred to generally as V_{CCO} when no distinction is needed, or when the output supply can be inferred by the output bank/type.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and notes. Typical specifications are estimations only and are not ensured.

(3) See *Power Supply Recommendations* for more information on current consumption and power dissipation calculations.

(4) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the V_{CCO} supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [$(2 \times 10^{(PSRR / 20)}) / (\pi \times f_{CLK})$] × 1E12

(5) See *Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD} voltages.

(6) The ESR requirements stated must be met to ensure that the oscillator circuitry has no start-up issues. However, lower ESR values for the crystal may be necessary to stay below the maximum power dissipation (drive level) specification of the crystal. Refer to *Crystal Interface* for crystal drive level considerations.

(7) For the 100-MHz and 156.25-MHz clock input conditions, Additive RMS Jitter (J_{ADD}) is calculated using Method #1: J_{ADD} = SQRT($J_{OUT}^2 - J_{SOURCE}^2$), where J_{OUT} is the total RMS jitter measured at the output driver and J_{SOURCE} is the RMS jitter of the clock source applied to CLKin. For the 625-MHz clock input condition, additive RMS jitter is approximated using Method #2: J_{ADD} = SQRT($2 \times 10^{dBc/10}$) / ($2 \times \pi \times f_{CLK}$), where dBc is the phase noise power of the output noise floor integrated from 1-MHz to 20-MHz bandwidth. The phase noise power can be calculated as: dBc = Noise Floor + 10 × $\log_{10}$(20 MHz – 1 MHz). The additive RMS jitter was approximated for 625 MHz using Method #2 because the RMS jitter of the clock source was not sufficiently low enough to allow practical use of Method #1. Refer to the *Noise Floor vs. CLKin Slew Rate* and *RMS Jitter vs. CLKin Slew Rate* plots in *Typical Characteristics*.

(8) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10 MHz, but for lower frequencies this measurement offset can be as low as 5 MHz due to measurement equipment limitations.

(9) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) is less susceptible to degradation in noise floor at lower slew rates due to its common-mode noise rejection.

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However, TI recommends using the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.

(10) Specification is ensured by characterization and is not tested in production.

(11) AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.

(12) Output enable time is the number of input clock cycles it takes for the output to be enabled after REFout_EN is pulled high. Similarly, output disable time is the number of input clock cycles it takes for the output to be disabled after REFout_EN is pulled low. The REFout_EN signal should have an edge transition much faster than that of the input clock period for accurate measurement.

(13) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

(14) Parameter is specified by design, not tested in production.

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6.6 Typical Characteristics

Unless otherwise specified: V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C, CLKin driven differentially, input slew rate ≥ 3 V/ns.

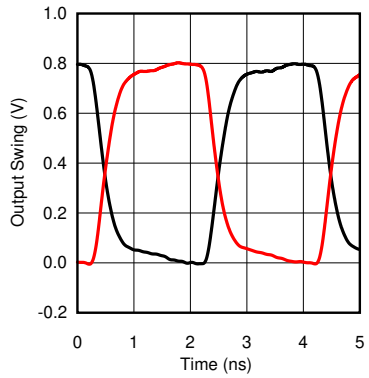


図 6-1. HCSL Output Swing at 250 MHz

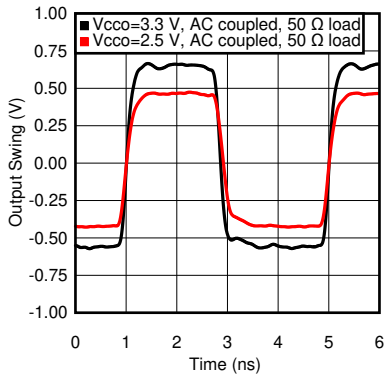
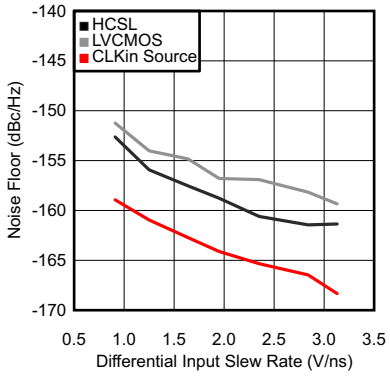
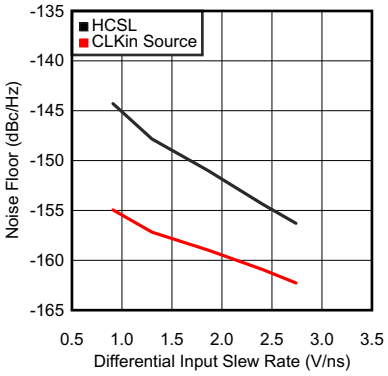


図 6-2. LVCMOS Output Swing at 250 MHz



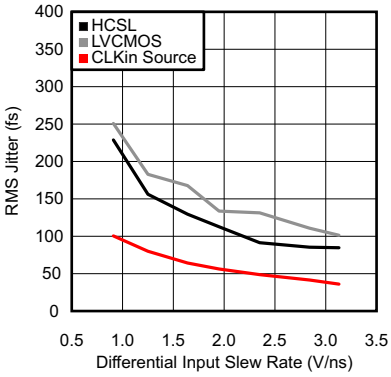
Fclk = 100 MHz F_{offset} = 20 MHz

図 6-3. Noise Floor vs CLKin Slew Rate at 100 MHz



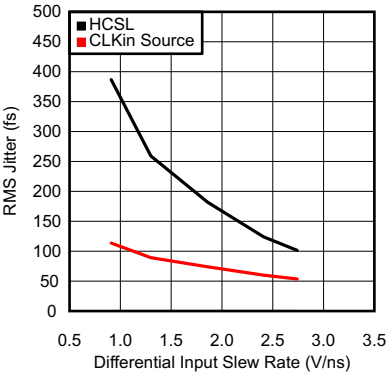
Fclk = 156.25 MHz F_{offset} = 20 MHz

図 6-4. Noise Floor vs CLKin Slew Rate at 156.25 MHz



Fclk = 100 MHz Int. BW = 1 to 20 MHz

図 6-5. RMS Jitter vs CLKin Slew Rate at 100 MHz



Fclk = 156.25 MHz Int. BW = 1 to 20 MHz

図 6-6. RMS Jitter vs CLKin Slew Rate at 156.25 MHz

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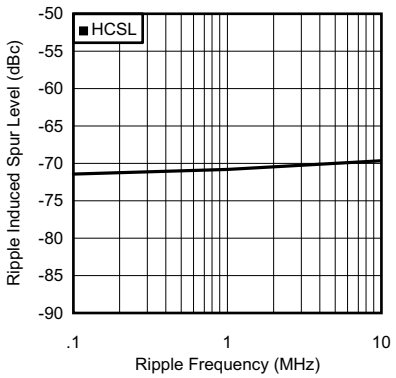
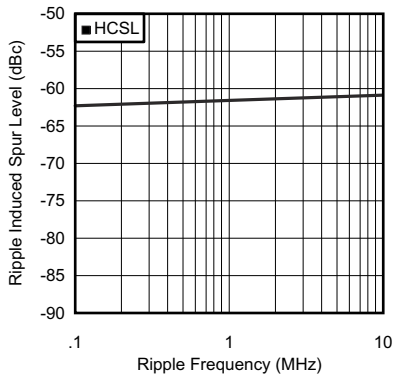


Fclk = 156.25 MHz V_{CCO} Ripple = 100

図 6-7. PSRR vs Ripple Frequency at 156.25 MHz



F_{clk} = 312.5 MHz V_{CCO} Ripple = 100 mVpp

図 6-8. PSRR vs Ripple Frequency at 312.5 MHz

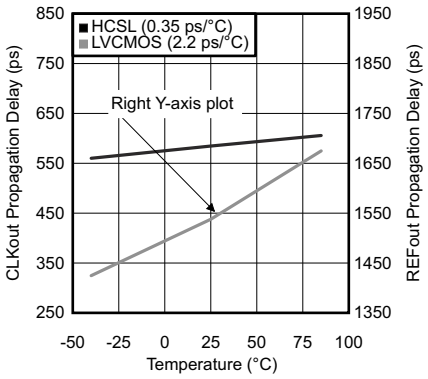


図 6-9. Propagation Delay vs Temperature

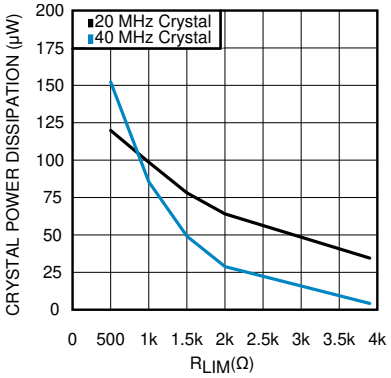


図 6-10. Crystal Power Dissipation vs R_{LIM}

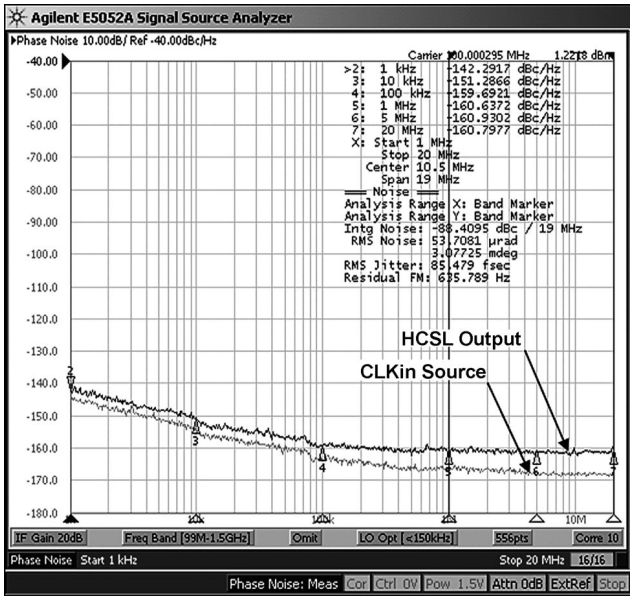


図 6-11. HCSL Phase Noise at 100 MHz

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7 Parameter Measurement Information

7.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground; it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described above.

図 7-1 illustrates the two different definitions side-by-side for inputs and 図 7-2 illustrates the two different definitions side-by-side for outputs. The V_{ID} (or V_{OD}) definition show the DC levels, V_{IH} and V_{OL} (or V_{OH} and V_{OL}), that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

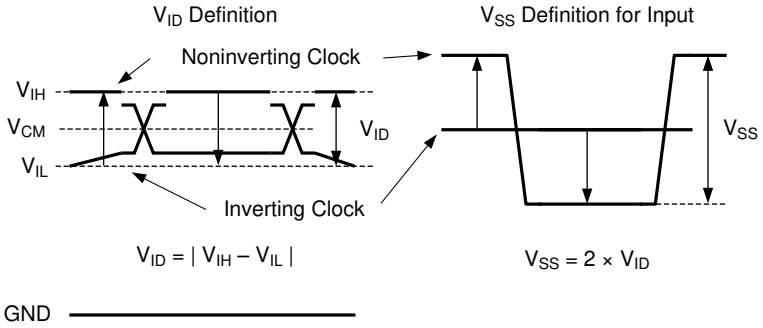

図 7-1. Two Different Definitions for Differential Input Signals

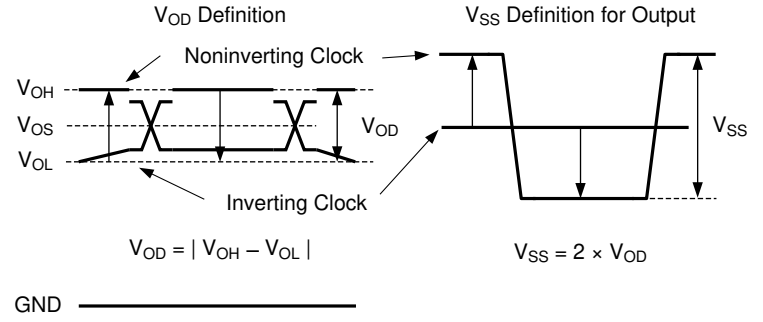

図 7-2. Two Different Definitions for Differential Output Signals

Refer to *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036) for more information.

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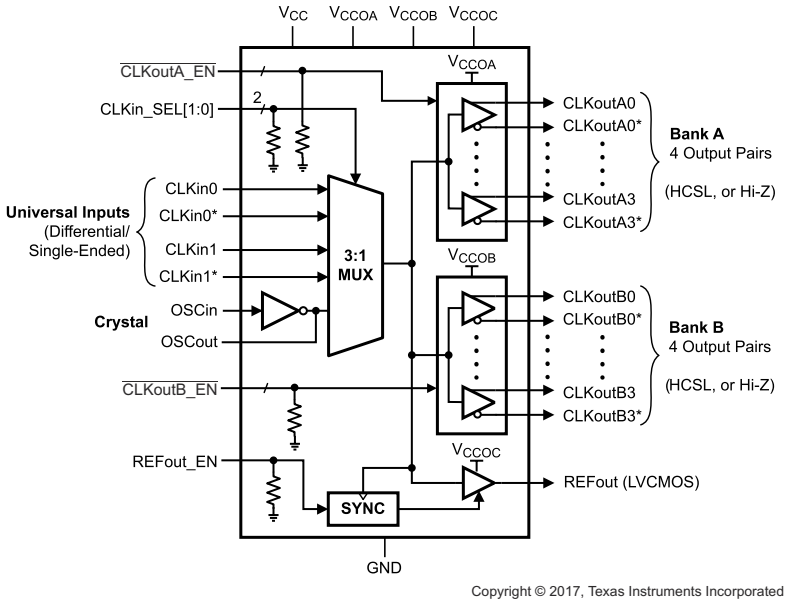
8 Detailed Description

8.1 Overview

The LMK00338 is an 8-output PCIe Gen1/Gen2/Gen3/Gen4/Gen5 clock fanout buffer with low additive jitter that can operate up to 400 MHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 4 HCSL outputs, one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled through pin strapping. The device is offered in a 40-pin WQFN package and leverages much of the high-speed, low-noise circuit design employed in the LMK04800 family of clock conditioners.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Crystal Power Dissipation vs. R_{LIM}

For 図 6-10, the following applies:

- The typical RMS jitter values in the plots show the total output RMS jitter (J_{OUT}) for each output buffer type and the source clock RMS jitter (J_{SOURCE}). From these values, the Additive RMS Jitter can be calculated as: $J_{ADD} = SQRT(J_{OUT}^{2} – J_{SOURCE}^{2})$
- 20-MHz crystal characteristics: Abracon ABL series, AT cut, C_L = 18 pF , C_0 = 4.4 pF measured (7 pF maximum), ESR = 8.5 Ω measured (40 Ω maximum), and Drive Level = 1 mW maximum (100 µW typical).

  40-MHz crystal characteristics: Abracon ABLS2 series, AT cut, C_L = 18 pF , C_0 = 5 pF measured (7 pF maximum), ESR = 5 Ω measured (40 Ω maximum), and Drive Level = 1 mW maximum (100 µW typical).

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8.3.2 Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, CLKin1/CLKin1*, or OSCin. Clock input selection is controlled using the CLKin_SEL[1:0] inputs as shown in 表 8-1. Refer to *Driving the Clock Inputs* for clock input requirements. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator circuit will start up and its clock will be distributed to all outputs. Refer to *Crystal Interface* for more information. Alternatively, OSCin may be driven by a single-ended clock (up to 250 MHz) instead of a crystal.

表 8-1. Input Selection

CLKin_SEL1	CLKin_SEL0	SELECTED INPUT
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin

表 8-2 shows the output logic state vs input state when either CLKin0/CLKin0* or CLKin1/CLKin1* is selected. When OSCin is selected, the output state becomes an inverted copy of the OSCin input state.

表 8-2. CLKin Input vs Output States

STATE of SELECTED CLKin	STATE of ENABLED OUTPUTS
CLKinX and CLKinX* inputs floating	Logic low
CLKinX and CLKinX* inputs shorted together	Logic low
CLKin logic low	Logic low
CLKin logic high	Logic high

8.3.3 Clock Outputs

The HCSL output buffer for Bank A and Bank B outputs can be separately disabled to Hi-Z using the $\overline{\text{CLKoutA\_EN}}$ and $\overline{\text{CLKoutB\_EN}}$ inputs, respectively, as shown in 表 8-3. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length (see note below) to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank will not be used, TI recommends to disable and Hi-Z the bank to reduce power. Refer to *Termination and Use of Clock Drivers* for more information on output interface and termination techniques.

Note

For best soldering practices, the minimum trace length for any unused output pin should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

表 8-3. Differential Output Buffer Type Selection

$\overline{\text{CLKoutX\_EN}}$	CLKoutX BUFFER TYPE (BANK A or B)
0	HCSL
1	Disabled (Hi-Z)

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8.3.3.1 Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the V_{CCO} voltage. REFout can be enabled or disabled using the enable input pin, REFout_EN, as shown in 表 8-4.

表 8-4. Reference Output Enable

REFout_EN	REFout STATE
0	Disabled (Hi-Z)
1	Enabled

The REFout_EN input is internally synchronized with the selected input clock by the SYNC block. This synchronizing function prevents glitches and runt pulses from occurring on the REFout clock when enabled or disabled. REFout is enabled within 3 cycles (t_{EN}) of the input clock after REFout_EN is toggled high. REFout is disabled within 3 cycles (t_{DIS}) of the input clock after REFout_EN is toggled low.

When REFout is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout is configured with a 1-kΩ load to ground, then the output will be pulled to low when disabled.

8.4 Device Functional Modes

8.4.1 V_{CC} and V_{CCO} Power Supplies

The LMK00338 has a 3.3-V core power supply (V_{CC}) and 3 independent 3.3-V or 2.5-V output power supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}). Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5-V receiver devices. The output levels for HCSL are relatively constant over the specified V_{CCO} range. Refer to *Power Supply Recommendations* for additional supply related considerations, such as power dissipation, power supply bypassing, and power supply ripple rejection (PSRR).

Note

Take care to ensure the V_{CCO} voltages do not exceed the V_{CC} voltage to prevent turning-on the internal ESD protection circuitry.

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Application and Implementation

Note

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9.1 Application Information

A common PCIe application, such as a server card, consists of several building blocks, which all need a reference clock. In the mostly used Common RefClk architecture, the clock is distributed from a single source to both RX and TX. This requires either a Clock generator with high output count or a buffer like the LMK00338. The buffer simplifies the clocking tree and provides a cost and space optimized solution. While using a buffer to distribute the clock, the additive jitter needs to be considered. The LMK00338 is an ultra-low additive jitter PCIe clock buffer suitable for all current and future PCIe Generations.

9.2 Typical Application

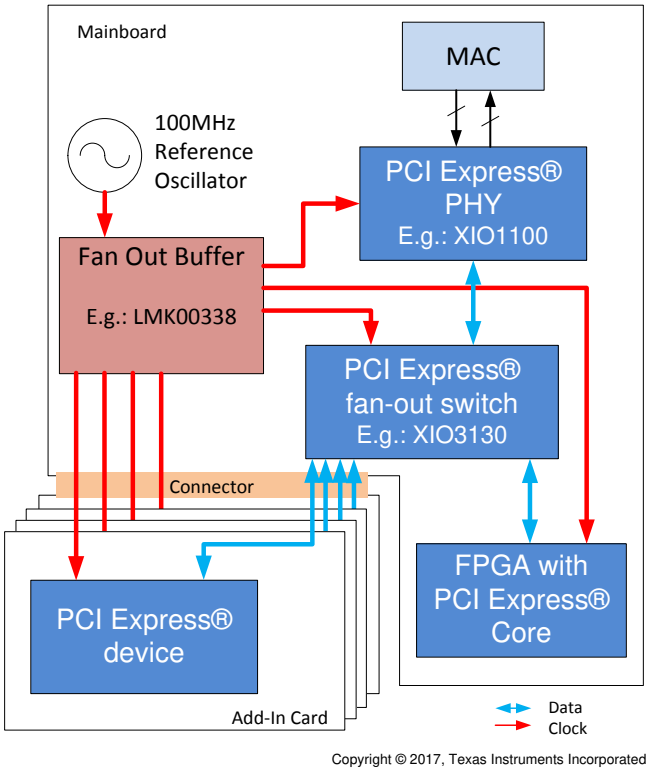

図 9-1. Example PCI Express Application Diagram

9.2.1 Design Requirements

9.2.1.1 Driving the Clock Inputs

The LMK00338 has two universal inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can accept AC- or DC-coupled, 3.3-V and 2.5-V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet the input requirements specified in the *Electrical Characteristics* table. The device can accept a wide range of signals due to its wide input common-mode voltage range (V_{CM}) and input voltage swing (V_{ID}) / dynamic range. For 50% duty cycle and DC-balanced signals, AC coupling may also be employed to shift the input signal to within the V_{CM} range. Refer to *Termination and Use of Clock Drivers* for signal interfacing and termination techniques.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode rejection. Refer to the *Noise Floor vs. CLKin Slew Rate* and *RMS Jitter vs. CLKin Slew Rate* plots in *Typical Characteristics*.

While TI recommends driving the CLKin/CLKin* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the *Electrical Characteristics* table. For large single-ended input signals, such as 3.3-V or 2.5-V LVCMOS, a 50-Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. Again, the single-ended input slew rate should be as high as possible to minimize performance degradation. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC-coupled as shown in 図 9-2. The output impedance of the LVCMOS driver plus Rs should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.

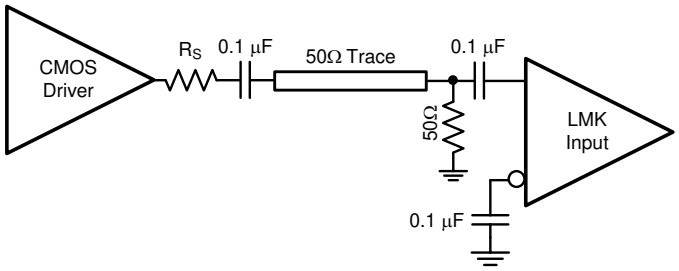

図 9-2. Single-Ended LVCMOS Input, AC Coupling

A single-ended clock may also be DC-coupled to CLKinX as shown in 図 9-3. A 50-Ω load resistor should be placed near the CLKinX input for signal attenuation and line termination. Because half of the single-ended swing of the driver ($V_{O,PP}$ / 2) drives CLKinX, CLKinX* should be externally biased to the midpoint voltage of the attenuated input swing (($V_{O,PP}$ / 2) × 0.5). The external bias voltage should be within the specified input common voltage (V_{CM}) range. This can be achieved using external biasing resistors in the kΩ range (R_{B1} and R_{B2}) or another low-noise voltage reference. This ensures the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

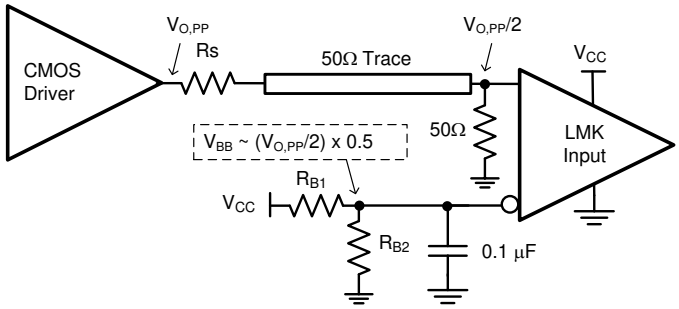

図 9-3. Single-Ended LVCMOS Input, DC Coupling With Common-Mode Biasing

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If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with an single-ended external clock as shown in 図 9-4. The input clock should be AC-coupled to the OSCin pin, which has an internally-generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, TI recommends using either differential input (CLKinX) because it offers higher operating frequency, better common-mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.

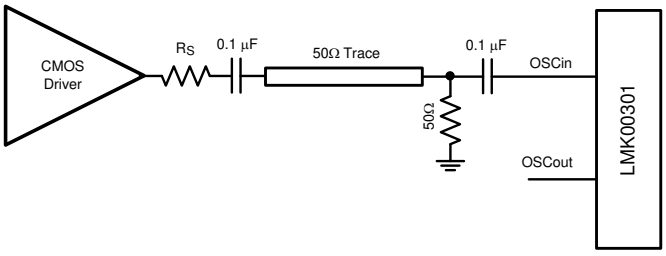

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図 9-4. Driving OSCin With a Single-Ended Input

9.2.1.2 Crystal Interface

The LMK00338 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in 図 9-5.

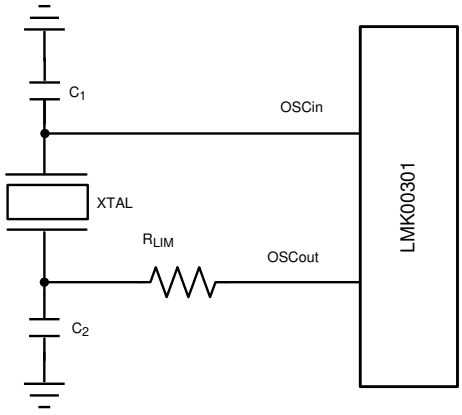

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図 9-5. Crystal Interface

The load capacitance (C_L) is specific to the crystal, but usually on the order of 18 to 20 pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 1 pF typical) of the device and PCB stray capacitance (C_{STRAY} = 1 to approximately 3 pF) can affect the discrete load capacitor values, C_1 and C_2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 \times C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically, $C_1 = C_2$ for optimum symmetry, so 式 1 can be rewritten in terms of C_1 only:

$$C_L = C_1{}^2 / (2 \times C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C_1:

$$C_1 = (C_L - C_{IN} - C_{STRAY}) \times 2 \quad (3)$$

The *Electrical Characteristics* table provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer must ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}^{2} \times R_{ESR} \times (1 + C_0/C_L)^2 \quad (4)$$

where

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the maximum equivalent series resistance specified for the crystal
- C_L is the load capacitance specified for the crystal
- C_0 is the minimum shunt capacitance specified for the crystal

I_{RMS} can be measured using a current probe (for example, Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in 図 9-5, an external resistor, R_{LIM}, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5 kΩ.

9.2.2 Detailed Design Procedure

9.2.2.1 Termination and Use of Clock Drivers

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads.
  - HCSL drivers are switched current outputs and require a DC path to ground through 50-Ω termination.
- Receivers should be presented with a signal biased to their specified DC bias level (common-mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal should normally be AC-coupled.

9.2.2.2 Termination for DC-Coupled Differential Operation

For DC-coupled operation of an HCSL driver, terminate with 50 Ω to ground near the driver output as shown in 図 9-6. Series resistors, Rs, may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50-Ω termination resistors.

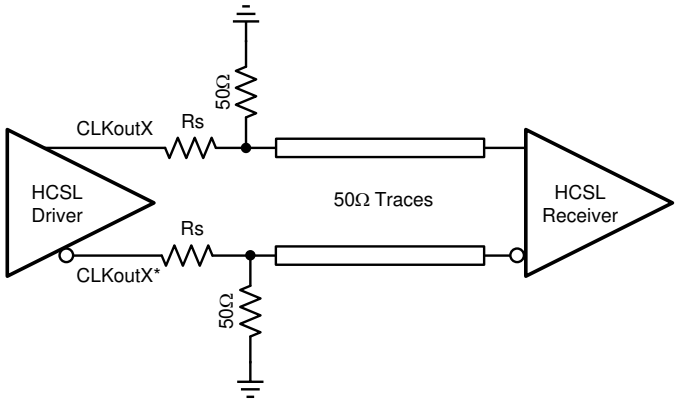

図 9-6. HCSL Operation, DC Coupling

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9.2.2.3 Termination for AC-Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common-mode voltage) when driving different receiver standards. Because AC coupling prevents the driver from providing a DC bias voltage at the receiver, it is important to ensure the receiver is biased to its ideal DC level.

9.2.3 Application Curve

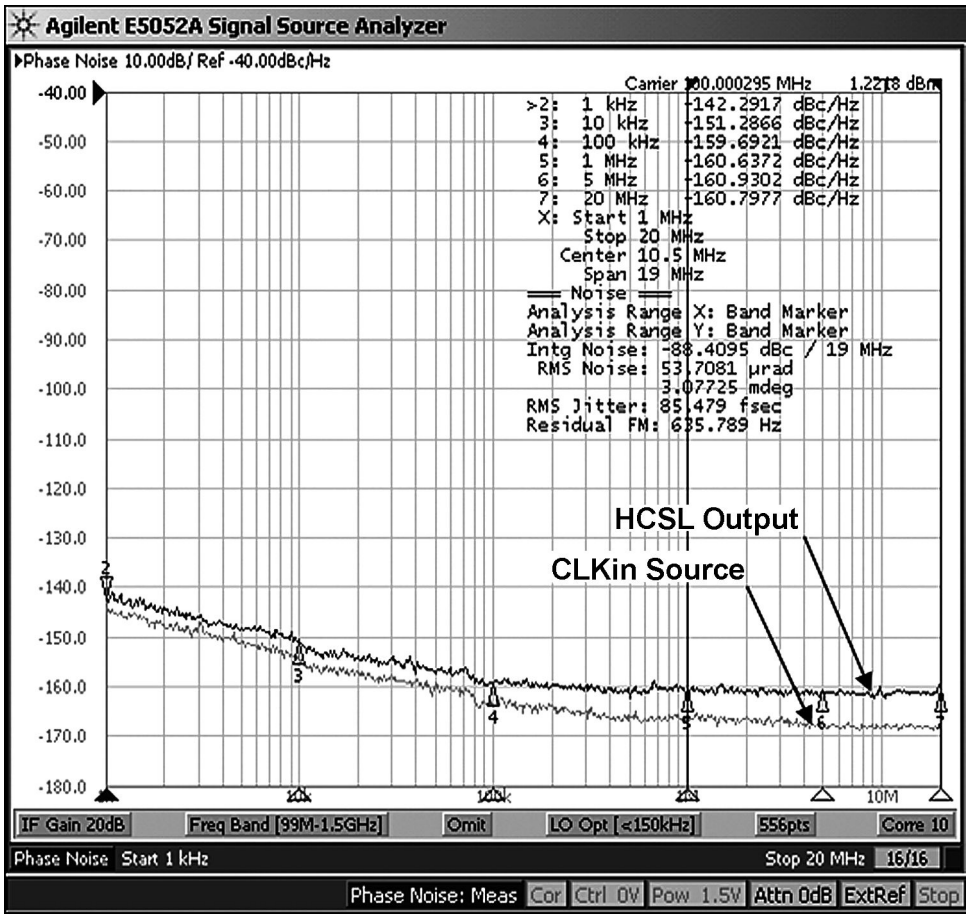

図 9-7. HCSL Phase Noise at 100 MHz

9 Power Supply Recommendations

9.1 Current Consumption and Power Dissipation Calculations

The current consumption values specified in the *Electrical Characteristics* table can be used to calculate the total power dissipation and IC power dissipation for any device configuration. The total V_{CC} core supply current (I_{CC_TOTAL}) can be calculated using 式 5:

$$I_{CC\_TOTAL} = I_{CC\_CORE} + I_{CC\_BANK\_A} + I_{CC\_BANK\_B} + I_{CC\_CMOS} \quad (5)$$

where

- I_{CC_CORE} is the current for core logic and input blocks and depends on selected input (CLKinX or OSCin).
- $I_{CC\_BANK\_A}$ is the current for Bank A.
- $I_{CC\_BANK\_B}$ is the current for Bank B.
- I_{CC_CMOS} is the current for the LVCMOS output (or 0 mA if REFout is disabled).

Because the output supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}) can be powered from 3 independent voltages, the respective output supply currents ($I_{CCO\_BANK\_A}$, $I_{CCO\_BANK\_B}$, and I_{CCO_CMOS}) should be calculated separately. I_{CCO_BANK} for either Bank A or B can be directly taken from the corresponding output supply current spec (I_{CCO_HCSL}) **provided the output loading matches the specified conditions**. Otherwise, I_{CCO_BANK} should be calculated as follows:

$$I_{CCO\_BANK} = I_{BANK\_BIAS} + (N \times I_{OUT\_LOAD}) \quad (6)$$

where

- I_{BANK_BIAS} is the output bank bias current (fixed value).
- I_{OUT_LOAD} is the DC load current per loaded output pair.
- N is the number of loaded output pairs per bank (N = 0 to 4).

表 9-1 shows the typical I_{BANK_BIAS} values and I_{OUT_LOAD} expressions for HCSL.

表 9-1. Typical Output Bank Bias and Load Currents

CURRENT PARAMETER	HCSL
I_{BANK_BIAS}	4.8 mA
I_{OUT_LOAD}	V_{OH}/R_T

Once the current consumption is calculated for each supply, the total power dissipation (P_{TOTAL}) can be calculated as:

$$P_{TOTAL} = (V_{CC} \times I_{CC\_TOTAL}) + (V_{CCOA} \times I_{CCO\_BANK\_A}) + (V_{CCOB} \times I_{CCO\_BANK\_B}) + (V_{CCOC} \times I_{CCO\_CMOS}) \quad (7)$$

If the device configuration is configured with HCSL outputs, then it is also necessary to calculate the power dissipated in any termination resistors (P_{RT_HCSL}). The external power dissipation values can be calculated as follows:

$$P_{RT\_HCSL} \text{ (per HCSL pair)} = V_{OH}^{\ 2} / R_T \quad (8)$$

Finally, the IC power dissipation (P_{DEVICE}) can be computed by subtracting the external power dissipation values from P_{TOTAL} as follows:

$$P_{DEVICE} = P_{TOTAL} - N \times P_{RT\_HCSL} \quad (9)$$

where

- N_2 is the number of HCSL output pairs with termination resistors to GND.

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9.1.1 Power Dissipation Example: Worst-Case Dissipation

This example shows how to calculate IC power dissipation for a configuration to estimate worst-case power dissipation. In this case, the maximum supply voltage and supply current values specified in *セクション 6.5* are used.

- V_{CC} = V_{CCO} = 3.465 V. Maximum I_{CC} and I_{CCO} values.
- CLKin0/CLKin0* input is selected.
- Banks A and B are enabled: all outputs terminated with 50 Ω to GND.
- REFout is enabled with 5-pF load.
- T_A = 85°C

Using the power calculations from the previous section and *maximum* supply current specifications, we can compute P_{TOTAL} and P_{DEVICE}.

- From 式 5: I_{CC_TOTAL} = 10.5 mA + 38.5 mA + 38.5 mA + 5.5 mA = 93 mA
- From I_{CCO_HCSL} maximum spec: $I_{CCO\_BANK\_A}$ = $I_{CCO\_BANK\_B}$ = 84 mA
- From 式 7: P_{TOTAL} = 3.465 V × (93 mA + 84 mA + 84 mA + 10 mA) = 939 mW
- From 式 8: P_{RT_HCSL} = (0.92 V) 2 / 50 Ω = 16.9 mW (per output pair)
- From 式 9: P_{DEVICE} = 939 mW – (8 × 16.9 mW) = 803.8 mW

In this worst-case example, the IC device will dissipate about 803.8 mW or 85.6 of the total power (939 mW), while the remaining 14.4% will be dissipated in the termination resistors (135.2 mW for 8 pairs). Based on θ_{JA} of 31.4°C/W, the estimated die junction temperature would be about 25.2°C above ambient, or 110.2°C when T_A = 85°C.

9.2 Power Supply Bypassing

The V_{CC} and V_{CCO} power supplies should have a high-frequency bypass capacitor, such as 0.1 µF or 0.01 µF, placed very close to each supply pin. 1-µF to 10-µF decoupling capacitors should also be placed nearby the device between the supply and ground planes. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

9.2.1 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, and so on. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00338, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the single-side band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00338, power supply ripple rejection, or PSRR, was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the V_{CCO} supply. The PSRR test setup is shown in 図 9-1.

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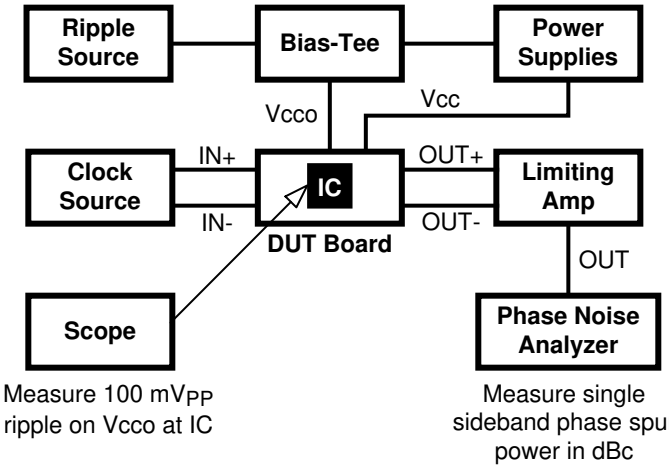

図 9-1. PSRR Test Setup

A signal generator was used to inject a sinusoidal signal onto the V_{CCO} supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the V_{CCO} pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 156.25 MHz and 312.5 MHz under the following power supply ripple conditions:

- Ripple amplitude: 100 mVpp on V_{CCO} = 2.5 V
- Ripple frequencies: 100 kHz, 1 MHz, and 10 MHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$DJ\ (ps\ pk\text{-}pk) = [(2*10^{(PSRR\ /\ 20)}) / (\pi \times f_{CLK})] \times 10^{12} \quad (10)$$

The *PSRR vs. Ripple Frequency* plots in *Typical Characteristics* show the ripple-induced phase spur levels at 156.25 MHz and 312.5 MHz. The LMK00338 exhibits very good and well-behaved PSRR characteristics across the ripple frequency range. The phase spur levels for HCSL are below –72 dBc at 156.25 MHz and below –63 dBc at 312.5 MHz. Using 式 10, these phase spur levels translate to Deterministic Jitter values of 1.02 ps pk-pk at 156.25 MHz and 1.44 ps pk-pk at 312.5 MHz. Testing has shown that the PSRR performance of the device improves for V_{CCO} = 3.3 V under the same ripple amplitude and frequency conditions.

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10 Layout

10.1 Layout Guidelines

- For DC-coupled operation of an HCSL driver, terminate with 50 Ω to ground near the driver output as shown in 図 10-1.
- Keep the connections between the bypass capacitors and the power supply on the device as short as possible
- Ground the other side of the capacitor using a low impedance connection to the ground plane
- If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult
- For component side mounting, use 0201 body size capacitors to facilitate signal routing

10.2 Layout Example

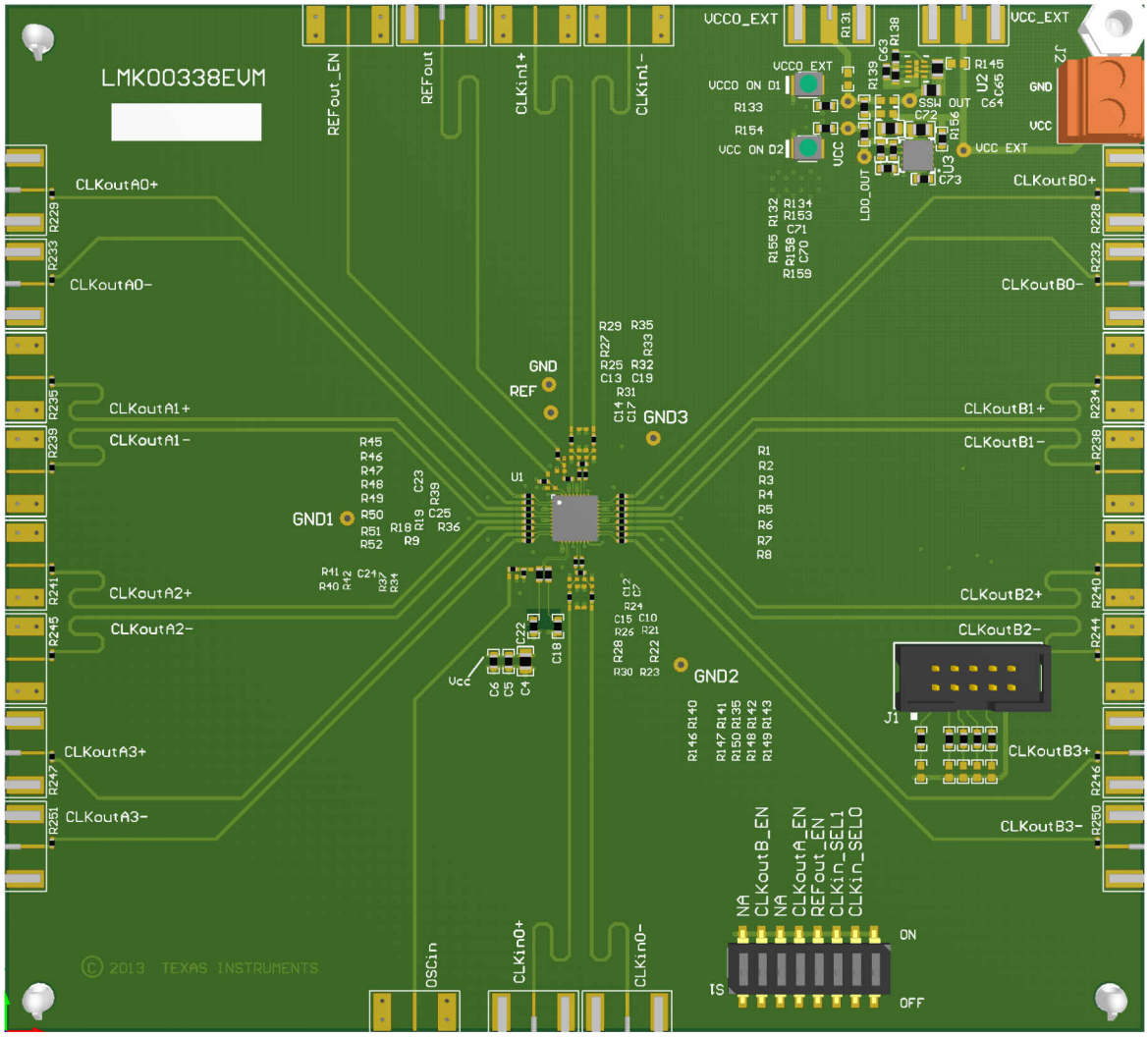

図 10-1. LMK00338 Layout Example

10.3 Thermal Management

Power dissipation in the LMK00338 device can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power dissipation times $R_{\theta JA}$ should not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed-circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in 図 10-2. More information on soldering WQFN packages can be obtained at: https://www.ti.com/packaging.

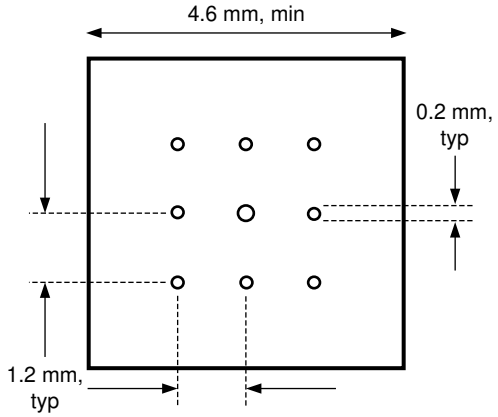

図 10-2. Recommended Land and Via Pattern

To minimize junction temperature, TI recommends building a simple heat sink into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in 図 10-2 should connect these top and bottom copper layers and to the ground layer. These vias act as *heat pipes* to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documents, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549).
- *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036)
- *How to Optimize Clock Distribution in PCIe Applications* on the Texas Instruments E2E community forum.
- *LMK00338EVM User's Guide* (SNAU155).

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11.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK00338RTAR	Active	Production	WQFN (RTA) | 40	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K00338
LMK00338RTAR.A	Active	Production	WQFN (RTA) | 40	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K00338
LMK00338RTAT	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K00338
LMK00338RTAT.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K00338

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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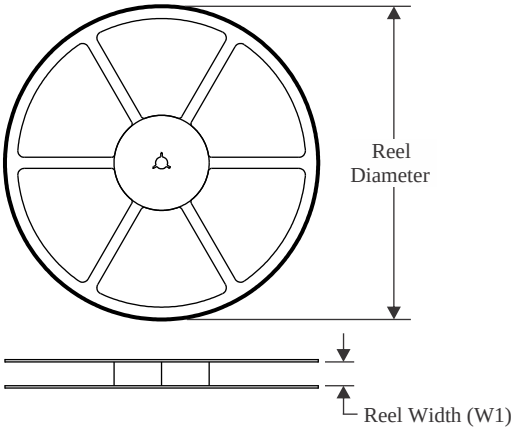
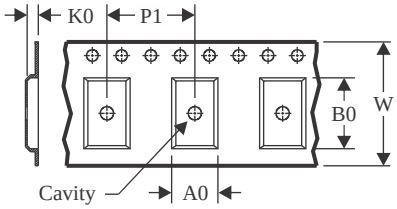
TAPE AND REEL INFORMATION

REEL DIMENSIONS

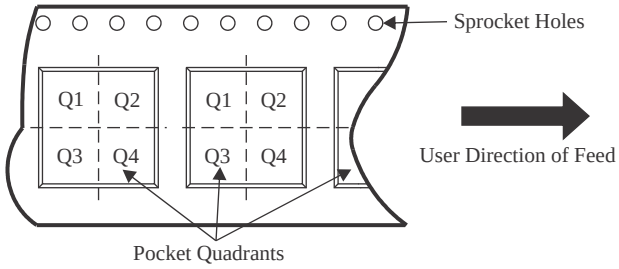


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

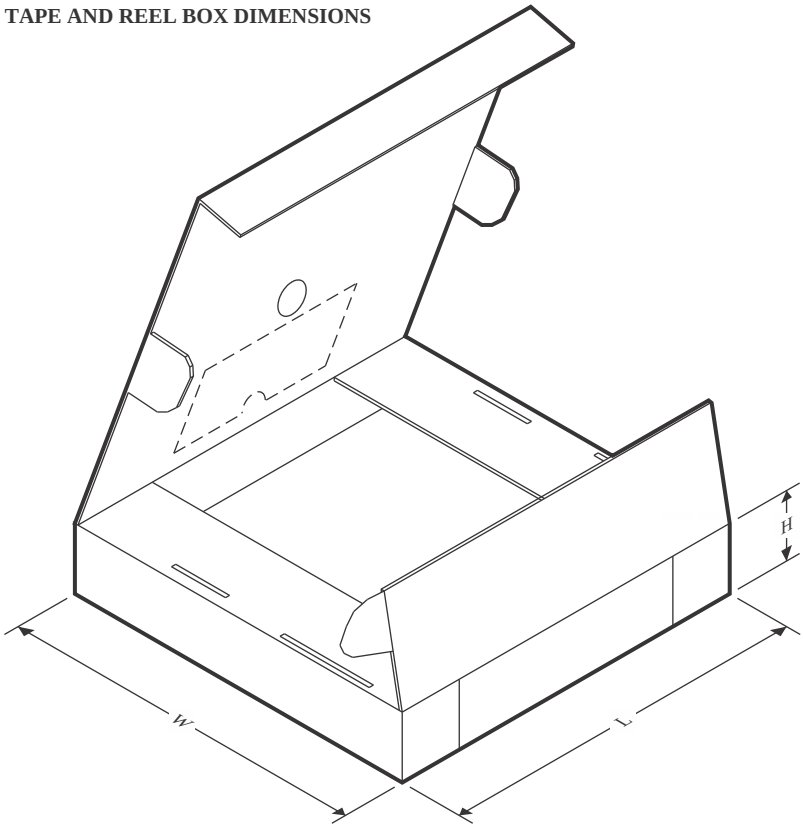
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00338RTAR	WQFN	RTA	40	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMK00338RTAT	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

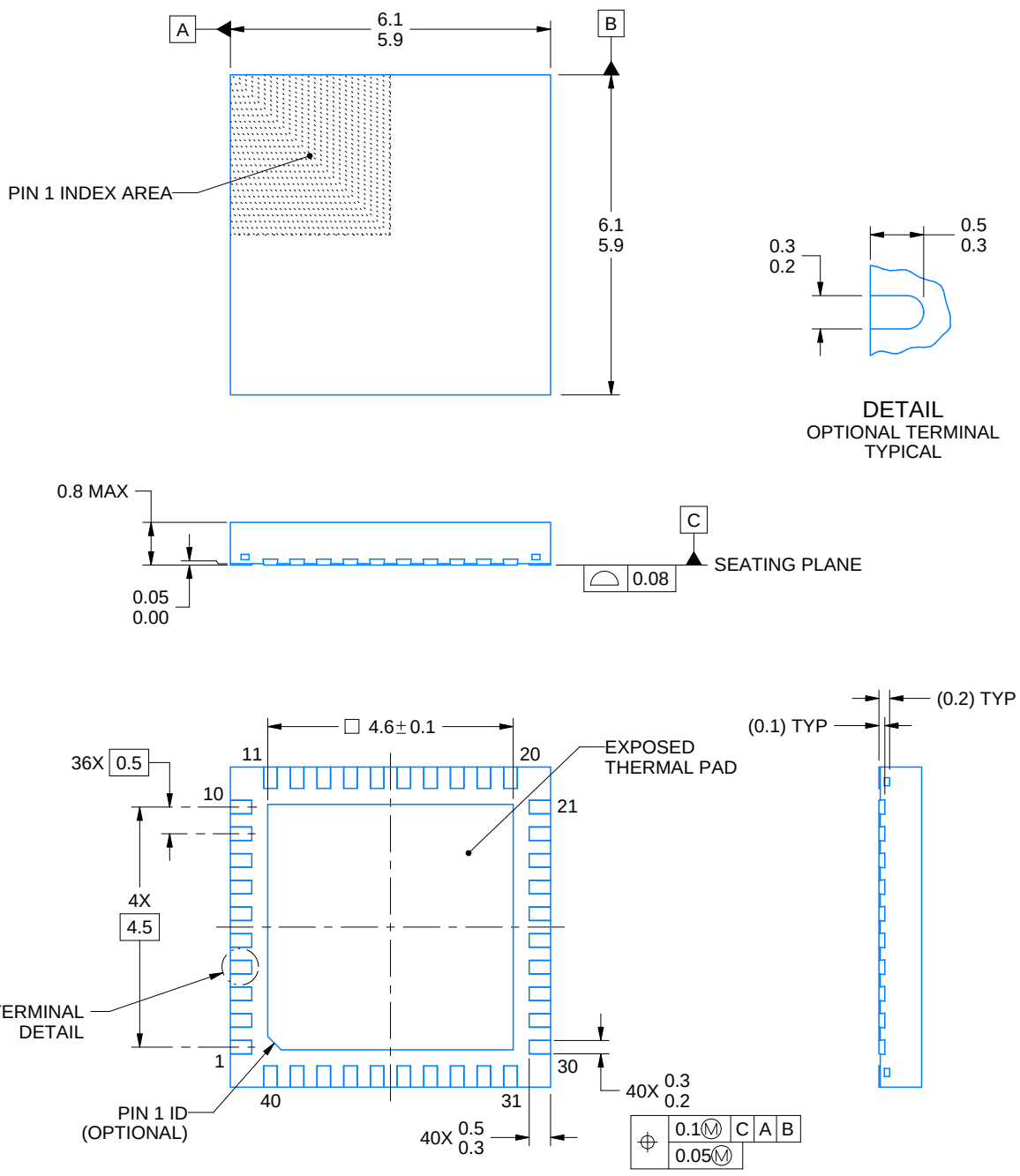
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00338RTAR	WQFN	RTA	40	1000	356.0	356.0	36.0
LMK00338RTAT	WQFN	RTA	40	250	208.0	191.0	35.0

PACKAGE OUTLINE

RTA0040A

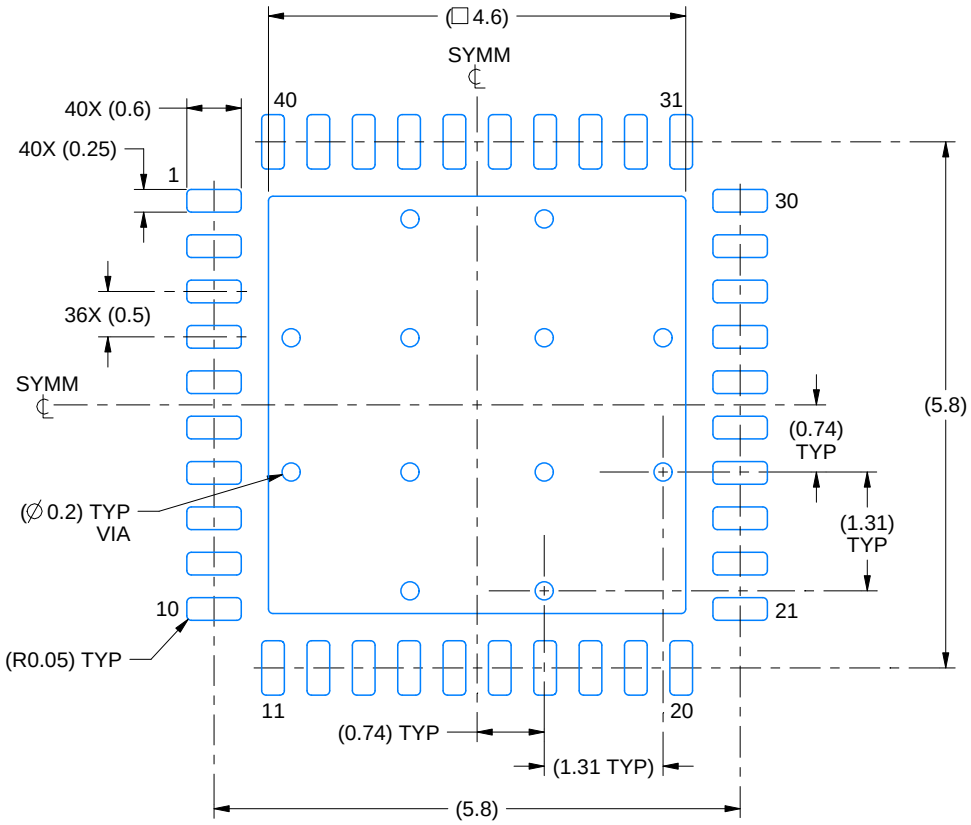
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

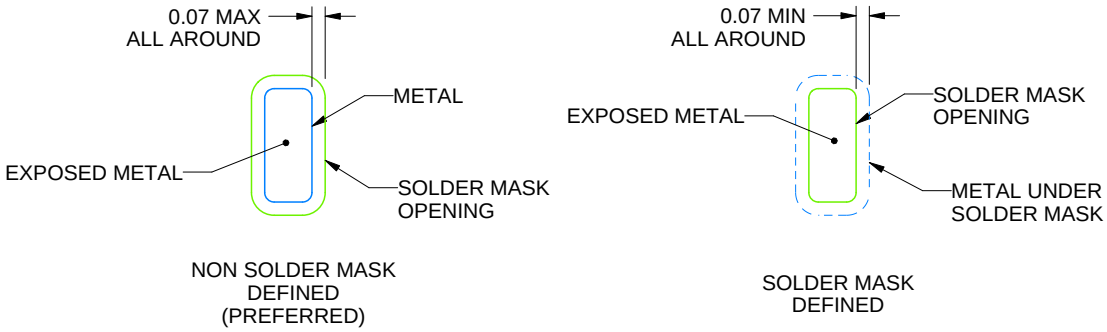


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

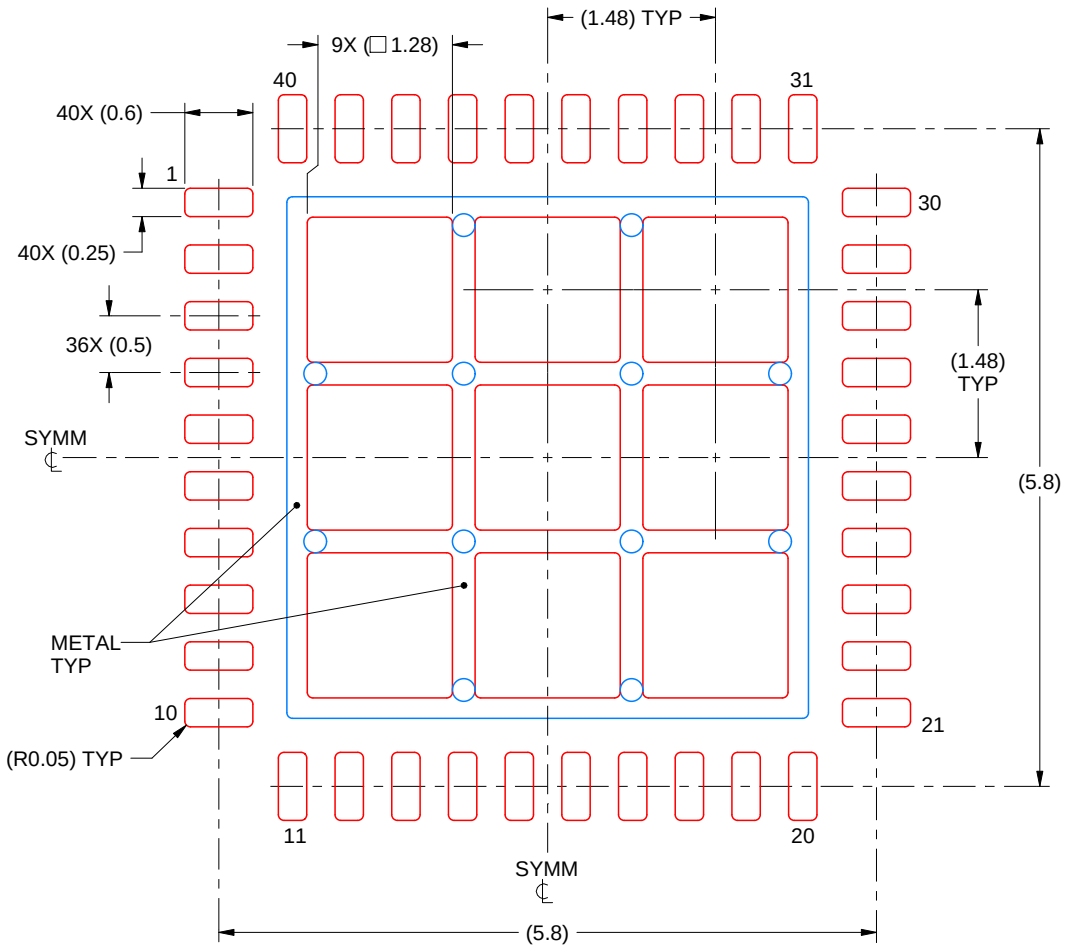


SOLDER MASK DETAILS

4214989/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4214989/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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