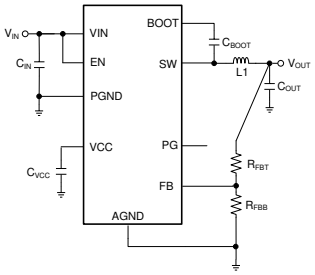
TEXAS INSTRUMENTS
LMR33630
JAJSEU2F – AUGUST 2017 – REVISED NOVEMBER 2020

LMR33630 SIMPLE SWITCHER® 3.8V～36V、3A 同期整流降圧型電圧コンバータ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 堅牢な産業用アプリケーション向けの構成
  - 入力電圧範囲:3.8V～36V
  - 出力電圧範囲:1V～24V
  - 出力電流:3A
  - 75mΩ/50mΩ R_{DS-ON} のパワー MOSFET
  - ピーク電流モード制御
  - 短い最小オン時間:68ns
  - 周波数:400kHz、1.4MHz、2.1MHz
  - 接合部温度範囲:–40℃～+125℃
  - 低い EMI およびスイッチング・ノイズ
  - 補償ネットワークを内蔵
- 低 EMI およびスイッチング・ノイズ
  - HotRod™ パッケージ
  - 並列の入力電流パス
- あらゆる負荷条件での高効率の電力変換
  - ピーク効率:95% 超
  - 低い動作時静止電流:25µA
- 柔軟なシステム・インターフェイス
  - パワー・グッド・フラグおよび高精度イネーブル
- TPSM53603 モジュールを使用して、開発期間を短縮
- WEBENCH® Power Designer により、LMR33630 を使用するカスタム設計を作成



概略回路図

2 アプリケーション

- モータ・ドライブ・システム:ドローン、AC インバータ、VF ドライブ、サーボ
- ファクトリおよびビルディング・オートメーション・システム:
  PLC CPU、HVAC 制御、エレベータ制御
- V_{IN} が広い汎用電源

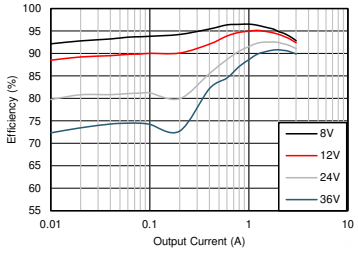
3 概要

LMR33630 SIMPLE SWITCHER® レギュレータは使いやすい同期整流降圧 DC/DC コンバータで、堅牢な産業用アプリケーション向けに、クラス最高の効率を実現しています。LMR33630 デバイスは、最高 36V の入力から最大 3A の負荷電流を駆動でき、非常に小さなソリューション・サイズで、高い軽負荷時効率と出力精度を実現します。パワー・グッド・フラグや高精度イネーブルなどの特長から、広範なアプリケーションにおいて、柔軟で使いやすいソリューションとなります。LMR33630 は軽負荷時に効率向上のため自動的に周波数をフォールドバックします。高度な統合により、ほとんどの外付け部品が不要で、PCB レイアウトが単純になるようピン配置が設計されています。保護機能として、サーマル・シャットダウン、入力低電圧誤動作防止、サイクル単位の電流制限、ヒカップ短絡保護機能が搭載されています。LMR33630 は、8 ピンの HSOIC パッケージと、ウェッタブル・フランク付きの 12 ピン、3mm × 2mm の次世代型 VQFN パッケージで供給されます。また、AEC-Q100 認定済みバージョンも提供しています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LMR33630	HSOIC (8)	5.00mm × 4.00mm
LMR33630	VQFN (12)	3.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流の関係 V_{OUT} = 5V、400kHz、VQFN

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (May 2020) to Revision F (November 2020) — **Page**

- *「特長」*に機能安全の箇条書き項目を追加 ... 1
- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Added RNX pinout drawing ... 4
- Added VQFN package drawing ... 34

Changes from Revision D (March 2019) to Revision E (May 2020) — **Page**

- TPSM53603 製品ページへのリンクを追加 ... 1

Changes from Revision C (June 2018) to Revision D (March 2019) — **Page**

- Changed heading to device option ... 3
- Changed Minimum peak current to reflect ATE data ... 6
- Changed zero cross to reflect ATE data ... 6
- Changed to new current limit equation ... 13
- Added new de-rate curve ... 23

Changes from Revision B (April 2018) to Revision C (June 2018) — **Page**

- Changed heading to device option ... 3
- Added graphs for Typical Switching Frequency in Dropout Mode ... 16

Changes from Revision A (February 2018) to Revision B (April 2018) — **Page**

- データシート全体にわたって WSON の情報を追加 ... 1
- Changed block diagram to fix drawing error ... 10
- Added RNX package drawings ... 0

Changes from Revision * (August 2017) to Revision A (February 2018) — **Page**

- 量産データのデータシートの初版 ... 1

5 Device Comparison Table

DEVICE OPTION	PACKAGE	FREQUENCY	RATED CURRENT	OUTPUT VOLTAGE
LMR33630ADDA	DDA (8-pin HSOIC) 5 × 4 mm	400 kHz	3 A	Adjustable
LMR33630BDDA		1400 kHz	3 A	
LMR33630CDDA		2100 kHz	3 A	
LMR33630ARNX	RNX (12-pin VQFN) 3 × 2 × 0.85 mm	400 kHz	3 A	Adjustable
LMR33630BRNX		1400 kHz	3 A	
LMR33630CRNX		2100 kHz	3 A	

6 Pin Configuration and Functions

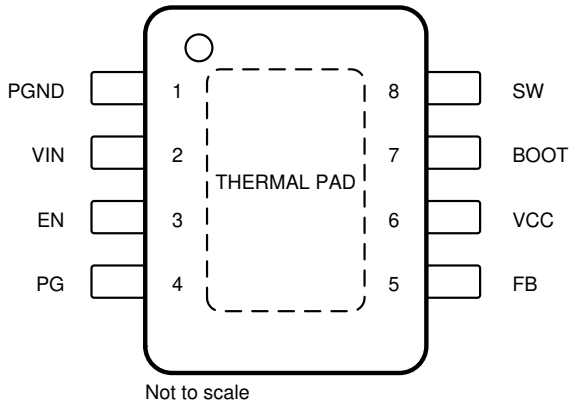


図 6-1. DDA Package 8-Pin HSOIC With PowerPAD™ Top View

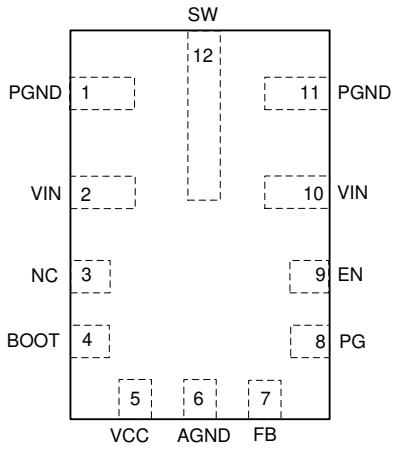


図 6-2. RNX Package 12-Pin VQFN Top View

表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
HSOIC	VQFN	NAME		
1	1,11	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
2	2,10	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and PGND.
3	9	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; *Do not float*.
4	8	PG	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be left open when not used.
5	7	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. *Do not float. Do not ground*.
6	5	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
7	4	BOOT	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
8	12	SW	P	Regulator switch node. Connect to power inductor. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
THERMAL PAD	6	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. For the HSOIC package, the pad on the bottom of the device serves as both the AGND connection and a thermal connection to the heat sink ground plane. This pad must be soldered to a ground plane to achieve good electrical and thermal performance.
—	3	NC	—	On the VQFN package the SW pin must be connected to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin. This pin has no internal connection to the regulator.
A = Analog, P = Power, G = Ground				

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to PGND	–0.3	38	V
	EN to AGND(2)	–0.3	V_{IN} + 0.3	
	FB to AGND	–0.3	5.5	
	PG to AGND(2)	0	22	
	AGND to PGND	–0.3	0.3	
	SW to PGND	–0.3	V_{IN} + 0.3	V
	SW to PGND less than 100-ns transients	–3.5	38	
	BOOT to SW	–0.3	5.5	
	VCC to AGND(4)	–0.3	5.5	
T_J	Junction temperature(3)	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V
(3) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.
(4) Under some operating conditions the VCC LDO voltage may increase beyond 5.5V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±2500	V
		Charged-device model (CDM) (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating temperature range of –40 °C to 125 °C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	3.8	36	V
	EN (2)	0	V_{IN}	
	PG(2)	0	18	
Adjustable output voltage	V_{OUT} (3)	1	24	V
Output current	I_{OUT}	0	3	A

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *セクション 7.5*.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The maximum output voltage can be extended to 95% of V_{IN}; contact TI for details. Under no conditions should the output voltage be allowed to fall below zero volts.

7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

THERMAL METRIC(1) (2)		LMR336x0		UNIT
		DDA (HSOIC)	RNX (VQFN)	
		8 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9(2)	72.5(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.8	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

7.5 Electrical Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Minimum operating input voltage				3.8	V
I_Q	Non-switching input current; measured at VIN pin (2)	V_{FB} = 1.2 V		24	34	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN = 0		5	10	µA
ENABLE						
$V_{EN-VCC-H}$	EN input level required to turn on internal LDO	Rising threshold			1	V
$V_{EN-VCC-L}$	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V_{EN-H}	EN input level required to start switching	Rising threshold	1.2	1.231	1.26	V
V_{EN-HYS}	Hysteresis below V_{EN-H}	Hysteresis below V_{EN-H}; falling		100		mV
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3 V		0.2		nA
INTERNAL SUPPLIES						
VCC	Internal LDO output voltage appearing at the VCC pin	6 V ≤ V_{IN} ≤ 36 V	4.75	5	5.25	V
$V_{BOOT-UVLO}$	Bootstrap voltage undervoltage lock-out threshold(3)			2.2		V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage; ADJ option		0.985	1	1.015	V
I_{FB}	Current into FB pin; ADJ option	FB = 1 V		0.2	50	nA
CURRENT LIMITS(4)						
I_{SC}	High-side current limit	LMR33630	3.85	4.5	5.05	A
I_{LIMIT}	Low-side current limit	LMR33630	2.9	3.5	4.1	A
$I_{PEAK-MIN}$	Minimum peak inductor current	LMR33630		0.69		A

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ZC}	Zero current detector threshold			-0.106		A
SOFT START						
t_{SS}	Internal soft-start time		2.9	4	6	ms
POWER GOOD (PG PIN)						
$V_{PG-HIGH-UP}$	Power-good upper threshold - rising	% of FB voltage	105%	107%	110%	
$V_{PG-HIGH-DN}$	Power-good upper threshold - falling	% of FB voltage	103%	105%	108%	
$V_{PG-LOW-UP}$	Power-good lower threshold - rising	% of FB voltage	92%	94%	97%	
$V_{PG-LOW-DN}$	Power-good lower threshold - falling	% of FB voltage	90%	92%	95%	
t_{PG}	Power-good glitch filter delay(1)		60		170	µs
R_{PG}	Power-good flag R_{DSON}	V_{IN} = 12 V, V_{EN} = 4 V		76	150	Ω
		V_{EN} = 0 V		35	60	
V_{IN-PG}	Minimum input voltage for proper PG function	50-µA, EN = 0 V			2	V
V_{PG}	PG logic low output	50-µA, EN = 0 V, V_{IN} = 2V			0.2	V
OSCILLATOR						
f_{SW}	Switching frequency	"A" Version	340	400	460	kHz
f_{SW}	Switching frequency	"B" Version	1.2	1.4	1.6	MHz
f_{SW}	Switching frequency	"C" Version, DDA package	1.8	2.1	2.4	MHz
f_{SW}	Switching frequency	"C" Version, RNX package	1.8	2.1	2.3	MHz
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	RNX package		75	145	mΩ
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	DDA package		95	160	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	RNX package		50	95	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	DDA package		66	110	mΩ

(1) See *Power-Good Flag Output* for details.
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turned on to recharge C_{BOOT}.
(4) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

7.6 Timing Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

			MIN	NOM	MAX	UNIT
t_{ON-MIN}	Minimum switch on-time	RNX package		68	80	ns
t_{ON-MIN}	Minimum switch on-time	DDA package		75	108	ns
$t_{OFF-MIN}$	Minimum switch off-time	RNX package		52	70	ns
$t_{OFF-MIN}$	Minimum switch off-time	DDA package		50	85	ns
t_{ON-MAX}	Maximum switch on-time			7	9	µs

7.7 System Characteristics

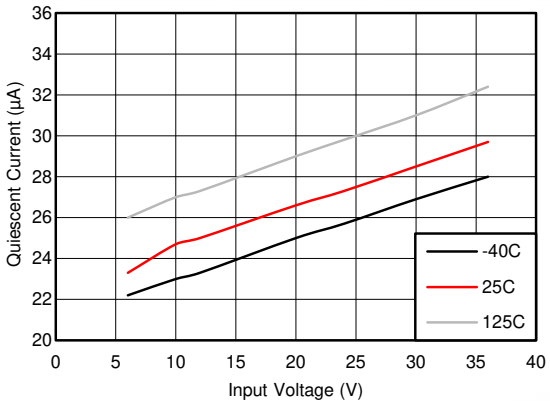
The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. *These specifications are not ensured by production testing.*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range	V_{OUT} = 3.3 V, I_{OUT}= 0 A	3.8		36	V
V_{OUT}	Output voltage regulation for V_{OUT} = 5 V(1)	V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 0 A to max. load	–1.5%		2.5%	
		V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 1 A to max. load	–1.5%		1.5%	
	Output voltage regulation for V_{OUT} = 3.3 V(1)	V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 0 A to max. load	–1.5%		2.5%	
		V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 1 A to max. load	–1.5%		1.5%	
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, R_{FBT} = 1 MΩ		25		µA
V_{DROP}	Dropout voltage; (V_{IN} – V_{OUT})	V_{OUT} = 5 V, I_{OUT} = 1A Dropout at –1% of regulation, f_{SW} = 140 kHz		150		mV
D_{MAX}	Maximum switch duty cycle(2)	V_{IN} = V_{OUT} = 12 V, I_{OUT} = 1 A		98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
t_D	Switch voltage dead time			2		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		165		°C
		Recovery temperature		148		°C

(1) Deviation is with respect to V_{IN} =12 V, I_{OUT} = 1 A.
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $t_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} /(t_{ON-MAX} + $t_{OFF-MIN}$).

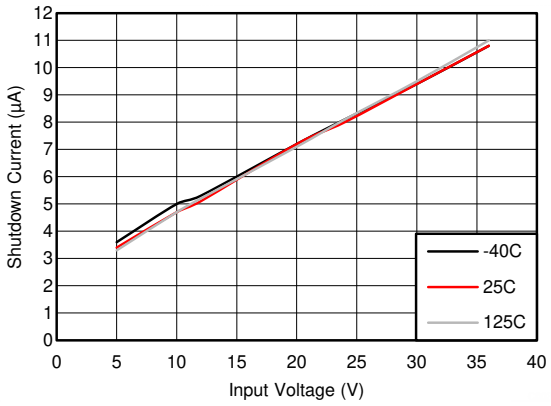
7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: T_A = 25°C and V_{IN} = 12 V



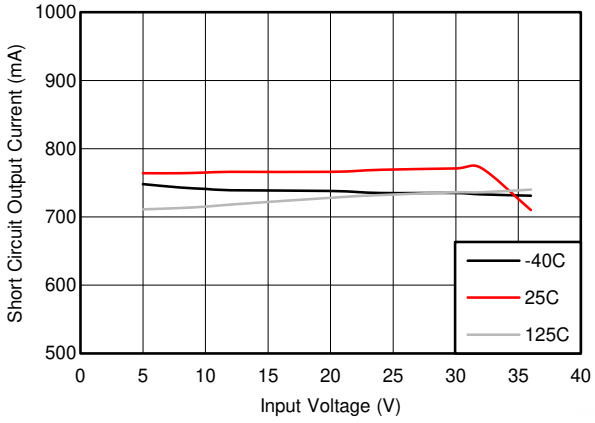
V_{FB} = 1.2 V

図 7-1. Non-Switching Input Supply Current



EN = 0 V

図 7-2. Shutdown Supply Current



V_{OUT} = 0 V f_S = 400 kHz See 図 9-31

図 7-3. Short-Circuit Output Current

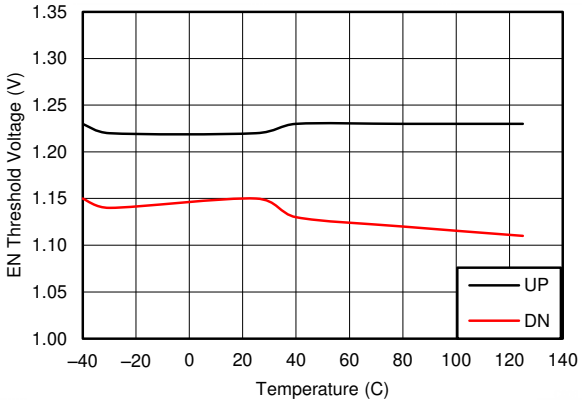
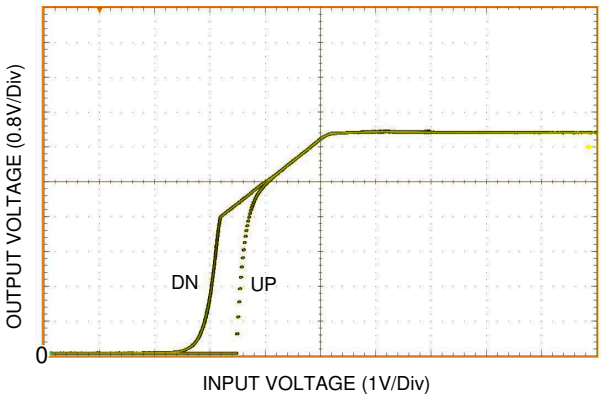
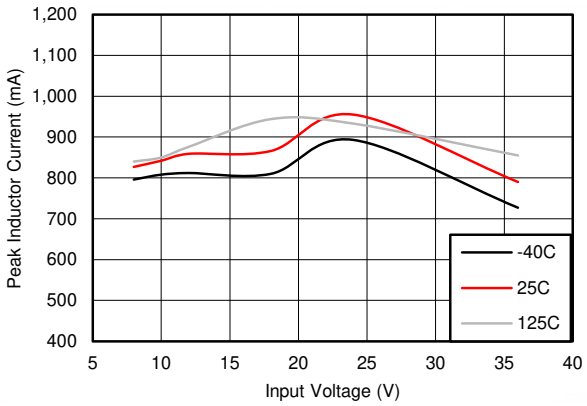


図 7-4. Precision Enable Thresholds



I_{OUT} = 1 mA See 図 9-31

図 7-5. UVLO Thresholds



I_{OUT} = 0 A V_{OUT} = 5 V See 図 9-31
f_{SW} = 400 kHz

図 7-6. $I_{PEAK-MIN}$

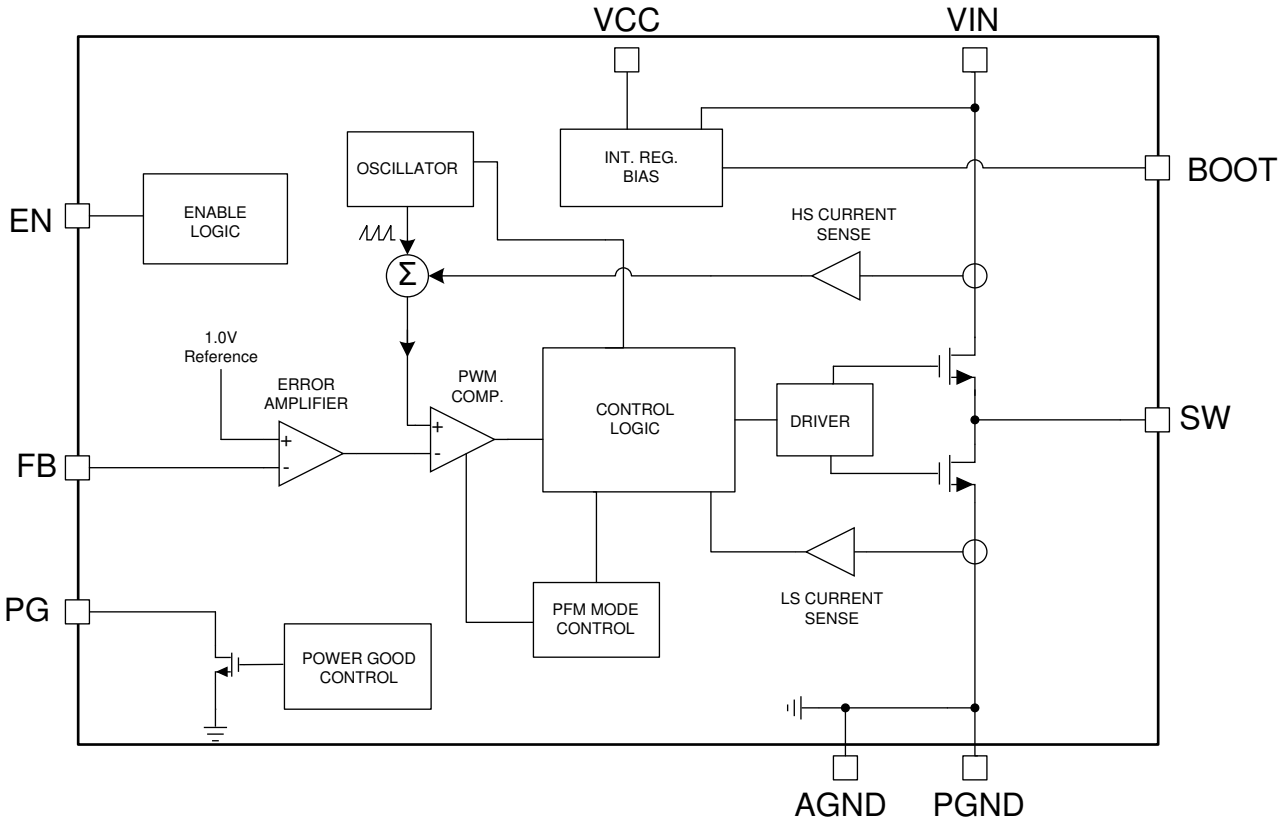
8 Detailed Description

8.1 Overview

The LMR33630 is a synchronous peak-current-mode buck regulator designed for a wide variety of industrial applications. Advanced high speed circuitry allows the device to regulate from an input voltage of 20 V, while providing an output voltage of 3.3 V at a switching frequency of 2.1 MHz. The innovative architecture allows the device to regulate a 3.3-V output from an input of only 3.8 V. The regulator automatically switches modes between PFM and PWM depending on load. At heavy loads, the device operates in PWM at a constant switching frequency. At light loads, the mode changes to PFM with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

The LMR33630 is available in an ultra-miniature VQFN package with wettable flanks. This package features extremely small parasitic inductance and resistance, enabling very high efficiency while minimizing switch node ringing and dramatically reducing EMI. The VIN/PGND pin layout is symmetrical on either side of the VQFN package. This allows the input current magnetic fields to partially cancel, resulting in reduce EMI generation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR33630 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in *セクション 7.5*. Output voltage excursions lasting less than t_{PG} do not trip the power-good flag. Power-good operation can best be understood by reference to 図 8-1 and 図 8-2. Note that during initial power up, a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open-drain NMOS, requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or V_{OUT}, through a 100-kΩ resistor, as desired. If this function is not needed, the PG pin must be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into the power-good flag pin to less than 5 mA D.C. The maximum current is internally limited to about 35 mA when the device is enabled and about 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that can occur when discharging a filter capacitor connected to this output.

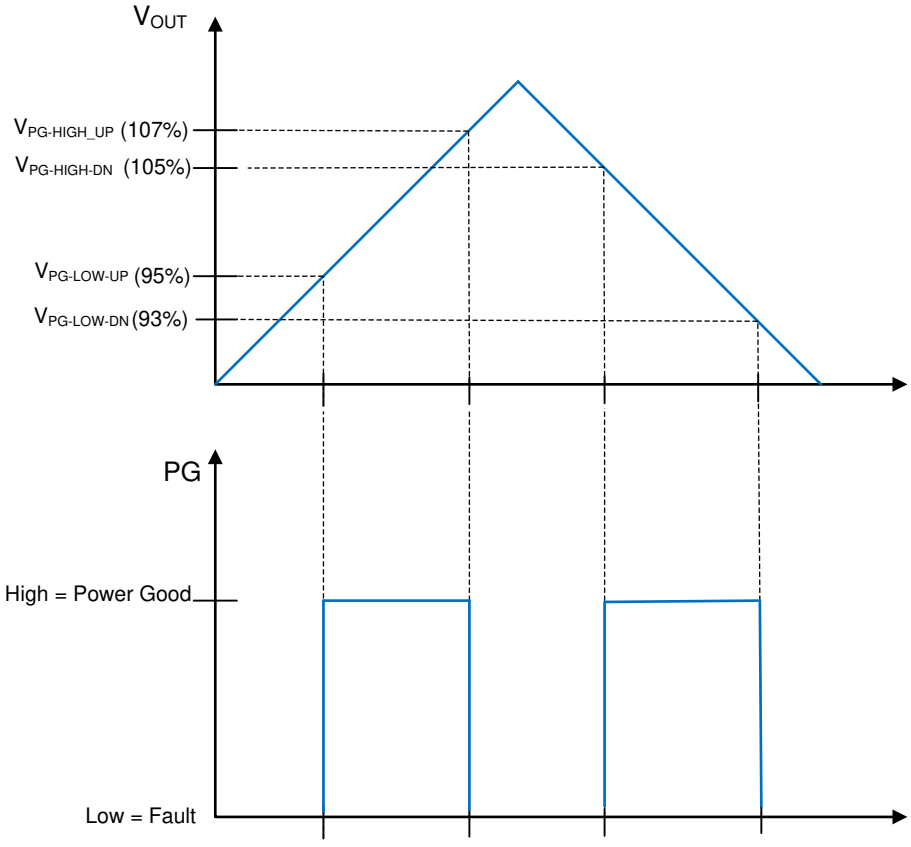


図 8-1. Static Power-Good Operation

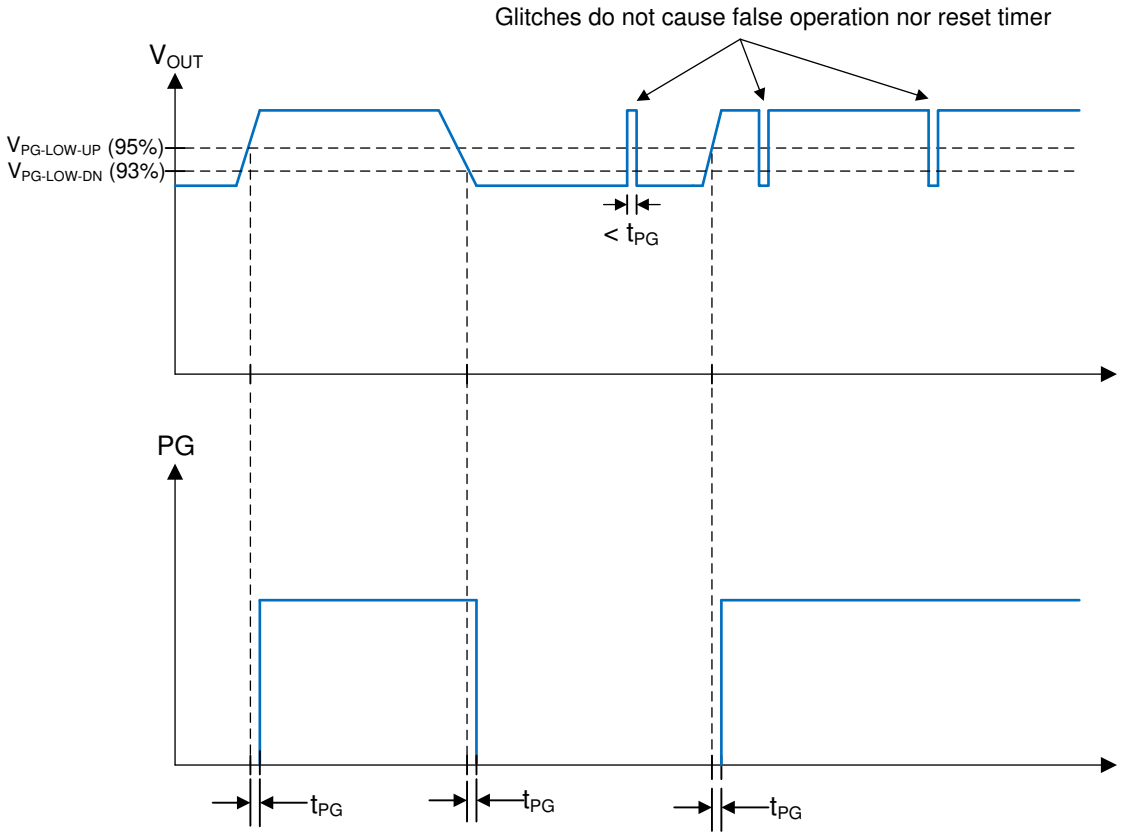


図 8-2. Power-Good-Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see *セクション 9.2.2.10*). Applying a voltage of ≥ V_{EN-VCC_H} causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to V_{EN-H} fully enables the device, allowing it to enter start-up mode and starting the soft-start period. When the EN input is brought below V_{EN-H} by V_{EN-HYS}, the regulator stops running and enters standby mode. Further decrease in the EN voltage to below $V_{EN-VCC-L}$ completely shuts down the device. This behavior is shown in 図 8-3. The EN input can be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in *セクション 7.5* .

The LMR33630 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. A typical start-up waveform is shown in 図 8-4, indicating typical timings. The rise time of the output voltage is about 4 ms (see *セクション 7.5*).

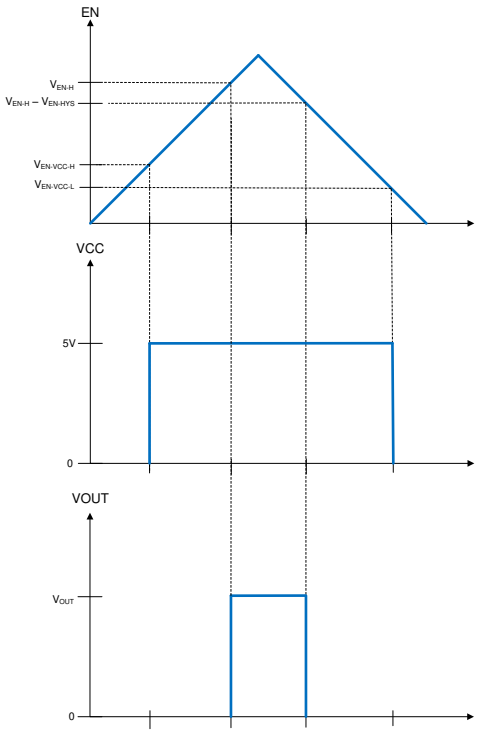


図 8-3. Precision Enable Behavior

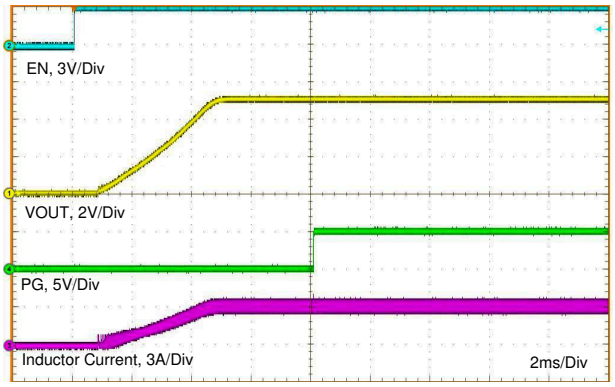


図 8-4. Typical Start-up Behavior V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A

8.3.3 Current Limit and Short Circuit

The LMR33630 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see the *Glossary*). The typical value of this current limit is found under I_{ZC} in *セクション 7.5* .

When the device is overloaded, the valley of the inductor current may not reach below I_{LIMIT} (see *セクション 7.5*) before the next clock cycle. When this occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, and the inductor ripple current to increase. When the peak of the inductor current reaches the high-side current limit, I_{SC}

(see セクション 7.5), the switch duty cycle is reduced and the output voltage falls out of regulation. This represents the maximum output current from the converter and is given approximately by 式 1.

$$I_{OUT}|_{max} = \frac{I_{LIMIT} + I_{SC}}{2} \quad (1)$$

If, during current limit, the voltage on the FB input falls below about 0.4 V due to a short circuit, the device enters into hiccup mode. In this mode, the device stops switching for t_{HC} (see セクション 7.7), or about 94 ms and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in 図 8-5 as long as the short-circuit-condition persists. This mode of operation helps reduce the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode. Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally as shown in 図 8-6.

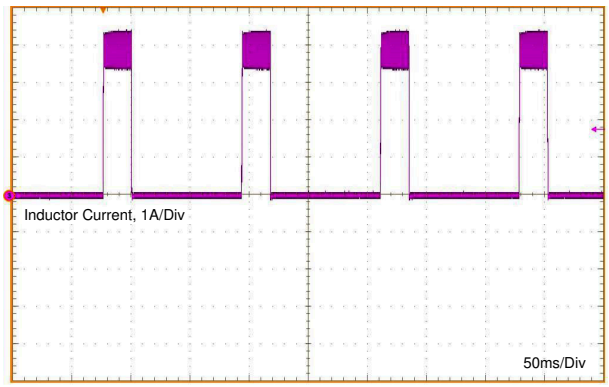


図 8-5. Inductor Current Burst in Short-Circuit Mode

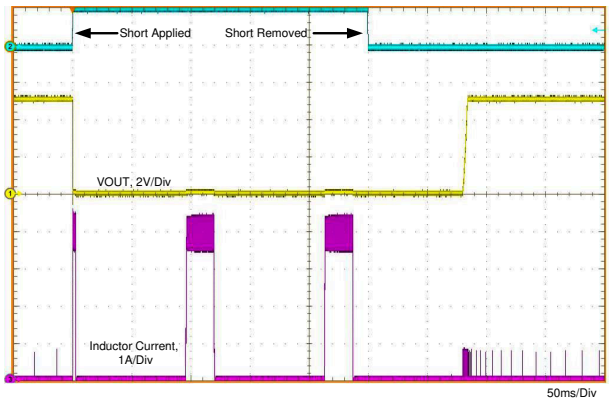


図 8-6. Short-Circuit Transient and Recovery

8.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR33630 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V, the device is ready to receive an EN signal and start up. When VCC falls below about 3 V, the device shuts down, regardless of EN status. Because the LDO is in dropout during these transitions, the above values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C the device shuts down; re-start occurs when the temperature falls to about 148°C.

8.4 Device Functional Modes

8.4.1 Auto Mode

In auto mode, the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM. The load current for which the device moves from PFM to PWM can be found in セクション 9.2.3. The output current at which the device changes modes depends on the input voltage, inductor value, and the nominal switching frequency. For output currents above the curve, the device is in PWM mode. For currents below the curve, the device is in PFM. The curves apply for and the BOM shown in 表 9-4 and a nominal switching frequency of 400 kHz. At higher switching frequencies, the load at which the mode change occurs is greater. For applications where the switching frequency must be known for a given condition, the transition between PFM and PWM must be carefully tested before the design is finalized.

In PWM mode, the regulator operates as a constant frequency converter using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and

modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The periodicity of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see the *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at light loads. PFM results in very good light-load efficiency, but also yields larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. Typical switching waveforms in PFM and PWM are shown in 図 8-7 and 図 8-8.

See *セクション 9.2.3* for output voltage variation with load in auto mode.

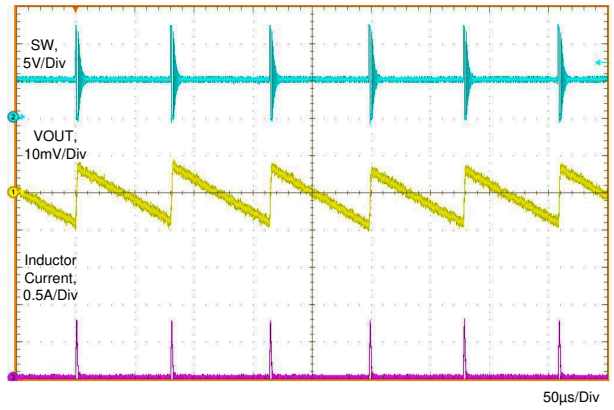


図 8-7. Typical PFM Switching Waveforms V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 10 mA

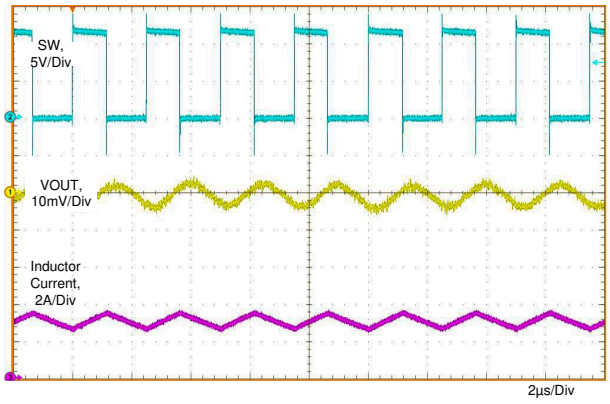


図 8-8. Typical PWM Switching Waveforms V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A, f_S = 400 kHz

8.4.2 Dropout

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off-time of the high-side MOSFET starts to approach the minimum value (see *セクション 7.6*). Beyond this point, the switching can become erratic, and the output voltage falls out of regulation. To avoid this problem, the LMR33630 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet, the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition, the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode. Typical dropout characteristics can be found in 図 8-9, 図 8-10, 図 8-11, and 図 8-12.

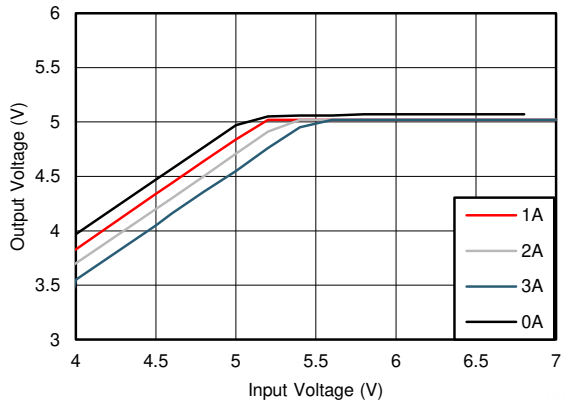


図 8-9. Overall Dropout Characteristic V_{OUT} = 5 V

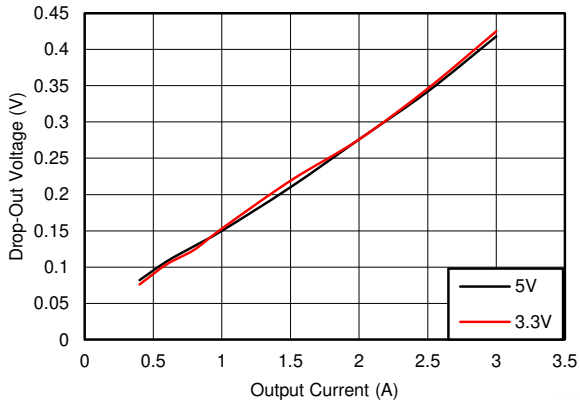


図 8-10. Typical Dropout Voltage versus Output Current in Frequency Foldback f_{SW} = 140 kHz

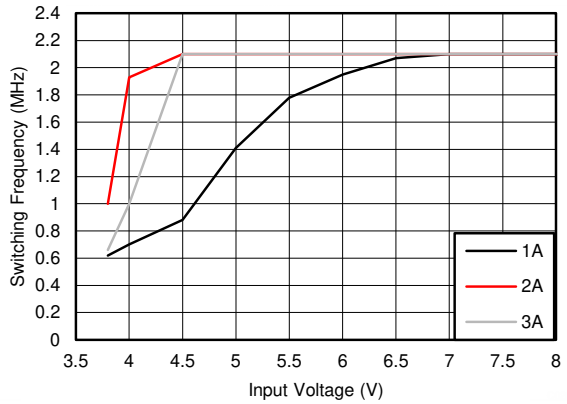


図 8-11. Typical Switching Frequency in Dropout Mode V_{OUT} = 3.3 V, f_{SW} = 2.1 MHz

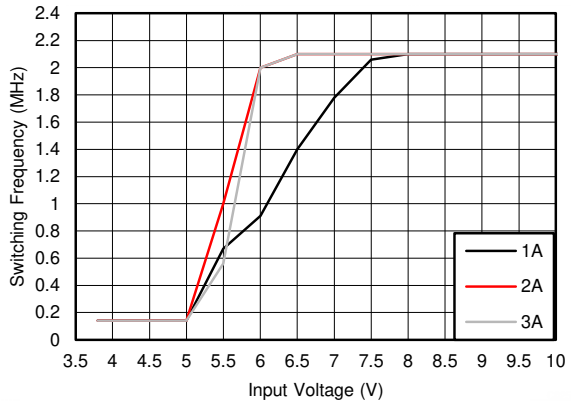


図 8-12. Typical Switching Frequency in Dropout Mode V_{OUT} = 5 V, f_{SW} = 2.1 MHz

8.4.3 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR33630 automatically reduces the switching frequency when the minimum on-time limit is reached. This way the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage, for a given output voltage, before frequency foldback occurs is found in 式 2. The values of t_{ON} and f_{SW} can be found in *セクション 7.5*. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops, while the on-time remains fixed. This relationship is highlighted in 図 8-13 for a nominal switching frequency of 2.1 MHz.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \tag{2}$$

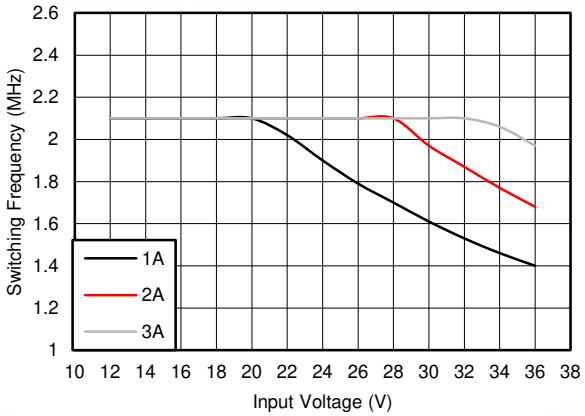


図 8-13. Switching Frequency versus Input Voltage V_{OUT} = 3.3 V

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The LMR33630 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LMR33630. Alternately, the WEBENCH Design Tool can be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

Note

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature; not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias the capacitance drops considerably. Large case sizes and/or higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank should be made in order to ensure that the minimum value of *effective* capacitance is provided.

9.2 Typical Application

図 9-1 shows a typical application circuit for the LMR33630. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, 図 9-1 provides typical component values for a range of the most common output voltages. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application. Note that for the VQFN package, the input capacitors are split and placed on either side of the package; see *セクション 9.2.2.6* for more details.

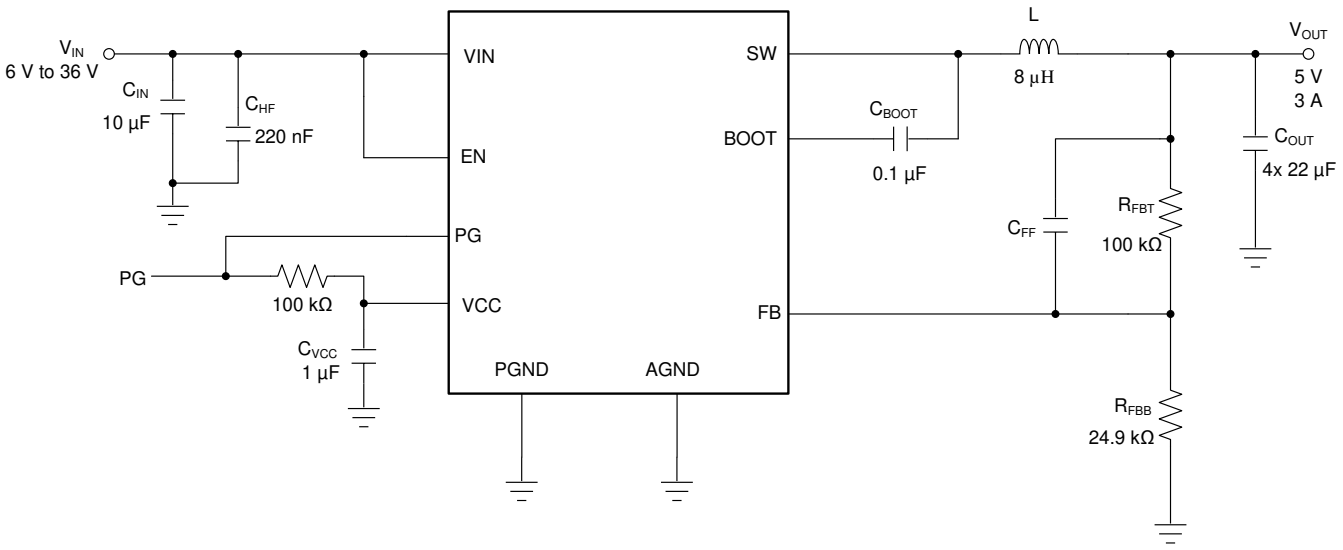


図 9-1. Example Application Circuit (400 kHz)

9.2.1 Design Requirements

表 9-1 provides the parameters for our detailed design procedure example:

表 9-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 3 A
Switching frequency	400 kHz

表 9-2. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN} + C_{HF}	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3	6.8	4 × 22 µF	100 k	43.2 k	10 µF + 220 nF	100 nF	1 µF	open
1400	3.3	2.2	2 × 22 µF	100 k	43.2 k	10 µF + 220 nF	100 nF	1 µF	open
2100	3.3	1.2	2 × 22 µF	100 k	43.2 k	10 µF + 220 nF	100 nF	1 µF	open
400	5	8	4 × 22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF	open
1400	5	2.2	2 × 22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF	open
2100	5	1.5	2 × 22 µF	100 k	24.9 k	10 µF + 220 nF	100 nF	1 µF	open
400	12	15	4 × 22 µF	100 k	9.09 k	10 µF + 220 nF	100 nF	1 µF	open
1400	12	4.7	4 × 10 µF	100 k	9.09 k	10 µF + 220 nF	100 nF	1 µF	open
2100	12	3.3	4 × 10 µF	100 k	9.09 k	10 µF + 220 nF	100 nF	1 µF	open

9.2.2 Detailed Design Procedure

The following design procedure applies to 図 9-1 and 表 9-1.

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR33630 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence a more compact design. For this example, 400 kHz was chosen.

9.2.2.3 Setting the Output Voltage

The output voltage of the LMR33630is externally adjustable using a resistor divider network. The range of recommended output voltage is found in *セクション 7.3*. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pick-up and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ; with a maximum value of 1 MΩ. If a 1 MΩ is selected for R_{FBT}, then a feedforward capacitor must be used across this resistor to provide adequate loop phase margin (see *セクション 9.2.2.9*). Once R_{FBT} is selected, 式 3 is used to select R_{FBB}. V_{REF} is nominally 1 V (see *セクション 7.5* for limits).

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \tag{3}$$

For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ are chosen.

9.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current should be used. 式 4 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, K = 0.3 was chosen and an inductance L = 8.1 µH was found; the next standard value of 8 µH was selected.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{4}$$

Ideally, the saturation current rating of the inductor must be at least as large as the high-side switch current limit, I_{SC} (see *セクション 7.5*). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage; do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing for some relaxation in the current rating of the inductor. However, they have more core

losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device low-side current limit, I_{LIMIT} (see セクション 7.5). The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L_{MIN} \geq 0.28 \cdot \frac{V_{OUT}}{f_{SW}} \tag{5}$$

9.2.2.5 Output Capacitor Selection

The value of the output capacitor and the ESR of the capacitor determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. 式 6 can be used to estimate a lower bound on the total output capacitance and an upper bound on the ESR, which is required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}} \tag{6}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = ripple factor from セクション 9.2.2.4

Once the output capacitor and ESR have been calculated, 式 7 can be used to check the peak-to-peak output voltage ripple; V_r.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}} \tag{7}$$

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

For this example, a $\Delta V_{OUT} \leq 250$ mV for an output current step of $\Delta I_{OUT} = 2$ A is required. 式 6 gives a minimum value of 52 µF and a maximum ESR of 0.11 Ω. Assuming a 20% tolerance and a 10% bias de-rating, you arrive at a minimum capacitance of 72 µF. This can be achieved with a bank of 4 × 22-µF, 16-V ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance. In general, use a capacitor of at least 10 V for output voltages of 3.3 V or less and a capacitor of 16 V or more for output voltages of 5 V and above.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high frequency noise. Small case size ceramic capacitors in the range of 1

nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance must be limited to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the LMR33630. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size, 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 4.7-µF, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50 V with an X7R dielectric. The VQFN (RNX) package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, a single 4.7-µF and two 100-nF ceramic capacitors at each VIN/PGND location.

Many times, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate worst case RMS value of this current can be calculated from 式 8 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{8}$$

9.2.2.7 C_{BOOT}

The LMR33630 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 10 V is required.

9.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see *セクション 8.3.1*). A value of 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V; see *セクション 7.5* for limits. Do not short this output to ground or any other external voltage.

9.2.2.9 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT}, in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help to mitigate this effect. 式 9 can be used to estimate the value of C_{FF}. The value found with 式 9 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed-forward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (9)$$

9.2.2.10 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 図 9-2. The input voltage at which the device turns on is designated V_{ON}; while the turnoff voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ and then 式 10 is used to calculate R_{ENT} and V_{OFF}.

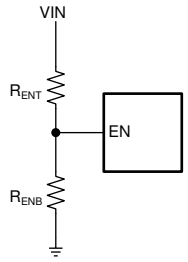


図 9-2. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN-H}} \right) \quad (10)$$

where

- V_{ON} = V_{IN} turnon voltage
- V_{OFF} = V_{IN} turnoff voltage

9.2.2.11 Maximum Ambient Temperature

As with any power conversion device, the LMR33630 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMR33630 must be limited to 125°C. This establishes a limit on the maximum device power dissipation and therefore the load current. 式 11 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in セクション 7.4 is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (11)$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as power dissipation, air temperature/flow, PCB area, copper heat-sink area, number of thermal vias under the package, and adjacent component placement; to mention just a few. The HSOIC (DDA) package utilizes a die attach paddle, or thermal pad (PAD) to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Due to the ultra-miniature size of the VQFN (RNX) package, a DAP is not available. This means that this package exhibits a somewhat large value $R_{\theta JA}$. Typical examples of $R_{\theta JA}$ vs copper board area can be found in 図 9-3 and 図 9-4. The copper area given in the graph is for each layer; the top and bottom layers are 2 oz. copper each, while the inner layers are 1 oz. Typical curves of maximum output current vs ambient temperature are shown in 図 9-5 and 図 9-6. This data was taken with a device/PCB combination giving an $R_{\theta JA}$ as noted in the graph. It must be remembered that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

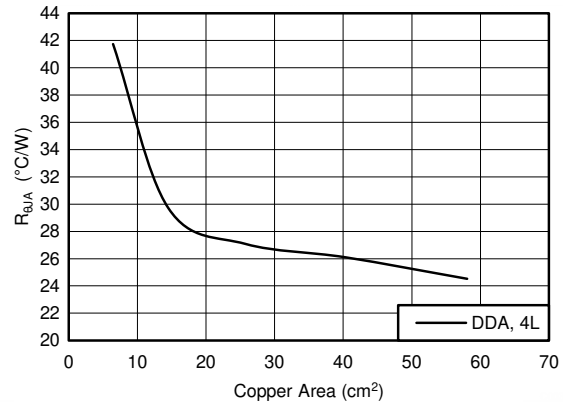


図 9-3. Typical $R_{\theta JA}$ versus Copper Area for a Four-Layer Board and the HSOIC (DDA) Package

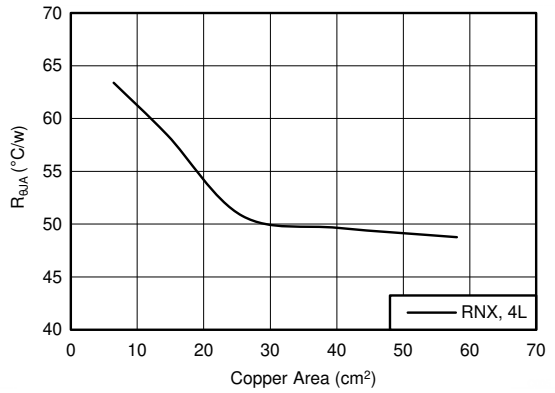
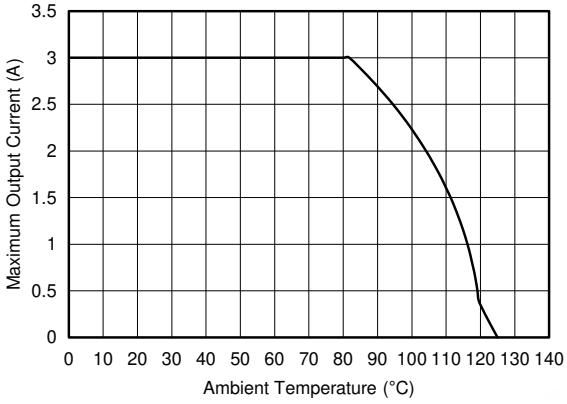
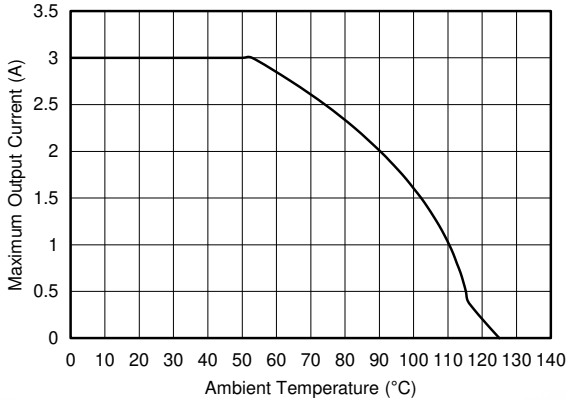


図 9-4. $R_{\theta JA}$ versus Copper Board Area for the VQFN (RNX) Package



V_{IN} = 12 V V_{OUT} = 5 V
f_{SW} = 400 kHz $R_{\theta JA}$ = 30°C/W

図 9-5. Maximum Output Current versus Ambient Temperature



V_{IN} = 12 V V_{OUT} = 5 V
f_{SW} = 400 kHz $R_{\theta JA}$ = 50°C/W

図 9-6. Maximum Output Current versus Ambient Temperature

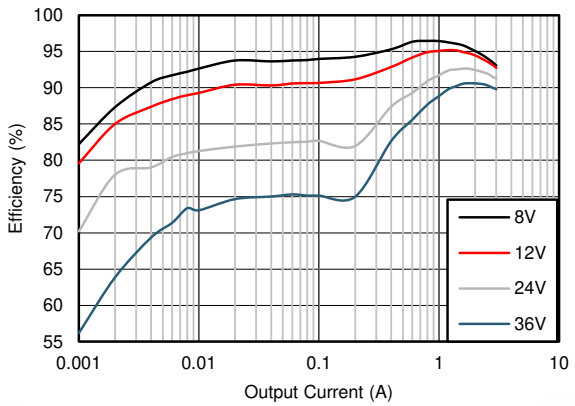
Use the following resources as a guide to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
- *Semiconductor and IC Package Thermal Metrics*
- *Thermal Design Made Simple with LM43603 and LM43602*
- *PowerPAD™ Thermally Enhanced Package*

- *PowerPAD™ Made Easy*
- *Using New Thermal Metrics*

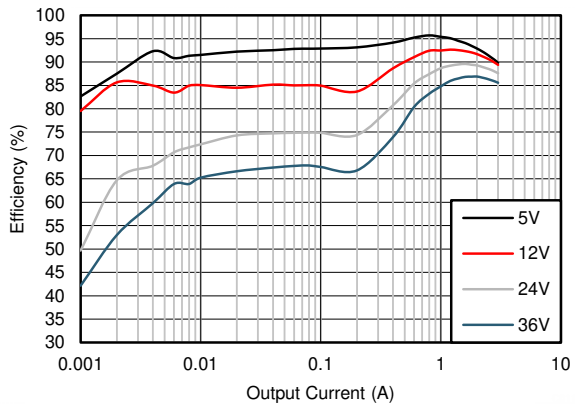
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25°C. The circuit is shown in 図 9-31, with the appropriate BOM from 表 9-3 or 表 9-4.



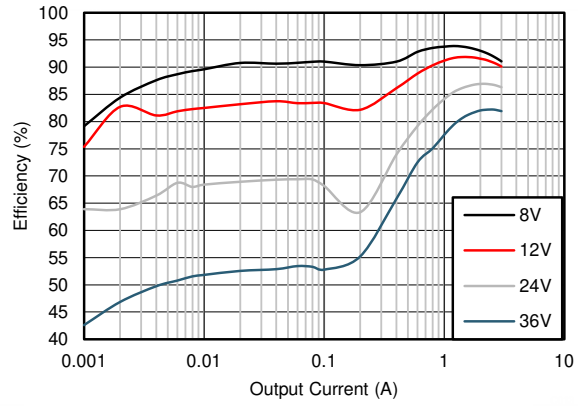
V_{OUT} = 5 V 400 kHz DDA Package

図 9-7. Efficiency



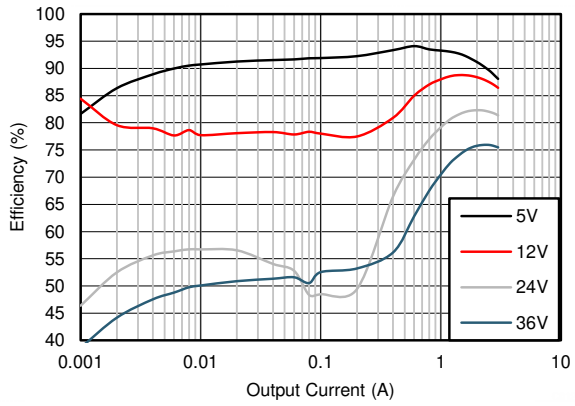
V_{OUT} = 3.3 V 400 kHz DDA Package

図 9-8. Efficiency



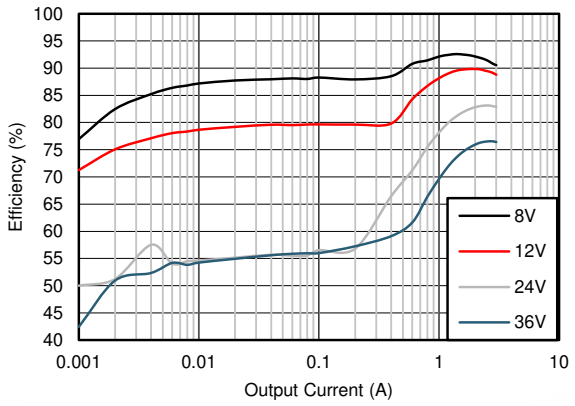
V_{OUT} = 5 V 1.4 MHz DDA Package

図 9-9. Efficiency



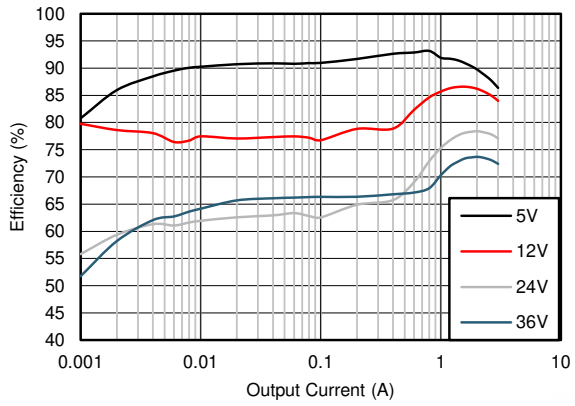
V_{OUT} = 3.3 V 1.4 MHz DDA Package

図 9-10. Efficiency



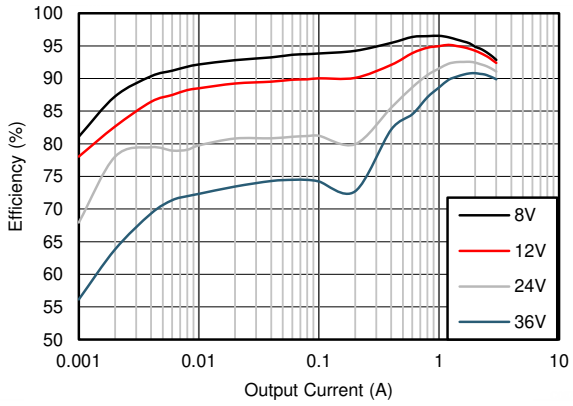
V_{OUT} = 5 V 2.1 MHz DDA Package

図 9-11. Efficiency



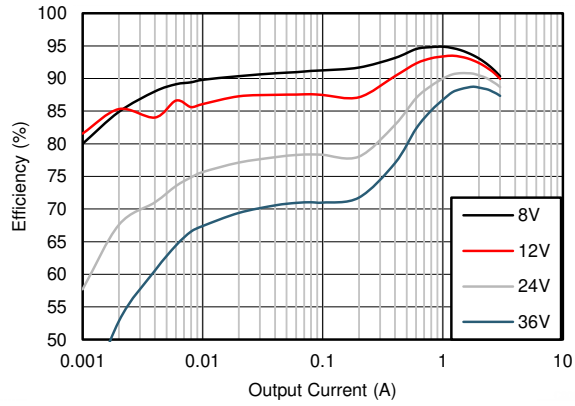
V_{OUT} = 3.3 V 2.1 MHz DDA Package

図 9-12. Efficiency



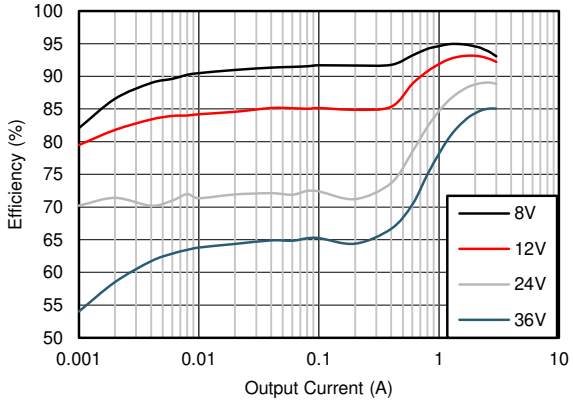
V_{OUT} = 5 V 400 kHz RNX Package

図 9-13. Efficiency



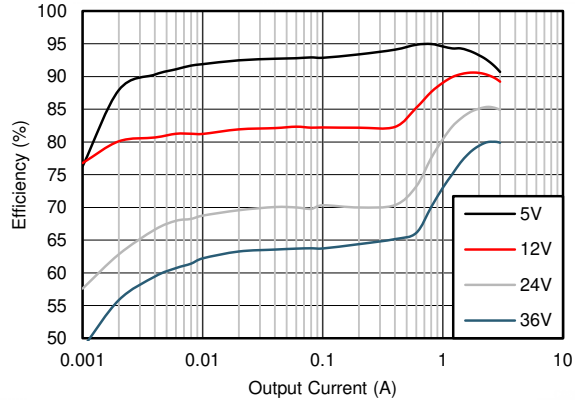
V_{OUT} = 3.3 V 400 kHz RNX Package

図 9-14. Efficiency



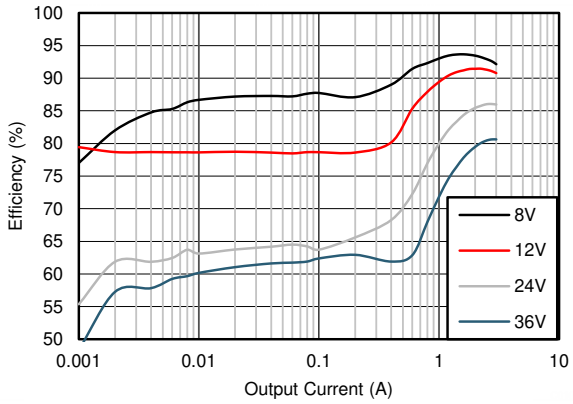
V_{OUT} = 5 V 1.4 MHz RNX Package

図 9-15. Efficiency



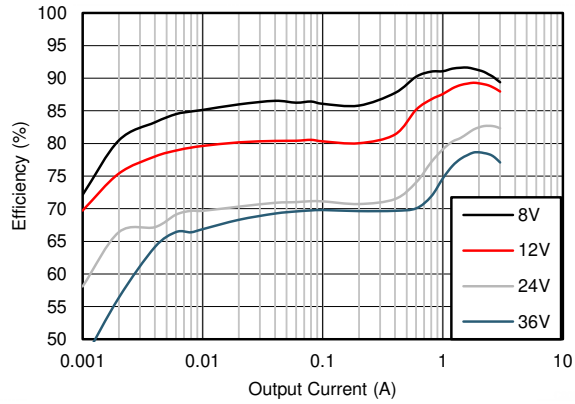
V_{OUT} = 3.3 V 1.4 MHz RNX Package

図 9-16. Efficiency



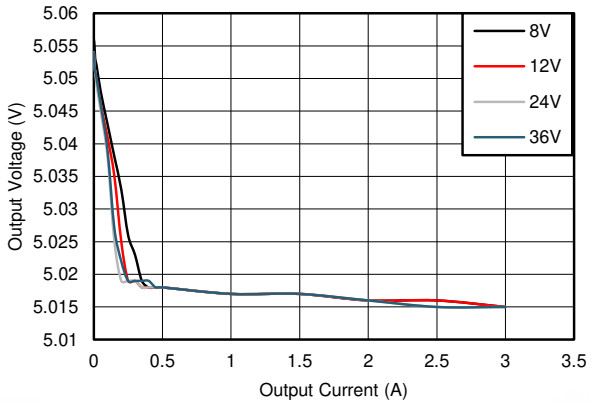
V_{OUT} = 5 V 2.1 MHz RNX Package

図 9-17. Efficiency



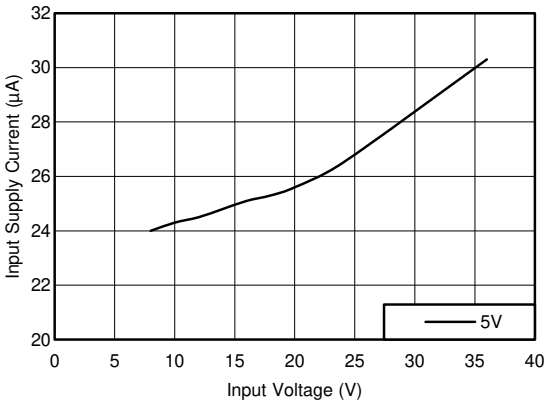
V_{OUT} = 3.3 V 2.1 MHz RNX Package

図 9-18. Efficiency



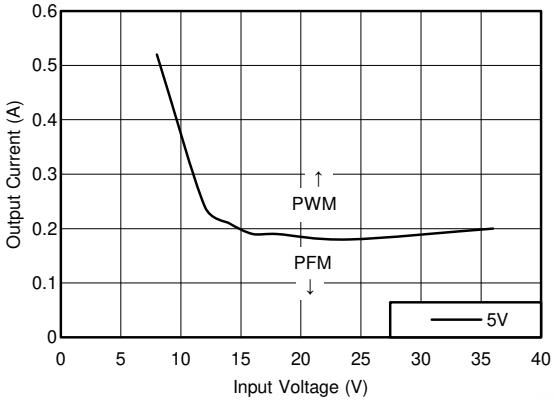
V_{OUT} = 5 V

図 9-19. Line and Load Regulation



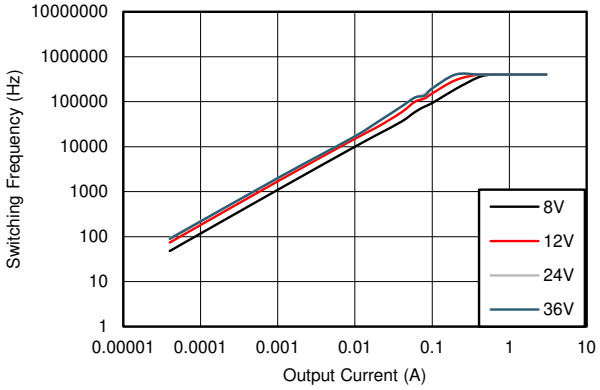
V_{OUT} = 5 V I_{OUT} = 0 A R_{FBT} = 1 MΩ

図 9-20. Input Supply Current



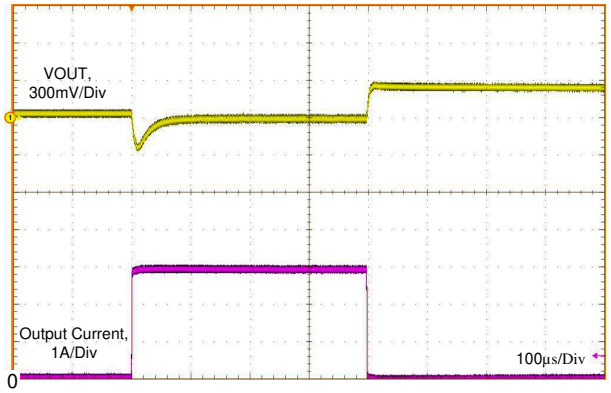
V_{OUT} = 5 V f_{SW} = 400 kHz

図 9-21. Mode Change Thresholds



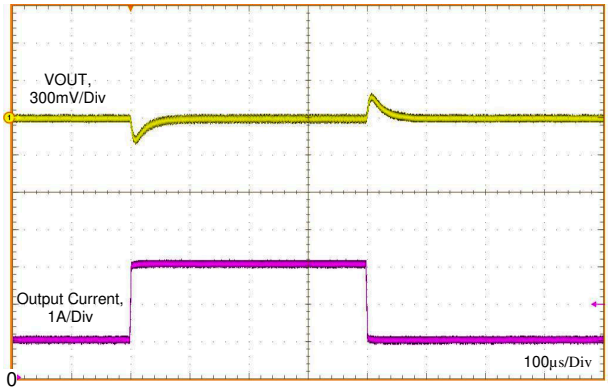
V_{OUT} = 5 V f_{SW} = 400 kHz

図 9-22. Switching Frequency versus Output Current



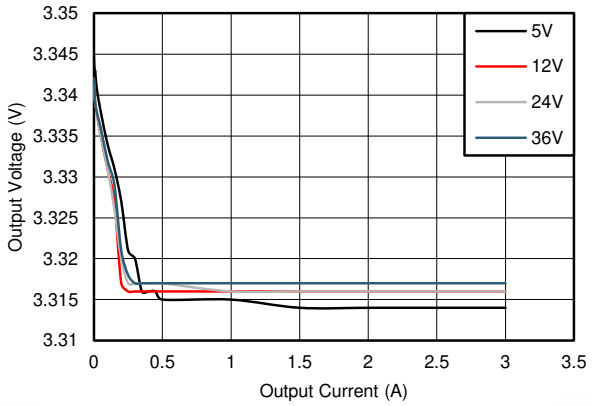
V_{IN} = 12 V V_{OUT} = 5 V
$t_f = t_r$ = 2 µs I_{OUT} = 0 A to 3 A

図 9-23. Load Transient



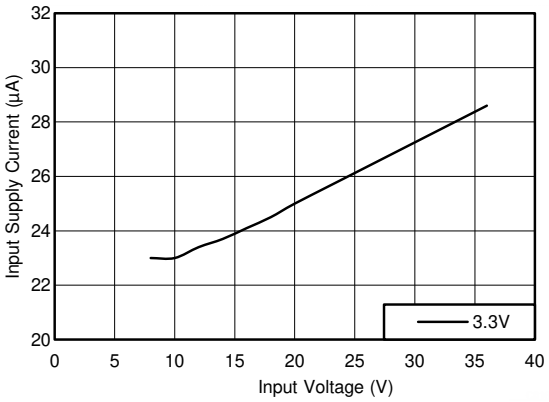
V_{IN} = 12 V V_{OUT} = 5 V
$t_f = t_r$ = 2 µs I_{OUT} = 1 A to 3 A

図 9-24. Load Transient



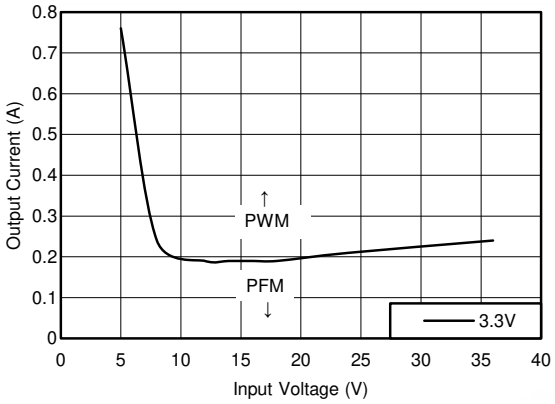
V_{OUT} = 3.3 V

図 9-25. Line and Load Regulation



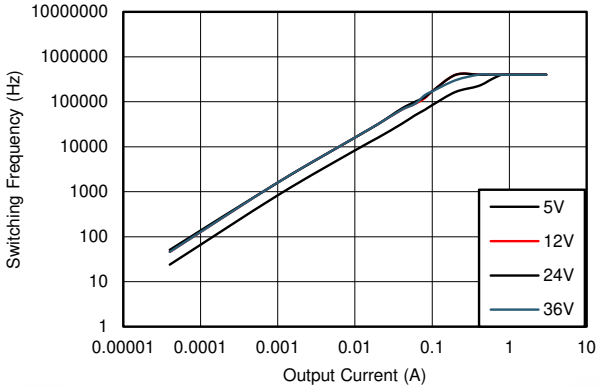
V_{OUT} = 3.3 V I_{OUT} = 0 A R_{FBT} = 1 MΩ

図 9-26. Input Supply Current



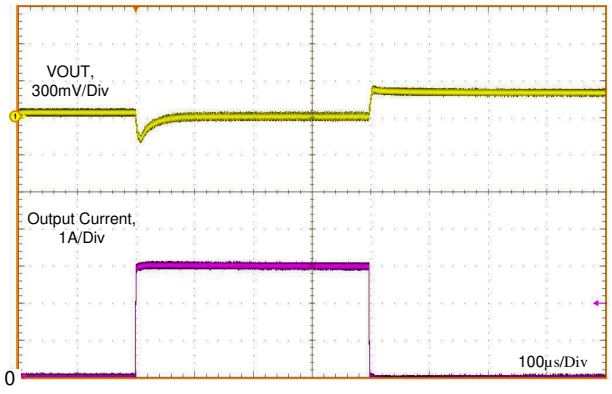
V_{OUT} = 3.3 V f_{SW} = 400 kHz

図 9-27. Mode Change Thresholds



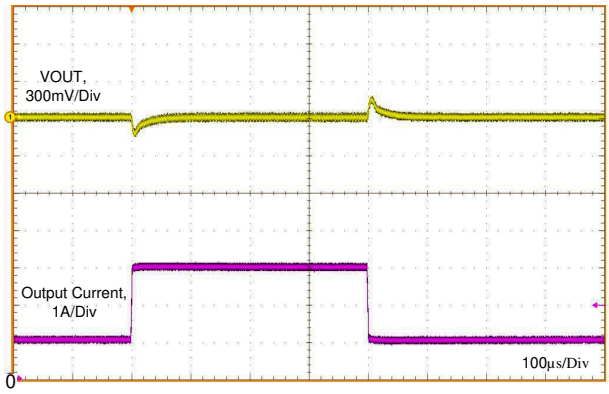
V_{OUT} = 3.3 V f_{SW} = 400 kHz

図 9-28. Switching Frequency versus Output Current



V_{IN} = 12 V V_{OUT} = 3.3 V
$t_f = t_r$ = 2 µs I_{OUT} = 0 A to 3 A

図 9-29. Load Transient



V_{IN} = 12 V V_{OUT} = 3.3V I_{OUT} = 1 A to 3 A
$t_f = t_r$ = 2 µs

図 9-30. Load Transient

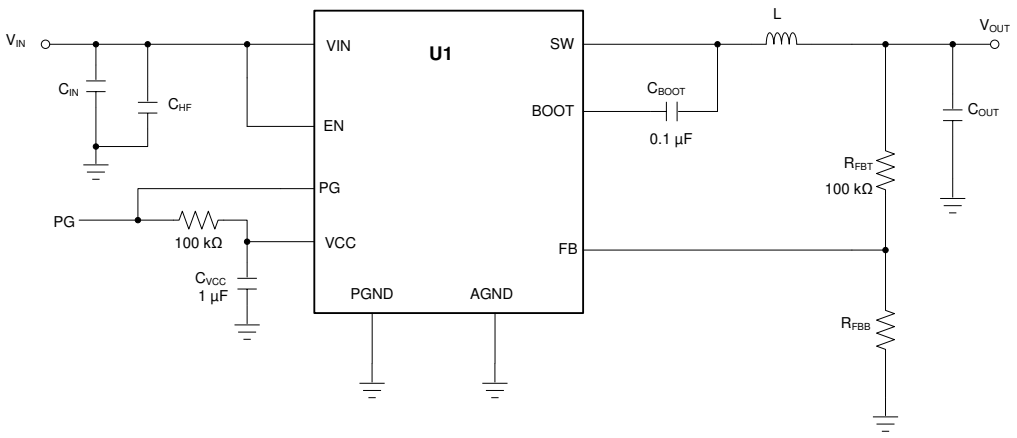


図 9-31. Circuit for Application Curves

The values in this table were selected to enhance certain performance criteria and may not represent typical values.

表 9-3. BOM for Typical Application Curves DDA Package

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	6.8 µH, 14 mΩ	LMR33630ADDA
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33630BDDA
3.3 V	2100 kHz	43.3 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.2 µH, 16 mΩ	LMR33630CDDA
5 V	400 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	8 µH, 14 mΩ	LMR33630ADDA
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	2.2 µH, 11.4 mΩ	LMR33630BDDA
5 V	2100 kHz	24.9 kΩ	4 × 22 µF	1 × 10 µF + 1 × 220 nF	1.5 µH, 8.2 mΩ	LMR33630CDDA

表 9-4. BOM for Typical Application Curves RNX Package

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	6.8 µH, 14 mΩ	LMR33630ARNX
3.3 V	1400 KHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33630BRNX
3.3 V	2100 kHz	43.3 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	1.2 µH, 7 mΩ	LMR33630CRNX
5 V	400 kHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	8 µH, 25 mΩ	LMR33630ARNX
5 V	1400 KHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	2.2 µH, 11.4 mΩ	LMR33630BRNX
5 V	2100 kHz	24.9 kΩ	4 × 22 µF	2 × 4.7 µF + 2 × 100 nF	1.5 µH, 8.2 mΩ	LMR33630CRNX

9.3 What to Do and What Not to Do

- **Don't:** Exceed the *Absolute Maximum Ratings*.
- **Don't:** Exceed the *ESD Ratings* .
- **Don't:** Exceed the *Recommended Operating Conditions*.
- **Don't:** Allow the EN input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the value of $R_{\theta JA}$ given in the table to design your application. Use the information in *セクション 9.2.2.11*.
- **Do:** Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success (see *Support Resources*).

Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 12, where η is the efficiency.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{12}$$

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The user guide *AN-2162 Simple Success With Conducted EMI From DCDC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharges through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output should be used.

10 Layout

10.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or input capacitors, and power ground, as shown in 図 10-1. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 図 10-2 and 図 10-3 show recommended layouts for the critical components of the LMR33630.

1. ***Place the input capacitor or capacitors as close as possible to the VIN and GND terminals.*** VIN and GND pins are adjacent, simplifying the input capacitor placement. With the VQFN package there are two VIN/PGND pairs on either side of the package. This provides for a symmetrical layout and helps minimize switching noise and EMI generation. A wide VIN plane must be used on a lower layer to connect both of the VIN pairs together to the input supply; see 図 10-3.
2. ***Place bypass capacitor for VCC close to the VCC pin.*** This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. ***Use wide traces for the C_{BOOT} capacitor.*** Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. For the VQFN package, it is important to route the SW connection under the device to the NC pin, and use this path to connect the BOOT capacitor to SW.
4. ***Place the feedback divider as close as possible to the FB pin of the device.*** Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. ***Use at least one ground plane in one of the middle layers.*** This plane acts as a noise shield and also act as a heat dissipation path.
6. ***Connect the thermal pad to the ground plane.*** The SOIC package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application.
7. ***Provide wide paths for VIN, VOUT, and GND.*** Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. ***Provide enough PCB area for proper heat sinking.*** As stated in *セクション 9.2.2.11*, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. With the SOIC package, use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. ***Keep switch area small.*** Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node should be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies*
- *Simple Switcher PCB Layout Guidelines*
- *Construction Your Power Supply- Layout Considerations*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x*

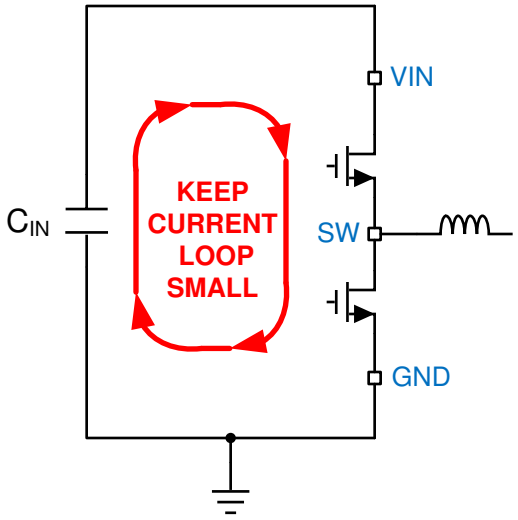


図 10-1. Current Loops with Fast Edges

10.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by utilizing the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10-mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

10.2 Layout Example

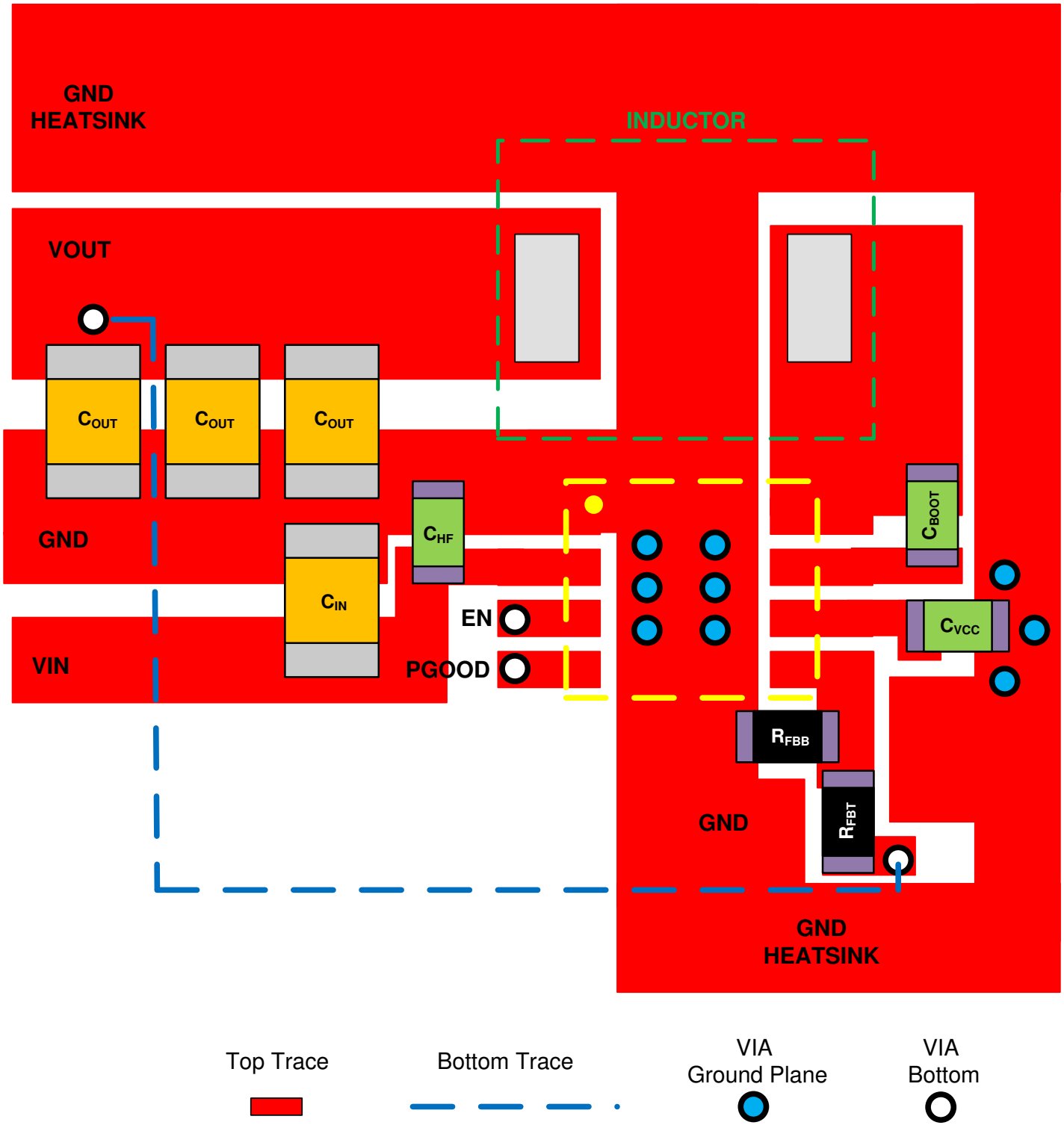
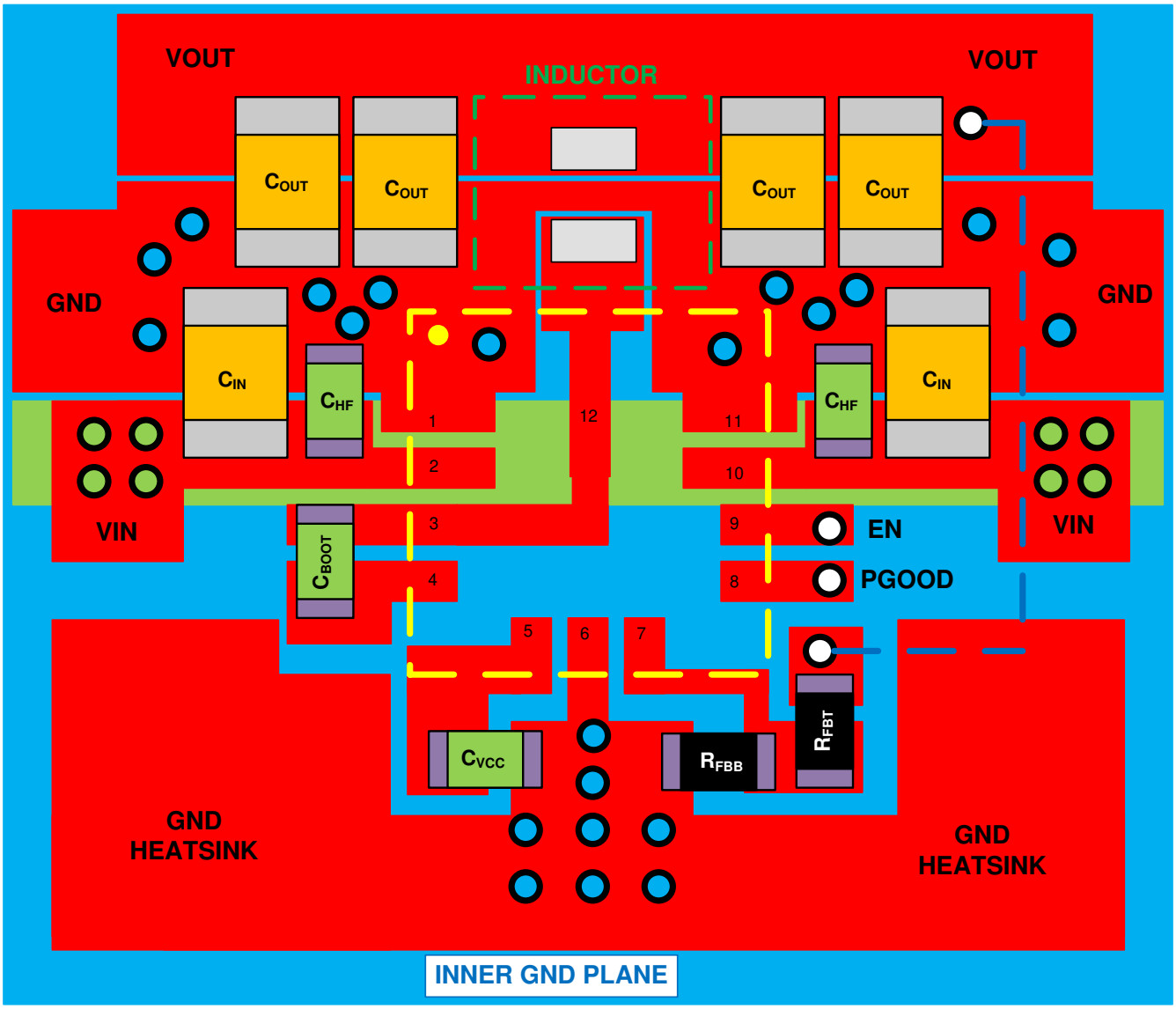


図 10-2. Example Layout for HSOIC (DDA) Package



Top Trace/Plane

Inner GND Plane

VIN Strap on Inner Layer

VIA to Signal Layer

VIA to GND Planes

VIA to VIN Strap

Trace on Signal Layer

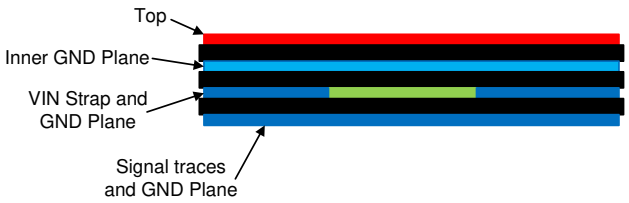


図 10-3. Example Layout for VQFN Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM33630 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Thermal Design by Insight not Hindsight*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
- *Semiconductor and IC Package Thermal Metrics*
- *Thermal Design Made Simple with LM43603 and LM43602*
- *PowerPAD™ Thermally Enhanced Package*
- *PowerPAD™ Made Easy*
- *Using New Thermal Metrics*
- *Layout Guidelines for Switching Power Supplies*
- *Simple Switcher PCB Layout Guidelines*
- *Construction Your Power Supply- Layout Considerations*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.5 Trademarks

HotRod™, TI E2E™ are trademarks of Texas Instruments.
PowerPAD™ is a trademark of TI.
WEBENCH® is a registered trademark of Texas Instruments.
SIMPLE SWITCHER® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR33630ADDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ADDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ADDAG4	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ADDAG4.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ADDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ADDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ARNXR	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ARNXR.A	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ARNXT	Active	Production	VQFN-HR (RNX) | 12	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630ARNXT.A	Active	Production	VQFN-HR (RNX) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630A
LMR33630BDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BDDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BRNXR	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BRNXR.A	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BRNXRG4	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BRNXRG4.A	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BRNXT	Active	Production	VQFN-HR (RNX) | 12	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630BRNXT.A	Active	Production	VQFN-HR (RNX) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630B
LMR33630CDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR33630CDDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CDDARG4	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CDDARG4.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CRNXR	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CRNXR.A	Active	Production	VQFN-HR (RNX) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CRNXT	Active	Production	VQFN-HR (RNX) | 12	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	33630C
LMR33630CRNXT.A	Active	Production	VQFN-HR (RNX) | 12	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	33630C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LMR33630 :

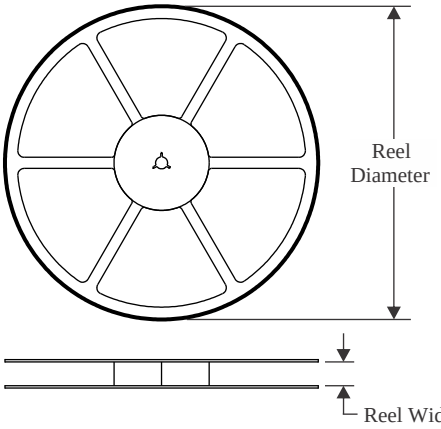
- Automotive : LMR33630-Q1

NOTE: Qualified Version Definitions:

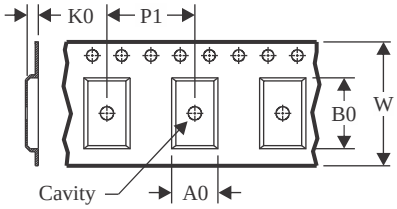
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

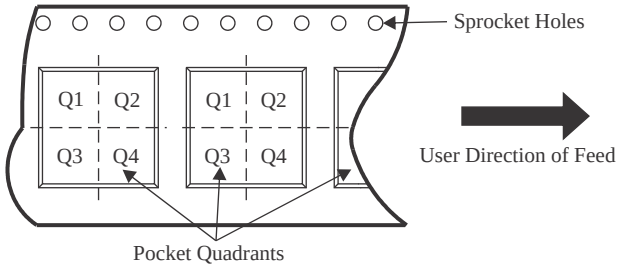


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

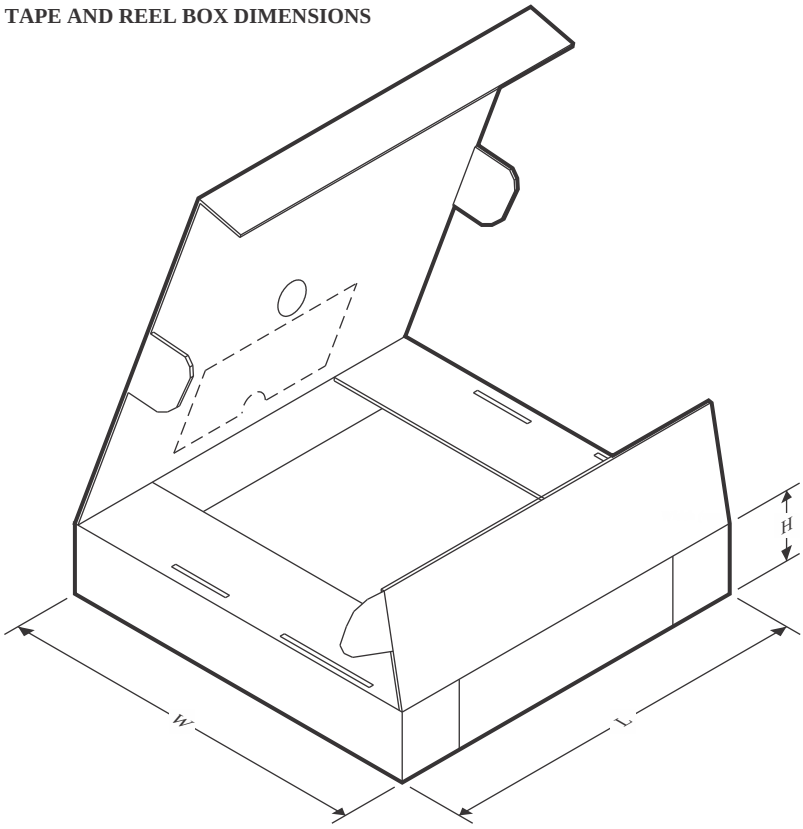
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR33630ARNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LMR33630ARNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LMR33630BRNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LMR33630BRNXRG4	VQFN-HR	RNX	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LMR33630BRNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LMR33630CRNXR	VQFN-HR	RNX	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LMR33630CRNXT	VQFN-HR	RNX	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

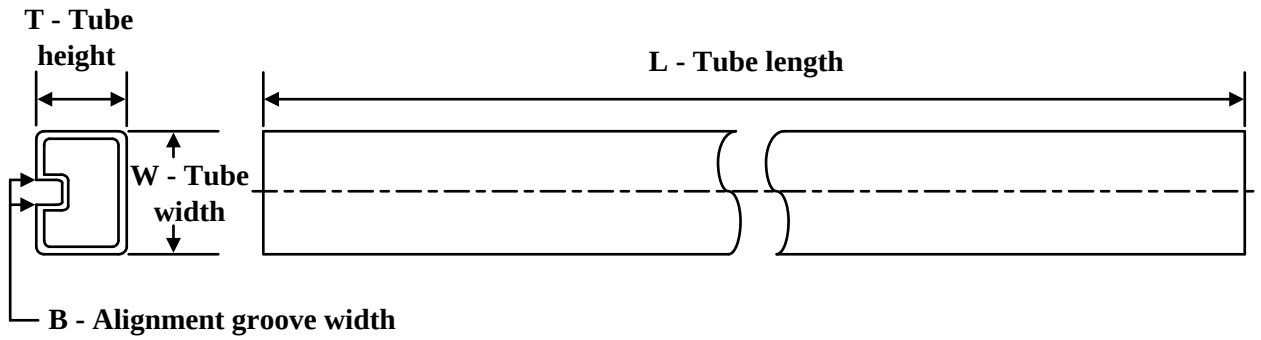
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR33630ARNXR	VQFN-HR	RNX	12	3000	210.0	185.0	35.0
LMR33630ARNXT	VQFN-HR	RNX	12	250	210.0	185.0	35.0
LMR33630BRNXR	VQFN-HR	RNX	12	3000	210.0	185.0	35.0
LMR33630BRNXRG4	VQFN-HR	RNX	12	3000	210.0	185.0	35.0
LMR33630BRNXT	VQFN-HR	RNX	12	250	210.0	185.0	35.0
LMR33630CRNXR	VQFN-HR	RNX	12	3000	210.0	185.0	35.0
LMR33630CRNXT	VQFN-HR	RNX	12	250	210.0	185.0	35.0

TUBE



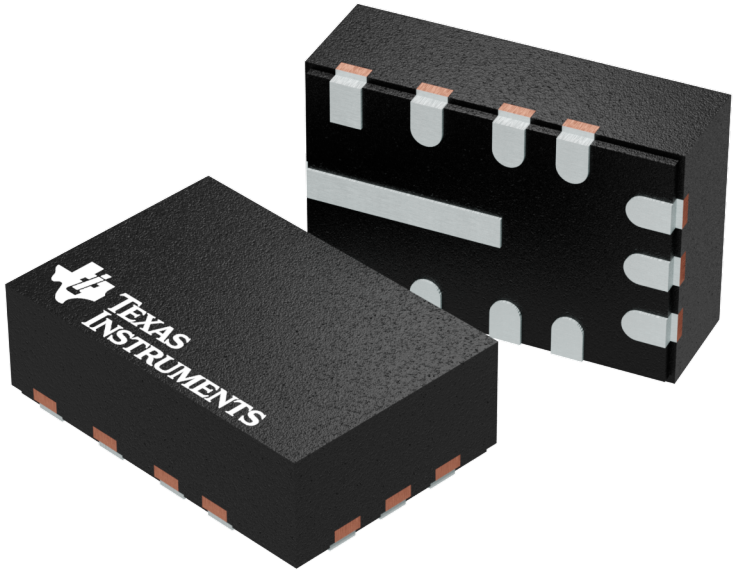
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMR33630ADDA	DDA	HSOIC	8	75	507.79	8	630	4.32
LMR33630ADDA	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR33630ADDA.A	DDA	HSOIC	8	75	507.79	8	630	4.32
LMR33630ADDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR33630ADDAG4	DDA	HSOIC	8	75	507.79	8	630	4.32
LMR33630ADDAG4.A	DDA	HSOIC	8	75	507.79	8	630	4.32
LMR33630BDDA	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR33630BDDA	DDA	HSOIC	8	75	507.79	8	630	4.32
LMR33630BDDA.A	DDA	HSOIC	8	75	507.79	8	630	4.32
LMR33630BDDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR33630CDDA	DDA	HSOIC	8	75	507.79	8	630	4.32
LMR33630CDDA	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR33630CDDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25
LMR33630CDDA.A	DDA	HSOIC	8	75	507.79	8	630	4.32

RNX 12 VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

2 x 3 mm, 0.5 mm pitch



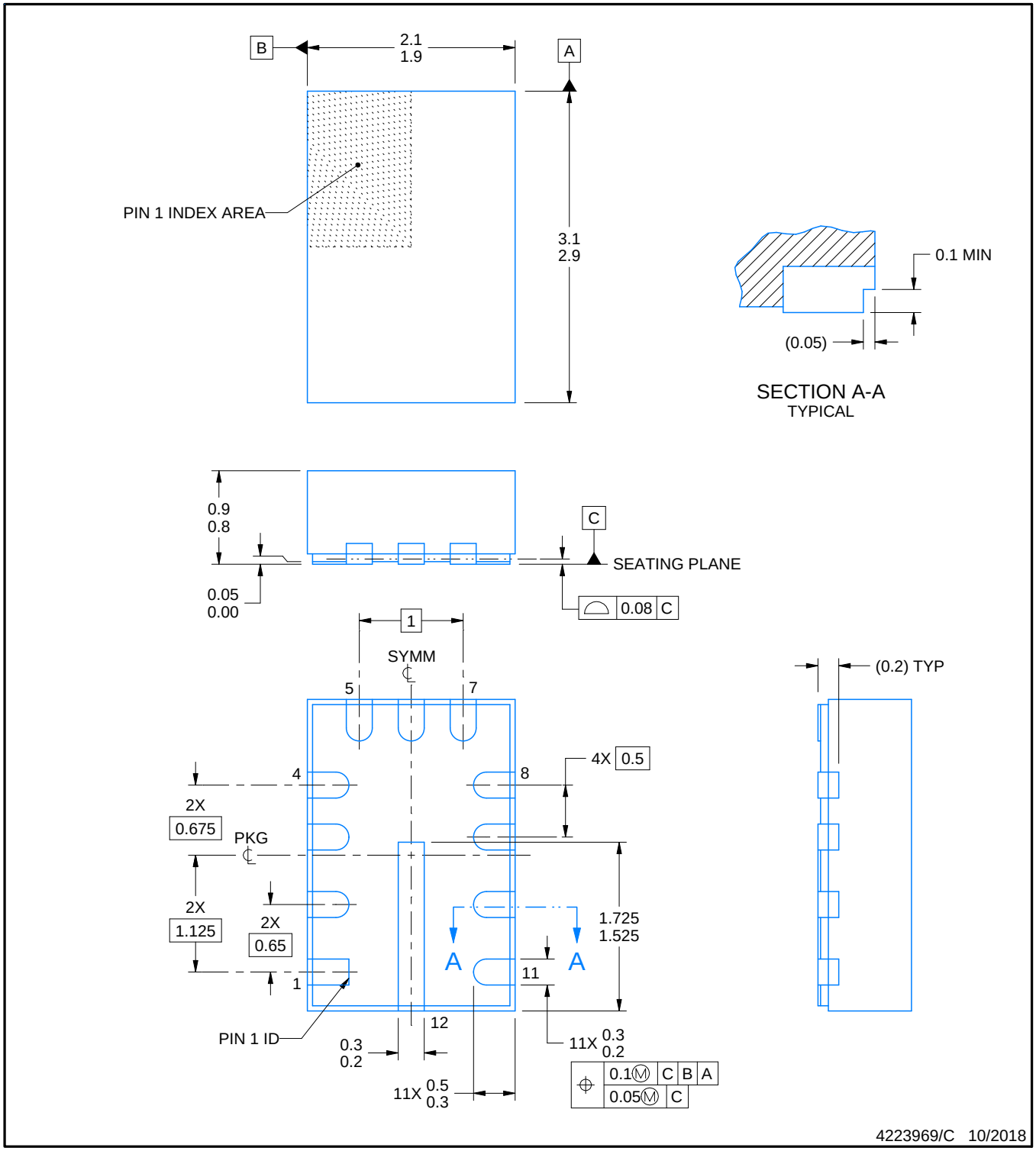
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RNX0012B

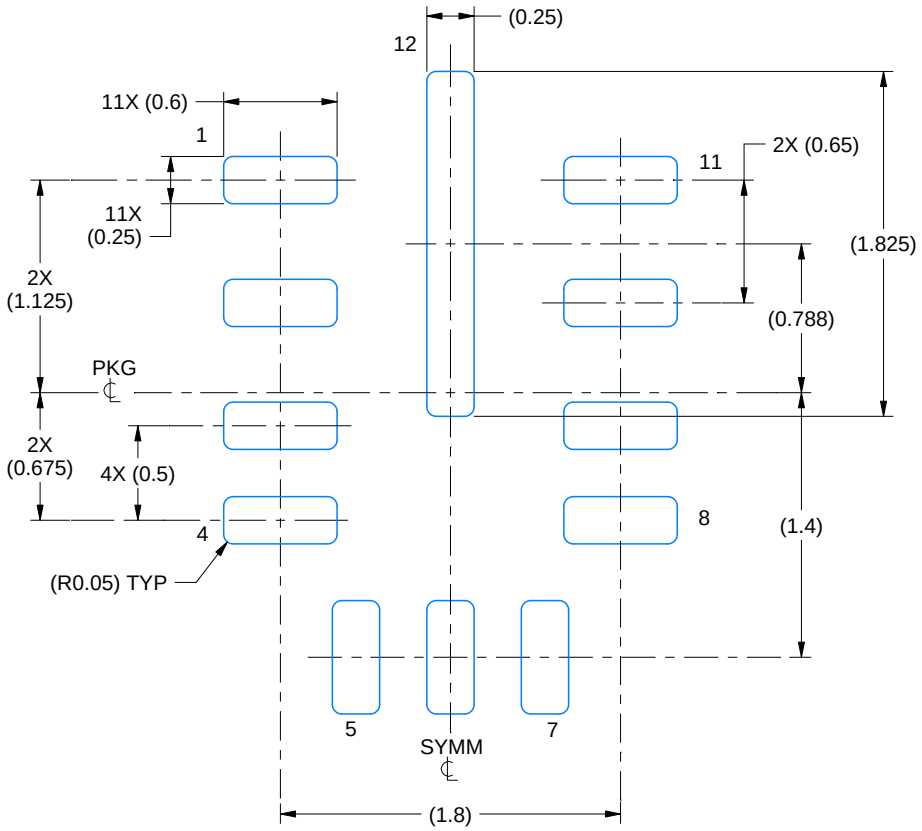
VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

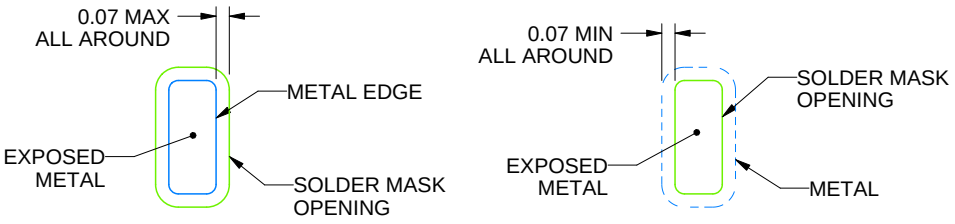


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

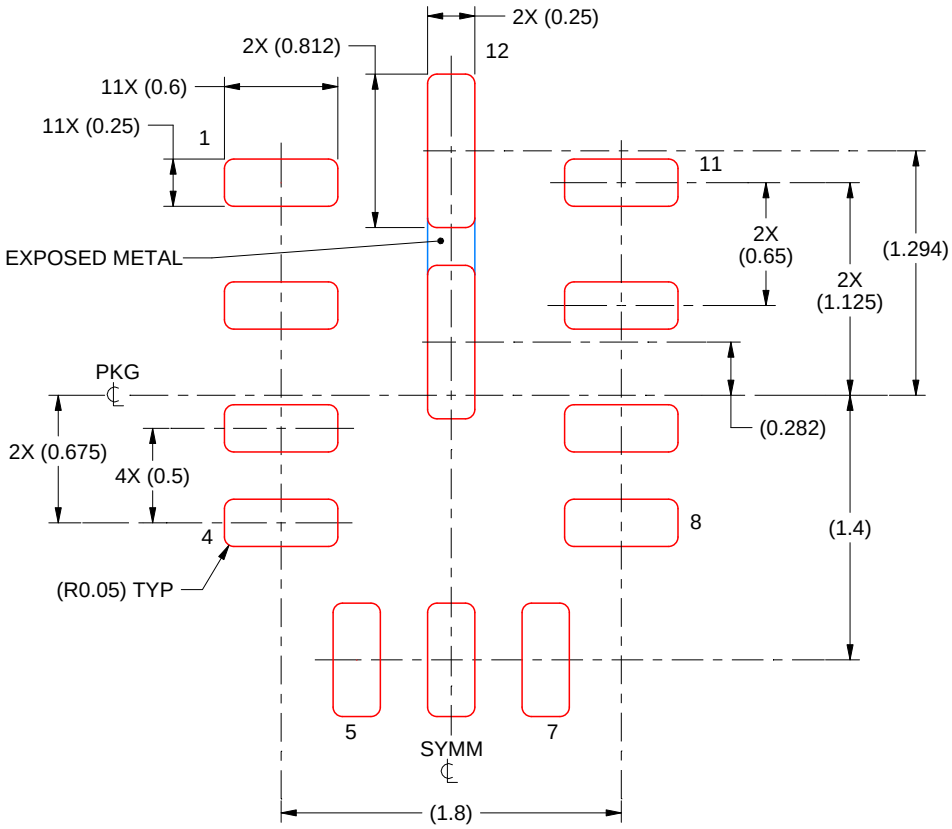


SOLDER MASK DETAILS

4223969/C 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



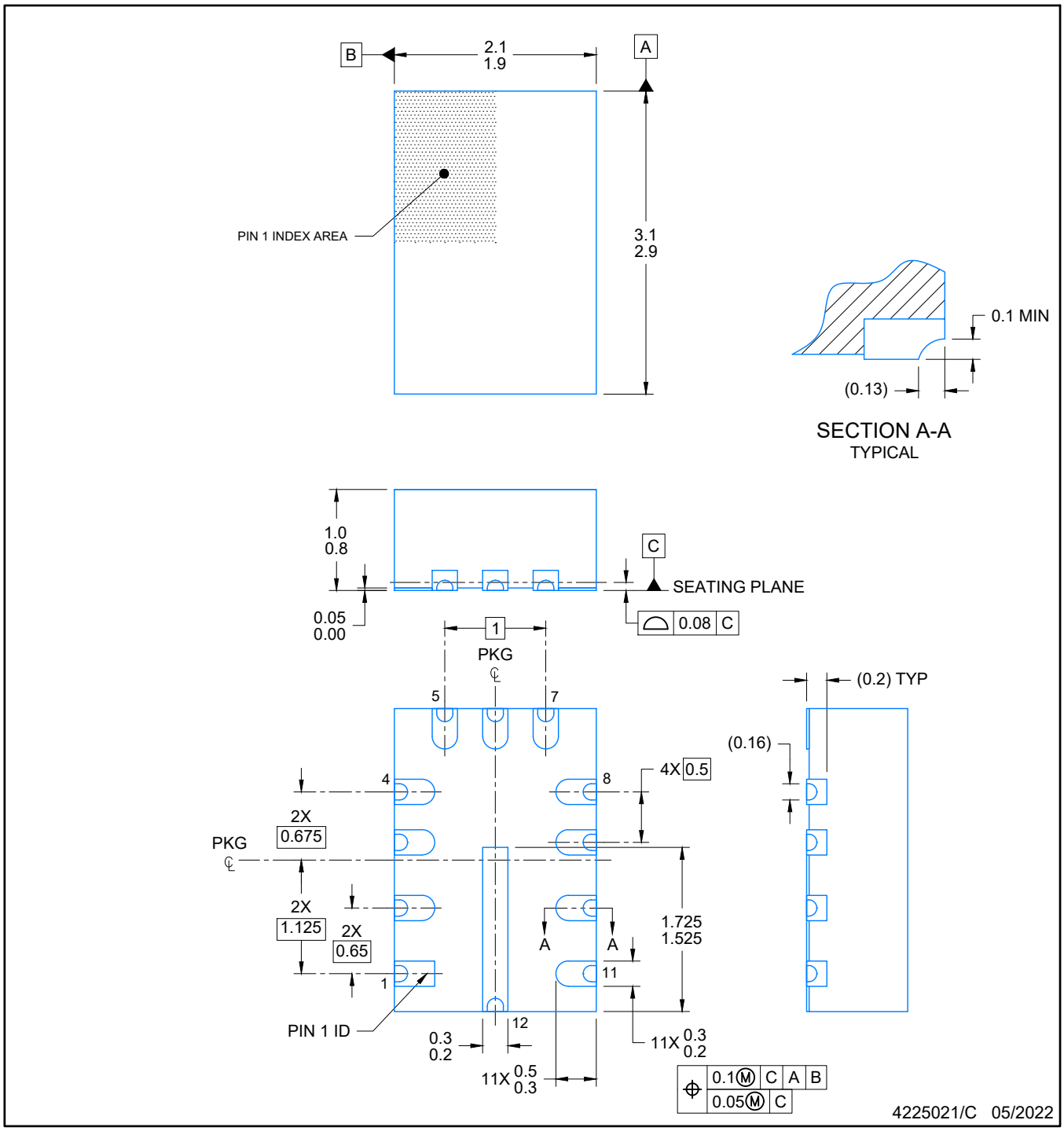
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PAD 12
87.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4223969/C 10/2018

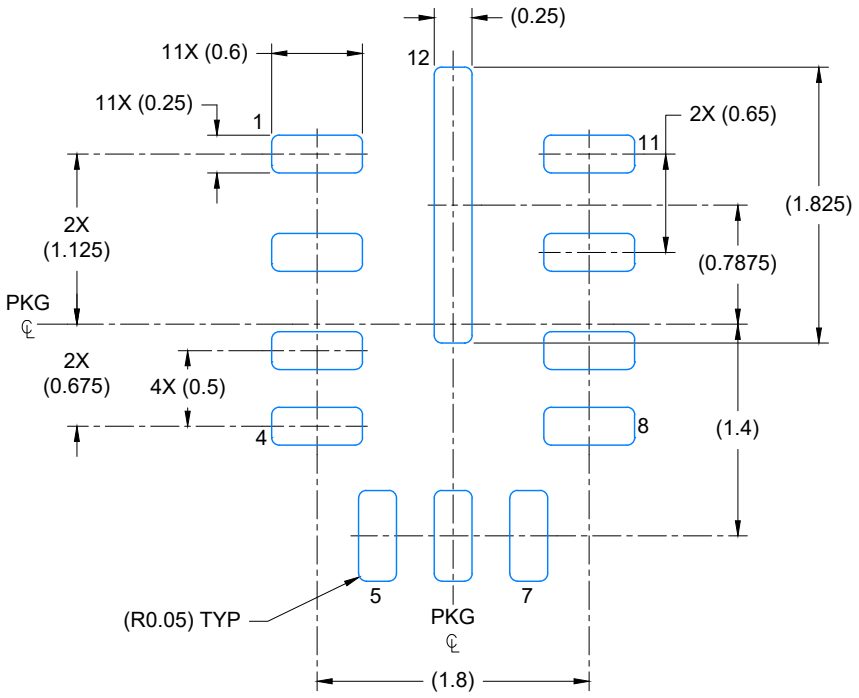
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



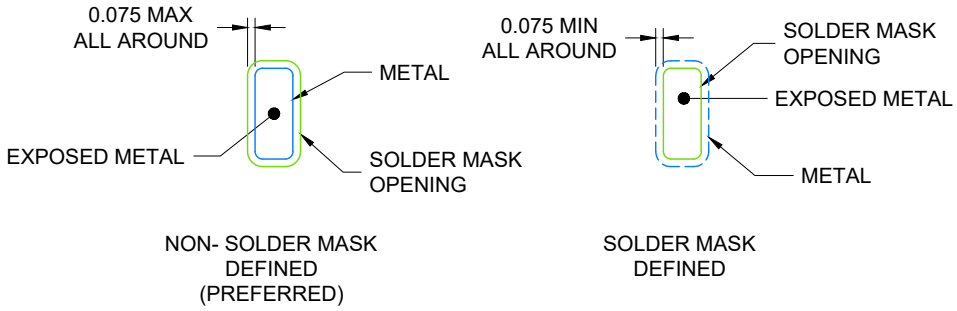
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 20X

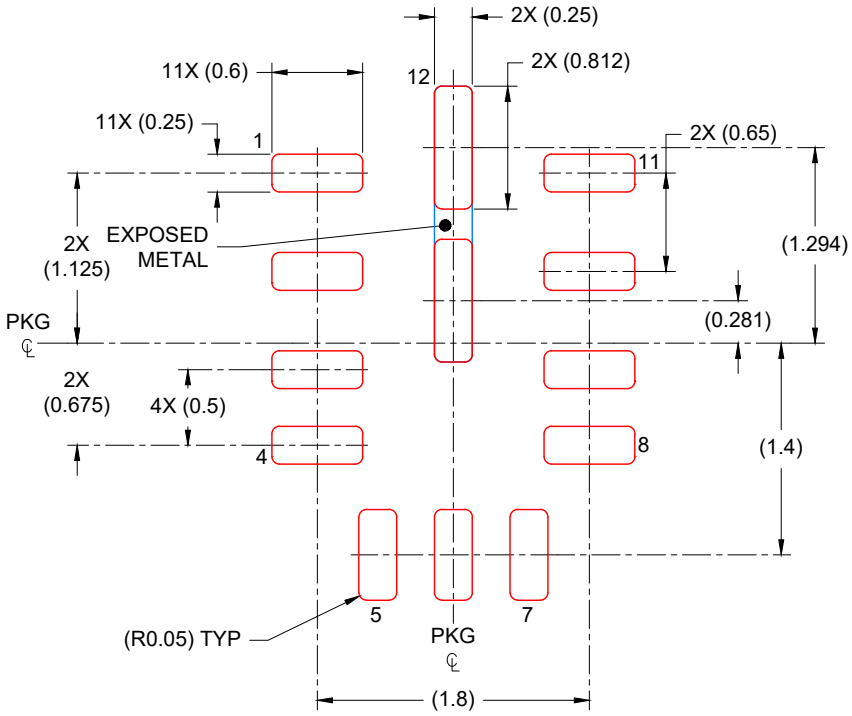


SOLDER MASK DETAILS

4225021/C 05/2022

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



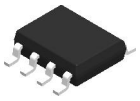
SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

FOR PAD 12
87.7% PRINTED COVERAGE BY AREA
SCALE: 20X

4225021/C 05/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

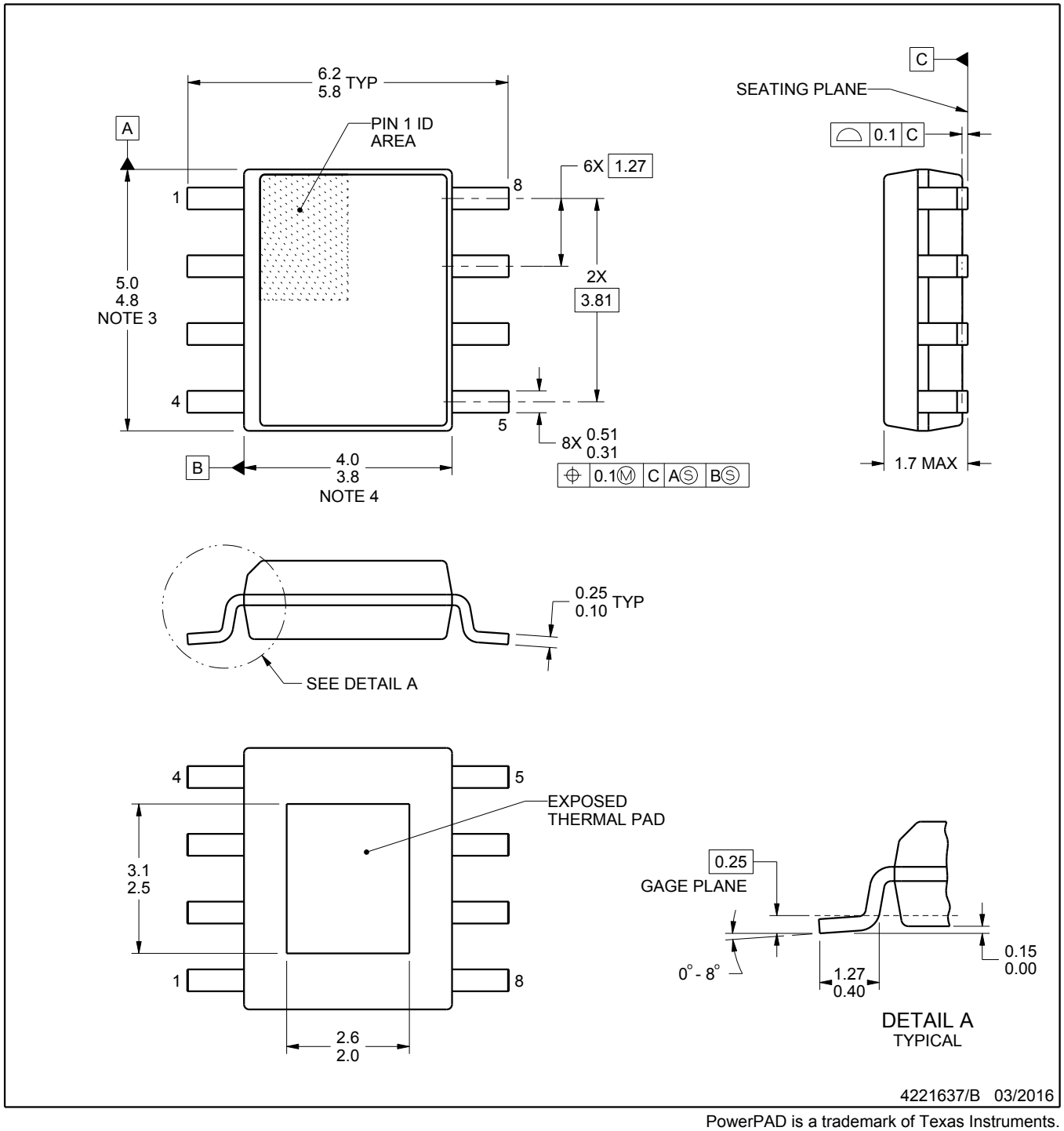


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

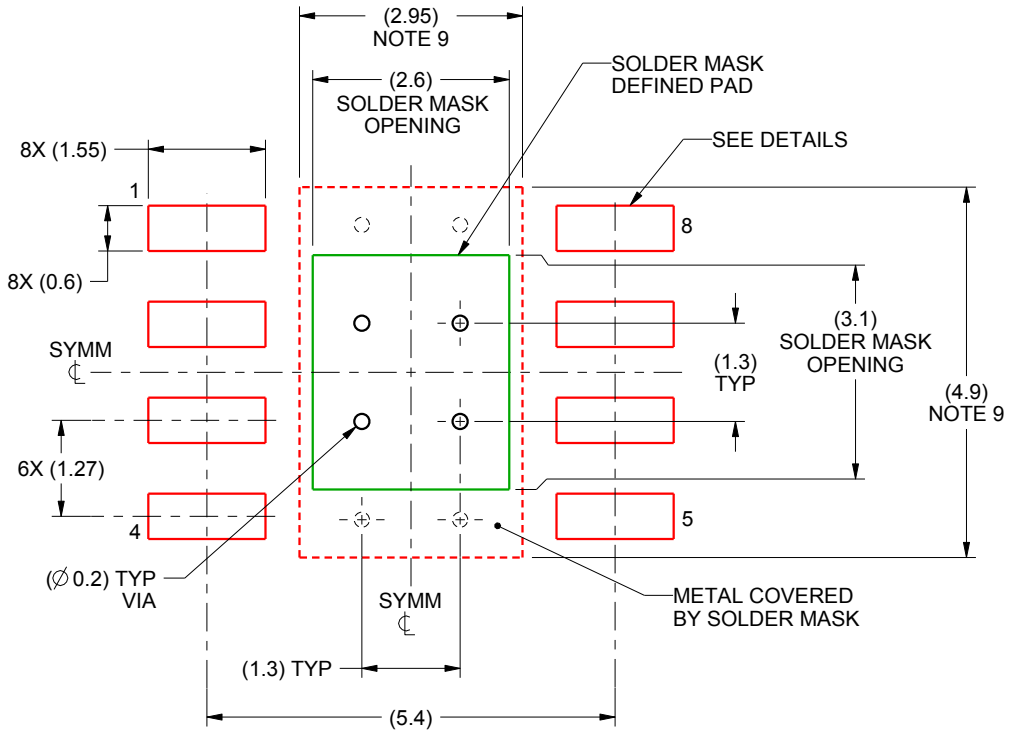
PLASTIC SMALL OUTLINE



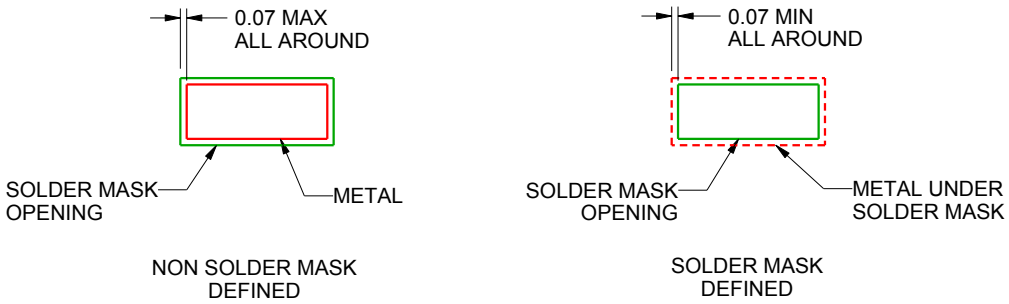
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

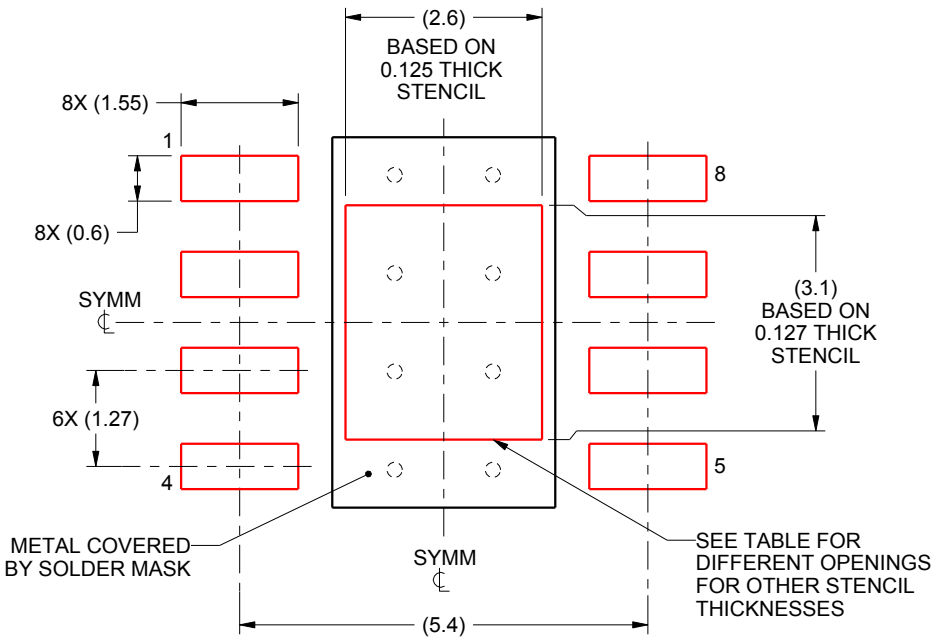


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

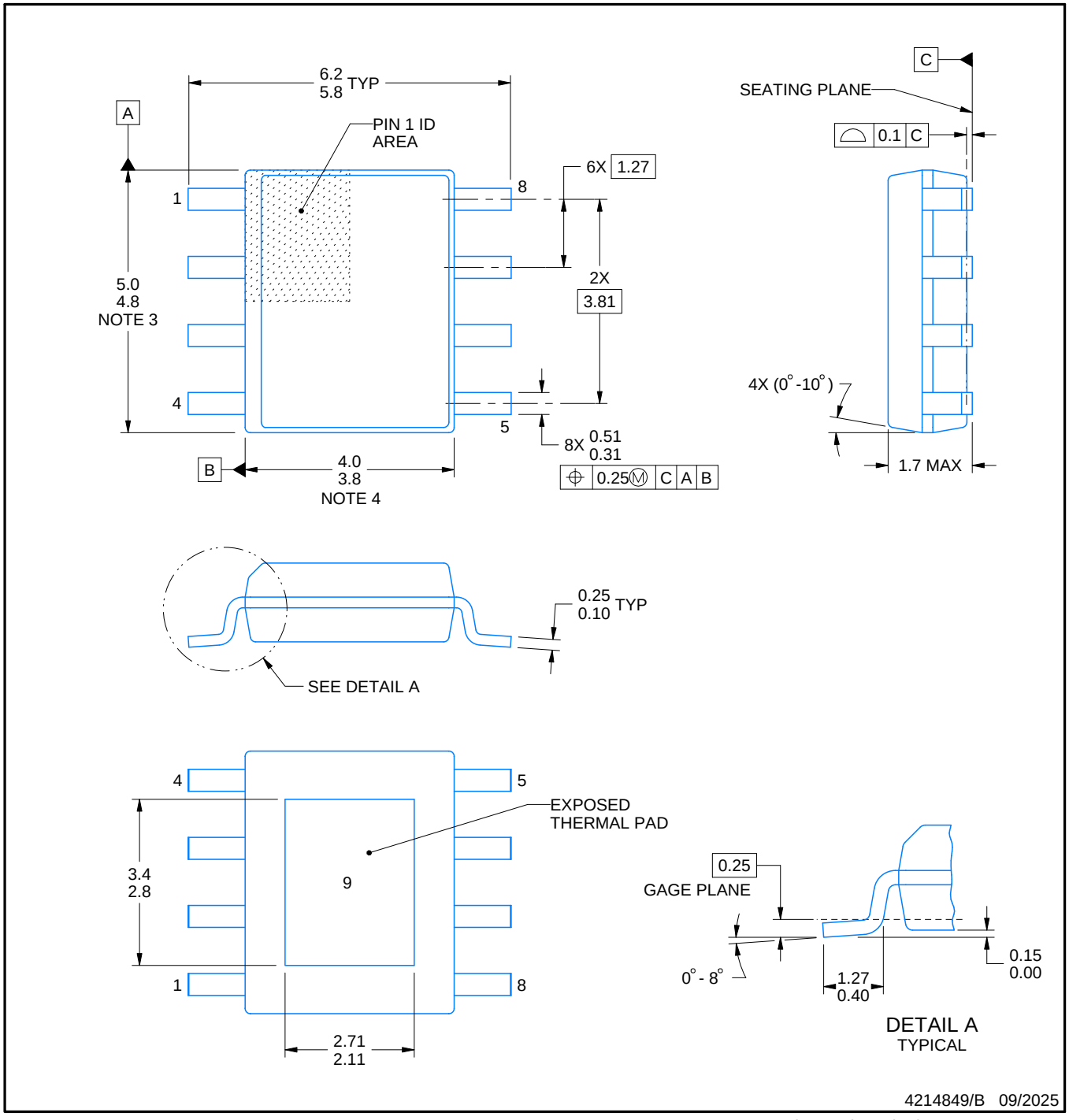
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

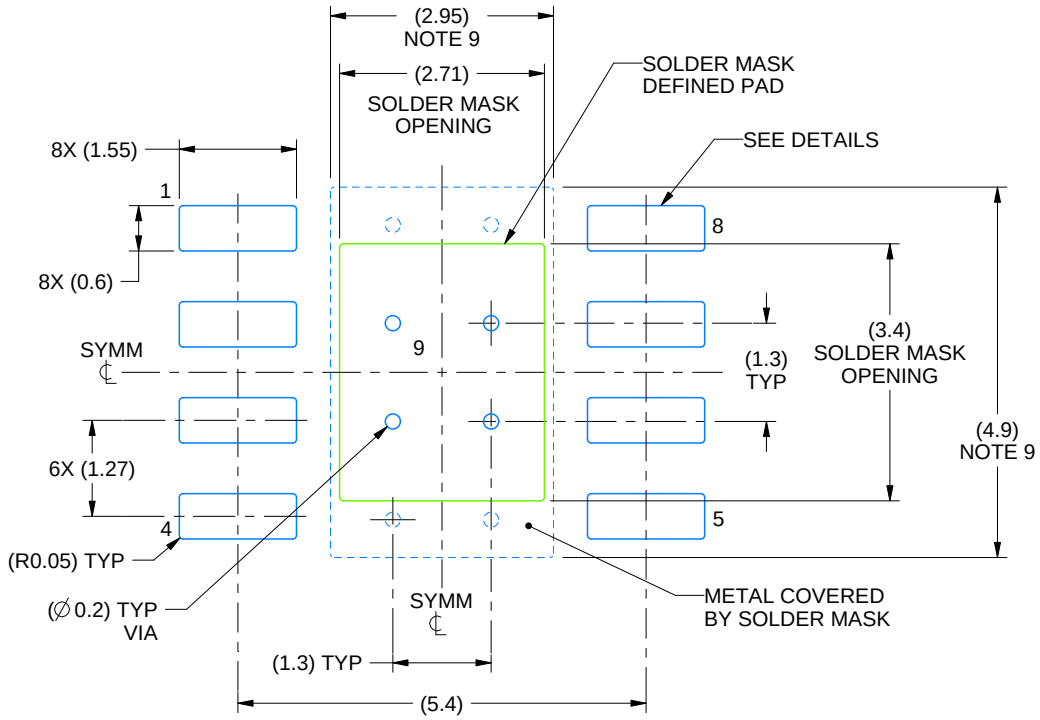
PLASTIC SMALL OUTLINE



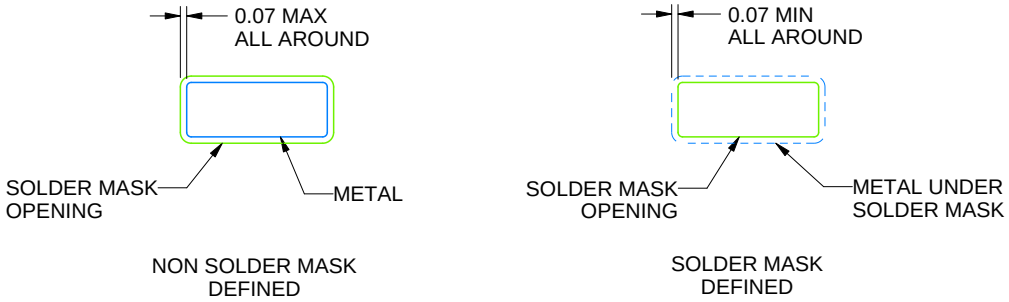
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

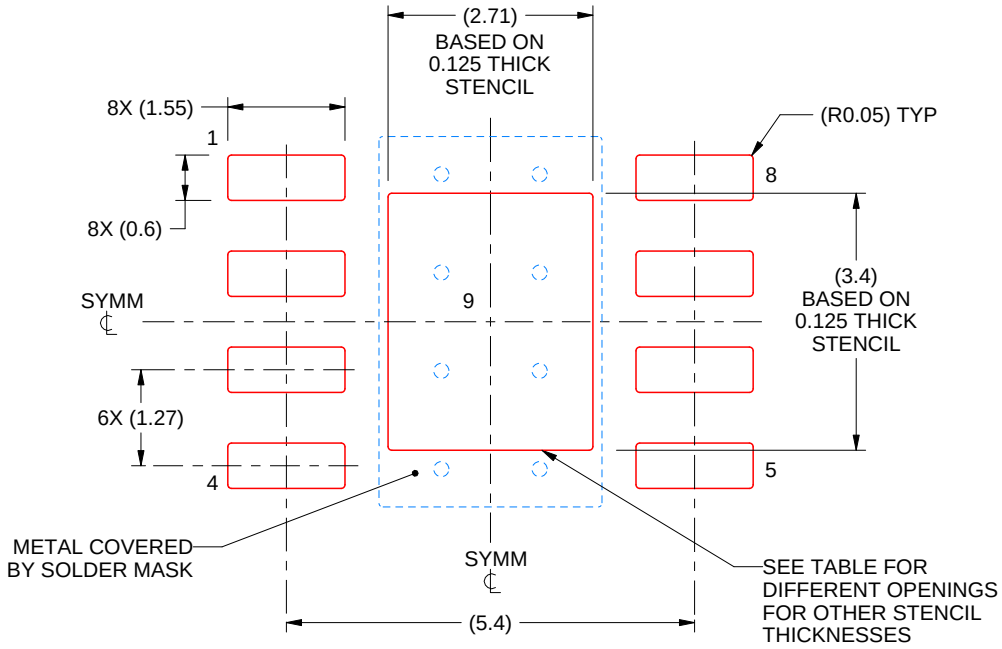
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月