LMR51603-Q1 65V、300mA、 車載用同期整流降圧コンバータ、低 I_Q

1 特長

- AEC-Q100 認定済み
  - 温度グレード 1:動作時周囲温度範囲 -40℃～125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 堅牢な産業用アプリケーション向けの構成
  - 入力電圧範囲:4V～65V
  - 最大 70V の過渡入力に対する保護
  - 連続出力電流:300mA
  - 最小スイッチング オン時間:80ns
  - 400kHz のスイッチング周波数を選択可能
  - 接合部温度範囲:-40℃～150℃
  - 最大デューティ サイクル:96%
  - プリバイアスされた出力への単調スタートアップ
  - ヒカップ モードによる短絡保護
  - 高精度のイネーブル
- 小型の設計サイズと使いやすさ
  - 同期整流器内蔵
  - 使いやすさを実現した内部補償
- ピン互換パッケージの各種オプション
  - PFM および強制 PWM (FPWM) オプション
- LMR16006Y-Q1、LM2842-Q1、LMR50410-Q1、TPS560430-Q1 とピン互換
- WEBENCH® Power Designer により、LMR51603-Q1 を使用するカスタム設計を作成

2 アプリケーション

- ボディ エレクトロニクスおよび照明
- インフォテインメントおよびクラスタ
- 先進運転支援システム (ADAS)

3 概要

LMR51603-Q1 は、最大 300mA の負荷電流を駆動でき、V_{IN} が広く使いやすい同期整流降圧コンバータです。このデバイスは、4V～65V の広い入力電圧範囲で動作し、レギュレートされていない電源からの電源調整を行うさまざまな産業用アプリケーションに適しています。

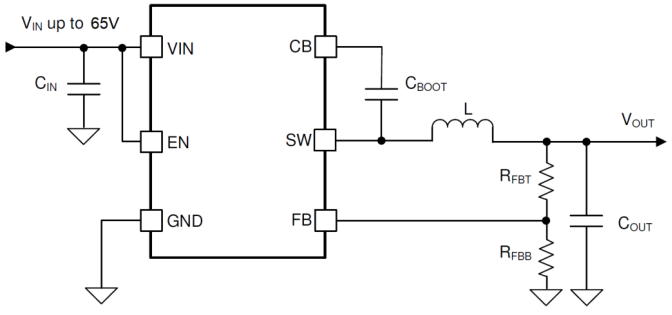
LMR51603-Q1 は 400kHz のスイッチング周波数で動作するため、比較的小型のインダクタを使用でき、設計サイズの最適化が可能です。LMR51603-Q1 には、軽負荷時に高効率を実現するパルス周波数変調 (PFM バージョン) と、一定の周波数を維持しながら、全負荷範囲にわたって出力電圧リップルが小さい強制パルス幅変調 (FPWM バージョン) があります。ソフト スタートと補償回路を内蔵しており、最小限の外付け部品でデバイスを使用できます。

このデバイスには、サイクル単位の電流制限、ヒカップ モード短絡保護、過剰な電力消費時のサーマル シャットダウンなどの保護機能が組み込まれています。

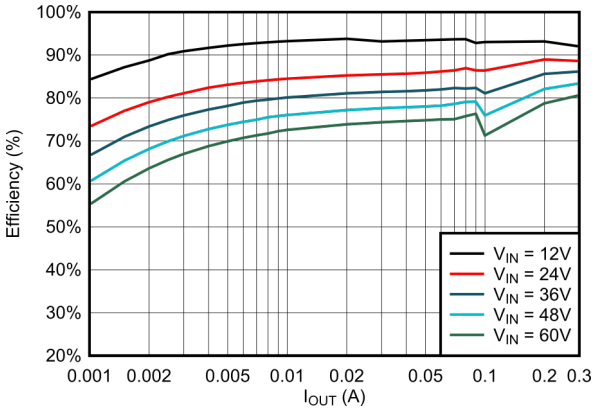
パッケージ情報

部品番号(3)	パッケージ(1)	パッケージ サイズ(2)
LMR51603-Q1	DBV (SOT-23、6)	2.90mm × 2.80 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 「製品比較表」を参照してください。



概略回路図



効率と出力電流との関係
V_{OUT} = 5V、400kHz

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4 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT CURRENT	FREQUENCY	PFM OR FPWM	OUTPUT
LMR51603XQDBVRQ1	300mA	400kHz	PFM	Adjustable
LMR51603XFQDBVRQ1	300mA	400kHz	FPWM	Adjustable

5 Pin Configuration and Functions

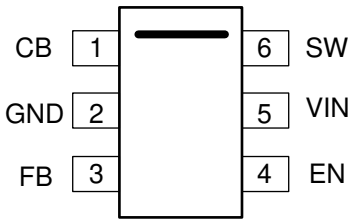


図 5-1. 6-Pin SOT-23 DBV Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
CB	1	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
GND	2	G	Power ground pins. Connected to the source of low-side FET internally. Connect to system ground, ground side of C_{IN} and C_{OUT}. The path to C_{IN} must be as short as possible.
FB	3	A	Feedback input to the converter. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
EN	4	A	Precision enable input to the converter. Do not float. High = On, Low = Off. Can be tied to VIN. Precision enable input allows an adjustable UVLO by an external resistor divider.
VIN	5	P	Supply input pin to the internal bias LDO and high-side FET. Connect to the input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
SW	6	P	Switching output of the converter. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to the power inductor.

(1) A = Analog, P = Power, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

Over junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to GND	–0.3	70	V
	EN to GND	–0.3	V_{IN} + 0.3	V
	FB to GND	–0.3	5.5	V
Output voltage	SW to GND	–0.3	70	V
	SW to GND less than 10ns transients	–5	70	V
	CBOOT to SW	–0.3	5.5	V
Junction Temperature T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input voltage	VIN to GND	4		65	V
	EN	0		V_{IN}	V
	FB	0		4.5	V
Output voltage	V_{OUT} (2)	0.8		28	V
Output current	I_{OUT} (3)			300	mA
T_J	Operating junction temperature(4)	–40		+150	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not specify specific performance limits. For compliant specifications, see Electrical Characteristics table.
(2) Under no conditions can the output voltage be allowed to fall below zero volts.
(3) Maximum continuous DC current can be derated when operating with high switching frequency or high ambient temperature. See Application section for details.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 150°C.

6.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 4-layer PCB, a $R_{\theta JA}$ = 67.2°C/W can be achieved. For design information, see Maximum Output Current Versus Ambient Temperature.

THERMAL METRIC(1)		LMR51603-Q1 DBV(SOT-23-6) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.8	°C/W
$R_{\theta JA(Effective)}$	Junction-to-ambient thermal resistance with EVM	67.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4V to 65V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	V_{EN} = 3V, FPWM operation		420		µA
$I_{Q(VIN)}$	VIN quiescent current (non-switching) (2)	V_{EN} = 3V, PFM variant only		26.5	40	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0V		0.8	3	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		3.82	4	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	3.4	3.56		V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.25		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.1	1.227	1.36	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.85	1.0	1.15	V
$I_{EN(P2)}$	EN pin sourcing current post EN rising threshold	V_{EN} = 3V		10	50	nA
REFERENCE VOLTAGE						
V_{FB}	Reference voltage		0.792	0.8	0.808	V
$I_{FB(LKG)}$	FB input leakage current	Adjustable configuration, V_{FB} = 0.8V		0.2		nA
SWITCHING FREQUENCY						
$f_{SW(CCM)}$	Switching frequency, CCM operation	"X" Version	360	400	440	KHz
STARTUP						
t_{SS}	Internal fixed soft-start time			2.3		ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 12V, T_J = 25°C		0.7		Ω
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 12V, T_J = 25°C		0.36		Ω
$t_{ON(min)}$	Minimum ON pulse width	V_{IN} = 12V, I_{OUT} = 0.1A		80		ns
$t_{ON(max)}$	Maximum ON pulse width	V_{IN} = 12V, I_{OUT} = 0.3A		5		µs
$t_{OFF(min)}$	Minimum OFF pulse width	V_{IN} = 5V		200		ns

6.5 Electrical Characteristics (続き)

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4V to 65V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERCURRENT PROTECTION						
$I_{HS\_PK(OC)}$	High-side peak current limit		0.4	0.55	0.7	A
$I_{LS\_V(OC)}$	Low-side valley current limit		0.32	0.42	0.51	A
$I_{LS(NOC)}$	Low-side negative current limit	FPWM only		–0.27		A
I_{ZC}	Zero-cross detection current threshold			0		A
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (3)	Temperature rising		165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (3)			20		°C

(1) MIN and MAX limits are 100% production tested at 25℃. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) Not production tested. Specified by correlation by design.

6.6 System Characteristics

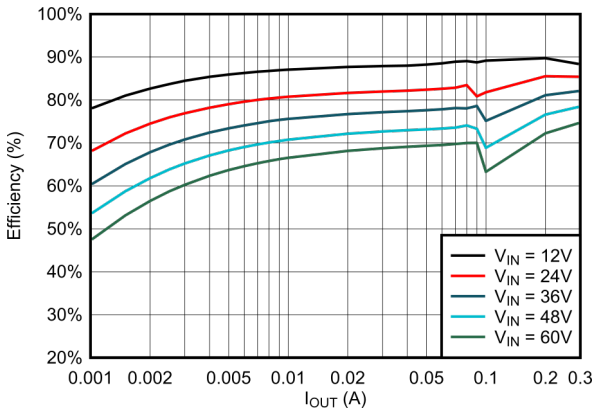
The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not specified by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range		4		65	V
V_{OUT}	Adjustable output voltage regulation(1)	PFM operation	–1.5%		2.5%	
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A, R_{FBB} = 22.1kΩ, PFM variant		38		µA
D_{MAX}	Maximum switch duty cycle(2)			96%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.32		V

(1) Deviation in V_{OUT} from nominal output voltage value at V_{IN} = 24V, I_{OUT} = 0A to full load
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: F_{MIN} = 1 / ($t_{ON\text{-}MAX}$ + $t_{OFF\text{-}MIN}$). D_{MAX} = $t_{ON\text{-}MAX}$ / ($t_{ON\text{-}MAX}$ + $t_{OFF\text{-}MIN}$).

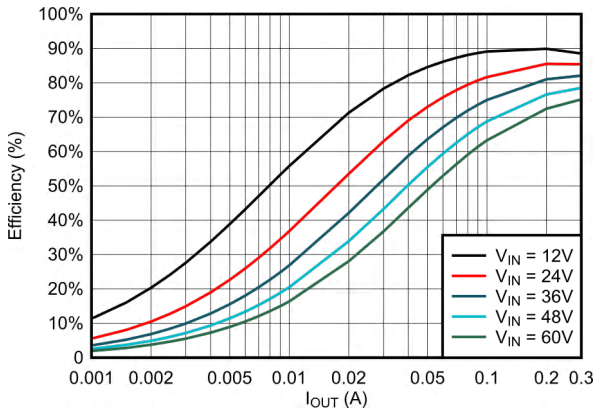
6.7 Typical Characteristics

V_{IN} = 24V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise specified



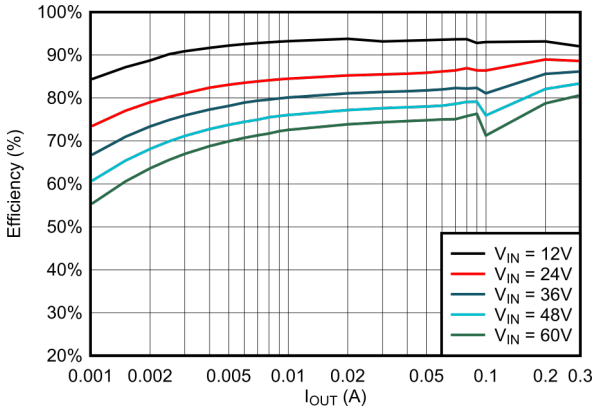
f_{SW} = 400kHz V_{OUT} = 3.3V LMR51603X-Q1

図 6-1. 3.3V PFM Efficiency Versus Load Current



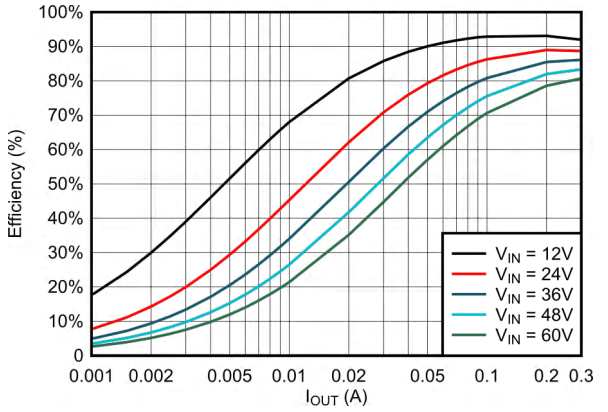
f_{SW} = 400kHz V_{OUT} = 3.3V LMR51603XF-Q1

図 6-2. 3.3V FPWM Efficiency Versus Load Current



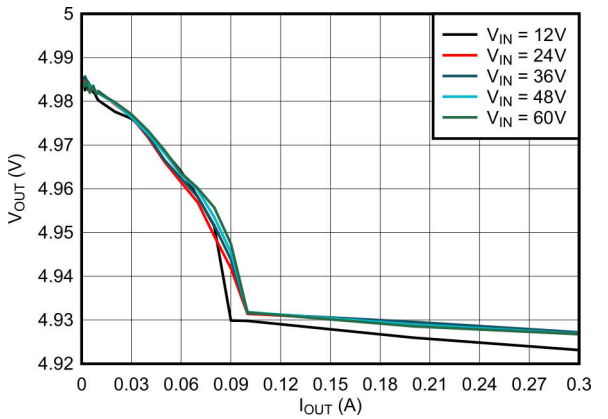
f_{SW} = 400kHz V_{OUT} = 5V LMR51603X-Q1

図 6-3. 5V PFM Efficiency Versus Load Current



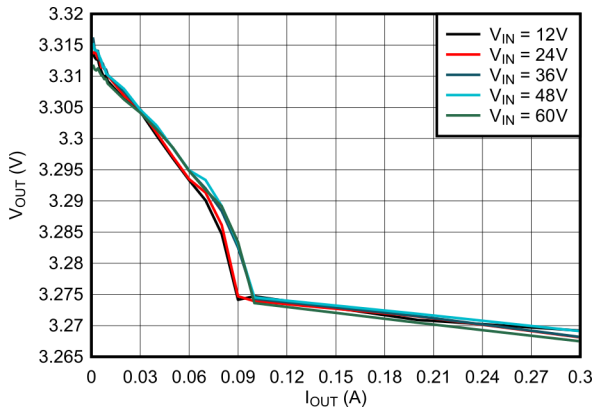
f_{SW} = 400kHz V_{OUT} = 5V LMR51603XF-Q1

図 6-4. 5V FPWM Efficiency Versus Load Current



f_{SW} = 400kHz V_{OUT} = 5V LMR51603X-Q1

図 6-5. 5V load Regulation



f_{SW} = 400kHz V_{OUT} = 3.3V LMR51603X-Q1

図 6-6. 3.3V Load Regulation

6.7 Typical Characteristics (continued)

V_{IN} = 24V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise specified

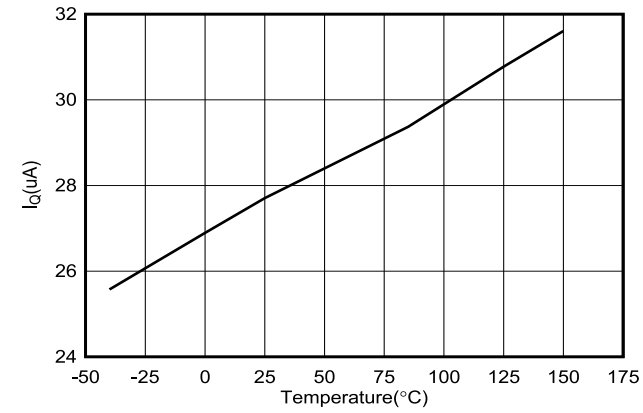


図 6-7. V_{IN} Quiescent Current Versus Temperature

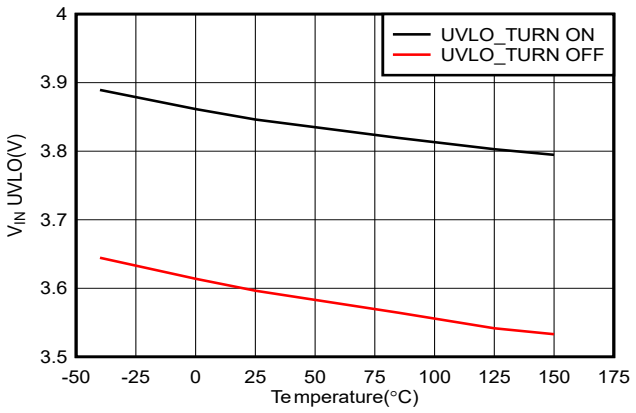


図 6-8. V_{IN} UVLO Versus Temperature

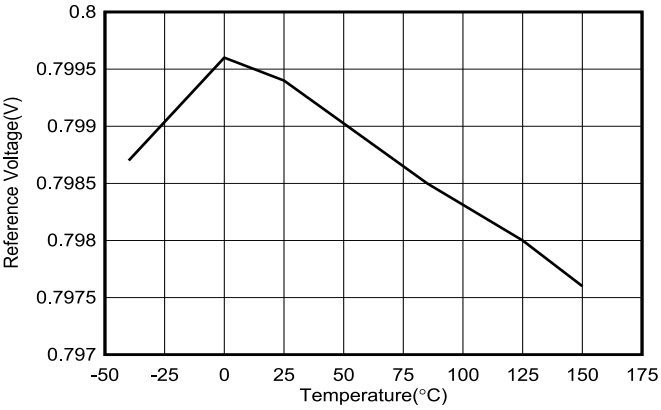


図 6-9. Reference Voltage Versus Temperature

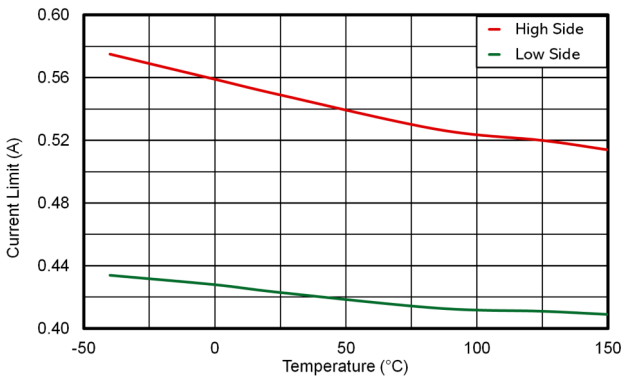


図 6-10. HS and LS Current Limit Versus Temperature

7 Detailed Description

7.1 Overview

The LMR51603-Q1 converter is an easy-to-use, synchronous, step-down DC/DC converter operating from a 4V to 65V supply voltage. The LMR51603-Q1 is capable of delivering up to 300mA DC load current in a very small design size. The family has multiple versions applicable to various applications. For detailed information, see the *Device Comparison Table*.

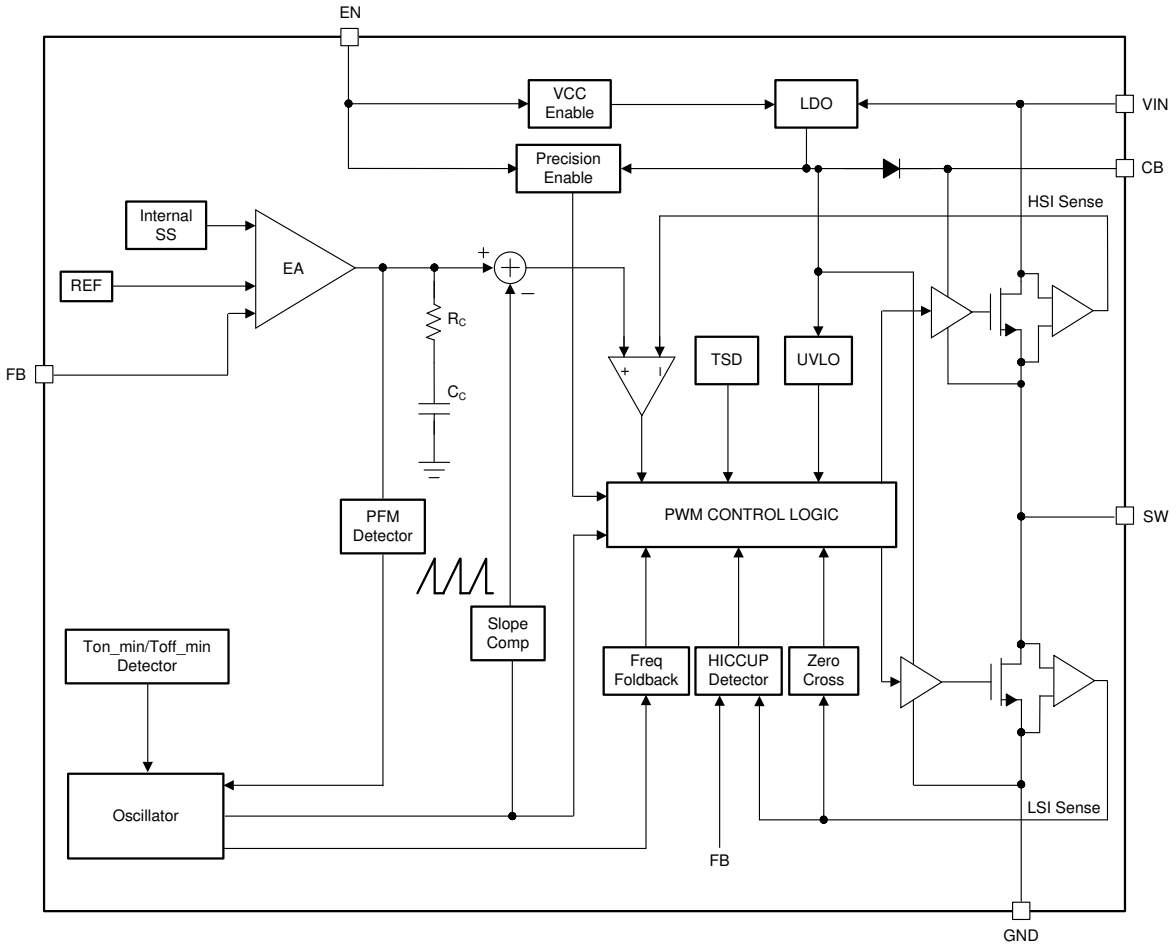
The LMR51603-Q1 employs fixed-frequency peak-current mode control. The PFM version enters PFM mode at light load to achieve high efficiency. A FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time and requires few external components.

Additional features, such as precision enable and internal soft start, provide a flexible and easy-to-use design for a wide range of applications. Protection features include the following:

- Thermal shutdown
- V_{IN} undervoltage lockout
- Cycle-by-cycle current limit
- Hiccup mode short-circuit protection

This family of devices requires very few external components and has a pinout designed for simple, designed for PCB layout.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LMR51603-Q1 refers to the *Functional Block Diagram* and to the waveforms in 図 7-1. The LMR51603-Q1 is a step-down synchronous buck converter with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR51603-Q1 supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope of (V_{IN} – V_{OUT}) / L. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of –V_{OUT} / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

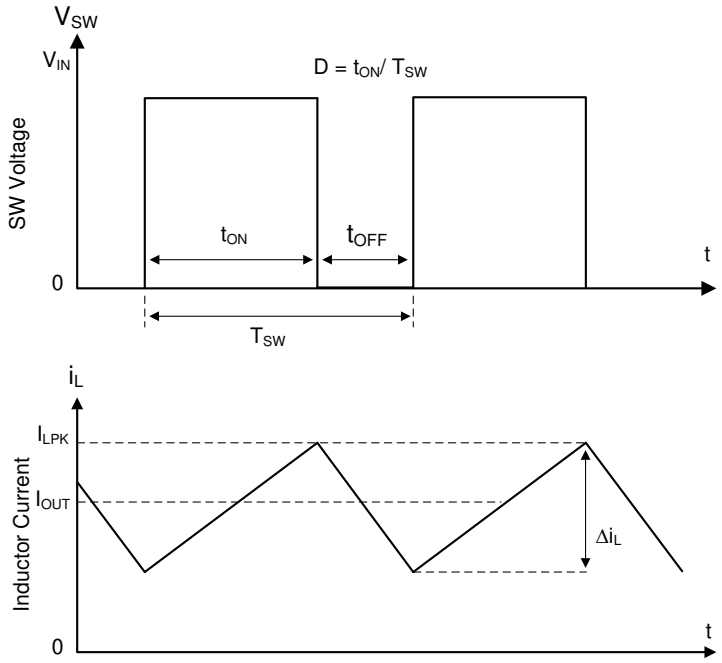


図 7-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR51603-Q1 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making designing easy and providing stable operation when using a variety of output capacitors. The converter operates with fixed switching frequency at normal load conditions. During light-load condition, the LMR51603-Q1 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

7.3.2 Adjustable Output Voltage

A precision 0.8V reference voltage (V_{REF}) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from V_{OUT} to the FB pin. TI recommends to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor, R_{FBB}, for the desired divider current and use 式 1 to calculate the top-side resistor, R_{FBT}. The recommended range for R_{FBT} is 10kΩ to 100kΩ. A lower R_{FBT} value can be used if pre-loading is desired to reduce the V_{OUT} offset in PFM operation. Lower R_{FBT} values reduce efficiency at very light load. Less static

current goes through a larger R_{FBT} value and can be more desirable when light-load efficiency is critical. However, TI does not recommend R_{FBT} values larger than 1MΩ make the feedback path more susceptible to noise. Larger R_{FBT} values require a more carefully designed feedback path trace from the feedback resistors to the feedback pin of the device. The tolerance and temperature variation of the resistor divider network affect the output voltage regulation.

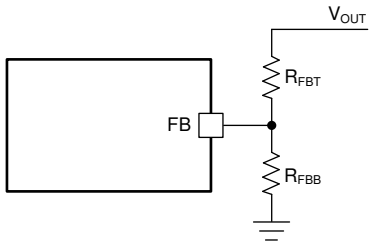


図 7-2. Output Voltage Setting

$$R_{FBT} = \frac{(V_{OUT} - V_{REF})}{V_{REF}} \times R_{FBB} \quad (1)$$

7.3.3 Enable

The voltage on the EN pin controls the ON and OFF operation of the LMR51603-Q1. A voltage of less than 1V (typical) shuts down the device, while a voltage of greater than 1.227V (typical) is required to start the converter. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR51603-Q1 is to connect EN to VIN. This connection allows self-start-up of the LMR51603-Q1 when V_{IN} is within the operating range.

Many applications benefit from the employment of an enable divider, R_{ENT} and R_{ENB} (図 7-3) to establish a precision system UVLO level for the converter. A system UVLO can be used for supplies operating from utility power as well as battery power. A system UVLO can be used for sequencing, make sure there is reliable operation, or supplying protection, such as a battery discharge level. An external logic signal can also be used to drive the EN input for system sequencing and protection.

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The EN pin voltage must not to be greater than V_{IN} + 0.3V. TI does not recommend to apply EN voltage when V_{IN} is 0V.

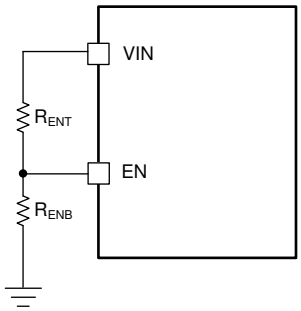

図 7-3. System UVLO by Enable Divider

7.3.4 Minimum ON Time, Minimum OFF Time, and Frequency Foldback

The minimum ON time (t_{ON_MIN}) is the shortest duration of time that the high-side switch can be turned on. t_{ON_MIN} is typically 80ns for the LMR51603-Q1. The minimum OFF time (t_{OFF_MIN}) is the shortest duration of time that the high-side switch can be off. t_{OFF_MIN} is typically 200ns. In CCM operation, t_{ON_MIN} and t_{OFF_MIN} limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (2)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (3)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \quad (4)$$

The minimum V_{IN} without frequency foldback can be calculated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \quad (5)$$

In the LMR51603-Q1, a frequency foldback scheme is employed after the t_{ON_MIN} or t_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on time decreases while V_{IN} voltage increases. After the on time decreases to t_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to 式 4.

The frequency foldback scheme also works after larger duty cycle is needed under a low V_{IN} condition. The frequency decreases after the device hits t_{OFF_MIN}, which extends the maximum duty cycle according to 式 5. In such condition, the frequency can be as low as approximately 200kHz. A wide range of frequency foldback allows for the LMR51603-Q1 output voltage to stay in regulation with a much lower supply voltage V_{IN}, which leads to a lower effective dropout.

With frequency foldback while maintaining a regulated output voltage, V_{IN_MAX} is raised and V_{IN_MIN} is lowered by decreased f_{SW}.

7.3.5 Bootstrap Voltage

The LMR51603-Q1 provides an integrated bootstrap voltage converter. A small capacitor between the CB and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch is on. The recommended value of the bootstrap capacitor is 0.1µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16V or higher for stable performance over temperature and voltage.

7.3.6 Overcurrent and Short-Circuit Protection

The LMR51603-Q1 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side switch current is sensed when the high-side is turned on after a set blanking time. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. See the *Functional Block Diagram* for more details. The peak current of high-side switch is limited by a clamped maximum peak current threshold $I_{HS\_PK(OC)}$ (see *Electrical Characteristics*), which is constant.

The current going through the low-side MOSFET is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down. The low-side switch is not turned OFF at the end of a switching

cycle if the current is above the low-side current limit, $I_{LS\_V(OC)}$ (see *Electrical Characteristics*). The low-side switch is kept ON so that inductor current keeps ramping down until the inductor current ramps below $I_{LS\_V(OC)}$. Then, the low-side switch is turned OFF and the high-side switch is turned on after a dead time. After $I_{LS\_V(OC)}$ is achieved, peak and valley current limit controls the maximum current delivered and can be calculated using 式 6.

$$I_{OUT\_MAX} = \frac{I_{HS\_PK(OC)} + I_{LS\_V(OC)}}{2} \quad (6)$$

If the feedback voltage is lower than 40% of the V_{REF}, the current of the low-side switch triggers $I_{HS\_PK(OC)}$ for 256 consecutive cycles and hiccup current protection mode is activated. In hiccup mode, the converter shuts down and keeps off for a period of hiccup, T_{HICCUP} (150ms typical) before the LMR51603-Q1 tries to start again. If overcurrent or a short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, preventing overheating and potential damage to the device.

For the FPWM version, the inductor current is allowed to go negative. When this current exceeds the low-side negative current limit, $I_{LS(NOC)}$, the low-side switch is turned off and high-side switch is turned on immediately. This event is used to protect the low-side switch from excessive negative current.

7.3.7 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the LMR51603-Q1 and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. The typical soft-start time is 2.3ms.

The LMR51603-Q1 also employs overcurrent protection blanking time, T_{OCP_BLK} (33ms typical), at the beginning of power up. Without this feature, in applications with a large amount of output capacitors and high V_{OUT}, the inrush current is large enough to trigger the current-limit protection, which can cause a false start as the device enters into hiccup mode. This event results in a continuous recycling of soft start without raising up to the programmed output voltage. The LMR51603-Q1 is able to charge the output capacitor to the programmed V_{OUT} by controlling the average inductor current during the start-up sequence in the blanking time, T_{OCP_BLK}.

7.3.8 Thermal Shutdown

The LMR51603-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 165°C. Both high-side and low-side FETs stop switching in thermal shutdown. After the die temperature falls below 145°C, the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMR51603-Q1. When V_{EN} is below 1V (typical) , the device is in shutdown mode. The LMR51603-Q1 also employs V_{IN} undervoltage lockout protection (UVLO). If V_{IN} voltage is below the UVLO threshold of 3.56V (typical), the converter turns off.

7.4.2 Active Mode

The LMR51603-Q1 is in active mode when both V_{EN} and V_{IN} are above the respective operating threshold. The simplest way to enable the LMR51603-Q1 is to connect the EN pin to VIN pin. This action allows self-start-up when the input voltage is in the operating range of 4V to 65V. See *Enable* for details on setting these operating levels.

In active mode, depending on the load current, the LMR51603-Q1 is in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is greater than half of the peak-to-peak inductor current ripple (for both PFM and FPWM versions)
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is less than half of the peak-to-peak inductor current ripple(only for PFM versions)
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM version)
4. Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM version)

7.4.3 CCM Mode

Continuous conduction mode (CCM) operation is employed in the LMR51603-Q1 when the load current is greater than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 300mA can be supplied by the LMR51603-Q1.

7.4.4 Light Load Operation (PFM Version)

For PFM versions, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR51603-Q1 operates in discontinuous conduction mode (DCM), also known as diode emulation mode (DEM). In DCM operation, the low-side switch is turned off when the inductor current drops to I_{ZC} (0mA typical) to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

During light load operation, pulse frequency modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum high-side switch ON time t_{ON_MIN} or the minimum peak inductor current I_{PEAK_MIN} (typically 180mA for LMR51603-Q1) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency.

7.4.5 Light-Load Operation (FPWM Version)

For FPWM versions, LMR51603-Q1 is locked in continuous conduction across the entire load range. This operation is maintained, even in no-load condition, by allowing the inductor current to reverse the normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMR51603-Q1 is a step-down DC-to-DC converter. The LMR51603-Q1 is typically used to convert a higher input voltage to a lower output DC voltage with a maximum output current of 300mA. The following design procedure can be used to select components for the LMR51603-Q1.

8.2 Typical Application

The LMR51603-Q1 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. The following image shows a basic schematic.

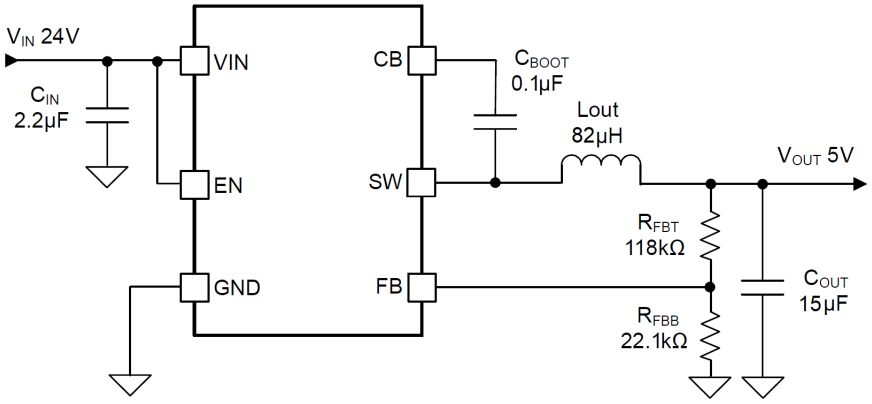

図 8-1. Application Circuit

The external components must fulfill the needs of the application and the stability criteria of the control loop of the device. The following table can be used to simplify the output filter component selection.

表 8-1. L and C_{OUT} Typical Values

f_{SW} (kHz)	V_{OUT} (V)	I_{OUT} (mA)	L (µH)	C_{OUT} (1)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
400	3.3	300	56	22µF / 10V	69.8	22.1
	5	300	82	15µF / 16V	118	22.1
	12	300	150	2 × 4.7µF / 35V	309	22.1

(1) A ceramic capacitor is used in this table.

8.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in the following table as the input parameters.

表 8-2. Design Example Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	24V typical, range from 6V to 65V
Output voltage, V_{OUT}	5V ±3%
Maximum output current, I_{OUT_MAX}	300mA
Output overshoot, undershoot (0mA to 300mA)	±5%
Output voltage ripple	0.5%
Operating frequency	400kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR51603-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the LMR51603-Q1 device is externally adjustable using a resistor divider network. The divider network is comprised of a top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. 式 7 is used to determine the output voltage of the converter:

$$R_{FBT} = \frac{(V_{OUT} - V_{REF})}{V_{REF}} \times R_{FBB} \quad (7)$$

Choose the value of R_{FBB} to be 22.1kΩ. With the desired output voltage set to 5V and the V_{REF} = 0.8V, the R_{FBT} value can then be calculated using 式 7. The formula yields to a value 116kΩ, a standard value of 118kΩ is selected.

8.2.2.3 Switching Frequency

For this example, the default switching frequency of 400kHz is selected.

8.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use 式 9 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% to 60% of maximum I_{OUT} supported by converter. During an instantaneous overcurrent operation event, the RMS

and peak inductor current can be high. The inductor saturation current must be higher than peak current limit level.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \quad (8)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (9)$$

In general, choose lower inductance in switching power supplies because lower inductance usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. Too low of an inductance also generates more inductor core loss because the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, TI recommends to have adequate amount of inductor ripple current. A larger inductor ripple current improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.5. The minimum inductor value is calculated to be 76.92µH. Choose the nearest standard 82µH inductor with a capability of 360mA RMS current and 850mA saturation current.

8.2.2.5 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. Minimize the output capacitance to keep cost and size down. The output capacitor or capacitors, C_{OUT}, must be chosen with care because the capacitors directly affects the steady state output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient. The output voltage ripple is essentially composed of two parts. One part is caused by the inductor ripple current flowing through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (10)$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

The two components of the voltage ripple are not in-phase, therefore, the actual peak-to-peak ripple is less than the sum of the two peaks.

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \quad (11)$$

The output capacitance value is limited by the load transient specifications of the system. When a large load step occurs, output capacitors provide the required charge before the inductor current can slew to an appropriate level. The control loop of the converter usually requires eight or more clock cycles to regulate the inductor current equal to the new load level during this time. The output capacitance must be large enough to supply the current difference for eight clock cycles to maintain the output voltage within the specified range. 式 12 shows the minimum output capacitance needed for a specified V_{OUT} overshoot and undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \quad (12)$$

where

- K_{IND} = Ripple ratio of the inductor current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{OUT_SHOOT} = Target output voltage overshoot or undershoot

For this design example, the target output ripple is 25mV. Assuming ΔV_{OUT_ESR} = ΔV_{OUT_C} = 15mV, choose K_{IND} = 0.5. 式 10 yields ESR no larger than 100mΩ and 式 11 yields C_{OUT} no smaller than 1.88µF. For the target

overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} is 250mV. The C_{OUT} can be calculated to be no less than 12µF by 式 12. In summary, the most stringent criteria for the output capacitor is 12µF. Considering derating, one 15µF, 16V, X7R ceramic capacitor with 10mΩ ESR is used.

8.2.2.6 Input Capacitor Selection

The LMR51603-Q1 device requires a high frequency input decoupling capacitor or capacitor. The typical recommended value for the high frequency decoupling capacitor is 1µF or higher. TI recommends a high-quality ceramic type X5R or X7R with sufficiency voltage rating. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage. For this design, one 1µF , X7R dielectric capacitor rated for 100V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 10mΩ, and the current rating is 100mA. Include a capacitor with a value of 0.1µF for high-frequency filtering and place the capacitor as close as possible to the device pins.

8.2.2.7 Bootstrap Capacitor

Every LMR51603-Q1 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.1µF and rated at 16V or higher. The bootstrap capacitor is located between the SW pin and the CB pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.8 Undervoltage Lockout Setpoint

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. 式 13 can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{EBT} + R_{ENB}}{R_{ENB}} \tag{13}$$

The EN rising threshold ($V_{EN(R)}$) for LMR51603-Q1 is set to be 1.227V (typical). Choose a value of 200kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} rising UVLO level is at 6.0V (typical), then the value of R_{ENT} can be calculated using 式 14:

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{EN(R)}} - 1\right) \times R_{ENB} \tag{14}$$

The above equation yields a value of 778kΩ, a standard value of 768kΩ is selected. The resulting V_{IN} falling UVLO threshold, equal to 4.84V, can be calculated by 式 15 where EN falling threshold ($V_{EN(F)}$) for LMR51603-Q1 is set to be 1.0V (typical).

$$V_{IN\_FALLING} = V_{EN(F)} \times \frac{R_{EBT} + R_{ENB}}{R_{ENB}} \tag{15}$$

8.2.2.9 Replacing Non Sync Buck Converter

The LMR51603-Q1 can also be used to replace asynchronous buck converters, which need a rectifying diode in the application circuit. The design works fine with or without a rectifying diode connected to the switch node of the LMR51603-Q1 as shown in 図 8-2.

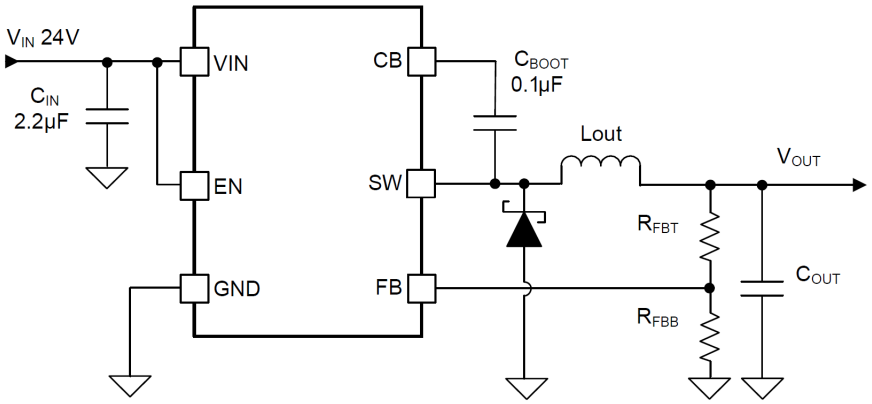

図 8-2. Replacing Non-Sync Buck Converter

8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, L = 82µH, C_{OUT} = 15µF, T_A = 25°C.

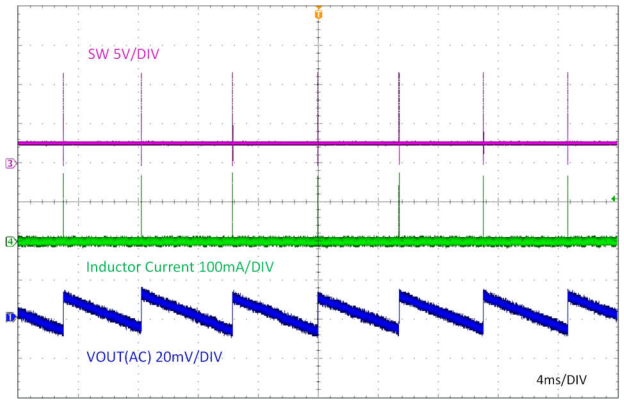

図 8-3. Ripple at No Load

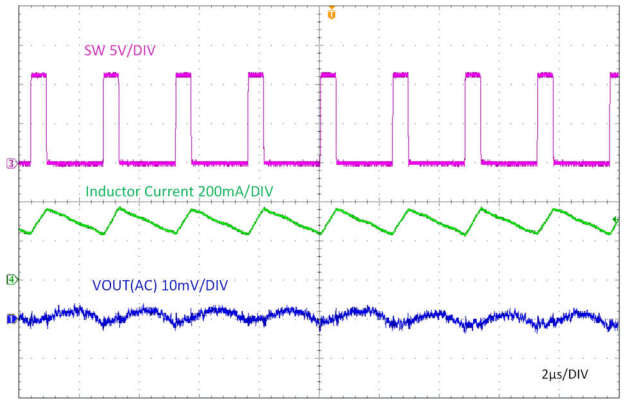

図 8-4. Ripple at Full Load

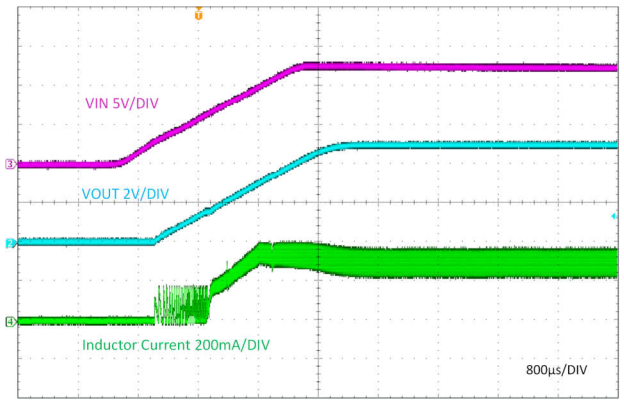

図 8-5. Start-Up by V_{IN}

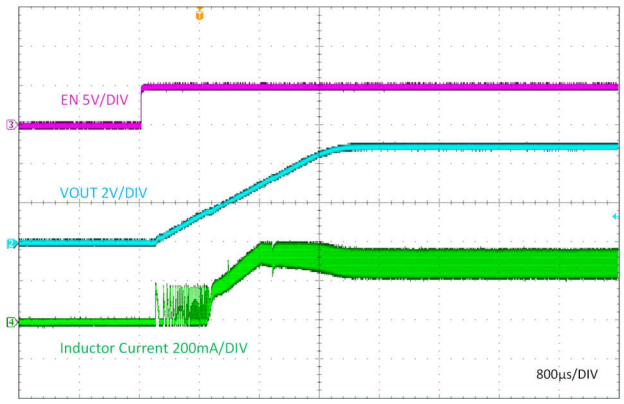

図 8-6. Start-Up by EN

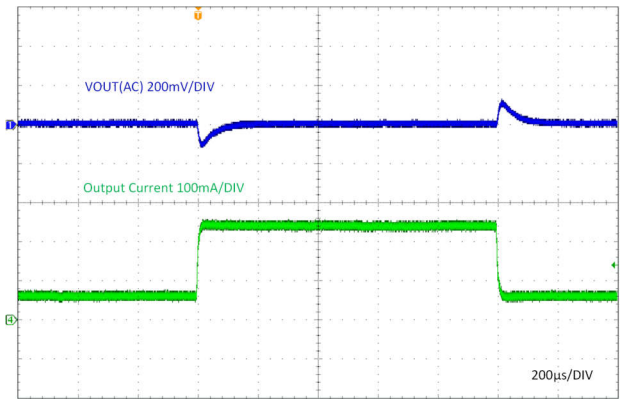

図 8-7. Load Transient (60mA – 240mA)

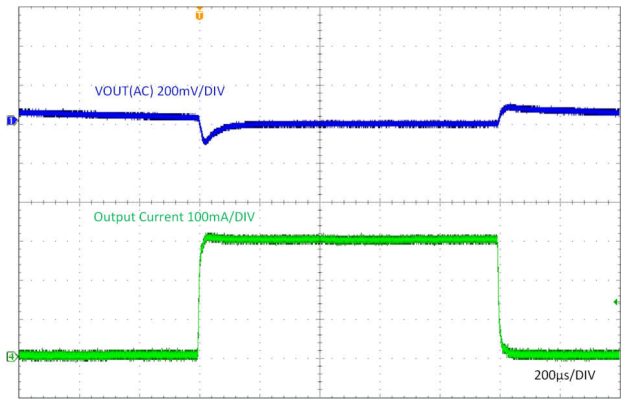

図 8-8. Load Transient (0mA – 300mA)

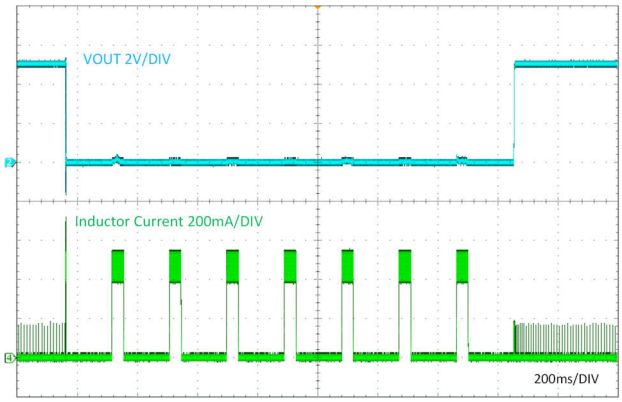

図 8-9. Short Protection and Recovery

8.3 Power Supply Recommendations

The LMR51603-Q1 is designed to operate from an input voltage supply range between 4V and 65V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR51603-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR51603-Q1 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 10µF or 22µF electrolytic capacitor is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

- Place the input bypass capacitor C_{IN} as close as possible to the VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the GND pin.
- Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB}, must be located close to the FB pin. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
- Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This action reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Provide adequate device heat-sinking. GND, VIN, and SW pins provide the main heat dissipation path and make the GND, VIN, and SW plane area as large as possible. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Make sure enough copper area is used for heat-sinking to keep the junction temperature below 150°C.

8.4.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing a ceramic bypass capacitor or capacitors as close as possible to the VIN and GND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to GND pin.

8.4.1.2 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so the pin is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provides the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This action is most important when high value resistors are used to set the output voltage. TI recommends to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This action provides further shielding for the voltage feedback path from EMI noises.

8.4.2 Layout Example

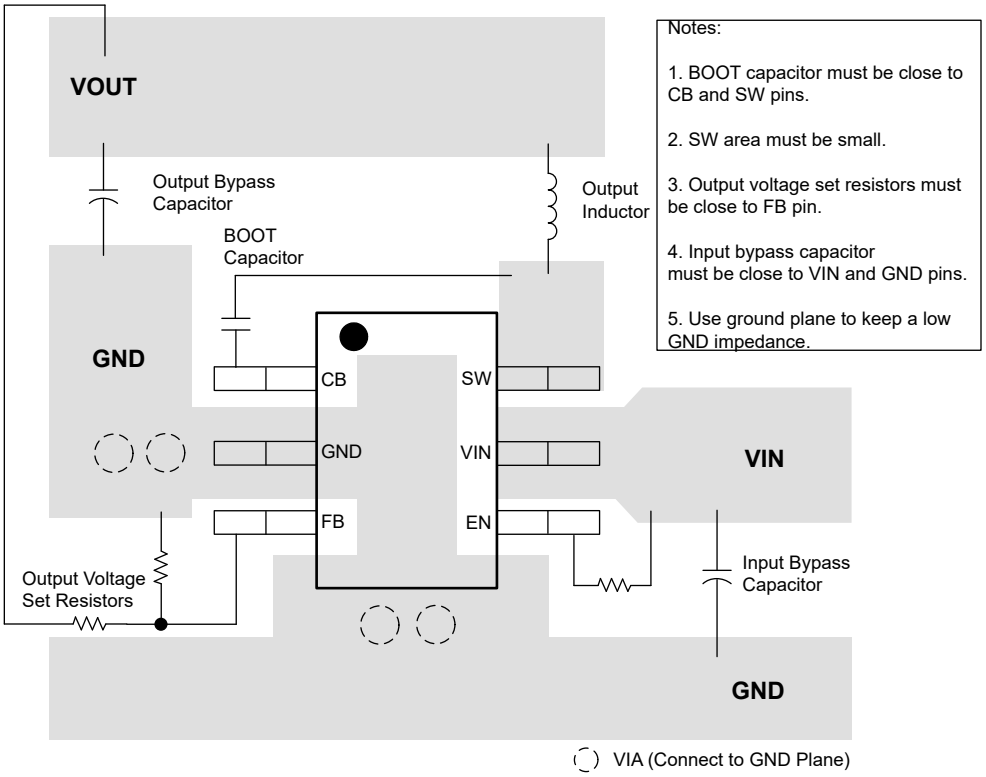

図 8-10. Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR51603-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application note

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

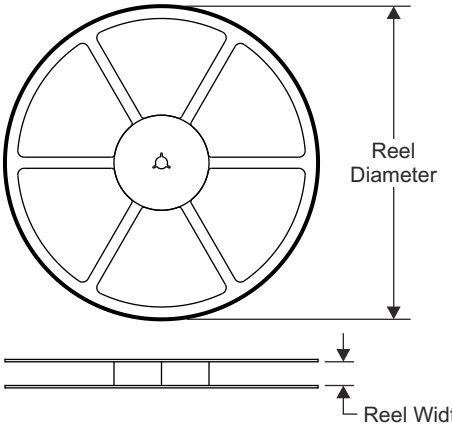
DATE	REVISION	NOTES
September 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

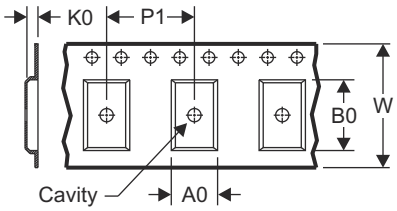
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

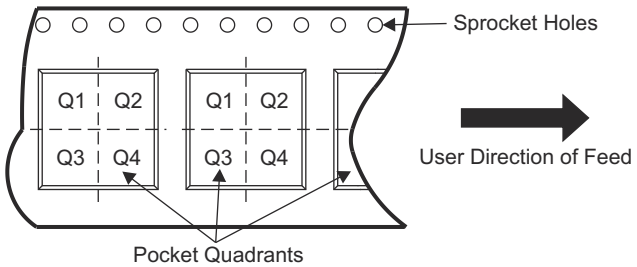


TAPE DIMENSIONS



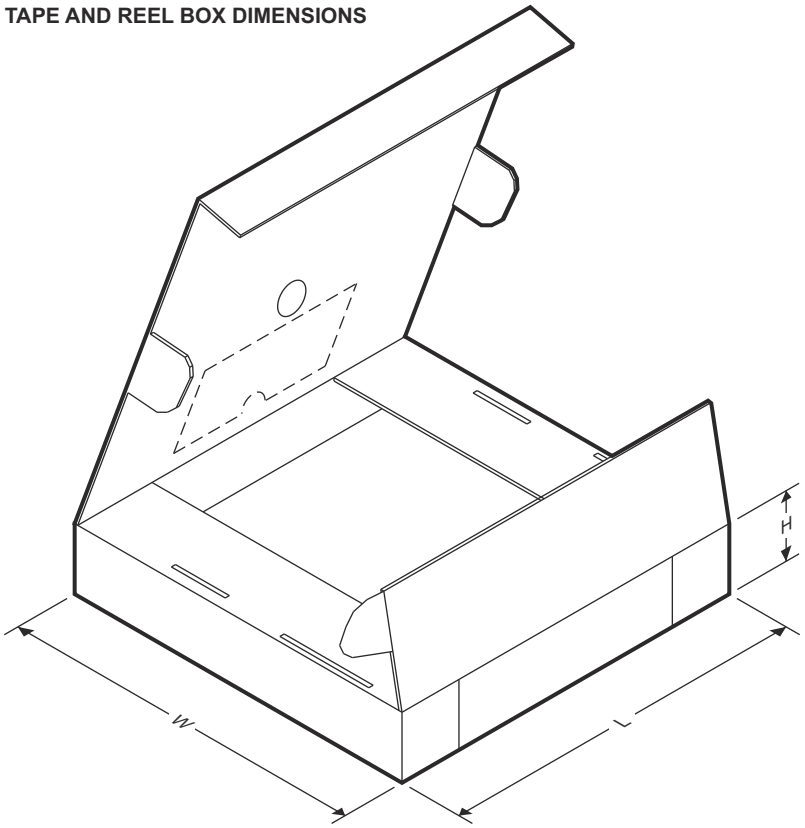
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR51603XQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51603XFQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR51603XQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
LMR51603XFQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR51603XFQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	3XFQ
LMR51603XFQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	3XFQ
LMR51603XQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	63XQ
LMR51603XQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	63XQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LMR51603-Q1 :

- Catalog : LMR51603

NOTE: Qualified Version Definitions:

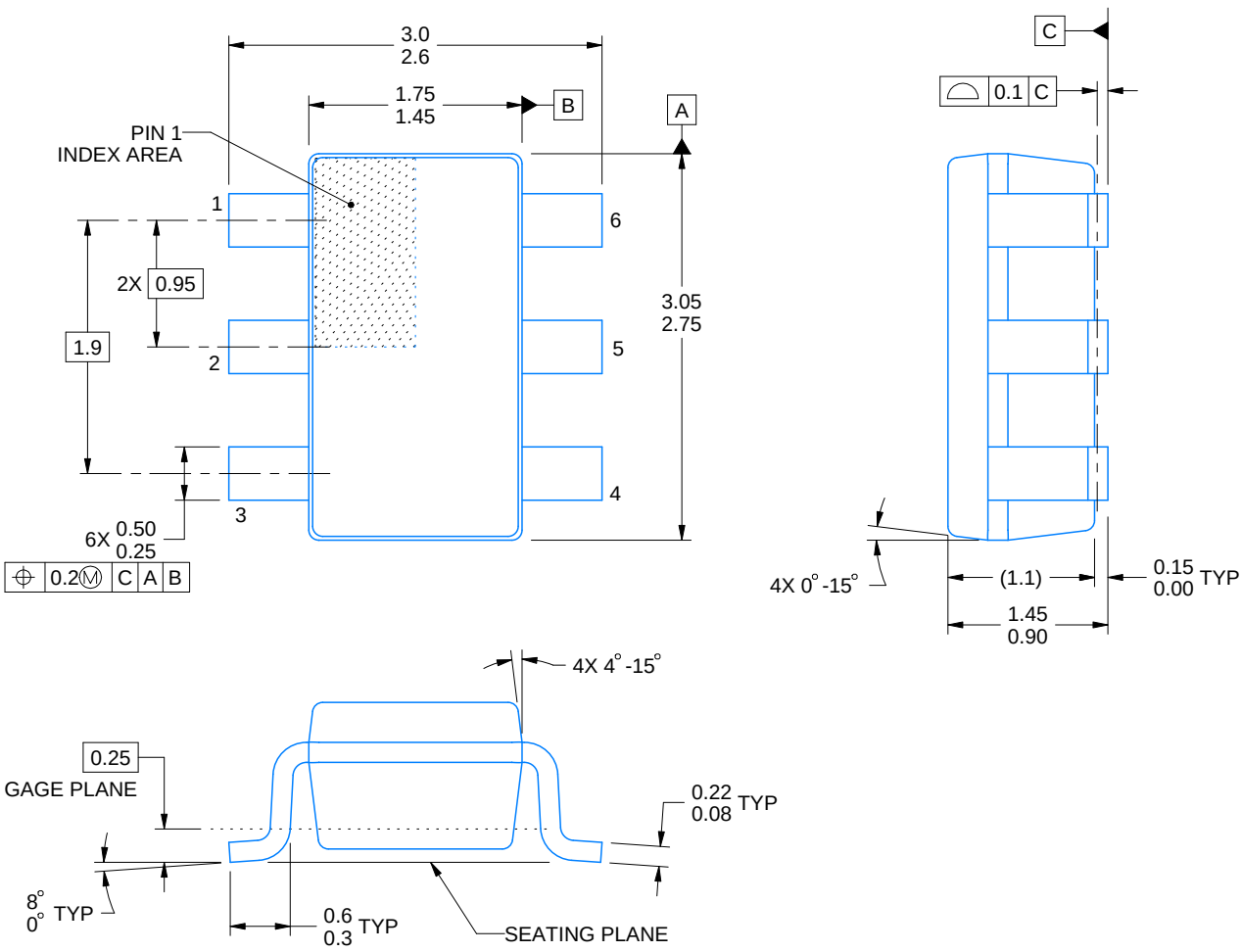
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

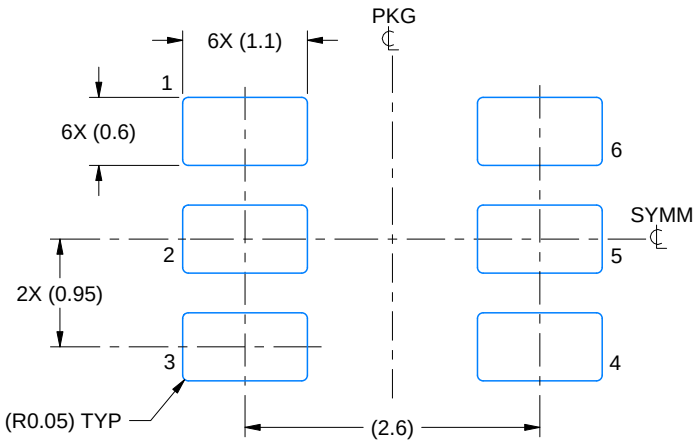
SMALL OUTLINE TRANSISTOR



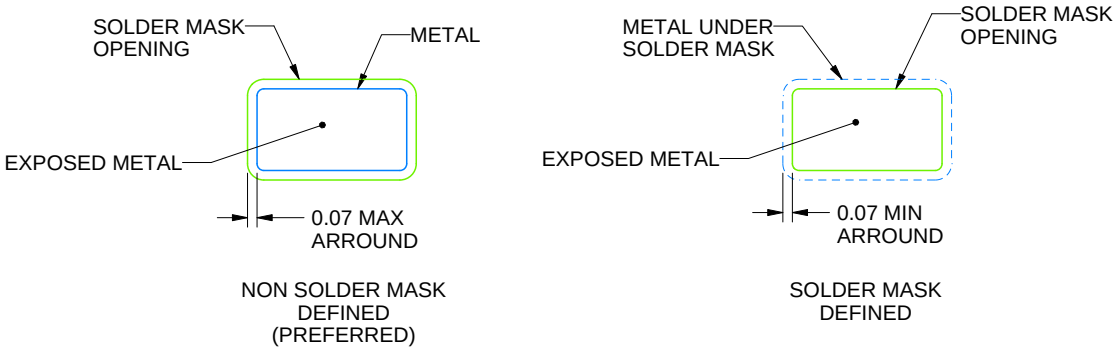
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

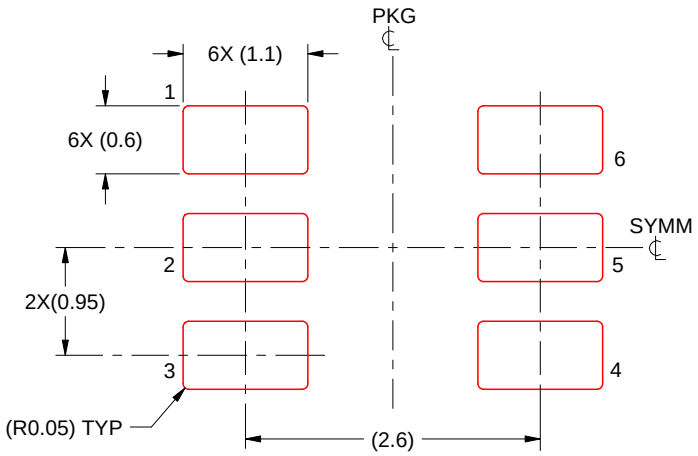


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月