TEXAS INSTRUMENTS
LMV841-Q1, LMV842-Q1, LMV844-Q1
JAJSE16 – OCTOBER 2017

# LMV84x-Q1 CMOS入力、RRIO、低消費電力、広い電源電圧範囲の4.5MHzオペアンプ

## 1 特長

- 次の結果でAEC-Q100車載用認定テスト・ガイダンス
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC3
- 特に記述のない限り、$T_A$ = 25℃、$V^+$ = 5Vでの標準値
- 小さな5ピンSC70パッケージ(2.00mm×1.25mm×0.95mm)
- 広い電源電圧範囲: 2.7V～12V
- 3.3V、5V、±5V動作を保証
- 低消費電流: チャネルごとに1mA
- ユニティ・ゲイン帯域幅: 4.5MHz
- オープンループ・ゲイン: 133dB
- 入力オフセット電圧: 最大500µV
- 入力バイアス電流: 0.3pA
- CMRR 112dB、PSSR 108dB
- 入力電圧ノイズ: 20nV/√Hz
- 温度範囲: -40℃～125℃
- レール・ツー・レール入出力(RRIO)

## 2 アプリケーション

- 高インピーダンスのセンサ・インターフェイス
- バッテリ駆動の計測機器
- 高ゲインおよび計装用のアンプ
- DACバッファおよびアクティブ・フィルタ

## 3 概要

LMV84x-Q1デバイスは、低電圧で低消費電力のオペアンプで、2.7V～12Vの範囲の電源電圧で動作し、レール・ツー・レールの入出力機能を持ちます。オフセット電圧と消費電流が低く、CMOS入力であるため、高インピーダンスのセンサ・インターフェイスやバッテリ駆動のアプリケーションに理想的です。

シングルのLMV841-Q1は、省スペースの5ピンSC70パッケージで、デュアルのLMV842-Q1は8ピンのVSSOPおよび8ピンのSOICパッケージで、クワッドのLMV844-Q1は14ピンのTSSOPおよび14ピンのSOICパッケージで供給されます。これらの小型パッケージは、面積が制限されるPCBや携帯電子機器に理想的なソリューションです。

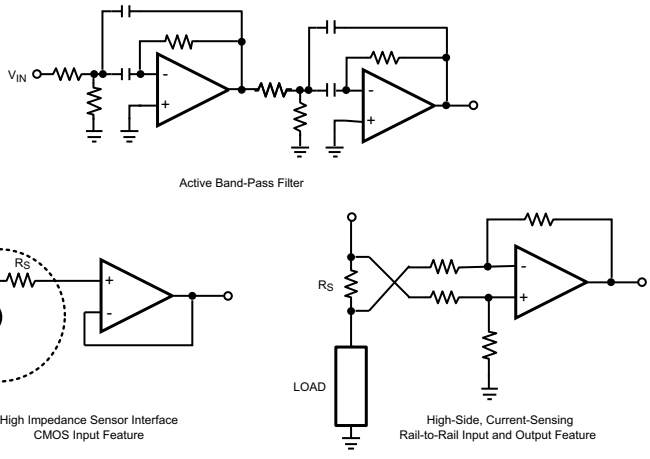
LMV841-Q1、LMV842-Q1、LMV844-Q1には、障害検出方式など、自動車市場向けの高度な製造およびサポート・プロセスが組み込まれています。AEC-Q100規格に定義されている要件および温度グレードに準拠して、信頼性が認定されています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| LMV841-Q1 | SC70 (5) | 2.00mm×1.25mm |
| LMV842-Q1 | VSSOP (8) | 3.00mm×3.00mm |
| | SOIC (8) | 4.90mm×3.91mm |
| LMV844-Q1 | SOIC (14) | 8.65mm×3.91mm |
| | TSSOP (14) | 5.00mm×4.40mm |

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

**代表的なアプリケーション**

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 日付 | 改訂内容 | 注 |
|---|---|---|
| 2017年10月 | * | 車載用データシートを商業用と分離、熱に関する情報を更新、「*代表的特性*」セクションで、位相マージンとCLの関係およびオーバーシュートとCLの関係のグラフを変更 |


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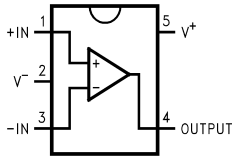
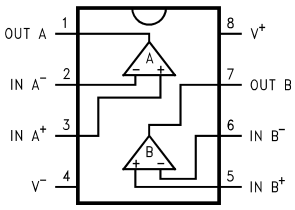
# 5 Pin Configuration and Functions

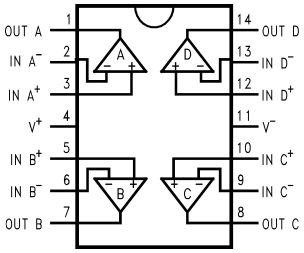
**DCK Package**
**5-Pin SC70**
**Top View**




**D or DGK Package**
**8-Pin SOIC and VSSOP**
**Top View**




**D or PW Package**
**14-Pin SOIC and TSSOP**
**Top View**




**Pin Functions**

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | I/O. | |
| +IN | I | Noninverting Input |
| –IN | I | Inverting Input |
| OUT | O | Output |
| V+ | P | Positive Supply |
| V– | P | Negative Supply |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

See (1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ differential | | –300 | 300 | mV |
| Supply voltage ($V^+ – V^–$) | | | 13.2 | V |
| Voltage at input and output pins | | $V^+$ + 0.3 | $V^–$ – 0.3 | V |
| Input current | | | 10 | mA |
| Junction temperature (3) | | | 150 | °C |
| Soldering information | Infrared or convection (20 s) | | 235 | °C |
| | Wave soldering lead temperature (10 s) | | 260 | °C |
| Storage temperature, $T_{stg}$ | | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±250 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Temperature(1) | −40 | 125 | °C |
| Supply voltage ($V^+ – V^–$) | 2.7 | 12 | V |

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LMV84x-Q1 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | DCK (SC70) | DGK (VSSOP) | D (SOIC) | | PW (TSSOP) | |
| | | 5 PINS | 8 PINS | 8 PINS | 14 PIN | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(2) | 269.9 | 179.2 | 121.4 | 85.4 | 113.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 93.8 | 69.2 | 65.7 | 43.5 | 38.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 48.8 | 99.7 | 62.0 | 39.8 | 56.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.0 | 10.0 | 16.5 | 9.2 | 3.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 47.9 | 98.3 | 61.4 | 39.6 | 55.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.


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## 6.5 Electrical Characteristics – 3.3 V

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = 3.3 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$ / 2, and $R_L$ > 10 MΩ to $V^+$ / 2.(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | | | –500 | ±50 | 500 | µV |
| | | at the temperature extremes | | –800 | | 800 | |
| $TCV_{OS}$ | Input offset voltage drift (4) | | | | 0.5 | | µV/°C |
| | | at the temperature extremes | | –5 | | 5 | |
| $I_B$ | Input bias current (4) (5) | | | | 0.3 | 10 | pA |
| | | at the temperature extremes | | | | 300 | |
| $I_{OS}$ | Input offset current | | | | 40 | | fA |
| CMRR | Common-mode rejection ratio LMV841-Q1 | 0 V ≤ $V_{CM}$ ≤ 3.3 V | | 84 | 112 | | dB |
| | | | at the temperature extremes | 80 | | | |
| | Common-mode rejection ratio LMV842-Q1 and LMV844-Q1 | 0 V ≤ $V_{CM}$ ≤ 3.3 V | | 77 | 106 | | dB |
| | | | at the temperature extremes | 75 | | | |
| PSRR | Power supply rejection ratio | 2.7 V ≤ $V^+$ ≤ 12 V, $V_O$ = $V^+$ / 2 | | 86 | 108 | | dB |
| | | | at the temperature extremes | 82 | | | |
| CMVR | Input common-mode voltage range | CMRR ≥ 50 dB, at the temperature extremes | | –0.1 | | 3.4 | V |
| $A_{VOL}$ | Large signal voltage gain | $R_L$ = 2 kΩ<br>$V_O$ = 0.3 V to 3 V | | 100 | 123 | | dB |
| | | | at the temperature extremes | 96 | | | |
| | | $R_L$ = 10 kΩ<br>$V_O$ = 0.2 V to 3.1 V | | 100 | 131 | | dB |
| | | | at the temperature extremes | 96 | | | |
| $V_O$ | Output swing high, (measured from $V^+$) | $R_L$ = 2 kΩ to $V^+$/2 | | | 52 | 80 | mV |
| | | | at the temperature extremes | | | 120 | |
| | | $R_L$ = 10 kΩ to $V^+$/2 | | | 28 | 50 | mV |
| | | | at the temperature extremes | | | 70 | |
| | Output swing low, (measured from $V^-$) | $R_L$ = 2 kΩ to $V^+$/2 | | | 65 | 100 | mV |
| | | | at the temperature extremes | | | 120 | |
| | | $R_L$ = 10 kΩ to $V^+$/2 | | | 33 | 65 | mV |
| | | | at the temperature extremes | | | 75 | |

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

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## Electrical Characteristics – 3.3 V (continued)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = 3.3 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$ / 2, and $R_L$ > 10 MΩ to $V^+$ / 2.(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| $I_O$ | Output short-circuit current(6)(7) | Sourcing $V_O$ = $V^+$/2<br>$V_{IN}$ = 100 mV | | 20 | 32 | | mA |
| | | | at the temperature extremes | 15 | | | |
| | | Sinking $V_O$ = $V^+$/2<br>$V_{IN}$ = −100 mV | | 20 | 27 | | mA |
| | | | at the temperature extremes | 15 | | | |
| $I_S$ | Supply current | Per channel | | | 0.93 | 1.5 | mA |
| | | | at the temperature extremes | | | 2 | |
| SR | Slew rate (8) | $A_V$ = 1, $V_O$ = 2.3 $V_{PP}$<br>10% to 90% | | | 2.5 | | V/µs |
| GBW | Gain bandwidth product | | | | 4.5 | | MHz |
| $\Phi_m$ | Phase margin | | | | 67 | | Deg |
| $e_n$ | Input-referred voltage noise | f = 1 kHz | | | 20 | | nV/√Hz |
| $R_{OUT}$ | Open-loop output impedance | f = 3 MHz | | | 70 | | Ω |
| THD+N | Total harmonic distortion + noise | f = 1 kHz , $A_V$ = 1<br>$R_L$ = 10 kΩ | | | 0.005% | | |
| $C_{IN}$ | Input capacitance | | | | 7 | | pF |

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D$ = ($T_{J(MAX)}$ – $T_A$) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.

## 6.6 Electrical Characteristics – 5 V

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = 5 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$ / 2, and $R_L$ > 10 MΩ to $V^+$ / 2.(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | | | –500 | ±50 | 500 | µV |
| | | at the temperature extremes | | –800 | | 800 | |
| $TCV_{OS}$ | Input offset voltage drift(4) | | | | 0.35 | | µV/°C |
| | | at the temperature extremes | | –5 | | 5 | |
| $I_B$ | Input bias current(4)(5) | | | | 0.3 | 10 | pA |
| | | at the temperature extremes | | | | 300 | |
| $I_{OS}$ | Input offset current | | | | 40 | | fA |
| CMRR | Common-mode rejection ratio LMV841-Q1 | 0 V ≤ $V_{CM}$ ≤ 5 V | | 86 | 112 | | dB |
| | | | at the temperature extremes | 80 | | | |
| | Common-mode rejection ratio LMV842-Q1 and LMV844-Q1 | 0 V ≤ $V_{CM}$ ≤ 5 V | | 81 | 106 | | dB |
| | | | at the temperature extremes | 79 | | | |
| PSRR | Power supply rejection ratio | 2.7 V ≤ $V^+$ ≤ 12 V, $V_O$ = $V^+$/2 | | 86 | 108 | | dB |
| | | | at the temperature extremes | 82 | | | |

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.


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## Electrical Characteristics – 5 V (continued)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = 5 V, $V^-$ = 0 V, $V_{CM}$ = $V^+$ / 2, and $R_L$ > 10 MΩ to $V^+$ / 2.(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| CMVR | Input common-mode voltage range | CMRR ≥ 50 dB, at the temperature extremes | | –0.2 | | 5.2 | V |
| $A_{VOL}$ | Large signal voltage gain | $R_L$ = 2 kΩ<br>$V_O$ = 0.3V to 4.7 V | | 100 | 125 | | dB |
| | | | at the temperature extremes | 96 | | | |
| | | $R_L$ = 10 kΩ<br>$V_O$ = 0.2V to 4.8V | | 100 | 133 | | dB |
| | | | at the temperature extremes | 96 | | | |
| $V_O$ | Output swing high, (measured from $V^+$) | $R_L$ = 2 kΩ to $V^+$/2 | | | 68 | 100 | mV |
| | | | at the temperature extremes | | | 120 | |
| | | $R_L$ = 10 kΩ to $V^+$/2 | | | 32 | 50 | mV |
| | | | at the temperature extremes | | | 70 | |
| | Output swing low, (measured from $V^-$) | $R_L$ = 2 kΩ to $V^+$/2 | | | 78 | 120 | mV |
| | | | at the temperature extremes | | | 140 | |
| | | $R_L$ = 10 kΩ to $V^+$/2 | | | 38 | 70 | mV |
| | | | at the temperature extremes | | | 80 | |
| $I_O$ | Output short-circuit current(6) (7) | Sourcing $V_O$ = $V^+$/2<br>$V_{IN}$ = 100 mV | | 20 | 33 | | mA |
| | | | at the temperature extremes | 15 | | | |
| | | Sinking $V_O$ = $V^+$/2<br>$V_{IN}$ = −100 mV | | 20 | 28 | | mA |
| | | | at the temperature extremes | 15 | | | |
| $I_S$ | Supply current | Per channel | | | 0.96 | 1.5 | mA |
| | | | at the temperature extremes | | | 2 | |
| SR | Slew rate (8) | $A_V$ = 1, $V_O$ = 4 $V_{PP}$<br>10% to 90% | | | 2.5 | | V/µs |
| GBW | Gain bandwidth product | | | | 4.5 | | MHz |
| $\Phi_m$ | Phase margin | | | | 67 | | Deg |
| $e_n$ | Input-referred voltage noise | f = 1 kHz | | | 20 | | nV/√Hz |
| $R_{OUT}$ | Open-loop output impedance | f = 3 MHz | | | 70 | | Ω |
| THD+N | Total harmonic distortion + noise | f = 1 kHz , $A_V$ = 1<br>$R_L$ = 10 kΩ | | | 0.003% | | |
| $C_{IN}$ | Input capacitance | | | | 6 | | pF |

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D$ = ($T_{J(MAX)}$ - $T_A$) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.

## 6.7 Electrical Characteristics – ±5-V

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = 5 V, $V^-$ = –5 V, $V_{CM}$ = 0 V, and $R_L$ > 10 MΩ to $V_{CM}$.(1)

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

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## Electrical Characteristics – ±5-V (continued)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = 5 V, $V^-$ = –5 V, $V_{CM}$ = 0 V, and $R_L$ > 10 MΩ to $V_{CM}$.(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | | | –500 | ±50 | 500 | µV |
| | | at the temperature extremes | | –800 | | 800 | |
| $TCV_{OS}$ | Input offset voltage drift (4) | | | | 0.25 | | µV/°C |
| | | at the temperature extremes | | –5 | | 5 | |
| $I_B$ | Input bias current (4) (5) | | | | 0.3 | 10 | pA |
| | | at the temperature extremes | | | | 300 | |
| $I_{OS}$ | Input offset current | | | | 40 | | fA |
| CMRR | Common-mode rejection ratio LMV841-Q1 | –5 V ≤ $V_{CM}$ ≤ 5 V | | 86 | 112 | | dB |
| | | | at the temperature extremes | 80 | | | |
| | Common-mode rejection ratio LMV842-Q1 and LMV844-Q1 | –5 V ≤ $V_{CM}$ ≤ 5 V | | 86 | 106 | | dB |
| | | | at the temperature extremes | 80 | | | |
| PSRR | Power supply rejection ratio | 2.7 V ≤ $V^+$ ≤ 12 V, $V_O$ = 0 V | | 86 | 108 | | dB |
| | | | at the temperature extremes | 82 | | | |
| CMVR | Input common-mode voltage range | CMRR ≥ 50 dB | | –5.2 | | 5.2 | V |
| $A_{VOL}$ | Large signal voltage gain | $R_L$ = 2 kΩ<br>$V_O$ = −4.7 V to 4.7 V | | 100 | 126 | | dB |
| | | | at the temperature extremes | 96 | | | |
| | | $R_L$ = 10 kΩ<br>$V_O$ = −4.8 V to 4.8 V | | 100 | 136 | | dB |
| | | | at the temperature extremes | 96 | | | |
| $V_O$ | Output swing high, (measured from $V^+$) | $R_L$ = 2 kΩ to 0 V | | | 95 | 130 | mV |
| | | | at the temperature extremes | | | 155 | |
| | | $R_L$ = 10 kΩ to 0 V | | | 44 | 75 | mV |
| | | | at the temperature extremes | | | 95 | |
| | Output swing low, (measured from $V^-$) | $R_L$ = 2 kΩ to 0 V | | | 105 | 160 | mV |
| | | | at the temperature extremes | | | 200 | |
| | | $R_L$ = 10 kΩ to 0 V | | | 52 | 80 | mV |
| | | | at the temperature extremes | | | 100 | |
| $I_O$ | Output short-circuit current (6) (7) | Sourcing $V_O$ = 0 V<br>$V_{IN}$ = 100 mV | | 20 | 37 | | mA |
| | | | at the temperature extremes | 15 | | | |
| | | Sinking $V_O$ = 0 V<br>$V_{IN}$ = −100 mV | | 20 | 29 | | mA |
| | | | at the temperature extremes | 15 | | | |

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.


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## Electrical Characteristics – ±5-V (continued)

Unless otherwise specified, all limits are ensured for $T_A$ = 25°C, $V^+$ = 5 V, $V^-$ = –5 V, $V_{CM}$ = 0 V, and $R_L$ > 10 MΩ to $V_{CM}$.(1)

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| $I_S$ | Supply current | Per channel | | | 1.03 | 1.7 | mA |
| | | | at the temperature extremes | | | 2 | |
| SR | Slew rate (8) | $A_V$ = 1, $V_O$ = 9 $V_{PP}$<br>10% to 90% | | | 2.5 | | V/µs |
| GBW | Gain bandwidth product | | | | 4.5 | | MHz |
| $\Phi_m$ | Phase margin | | | | 67 | | Deg |
| $e_n$ | Input-referred voltage noise | f = 1 kHz | | | 20 | | nV/√Hz |
| $R_{OUT}$ | Open-loop output impedance | f = 3 MHz | | | 70 | | Ω |
| THD+N | Total harmonic distortion + noise | f = 1 kHz , $A_V$ = 1<br>$R_L$ = 10kΩ | | | 0.006% | | |
| $C_{IN}$ | Input capacitance | | | | 3 | | pF |

(8) Number specified is the slower of positive and negative slew rates.

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## 6.8 Typical Characteristics

At $T_A$ = 25°C, $R_L$ = 10 kΩ, $V_S$ = 5 V. Unless otherwise specified.

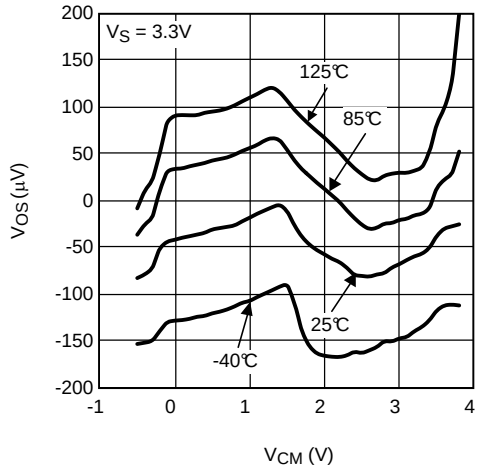


**Figure 1. $V_{OS}$ vs $V_{CM}$ Over Temperature at 3.3 V**

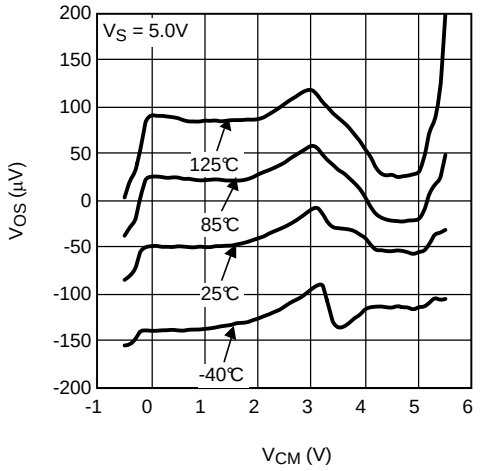


**Figure 2. $V_{OS}$ vs $V_{CM}$ Over Temperature at 5 V**

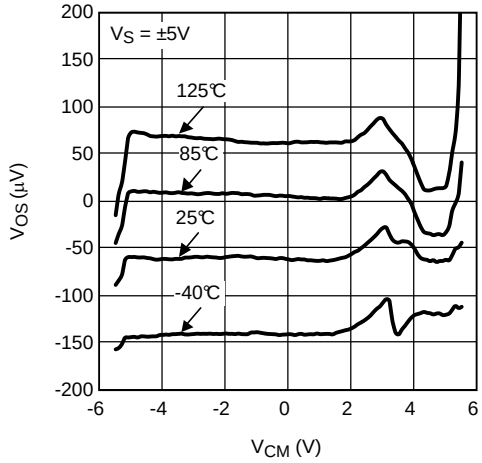


**Figure 3. $V_{OS}$ vs $V_{CM}$ Over Temperature at ±5 V**

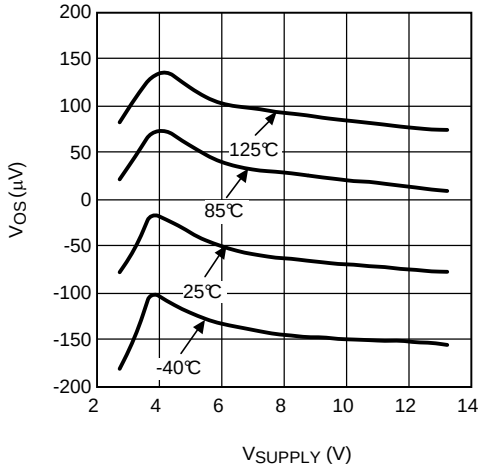


**Figure 4. $V_{OS}$ vs Supply Voltage**

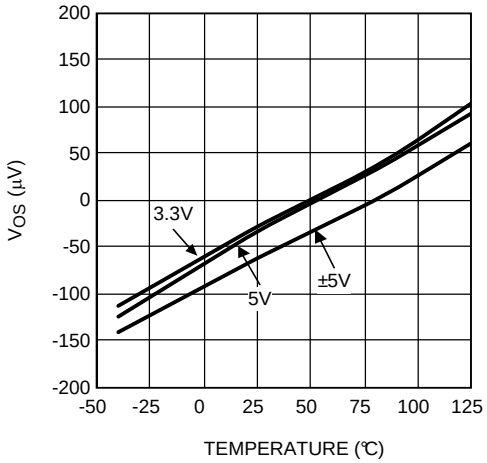


**Figure 5. $V_{OS}$ vs Temperature**

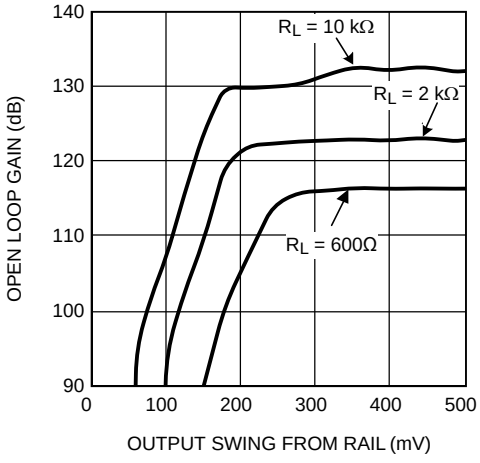


**Figure 6. DC Gain vs $V_{OUT}$**


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## Typical Characteristics (continued)

At $T_A$ = 25°C, $R_L$ = 10 kΩ, $V_S$ = 5 V. Unless otherwise specified.

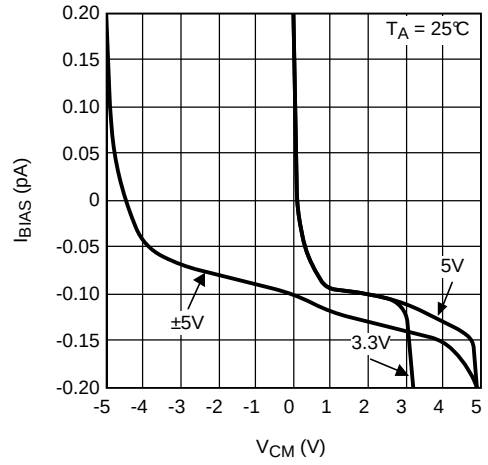


**Figure 7. Input Bias Current vs $V_{CM}$**

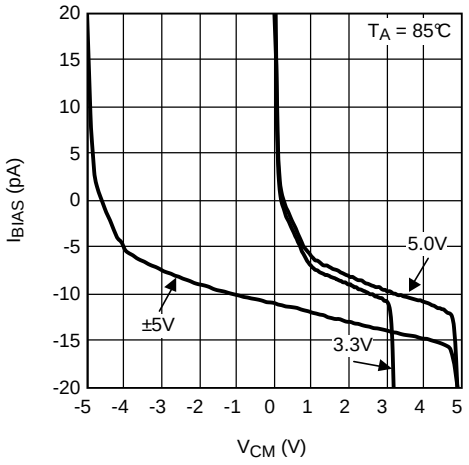


**Figure 8. Input Bias Current vs $V_{CM}$**

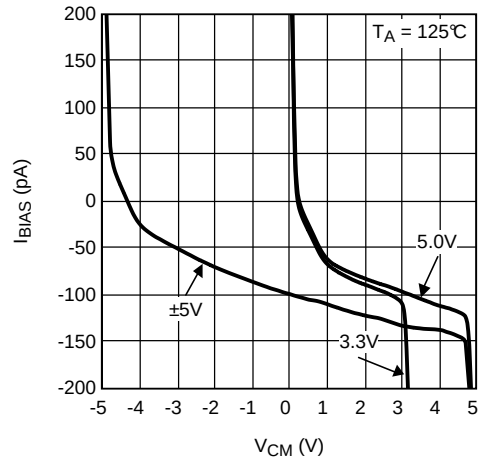


**Figure 9. Input Bias Current vs $V_{CM}$**

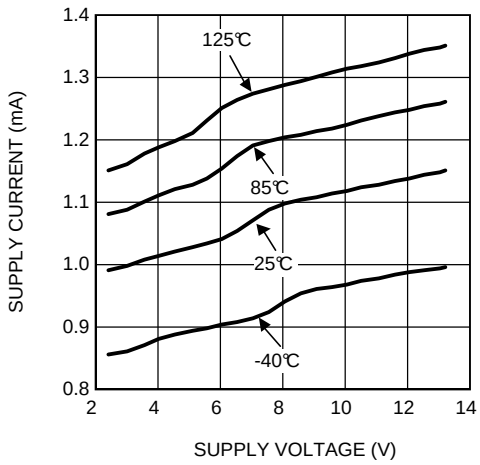


**Figure 10. Supply Current Per Channel vs Supply Voltage**

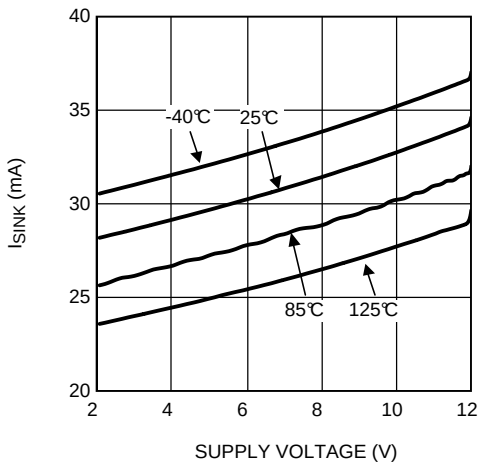


**Figure 11. Sinking Current vs Supply Voltage**

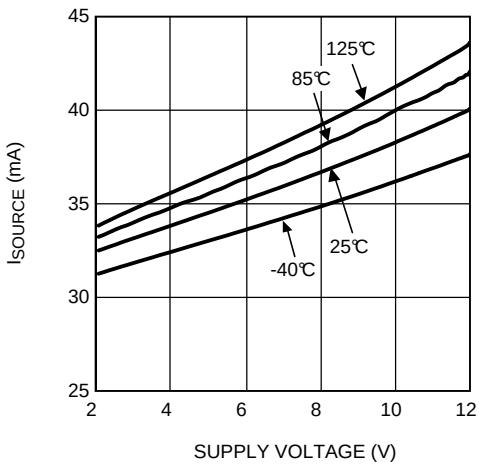


**Figure 12. Sourcing Current vs Supply Voltage**

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## Typical Characteristics (continued)

At $T_A$ = 25°C, $R_L$ = 10 kΩ, $V_S$ = 5 V. Unless otherwise specified.

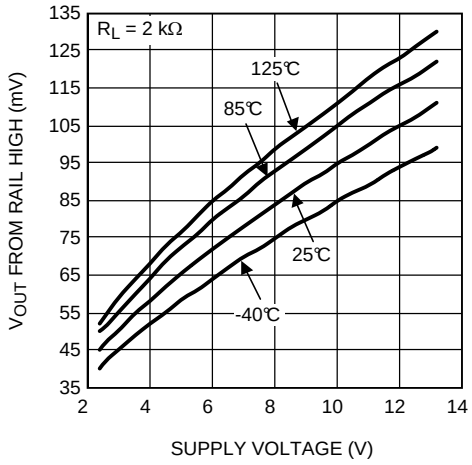


**Figure 13. Output Swing High vs Supply Voltage $R_L$ = 2 kΩ**

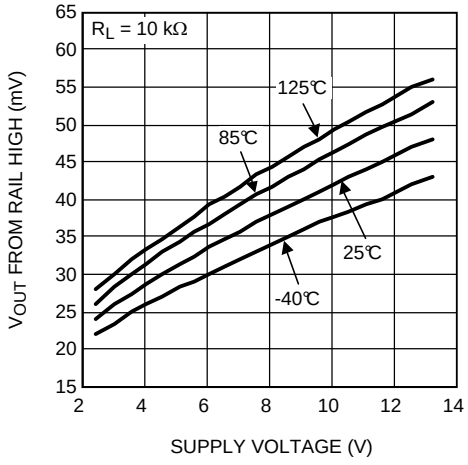


**Figure 14. Output Swing High vs Supply Voltage $R_L$ = 10 kΩ**

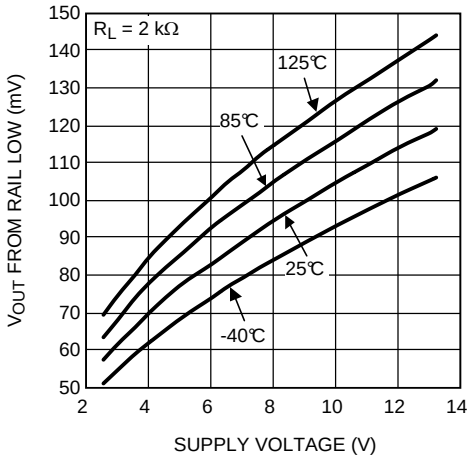


**Figure 15. Output Swing Low vs Supply Voltage $R_L$ = 2 kΩ**

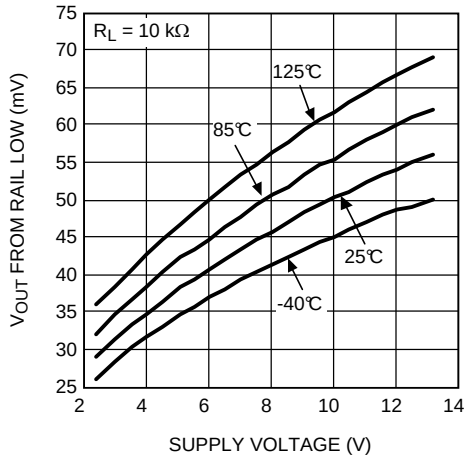


**Figure 16. Output Swing Low vs Supply Voltage $R_L$ = 10 kΩ**

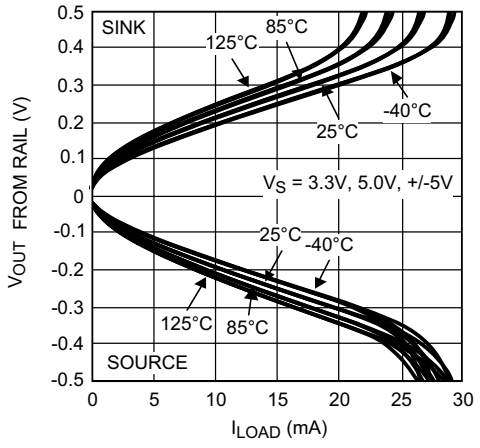


**Figure 17. Output Voltage Swing vs Load Current**

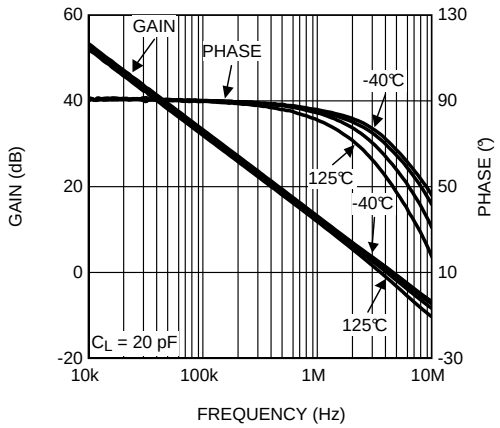


**Figure 18. Open-Loop Frequency Response Over Temperature**


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## Typical Characteristics (continued)

At $T_A$ = 25°C, $R_L$ = 10 kΩ, $V_S$ = 5 V. Unless otherwise specified.

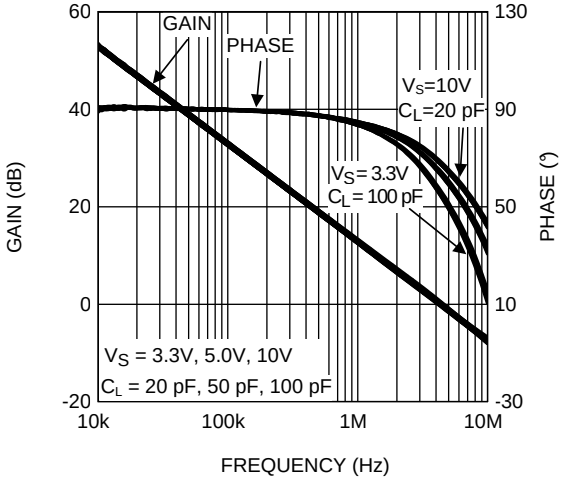


**Figure 19. Open-Loop Frequency Response Over Load Conditions**

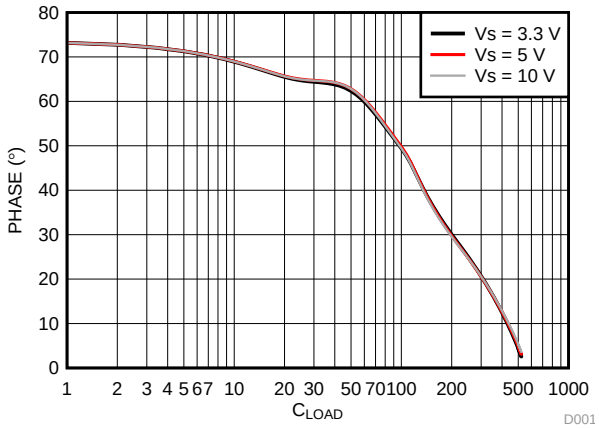


**Figure 20. Phase Margin vs $C_L$**

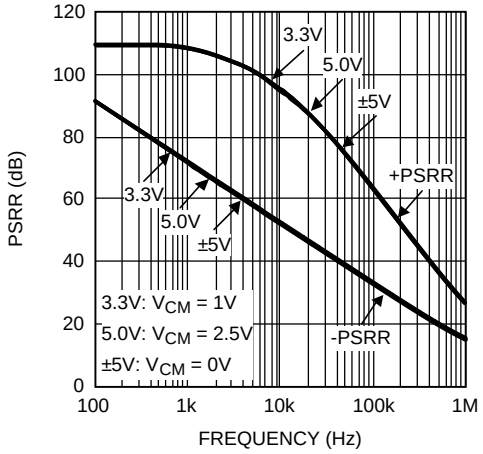


**Figure 21. PSRR vs Frequency**

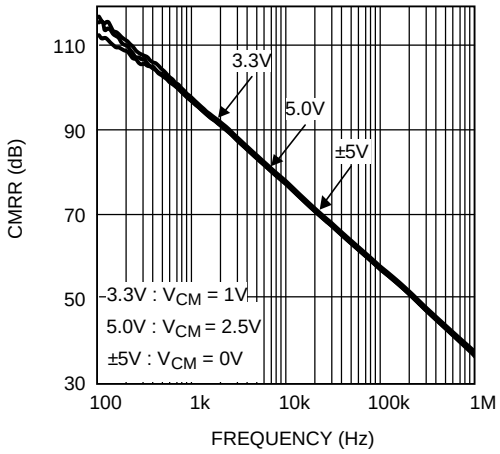


**Figure 22. CMRR vs Frequency**

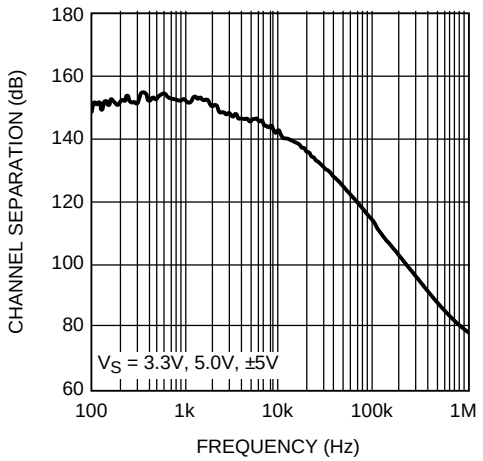


**Figure 23. Channel Separation vs Frequency**

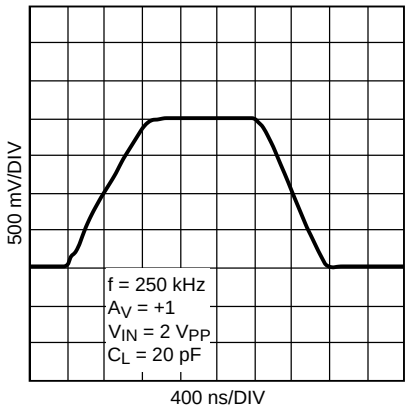


**Figure 24. Large Signal Step Response With Gain = 1**

## Typical Characteristics (continued)

At $T_A$ = 25°C, $R_L$ = 10 kΩ, $V_S$ = 5 V. Unless otherwise specified.

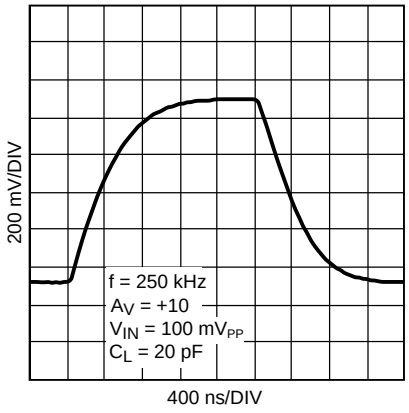


**Figure 25. Large Signal Step Response With Gain = 10**

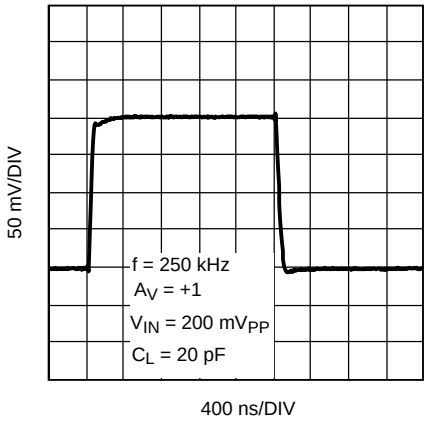


**Figure 26. Small Signal Step Response With Gain = 1**

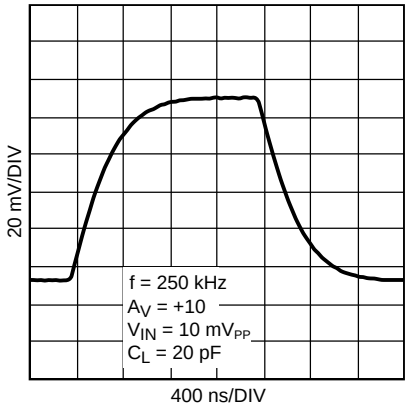


**Figure 27. Small Signal Step Response With Gain = 10**

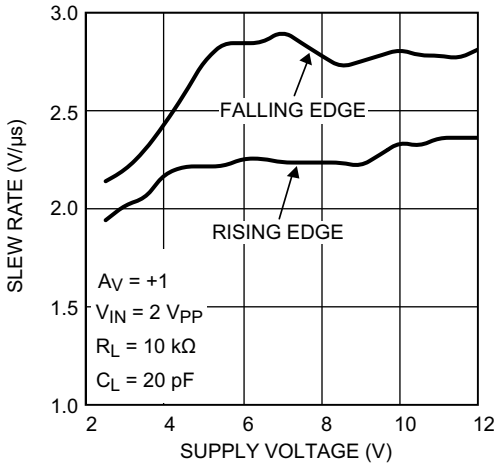


**Figure 28. Slew Rate vs Supply Voltage**

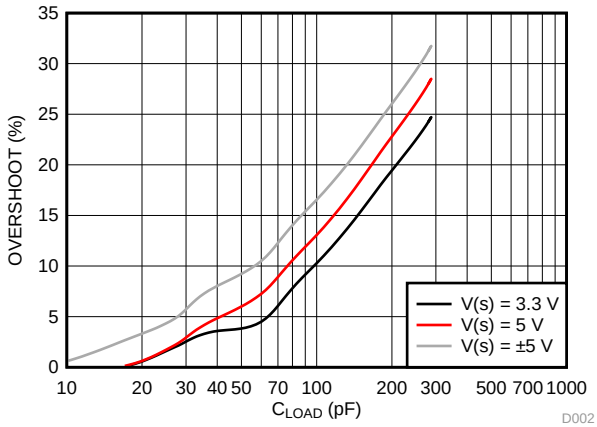


**Figure 29. Overshoot vs $C_L$**

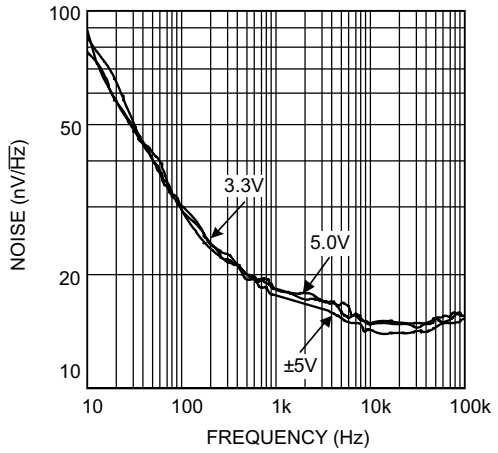


**Figure 30. Input Voltage Noise vs Frequency**


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## Typical Characteristics (continued)

At $T_A$ = 25°C, $R_L$ = 10 kΩ, $V_S$ = 5 V. Unless otherwise specified.

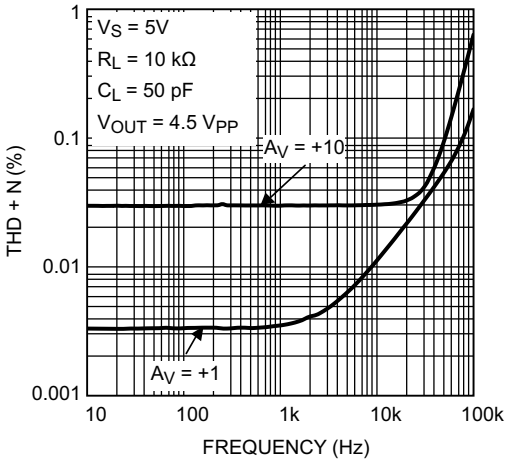


**Figure 31. THD+N vs Frequency**

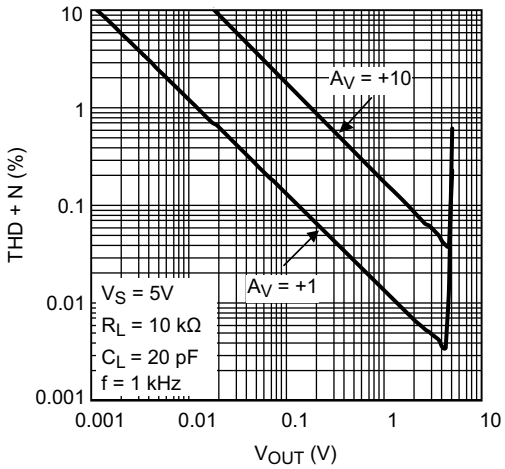


**Figure 32. THD+N vs $V_{OUT}$**

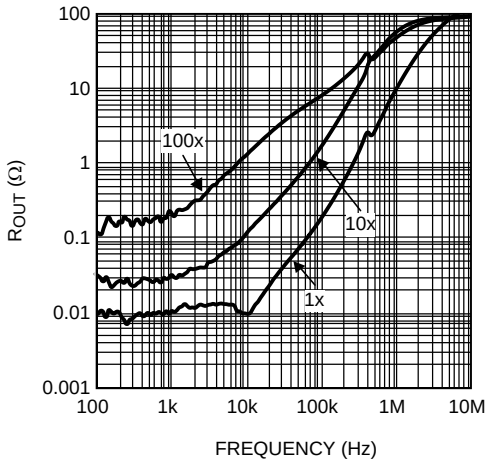


**Figure 33. Closed-Loop Output Impedance vs Frequency**

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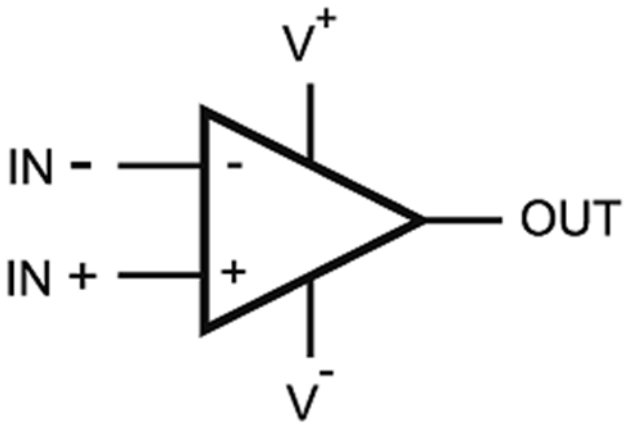
# 7 Detailed Description

## 7.1 Overview

The LMV84x-Q1 devices are operational amplifiers with near-precision specifications: low noise, low temperature drift, low offset, and rail-to-rail input and output. Possible application areas include instrumentation, medical, test equipment, audio, and automotive applications.

Its low supply current of 1 mA per amplifier, temperature range of −40°C to +125°C, 12-V supply with CMOS input, and the small SC70 package for the LMV841-Q1 make the LMV84x-Q1 a unique op amp family and a perfect choice for portable electronics.

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

### 7.3.1 Input Protection

The LMV84x-Q1 devices have a set of anti-parallel diodes $D_1$ and $D_2$ between the input pins, as shown in Figure 34. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins.

A differential signal larger than one diode voltage drop can damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA.

**NOTE**

When the op amp is slewing, a differential input voltage exists that forward-biases the protection diodes. This may result in current being drawn from the signal source. While this current is already limited by the internal resistors $R_1$ and $R_2$ (both 130 Ω), a resistor of 1 kΩ can be placed in the feedback path, or a 500-Ω resistor can be placed in series with the input signal for further limitation.


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## Feature Description (continued)

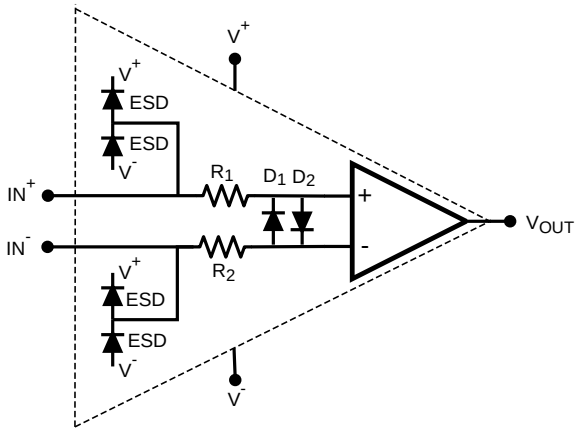


**Figure 34. Protection Diodes Between the Input Pins**

### 7.3.2 Input Stage

The input stage of this amplifier consists of both a PMOS and an NMOS input pair to achieve a rail-to-rail input range. For input voltages close to the negative rail, only the PMOS pair is active. Close to the positive rail, only the NMOS pair is active. In a transition region that extends from approximately 2 V below $V^+$ to 1 V below $V^+$, both pairs are active, and one pair gradually takes over from the other. In this transition region, the input-referred offset voltage changes from the offset voltage associated with the PMOS pair to that of the NMOS pair. The input pairs are trimmed independently to ensure an input offset voltage of less then 0.5 mV at room temperature over the complete rail-to-rail input range. This also significantly improves the CMRR of the amplifier in the transition region.

**NOTE**

The CMRR and PSRR limits in the tables are large-signal numbers that express the maximum variation of the input offset of the amplifier over the full common-mode voltage and supply voltage range, respectively. When the common-mode input voltage of the amplifier is within the transition region, the small signal CMRR and PSRR may be slightly lower than the large signal limits.

## 7.4 Device Functional Modes

### 7.4.1 Driving Capacitive Load

The LMV84x-Q1 can be connected as noninverting unity gain amplifiers. This configuration is the most sensitive to capacitive loading. The combination of a capacitive load placed on the output of an amplifier along with the output impedance of the amplifier creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is under-damped, which causes peaking in the transfer. When there is too much peaking, the op amp might start oscillating.

The LMV84x-Q1 can directly drive capacitive loads up to 100 pF without any stability issues. To drive heavier capacitive loads, an isolation resistor ($R_{ISO}$) must be used, as shown in Figure 35. By using this isolation resistor, the capacitive load is isolated from the output of the amplifier, and hence, the pole caused by $C_L$ is no longer in the feedback loop. The larger the value of $R_{ISO}$, the more stable the output voltage is. If values of $R_{ISO}$ are sufficiently large, the feedback loop is stable, independent of the value of $C_L$. However, larger values of $R_{ISO}$ result in reduced output swing and reduced output current drive.

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## Device Functional Modes (continued)

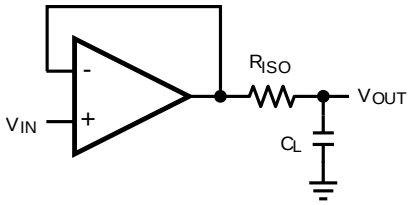


**Figure 35. Isolating Capacitive Load**

### 7.4.2 Noise Performance

The LMV84x-Q1 devices have good noise specifications and are frequently used in low-noise applications. Therefore it is important to determine the noise of the total circuit. Besides the input-referred noise of the op amp, the feedback resistors may have an important contribution to the total noise.

For applications with a voltage input configuration, in general it is beneficial general, beneficial to keep the resistor values low. In these configurations high resistor values mean high noise levels. However, using low resistor values will increase the power consumption of the application. This is not always acceptable for portable applications, so there is a trade-off between noise level and power consumption.

Besides the noise contribution of the signal source, three types of noise need to be taken into account for calculating the noise performance of an op amp circuit:

- Input-referred voltage noise of the op amp
- Input-referred current noise of the op amp
- Noise sources of the resistors in the feedback network, configuring the op amp

To calculate the noise voltage at the output of the op amp, the first step is to determine a total equivalent noise source. This requires the transformation of all noise sources to the same reference node. A convenient choice for this node is the input of the op amp circuit. The next step is to add all the noise sources. The final step is to multiply the total equivalent input voltage noise with the gain of the op amp configuration.

If the input-referred voltage noise of the op amp is already placed at the input, the user can use the input-referred voltage noise without further transferring. The input-referred current noise needs to be converted to an input-referred voltage noise. The current noise is negligibly small, as long as the equivalent resistance is not unrealistically large, so the user can leave the current noise out for these examples. That leaves the user with the noise sources of the resistors, being the thermal noise voltage. The influence of the resistors on the total noise can be seen in the following examples, one with high resistor values and one with low resistor values. Both examples describe an op amp configuration with a gain of 101 which gives the circuit a bandwidth of 44.5 kHz. The op amp noise is the same for both cases, that is, an input-referred noise voltage of 20 nV/$\sqrt{\text{Hz}}$ and a negligibly small input-referred noise current.

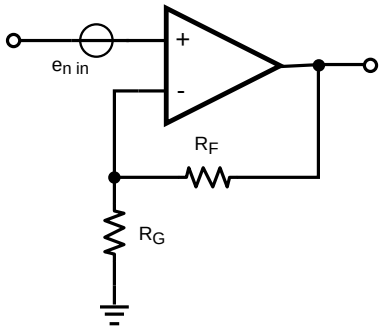


**Figure 36. Noise Circuit**


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## Device Functional Modes (continued)

To calculate the noise of the resistors in the feedback network, the equivalent input-referred noise resistance is needed. For the example in Figure 36, this equivalent resistance $R_{eq}$ can be calculated using Equation 1:

$$R_{eq} = \frac{R_F \times R_G}{R_F + R_G} \tag{1}$$

The voltage noise of the equivalent resistance can be calculated using Equation 2:

$$e_{nr} = \sqrt{4kTR_{eq}}$$

where

- $e_{nr}$ = thermal noise voltage of the equivalent resistor
- $R_{eq}$ ($V/\sqrt{Hz}$)
- k = Boltzmann constant (1.38 x $10^{-23}$ J/K)
- T = absolute temperature (K)
- $R_{eq}$ = resistance (Ω) (2)

The total equivalent input voltage noise is given by Equation 3:

$$e_{n\ in} = \sqrt{e_{nv}^{\ 2} + e_{nr}^{\ 2}}$$

where

- $e_{n\ in}$ = total input equivalent voltage noise of the circuit
- $e_{nv}$ = input voltage noise of the op amp (3)

The final step is multiplying the total input voltage noise by the noise gain using Equation 4, which is in this case the gain of the op amp configuration:

$$e_{n\ out} = e_{n\ in} \times A_{noise} \tag{4}$$

The equivalent resistance for the first example with a resistor $R_F$ of 10 MΩ and a resistor $R_G$ of 100 kΩ at 25°C (298 K) equals Equation 5:

$$R_{eq} = \frac{R_F \times R_G}{R_F + R_G} = \frac{10\ M\Omega \times 100\ k\Omega}{10\ M\Omega + 100\ k\Omega} = 99\ k\Omega \tag{5}$$

Now the noise of the resistors can be calculated using Equation 6, yielding:

$$\begin{aligned} e_{nr} &= \sqrt{4kTR_{eq}} \\ &= \sqrt{4 \times 1.38 \times 10^{-23}\ J/K \times 298K \times 99\ k\Omega} \\ &= 40\ nV/\sqrt{Hz} \end{aligned} \tag{6}$$

The total noise at the input of the op amp is calculated in Equation 7:

$$\begin{aligned} e_{n\ in} &= \sqrt{e_{nv}^{\ 2} + e_{nr}^{\ 2}} \\ &= \sqrt{(20\ nV/\sqrt{Hz})^2 + (40\ nV/\sqrt{Hz})^2} = 45\ nV/\sqrt{Hz} \end{aligned} \tag{7}$$

For the first example, this input noise, multiplied with the noise gain, in Equation 8 gives a total output noise of:

$$\begin{aligned} e_{n\ out} &= e_{n\ in} \times A_{noise} \\ &= 45\ nV/\sqrt{Hz} \times 101 = 4.5\ \mu V/\sqrt{Hz} \end{aligned} \tag{8}$$

In the second example, with a resistor $R_F$ of 10 kΩ and a resistor $R_G$ of 100 Ω at 25°C (298 K), the equivalent resistance equals Equation 9:

$$R_{eq} = \frac{R_F \times R_G}{R_F + R_G} = \frac{10\ k\Omega \times 100\ \Omega}{10\ k\Omega + 100\ \Omega} = 99\ \Omega \tag{9}$$

The resistor noise for the second example is calculated in Equation 10:

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## Device Functional Modes (continued)

$$e_{nr} = \sqrt{4kTR_{eq}}$$
$$= \sqrt{4 \times 1.38 \times 10^{-23}\ J/K \times 298\ K \times 99\ \Omega}$$
$$= 1\ nV/\sqrt{Hz} \quad (10)$$

The total noise at the input of the op amp is calculated in Equation 10:

$$e_{n\ in} = \sqrt{{e_{nv}}^2 + {e_{nr}}^2}$$
$$= \sqrt{(20\ nV/\sqrt{Hz})^2 + (1\ nV/\sqrt{Hz})^2}$$
$$= 20\ nV/\sqrt{Hz} \quad (11)$$

For the second example the input noise, multiplied with the noise gain, in Equation 12 gives an output noise of:

$$e_{n\ out} = e_{n\ in} \times A_{noise}$$
$$= 20\ nV/\sqrt{Hz} \times 101 = 2\ \mu V/\sqrt{Hz} \quad (12)$$

In the first example the noise is dominated by the resistor noise due to the very high resistor values, in the second example the very low resistor values add only a negligible contribution to the noise and now the dominating factor is the op amp itself. When selecting the resistor values, it is important to choose values that do not add extra noise to the application. Choosing values above 100 kΩ may increase the noise too much. Low values keep the noise within acceptable levels; choosing very low values however, does not make the noise even lower, but can increase the current of the circuit.

## 7.5 Interfacing to High Impedance Sensor

With CMOS inputs, the LMV84x-Q1 are particularly suited to be used as high impedance sensor interfaces.

Many sensors have high source impedances that may range up to 10 MΩ. The input bias current of an amplifier loads the output of the sensor, and thus cause a voltage drop across the source resistance, as shown in Figure 37. When an op amp is selected with a relatively high input bias current, this error may be unacceptable.

The low input current of the LMV84x-Q1 significantly reduces such errors. The following examples show the difference between a standard op amp input and the CMOS input of the LMV84x-Q1.

The voltage at the input of the op amp can be calculated with Equation 13:

$$V_{IN+} = V_S - I_B \times R_S \quad (13)$$

For a standard op amp, the input bias Ib can be 10 nA. When the sensor generates a signal of 1 V ($V_S$) and the sensors impedance is 10 MΩ ($R_S$), the signal at the op amp input is calculated in Equation 14:

$$V_{IN} = 1\ V - 10\ nA \times 10\ M\Omega = 1\ V - 0.1\ V = 0.9\ V \quad (14)$$

For the CMOS input of the LMV84x-Q1, which has an input bias current of only 0.3 pA, this would give Equation 15:

$$V_{IN} = 1\ V - 0.3\ pA \times 10\ M\Omega = 1\ V - 3\ \mu V = 0.999997\ V \quad (15)$$

The conclusion is that a standard op amp, with its high input bias current input, is not a good choice for use in impedance sensor applications. The LMV84x-Q1 devices, in contrast, are much more suitable due to the low input bias current. The error is negligibly small; therefore, the LMV84x-Q1 are a must for use with high-impedance sensors.


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## Interfacing to High Impedance Sensor (continued)

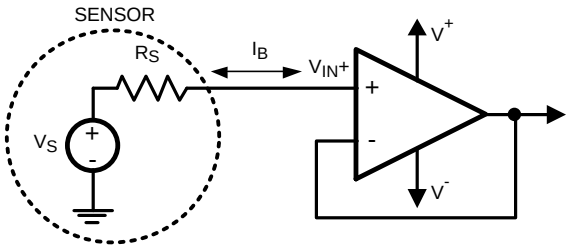


**Figure 37. High Impedance Sensor Interface**

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The rail-to-rail input and output of the LMV84x-Q1 and the wide supply voltage range make these amplifiers ideal to use in numerous applications. Three sample applications, namely the active filter circuit, high-side current sensing, and thermocouple sensor interface, are provided in the *Typical Applications* section.

## 8.2 Typical Applications

### 8.2.1 Active Filter Circuit

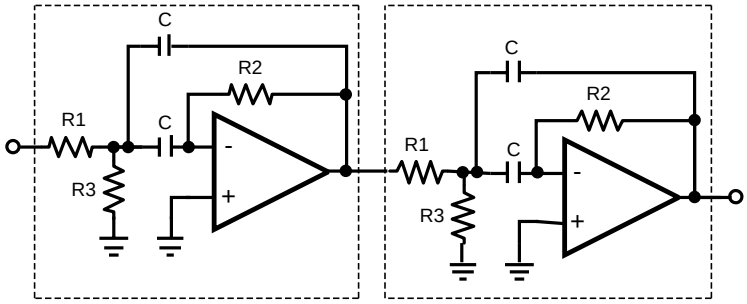


**Figure 38. Active Band-Pass Filter Implementation**

#### *8.2.1.1 Design Requirements*

In this example it is required to design a bandpass filter with band-pass frequency of 10 kHz, and a center frequence of approximately 10% from the total frequence of the filter. This is achieved by cascading two band-pass filters, A and B, with slightly different center frequencies.

#### *8.2.1.2 Detailed Design Procedure*

The center frequency of the separate band-pass filters A, and B can be calculated by Equation 16:

$$f_{mid} = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}} \tag{16}$$

where

- C = 33 nF
- R1 = 2 KΩ
- R2 = 6.2 KΩ
- and R3 = 45 Ω

This gives Equation 17 for filter A:

$$f_{mid} = \frac{1}{\pi \times 33\ nF}\sqrt{\frac{2\ k\Omega + 6.2\ k\Omega}{2\ k\Omega \times 6.2\ k\Omega \times 45\ k\Omega}} = 9.2\ kHz \tag{17}$$

and Equation 18 for filter B with C = 27nF:

$$f_{mid} = \frac{1}{\pi \times 27\ nF}\sqrt{\frac{2\ k\Omega + 6.2\ k\Omega}{2\ k\Omega \times 6.2\ k\Omega \times 45\ k\Omega}} = 11.2\ kHz \tag{18}$$

Bandwidth can be calculated by Equation 19:


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## Typical Applications (continued)

$$B = \frac{1}{\pi R_2 C} \tag{19}$$

For filter A, this gives Equation 20:

$$B = \frac{1}{\pi \times 6.2\ k\Omega \times 33\ nF} = 1.6\ kHz \tag{20}$$

and Equation 21 for filter B:

$$B = \frac{1}{\pi \times 6.2\ k\Omega \times 27\ nF} = 1.9\ kHz \tag{21}$$

#### 8.2.1.3 Application Curve

The responses of filter A and filter B are shown as the thin lines in Figure 39; the response of the combined filter is shown as the thick line. Shifting the center frequencies of the separate filters farther apart, results in a wider band; however, positioning the center frequencies too far apart results in a less flat gain within the band. For wider bands more band-pass filters can be cascaded.

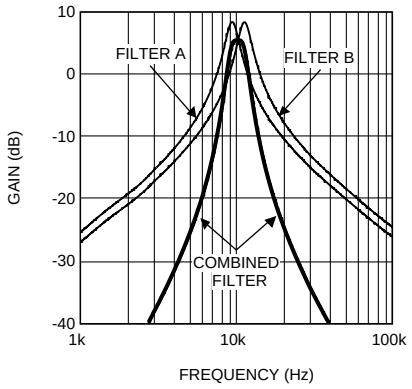


**Figure 39. Active Band-Pass Filter Curve**

**NOTE**

Use the WEBENCH internet tools at www.ti.com for your filter application.

### 8.2.2 High-Side, Current-Sensing Circuit

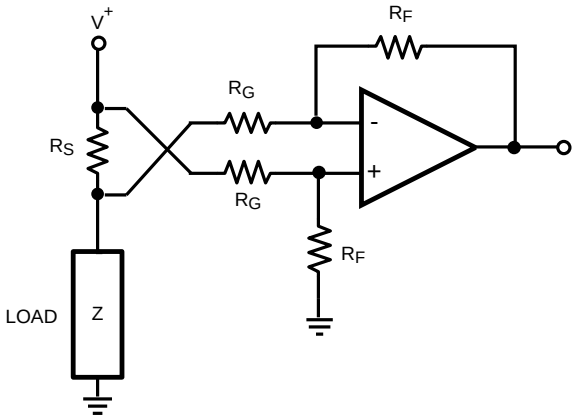


**Figure 40. High-Side, Current-Sensing Circuit**

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## Typical Applications (continued)

### 8.2.2.1 Design Requirements

In this example, it is desired to measure a current between 0 A and 2 A using a sense resistor of 100 mΩ, and convert it to an output voltage of 0 to 5 V. A current of 2 A flowing through the load and the sense resistor results in a voltage of 200 mV across the sense resistor. The op amp amplifies this 200 mV to fit the current range to the output voltage range.

### 8.2.2.2 Detailed Design Procedure

To measure current at a point in a circuit, a sense resistor is placed in series with the load, as shown in Figure 40. The current flowing through this sense resistor results in a voltage drop, that is amplified by the op amp. The rail-to-rail input and the low $V_{OS}$ features make the LMV84x-Q1 ideal op amps for high-side, current-sensing applications.

The input and the output relation of the circuit is given by Equation 22:

$$V_{OUT} = R_F/R_G \times V_{SENSE} \quad (22)$$

For a load current of 2 A and an output voltage of 5 V the gain would be $V_{OUT} / V_{SENSE} = 25$.

If the feedback resistor, $R_F$, is 100 kΩ, then the value for $R_G$ is 4 kΩ. The tolerance of the resistors has to be low to obtain a good common-mode rejection.

### 8.2.3 Thermocouple Sensor Signal Amplification

Figure 41 is a typical example for a thermocouple amplifier application using an LMV841-Q1, LMV842-Q1, or LMV844-Q1. A thermocouple senses a temperature and converts it into a voltage. This signal is then amplified by the LMV841-Q1, LMV842-Q1, or LMV844-Q1. An ADC can then convert the amplified signal to a digital signal. For further processing the digital signal can be processed by a microprocessor, and can be used to display or log the temperature, or the temperature data can be used in a fabrication process.

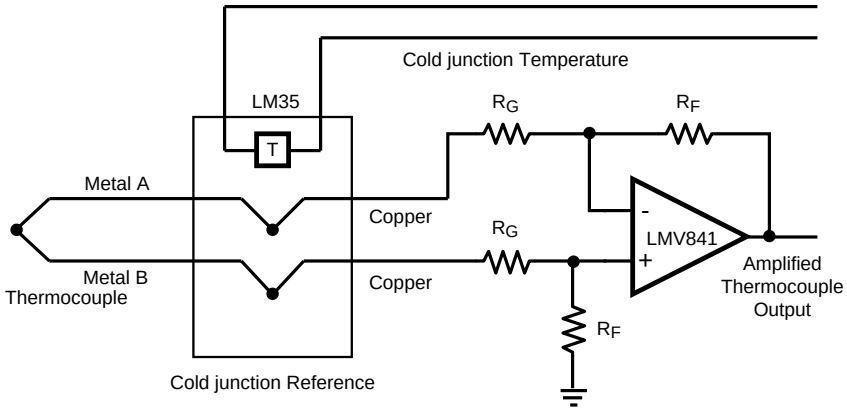


**Figure 41. Thermocouple Sensor Interface**

### 8.2.3.1 Design Requirements

In this example it is desired to measure temperature in the range of 0°C to 500°C with a resolution of 0.5°C using a K-type thermocouple sensor. The power supply for both the LMV84x-Q1 and the ADC is 3.3 V.

### 8.2.3.2 Detailed Design Procedure

A thermocouple is a junction of two different metals. These metals produce a small voltage that increases with temperature. A K-type thermocouple is a very common temperature sensor made of a junction between nickel-chromium and nickel-aluminum. There are several reasons for using the K-type thermocouple. These include temperature range, the linearity, the sensitivity, and the cost.


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## Typical Applications (continued)

A K-type thermocouple has a wide temperature range. The range of this thermocouple is from approximately −200°C to approximately 1200°C, as can be seen in Figure 42. This covers the generally used temperature ranges.

Over the main part of the range the behavior is linear. This is important for converting the analog signal to a digital signal. The K-type thermocouple has good sensitivity when compared to many other types; the sensitivity is 41 µV/°C. Lower sensitivity requires more gain and makes the application more sensitive to noise. In addition, a K-type thermocouple is not expensive, many other thermocouples consist of more expensive materials or are more difficult to produce.

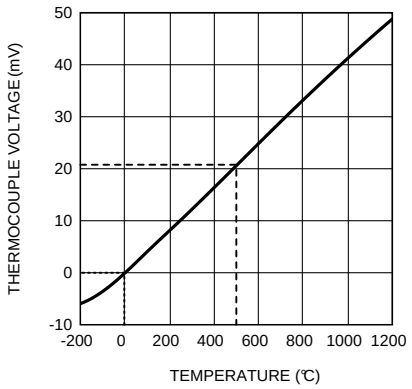


**Figure 42. K-Type Thermocouple Response**

The temperature range of 0°C to 500°C results in a voltage range from 0 mV to 20.6 mV produced by the thermocouple. This is shown in Figure 42.

To obtain the best accuracy the full ADC range of 0 to 3.3 V is used and the gain needed for this full range can be calculated Equation 23:

$$A_V = 3.3\ V / 0.0206\ V = 160 \quad (23)$$

If $R_G$ is 2 kΩ, then the value for $R_F$ can be calculated with this gain of 160. Because $A_V = R_F / R_G$, $R_F$ can be calculated in Equation 24:

$$R_F = A_V \times R_G = 160 \times 2\ k\Omega = 320\ k\Omega \quad (24)$$

To achieve a resolution of 0.5°C a step smaller than the minimum resolution is needed. This means that at least 1000 steps are necessary (500°C/0.5°C). A 10-bit ADC would be sufficient as this gives 1024 steps. A 10-bit ADC such as the two channel 10-bit ADC102S021 would be a good choice.

At the point where the thermocouple wires are connected to the circuit on the PCB unwanted parasitic thermocouple is formed, introducing error in the measurements of the actual thermocouple sensor.

Using an isothermal block as a reference will compensate for this additional thermocouple effect. An isothermal block is a good heat conductor. This means that the two thermocouple connections both have the same temperature. The temperature of the isothermal block can be measured, and thereby the temperature of the thermocouple connections. This is usually called the cold junction reference temperature. In the example, an LM35 is used to measure this temperature. This semiconductor temperature sensor can accurately measure temperatures from −55°C to 150°C.

The ADC in this example also coverts the signal from the LM35 to a digital signal, hence, the microprocessor can compensate for the amplified thermocouple signal of the unwanted thermocouple junction at the connector.

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# 9 Power Supply Recommendations

The LMV84x-Q1 is specified for operation from 2.7 V to 12 V (±1.35 V to ±6 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Absolute Maximum Ratings*.

**CAUTION**

Supply voltages larger than 13.2 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI suggests placing 10-nF capacitors as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between $V^+$ and $V^-$ supply leads. For dual supplies, place one capacitor between $V^+$ and ground, and one capacitor between $V^-$ and ground.

# 10 Layout

## 10.1 Layout Guidelines

- The V+ pin must be bypassed to ground with a low-ESR capacitor.
- The optimum placement is closest to the V+ and ground pins.
- Take care to minimize the loop area formed by the bypass capacitor connection between V+ and ground.
- The ground pin must be connected to the PCB ground plane at the pin of the device.
- The feedback components must be placed as close to the device as possible to minimize strays.

## 10.2 Layout Example

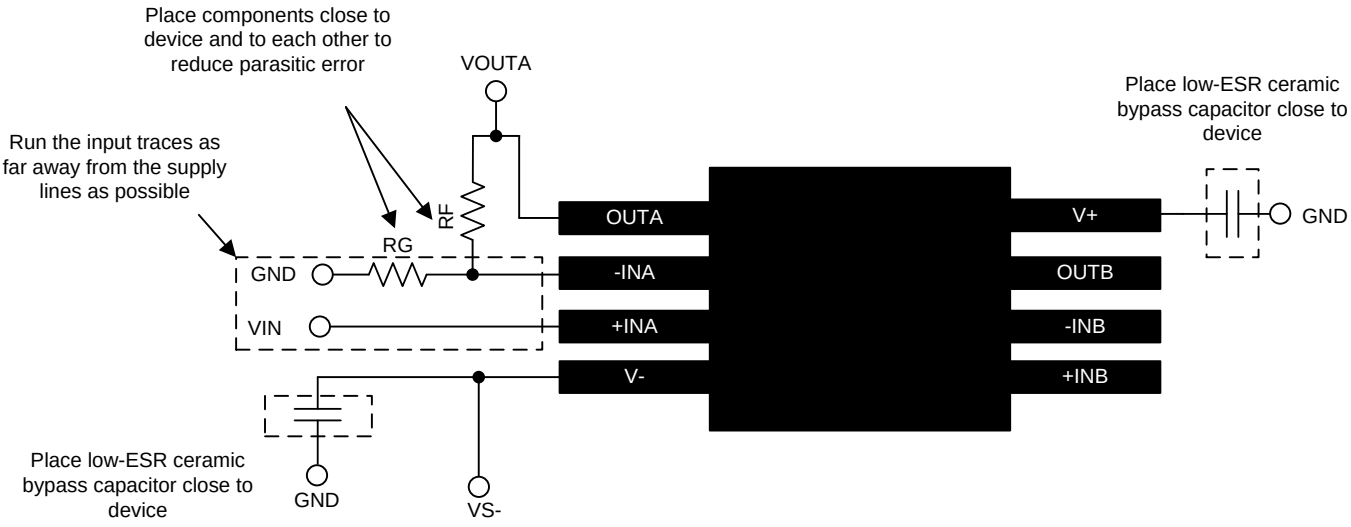


**Figure 43. Layout Example (Top View)**


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# 11 デバイスおよびドキュメントのサポート

## 11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

**表 1. 関連リンク**

| 製品 | プロダクト・フォルダ | ご注文はこちら | 技術資料 | ツールとソフトウェア | サポートとコミュニティ |
|---|---|---|---|---|---|
| LMV841-Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| LMV842-Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| LMV844-Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |

## 11.2 ドキュメントの更新通知を受け取る方法

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## 11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**設計サポート** ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMV841QMG/NOPB | Active | Production | SC70 (DCK) \| 5 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | ATA |
| LMV841QMG/NOPB.A | Active | Production | SC70 (DCK) \| 5 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | ATA |
| LMV841QMGX/NOPB | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | ATA |
| LMV841QMGX/NOPB.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | ATA |
| LMV842QMA/NOPB | Active | Production | SOIC (D) \| 8 | 95 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LMV84 2QMA |
| LMV842QMA/NOPB.A | Active | Production | SOIC (D) \| 8 | 95 \| TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LMV84 2QMA |
| LMV842QMAX/NOPB | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LMV84 2QMA |
| LMV842QMAX/NOPB.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LMV84 2QMA |
| LMV842QMM/NOPB | Active | Production | VSSOP (DGK) \| 8 | 1000 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | AA7A |
| LMV842QMM/NOPB.A | Active | Production | VSSOP (DGK) \| 8 | 1000 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AA7A |
| LMV842QMMX/NOPB | Active | Production | VSSOP (DGK) \| 8 | 3500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | AA7A |
| LMV842QMMX/NOPB.A | Active | Production | VSSOP (DGK) \| 8 | 3500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AA7A |
| LMV844QMA/NOPB | Active | Production | SOIC (D) \| 14 | 55 \| TUBE | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LMV844 QMA |
| LMV844QMA/NOPB.A | Active | Production | SOIC (D) \| 14 | 55 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV844 QMA |
| LMV844QMAX/NOPB | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LMV844 QMA |
| LMV844QMAX/NOPB.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV844 QMA |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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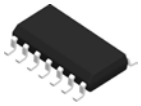
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LMV841-Q1, LMV842-Q1, LMV844-Q1 :**

- Catalog : LMV841, LMV842, LMV844

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

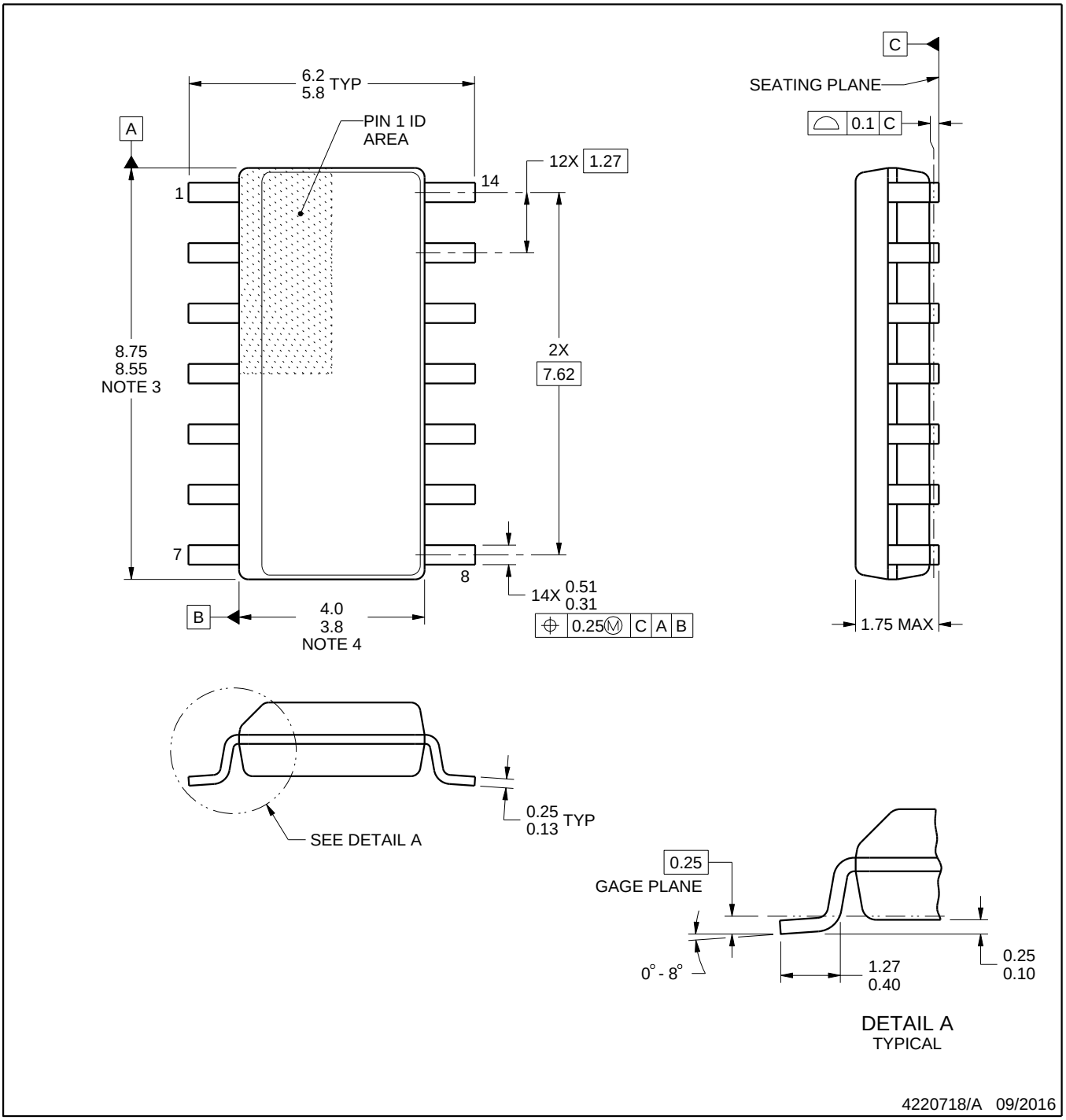


# PACKAGE OUTLINE

## D0014A

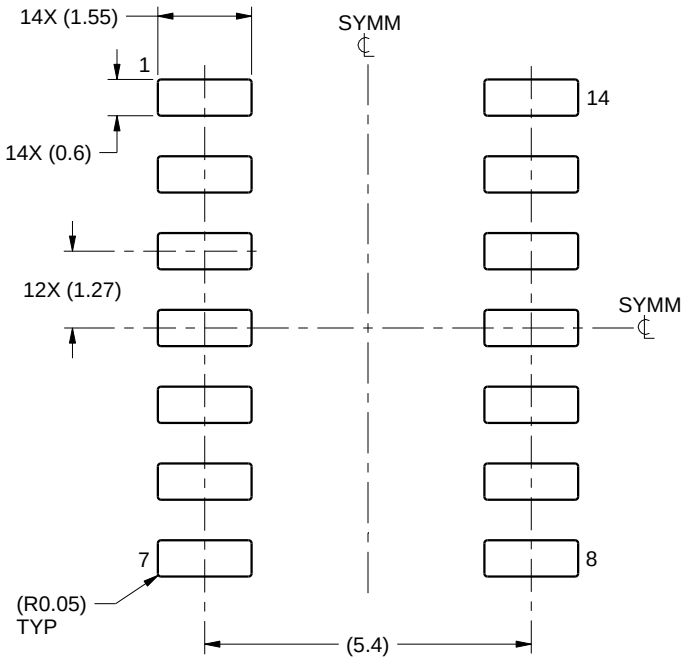
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

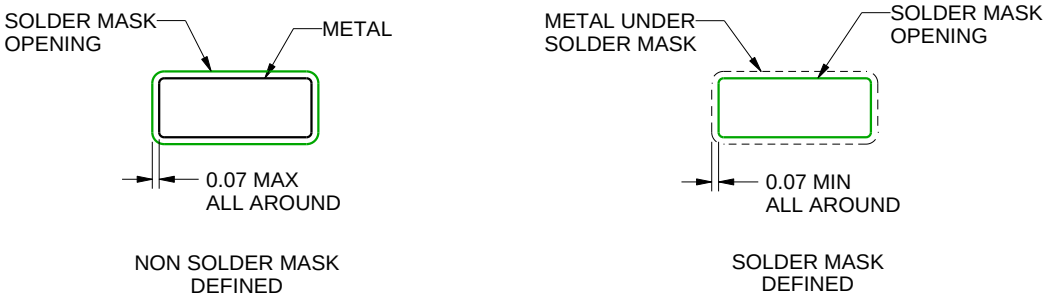



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

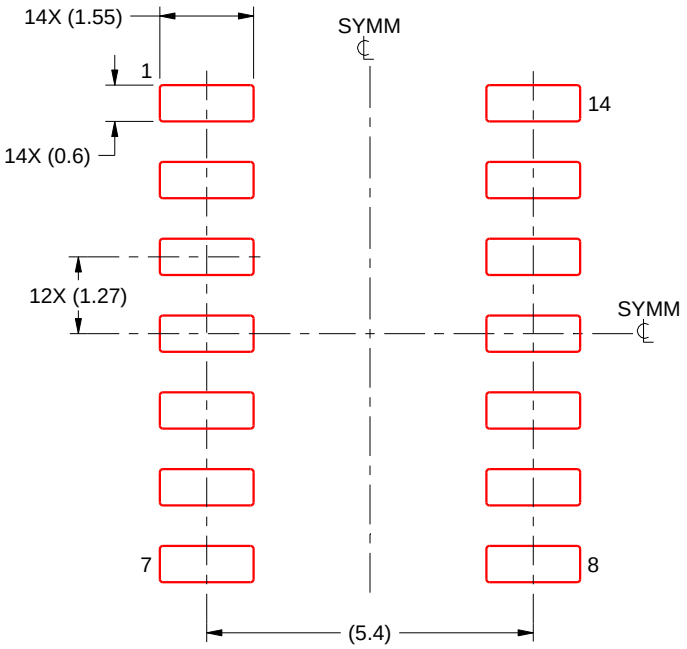
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

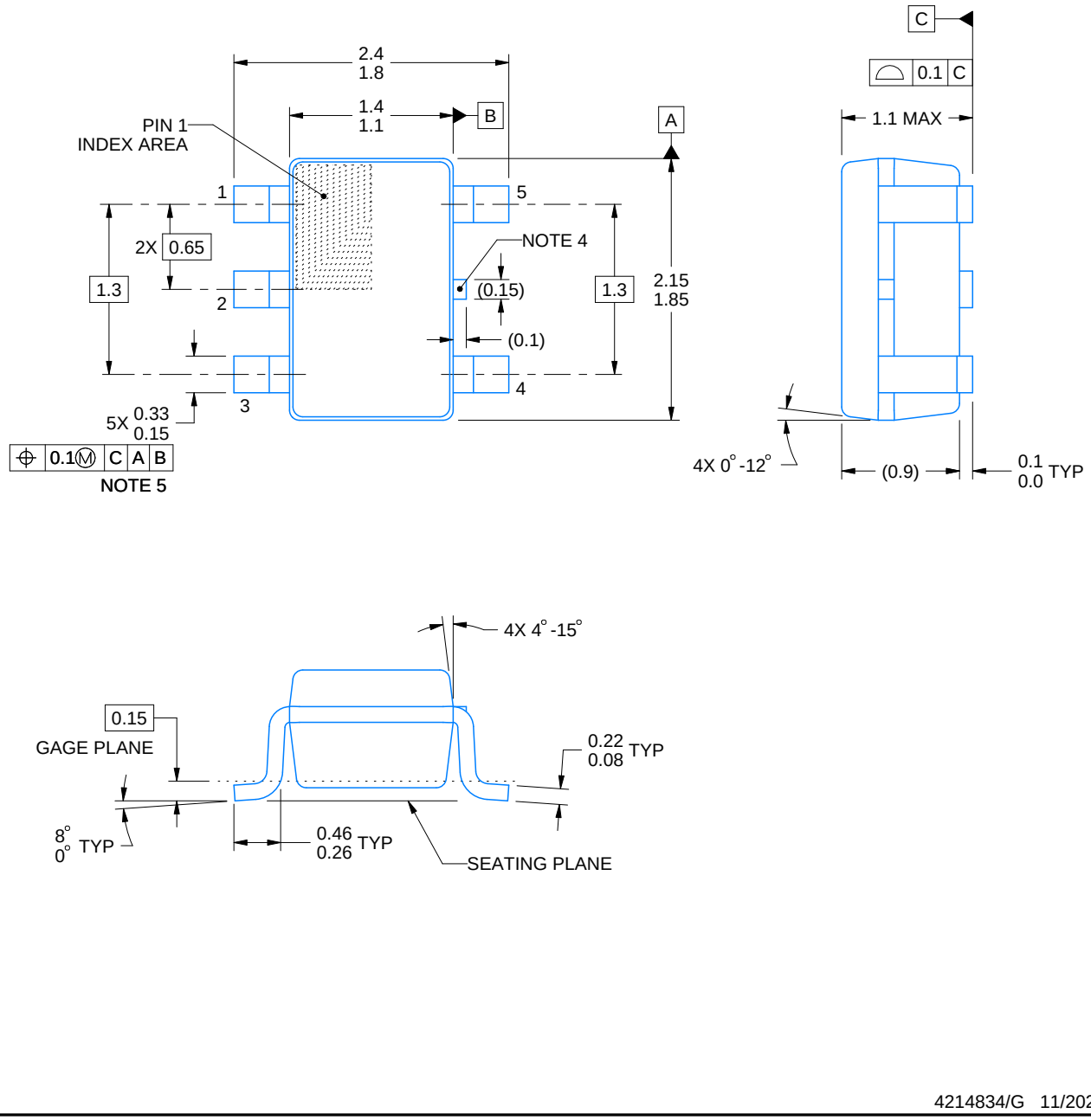
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

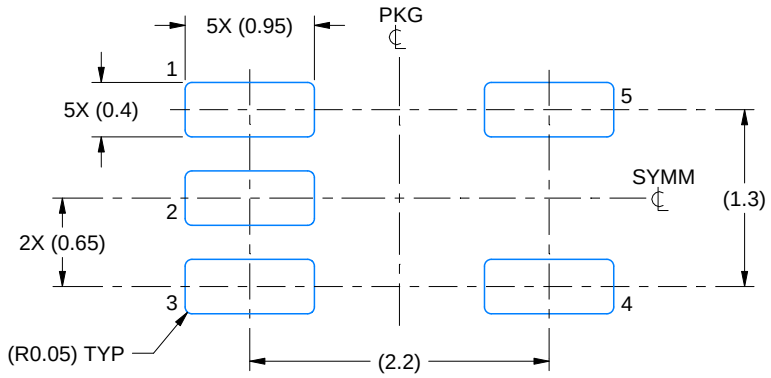
SMALL OUTLINE TRANSISTOR



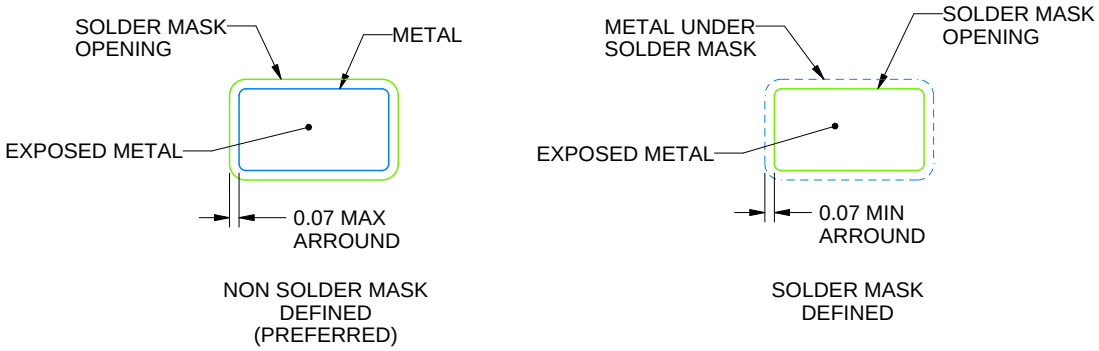

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

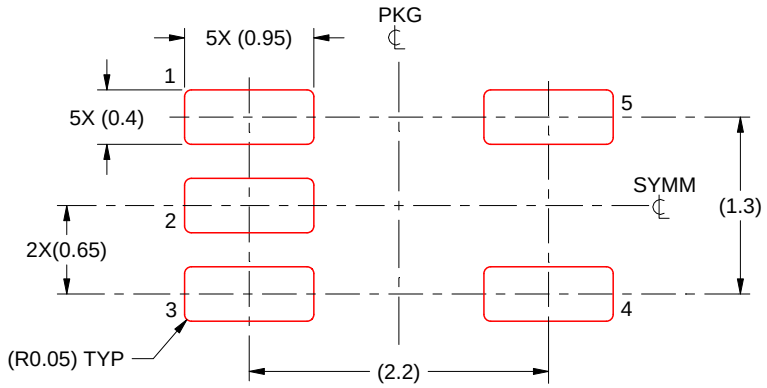



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

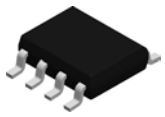



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

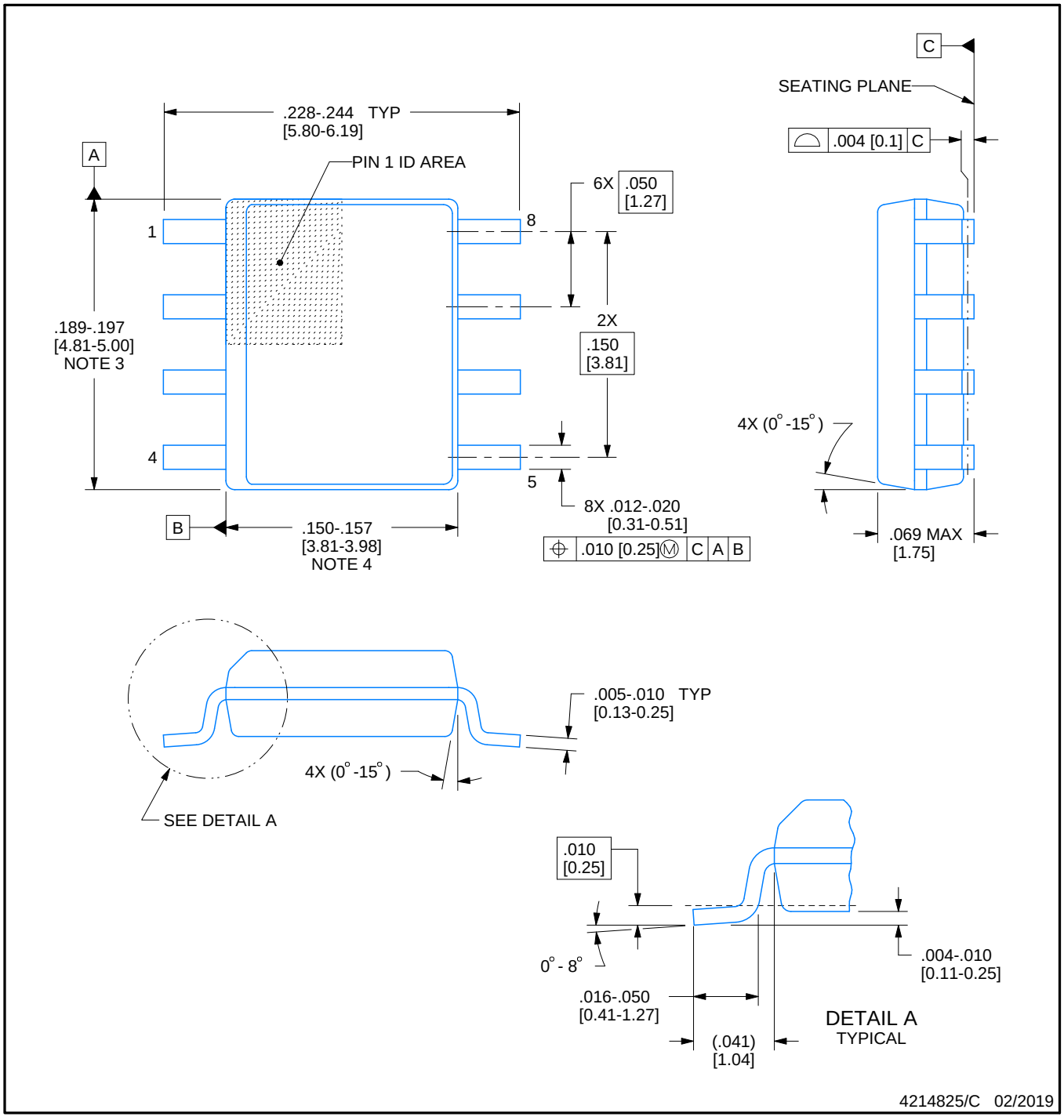


# PACKAGE OUTLINE

## D0008A

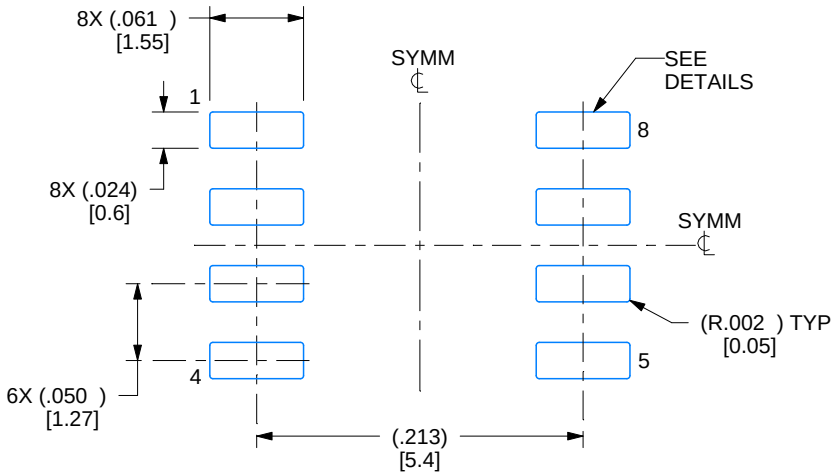
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

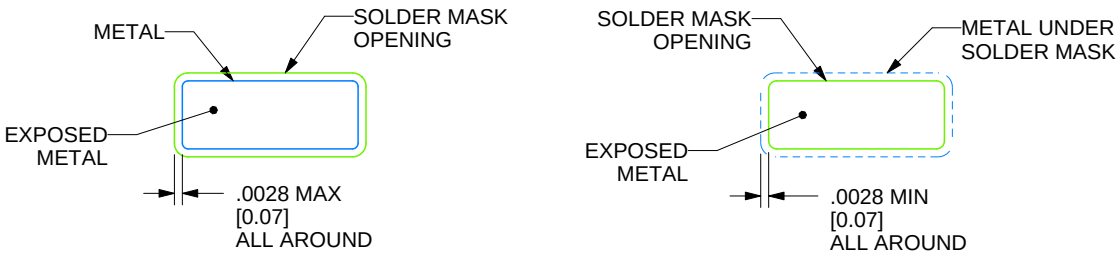



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

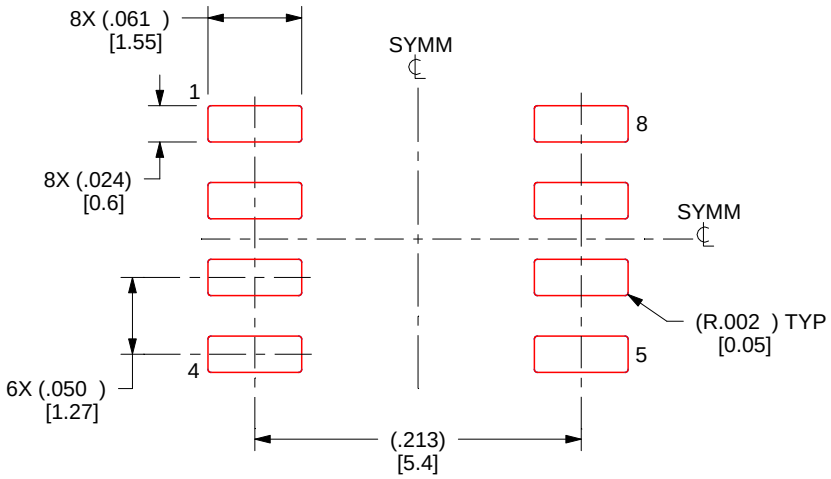
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

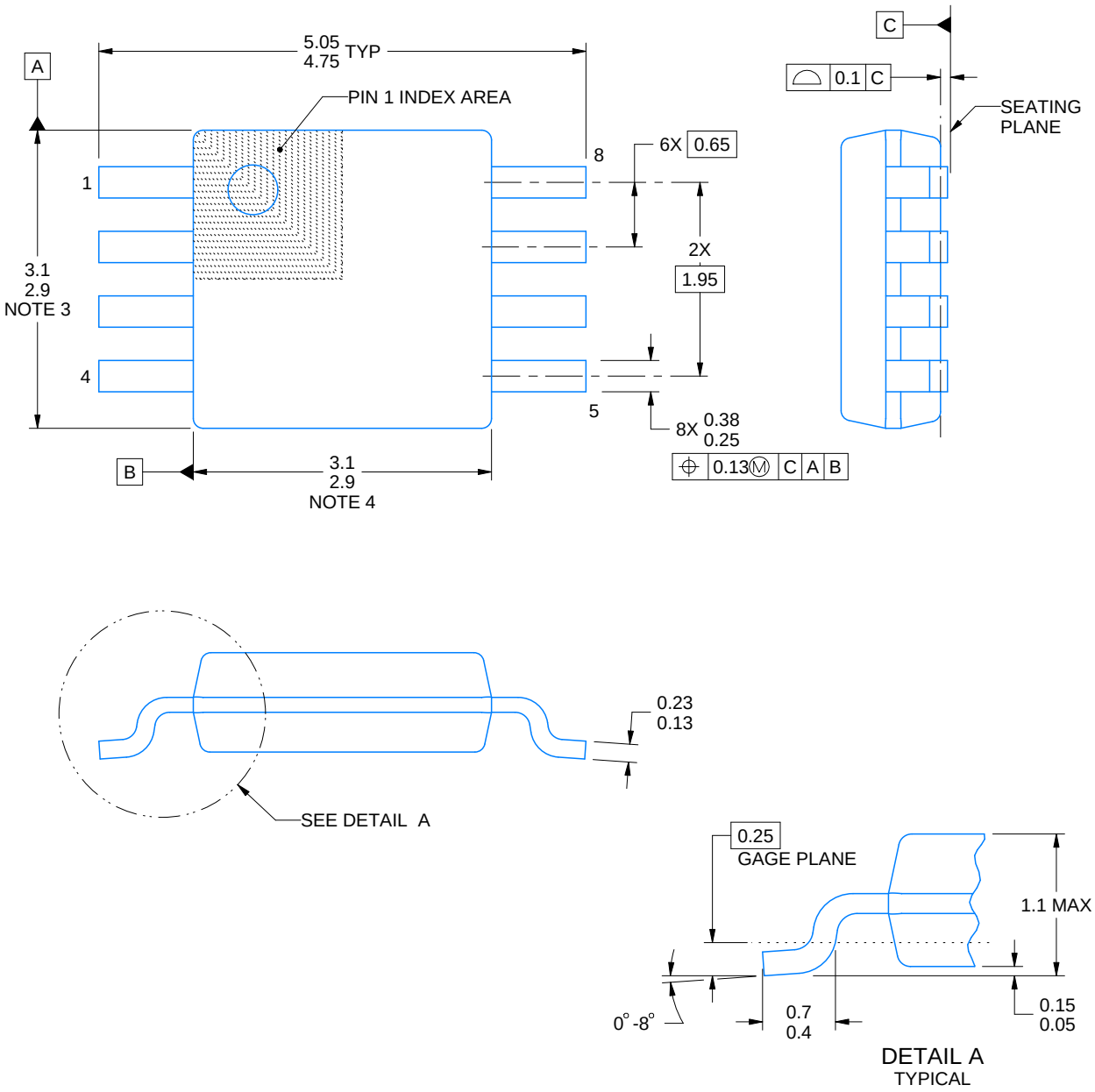
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

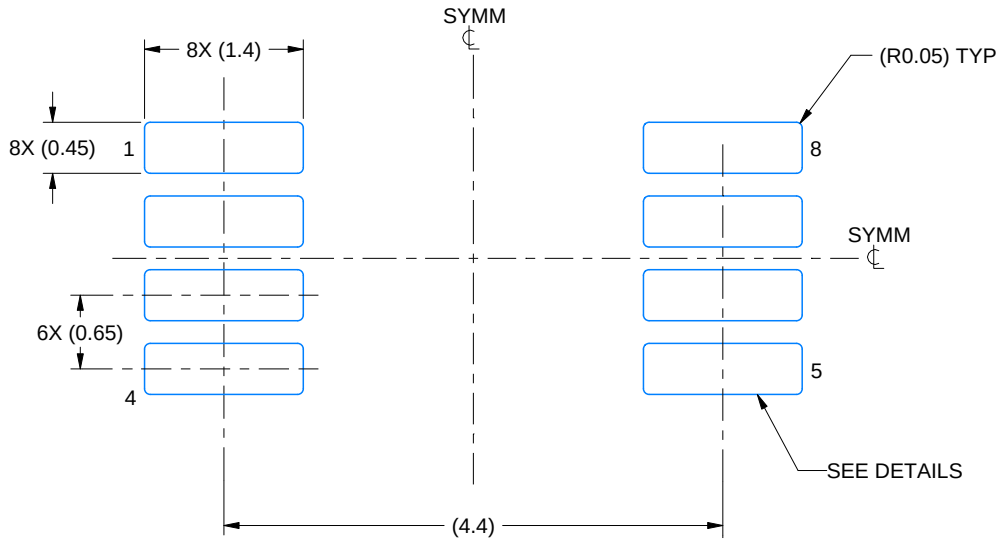
SMALL OUTLINE PACKAGE



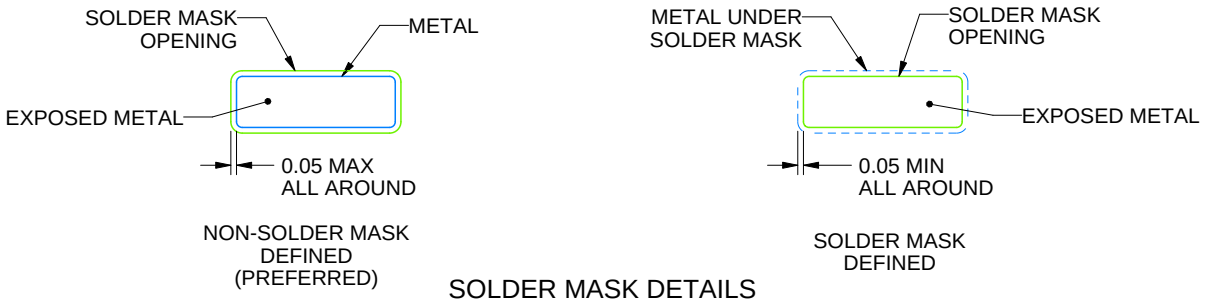

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

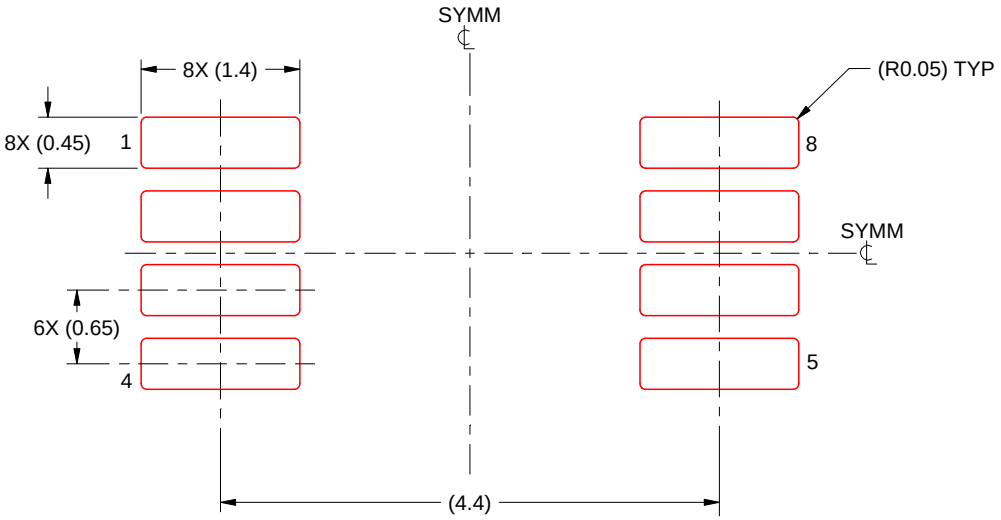



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月