

# LP5892-Q1 48 の電流源、32 のスキャンを備えた車載用 共通カソード LED マトリクス ドライバ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み:
  - 温度グレード 1: -40°C ~ +125°C, T<sub>A</sub>
- 独立した V<sub>CC</sub> および V<sub>R/G/B</sub> 電源
  - V<sub>CC</sub> 電圧範囲: 2.5V ~ 5.5V
  - V<sub>R/G/B</sub> 電圧範囲: 2.5V ~ 5.5V
- 48 個の 0.2mA ~ 40mA 電流源チャネル
  - チャネル間精度: ±0.5% (標準値)、±3% (最大値)、デバイス間精度: ±0.5% (標準値)、±2.5% (最大値)
  - 低いニー電圧: 0.27V (最大値) (I<sub>OUT</sub> = 5mA 時)
  - 3 ビット (8 ステップ) のグローバル輝度制御
  - 8 ビット (256 ステップ) の色輝度制御
  - 最大 16 ビット (65536 ステップ) の PWM グレイスケール制御
- 190mΩ R<sub>DS(ON)</sub> 付きの 16 個のスキャン ライン スイッチ
- 超低消費電力
  - 独立した最小 2.5V の V<sub>CC</sub>
  - 最小 3.6mA の小さい I<sub>CC</sub> (GCLK = 50MHz)
  - I<sub>CC</sub> を最小 0.9 mA に低減したインテリジェント省電力モード
- 1 ~ 64 のマルチプレクシングをサポートする内蔵 SRAM
  - 1 つのデバイス: 48 × 16 の LED または 16 × 16 の RGB ピクセルをサポート
  - 2 つのデバイスのスタック接続: 96 × 32 の LED または 32 × 32 の RGB ピクセルをサポート
- 高速および低 EMI の連続クロック シリーズ インターフェイス (CCSI)
  - わずか 3 本の信号線: SCLK / SIN / SOUT
  - 外部 50MHz (最大値) SCLK、rising エッジ転送メカニズム付き
  - 高い GCLK 周波数をサポートする内部周波数通倍器
- LED マトリクス ディスプレイの性能を最適化
  - 上側と下側のゴーストの除去
  - 低グレイスケール強調
  - LED の開放 / 短絡 / 弱短絡の検出と取り外し

## 2 アプリケーション

- オートモーティブ室内灯
- オートモーティブリア ライト
- 車載用フロント ライト

- 車載用ローカル調光バックライト

## 3 概要

LP5892-Q1 は、48 の定電流源と 16 のスキャン FET を備えた高集積の共通カソード マトリクス LED ディスプレイ ドライバです。1 つの LP5892-Q1 が 16 × 16 の RGB ピクセルの動作をサポートし、2 つの LP5892-Q1 デバイスが 32 × 32 の RGB ピクセルの動作をサポートしていません。低消費電力を実現するため、共通カソード構造によって、赤、緑、青の LED に独立した電源をサポートしていません。さらに、非常に低い動作電圧範囲 (最小 2.5V の V<sub>CC</sub>) と非常に低い動作電流 (最小 3.6mA の I<sub>CC</sub>) により、LP5892-Q1 の動作電力は大幅に低減されています。

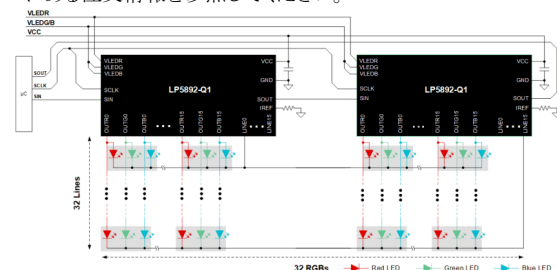
LP5892-Q1 は、多数のデバイスによるデジタイゼーション接続と高いリフレッシュ レートをサポートすると同時に、電磁干渉 (EMI) を最小化するため、高速立ち上がりエッジ伝送インターフェイスを実装しています。本デバイスは最大 50 MHz の SCLK (外部) と最大 160MHz の GCLK (内部) をサポートしています。その一方で本デバイスは、狭ピクセル ピッチ (NPP) LED ディスプレイ アプリケーションと小型 / 超小型 LED 製品における表示に関するさまざまな課題 (最初のスキャン ラインの輝度低下、上側および下側ゴースト、低グレイスケールでの不均一性、カップリング、LED の開放または短絡に起因するキャタピラー) を解決するための拡張回路とインテリジェント アルゴリズムを統合しています。そのため、LP5892-Q1 はこのような用途での理想的な選択肢と言えます。

LP5892-Q1 は LED の開放 / 弱短絡 / 短絡検出と動作中の取り外しにも対応しており、接続されているデジタル プロセッサにこの情報を報告することもできます。

### デバイスパッケージ情報

| 部品番号      | パッケージ <sup>(1)</sup> | 本体サイズ (公称)      |
|-----------|----------------------|-----------------|
| LP5892-Q1 | VQFN (76)            | 9.00mm × 9.00mm |

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



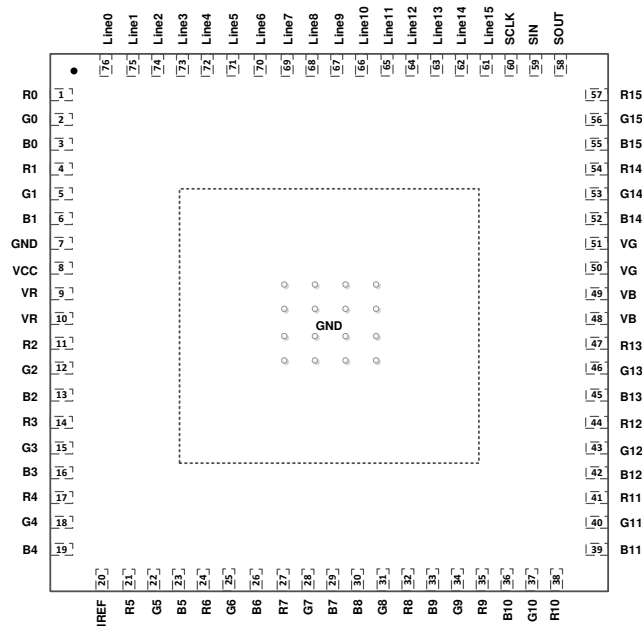
LP5892-Q1 デバイス スタック接続



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## 4 Pin Configuration and Functions



## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  |                       | MIN  | MAX | UNIT |
|--|-----------------------|------|-----|------|
| Voltage  | V <sub>CC</sub>       | -0.3 | 6   | V    |
|  | V <sub>R/G/B</sub>    | -0.3 | 6   | V    |
|  | IREF, SCLK, SIN, SOUT | -0.3 | 6   | V    |
|  | RX/GX/BX              | -0.3 | 6   | V    |
|  | LINE0 to LINE15       | -0.3 | 6   | V    |
| Operating junction temperature, T <sub>J</sub> |                       | -40  | 150 | °C   |
| Storage temperature, T <sub>stg</sub>          |                       | -55  | 150 | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings

|  |  | VALUE | UNIT |
|--|--|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup><br>HBM ESD classification level 3A | ±4000 | V    |
|  | Charged-device model (CDM), per AEC Q100-011<br>CDM ESD classification level C6            | ±1000 |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                        |  | MIN                   | NOM | MAX                   | UNIT |
|------------------------|--|-----------------------|-----|-----------------------|------|
| V <sub>CC</sub>        | Device supply voltage                      | 2.5                   |     | 5.5                   | V    |
| V <sub>LED R/G/B</sub> | LED supply voltage                         | 2.5                   |     | 5.5                   | V    |
| V <sub>IH</sub>        | High level logic input voltage (SCLK, SIN) | 0.7 × V <sub>CC</sub> |     |                       | V    |
| V <sub>IL</sub>        | Low level logic input voltage (SCLK, SIN)  |                       |     | 0.3 × V <sub>CC</sub> | V    |
| I <sub>OH</sub>        | High level logic output current (SOUT)     |                       |     | -2                    | mA   |
| I <sub>OL</sub>        | Low level logic output current (SOUT)      |                       |     | 2                     | mA   |
| I <sub>CH</sub>        | Constant output source current             | 0.2                   |     | 40                    | mA   |
| I <sub>LINE</sub>      | Line scan switch load current              | 0                     |     | 2                     | A    |
| T <sub>A</sub>         | Ambient operating temperature              | -40                   |     |                       | °C   |

### 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | LP5892-Q1  | UNIT |
|-------------------------------|--|------------|------|
|                               |  | RRF (VQFN) |      |
|                               |  | 76 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 22.2       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 10.7       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 7.2        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.1        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 7.1        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.7        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

At  $V_{CC} = V_R = 2.8V$ ,  $V_{G/B} = 3.8V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ ; Typical values are at  $T_A = 25^{\circ}C$  (unless otherwise specified)

| PARAMETER     |  | TEST CONDITIONS  | MIN       | TYP | MAX       | UNIT       |
|---------------|--|--|-----------|-----|-----------|------------|
| $V_{CC}$      | Device supply voltage                                | $I_{CH} \leq 20mA$   | 2.5       |     | 5.5       | V          |
|               |  | $I_{CH} \geq 20mA$   | 3.5       |     | 5.5       |            |
| $V_{UVR}$     | Undervoltage restart                                 | VCC rising   |           |     | 2.3       | V          |
| $V_{UVF}$     | Undervoltage shutdown                                | VCC falling  | 2.0       |     |           | V          |
| $V_{UV(HYS)}$ | Undervoltage shutdown hysteresis                     |  |           | 0.1 |           | V          |
| $I_{CC}$      | Device supply current                                | SCLK/SIN = 10MHz, MPSM_EN=1bit, Matrix PSM enable, internal GCLK off, GSn = 0000h, BC = 2h, CCR/G/B = 63h, PS_EN= 1h, VOUTn = floating, R <sub>IREF</sub> = 7.8k $\Omega$ (In intelligent power save mode) |           | 0.9 |           | mA         |
|               |  | SCLK/SIN = 10MHz, Standby enable, internal GCLK off, GSn = 0000h, BC = 2h, CCR/G/B = 63h, PS_EN= 1h, VOUTn = floating, R <sub>IREF</sub> = 7.8k $\Omega$ (In intelligent power save mode)                  |           | 0.9 |           | mA         |
|               |  | SCLK/SIN = 10MHz, PSP_MOD=1bit, internal GCLK=50MHz, GSn = 0000h, BC = 2h, CCR/G/B = 63h, PS_EN= 1h, VOUTn = floating, R <sub>IREF</sub> = 7.8k $\Omega$ (In power save mode)                              |           | 3.6 |           | mA         |
|               |  | SCLK = 10MHz, internal GCLK = 50 MHz, GSn = 1FFFh, BC = 2h, CCR/G/B = 63h, VOUTn = floating, R <sub>IREF</sub> = 7.8k $\Omega$ , $I_{CH} = 2mA$  |           | 3.6 |           | mA         |
|               |  | SCLK = 10MHz, internal GCLK = 100 MHz, GSn = 1FFFh, BC = 2h, CCR/G/B = 63h, VOUTn = floating, R <sub>IREF</sub> = 7.8k $\Omega$ , $I_{CH} = 2mA$   |           | 4.9 |           | mA         |
| $V_{R/G/B}$   | LED supply voltage                                   |  | 2.5       |     | 5.5       | V          |
| $V_{IH}$      | High level input voltage (SCLK, SIN)                 |  | 0.7 × VCC |     |           | V          |
| $V_{IL}$      | Low level input voltage (SCLK, SIN)                  |  |           |     | 0.3 × VCC | V          |
| $V_{OH}$      | High level output voltage (SOUT)                     | IOH = -2mA at SOUT   | VCC-0.4   |     | VCC       | V          |
| $V_{OL}$      | Low level output voltage (SOUT)                      | IOL = 2mA at SOUT  |           |     | 0.4       | V          |
| $I_{LOGIC}$   | Logic pin current (SCLK, SIN)                        | SCLK/SIN = VCC or GND  | -1        |     | 1         | $\mu A$    |
| $R_{DS(ON)}$  | Scan switches' on-state resistance (LINE0 to LINE15) | VCC = 2.8V, $T_A = 25^{\circ}C$  |           | 190 |           | m $\Omega$ |
| $V_{IREF}$    | Reference voltage                                    | SCLK/SIN = GND, internal GCLK= 0MHz, GSn = 0000h, BC = 2h, CCR/G/B = 63h, VOUTn = floating, R <sub>IREF</sub> = 7.8k $\Omega$  |           | 0.8 |           | V          |
| $V_{KNEE}$    | Channel knee voltage (R0-R15 / G0-G15 / B0-B15)      | VLEDR/G/B =2.5V, all channel outputs on, output current at 1mA   |           |     | 0.25      | V          |
|               |  | VLEDR/G/B =2.5V, all channel outputs on, output current at 5mA   |           |     | 0.27      | V          |
|               |  | VLEDR/G/B =2.5V, all channel outputs on, output current at 10mA  |           |     | 0.31      | V          |
|               |  | VLEDR/G/B =2.5V, IMAX = 1b, all channel outputs on, output current at 15mA   |           |     | 0.37      | V          |
|               |  | VLEDR/G/B =2.5V, IMAX=1b, all channel outputs on, output current at 20mA   |           |     | 0.41      | V          |
|               |  | VCC = 3.5V, IMAX=1b, all channel outputs on, output current at 25mA  |           |     | 0.45      | V          |
|               |  | VCC = 3.5V, IMAX=1b, all channel outputs on, output current at 30mA  |           |     | 0.53      | V          |
|               |  | VCC = 3.5V, IMAX=1b, all channel outputs on, output current at 35mA  |           |     | 0.62      | V          |
| $I_{CH(LKG)}$ | Channel leakage current (R0-R15 / G0-G15 / B0-B15)   | Channel voltage at 0V  |           |     | 1         | $\mu A$    |

### 5.5 Electrical Characteristics (続き)

At  $V_{CC} = V_R = 2.8V$ ,  $V_{G/B} = 3.8V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ ; Typical values are at  $T_A = 25^{\circ}C$  (unless otherwise specified)

| PARAMETER   |  | TEST CONDITIONS  | MIN     | TYP       | MAX       | UNIT |
|---|--|--|---------|-----------|-----------|------|
| $\Delta I_{ERR(C)}$   | Constant-current channel to channel deviation (R0-R15 / G0-G15 / B0-B15) (1) | All CHn = on, BC = 00h, CC = 31h, $V_{OUTn} = (V_{LED}-1)V$ , $R_{IREF} = 19.05k\Omega$ ( $I_{CH} = 0.2mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                             |         | $\pm 1$   | $\pm 2.5$ | %    |
|   |  | All CHn = on, BC = 00h, CC = 7Dh, $V_{OUTn} = (V_{LED}-1)V$ , $R_{IREF} = 19.05k\Omega$ ( $I_{CH} = 0.5mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                             |         | $\pm 0.5$ | $\pm 1.5$ | %    |
|   |  | All CHn = on, BC = 00h, CC = FBh, $V_{OUTn} = (V_{LED}-1)V$ , $R_{IREF} = 19.05k\Omega$ ( $I_{CH} = 1mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                               |         | $\pm 0.5$ | $\pm 1.5$ | %    |
|   |  | All CHn = on, BC = 2h, CC = FBh, $V_{OUTn} = (V_{LED}-1)V$ , $R_{IREF} = 7.8k\Omega$ ( $I_{CH} = 5mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                                  |         | $\pm 0.5$ | $\pm 2.5$ | %    |
|   |  | All CHn = on, BC = 6h, CC = A7h, $V_{OUTn} = (V_{LED}-1)V$ , $R_{IREF} = 7.8k\Omega$ ( $I_{CH} = 10mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                                 |         | $\pm 0.5$ | $\pm 2.5$ | %    |
|   |  | All CHn = on, BC = 7h, CC = FBh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED}-1)V$ , $R_{IREF} = 6.8k\Omega$ ( $I_{CH} = 20mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                  |         | $\pm 0.5$ | $\pm 2.7$ | %    |
|   |  | All CHn = on, BC = 7h, CC = FDh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED}-1)V$ , $V_{CC}=3.5V$ , $R_{IREF} = 5.49k\Omega$ ( $I_{CH} = 25mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |         | $\pm 0.5$ | $\pm 3$   | %    |
|   |  | All CHn = on, BC = 7h, CC = FAh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED}-1)V$ , $V_{CC}=3.5V$ , $R_{IREF} = 4.53k\Omega$ ( $I_{CH} = 30mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |         | $\pm 0.5$ | $\pm 3$   | %    |
|   |  | All CHn = on, BC = 7h, CC = FCh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED}-1)V$ , $V_{CC}=3.5V$ , $R_{IREF} = 3.92k\Omega$ ( $I_{CH} = 35mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |         | $\pm 0.5$ | $\pm 3$   | %    |
| All CHn = on, BC = 7h, CC = FAh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED}-1)V$ , $V_{CC}=3.5V$ , $R_{IREF} = 3.4k\Omega$ ( $I_{CH} = 40mA$ target), $T_A = 25^{\circ}C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |  | $\pm 0.5$  | $\pm 3$ | %         |           |      |

## 5.5 Electrical Characteristics (続き)

At  $V_{CC} = V_R = 2.8V$ ,  $V_{G/B} = 3.8V$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ ; Typical values are at  $T_A = 25^\circ C$  (unless otherwise specified)

| PARAMETER  | TEST CONDITIONS   | MIN       | TYP       | MAX       | UNIT       |
|--|---|-----------|-----------|-----------|------------|
| $\Delta I_{ERR(D)}$<br>Constant-current device to device deviation (R0-R15 / G0-G15 / B0-B15) (2)  | All CHn = on, BC = 00h, CC = 31h, $V_{OUTn} = (V_{LED-1})V$ , $R_{IREF} = 19.05k\Omega$ ( $I_{CH} = 0.2mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                             |           | $\pm 1$   | $\pm 2.5$ | %          |
|  | All CHn = on, BC = 00h, CC = 7Dh, $V_{OUTn} = (V_{LED-1})V$ , $R_{IREF} = 19.05k\Omega$ ( $I_{CH} = 0.5mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                             |           | $\pm 0.5$ | $\pm 2$   | %          |
|  | All CHn = on, BC = 00h, CC = FBh, $V_{OUTn} = (V_{LED-1})V$ , $R_{IREF} = 19.05k\Omega$ ( $I_{CH} = 1mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                               |           | $\pm 0.5$ | $\pm 1.5$ | %          |
|  | All CHn = on, BC = 2h, CC = FBh, $V_{OUTn} = (V_{LED-1})V$ , $R_{IREF} = 7.8k\Omega$ ( $I_{CH} = 5mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                                  |           | $\pm 0.5$ | $\pm 2$   | %          |
|  | All CHn = on, BC = 6h, CC = A7h, $V_{OUTn} = (V_{LED-1})V$ , $R_{IREF} = 7.8k\Omega$ ( $I_{CH} = 10mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                                 |           | $\pm 0.5$ | $\pm 2$   | %          |
|  | All CHn = on, BC = 7h, CC = FBh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED-1})V$ , $R_{IREF} = 6.8k\Omega$ ( $I_{CH} = 20mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15                  |           | $\pm 0.5$ | $\pm 2$   | %          |
|  | All CHn = on, BC = 7h, CC = FDh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED-1})V$ , $V_{CC}=3.5V$ , $R_{IREF} = 5.49k\Omega$ ( $I_{CH} = 25mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |           | $\pm 0.5$ | $\pm 2.5$ | %          |
|  | All CHn = on, BC = 7h, CC = FAh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED-1})V$ , $V_{CC}=3.5V$ , $R_{IREF} = 4.53k\Omega$ ( $I_{CH} = 30mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |           | $\pm 0.5$ | $\pm 2.5$ | %          |
|  | All CHn = on, BC = 7h, CC = FCh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED-1})V$ , $V_{CC}=3.5V$ , $R_{IREF} = 3.92k\Omega$ ( $I_{CH} = 35mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |           | $\pm 0.5$ | $\pm 2.5$ | %          |
| All CHn = on, BC = 7h, CC = FAh, $I_{MAX}=1b$ , $V_{OUTn} = (V_{LED-1})V$ , $V_{CC}=3.5V$ , $R_{IREF} = 3.4k\Omega$ ( $I_{CH} = 40mA$ target), $T_A = 25^\circ C$ , includes the $V_{IREF}$ tolerance, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15 |   | $\pm 0.5$ | $\pm 2.5$ | %         |            |
| $\Delta I_{REG(LINE)}$ Line regulation (R0-R15 / G0-G15 / B0-B15) (3)  | $V_{LED} = 2.5$ to $5.5V$ , All CHn = on, $V_{OUTn} = (V_{LED-1})V$ , at same color grouped outputs of R0-R15 / G0-G15 / B0-B15   |           |           | $\pm 1$   | %/V        |
| $\Delta I_{REG(LOAD)}$ Load regulation (R0-R15 / G0-G15 / B0-B15) (4)  | $V_{OUTn} = (V_{LED-1})V$ to $(V_{LED-3})V$ , $V_R=V_{G/B}=V_{LED}=3.8V$ , All CHn = on, at same color grouped outputs of R0-R15 / G0-G15 / B0-B15  |           |           | $\pm 1$   | %/V        |
| $T_{TSD}$ Thermal shutdown threshold   |   |           | 170       |           | $^\circ C$ |
| $T_{HYS}$ Thermal shutdown hysteresis  |   |           | 15        |           | $^\circ C$ |

(1) The deviation of each output in same color group (OUTR0-15 or OUTG0-15 or OUTB0-15) from the average of same color group

$$\Delta(\%) = \left[ \frac{I_{Xn}}{\frac{I_{X0} + I_{X1} + \dots + I_{X14} + I_{X15}}{16}} - 1 \right] \times 100$$

constant current. The deviation is calculated by the formula. (X = R or G or B, n = 0-15)

(2) The deviation of the average of constant-current in each color group from the ideal constant-current value. (X = R or G or B) :

$$\Delta(\%) = \left[ \frac{I_{X0} + I_{X1} + \dots + I_{X14} + I_{X15} - \text{Ideal Output Current}}{\text{Ideal Output Current}} \right] \times 100$$

Ideal current is calculated by the following equation:

$$I_{IDEAL\_R(or\ G\ or\ B)} = \frac{V_{IREF}}{R_{IREF}} \times GAIN_{(BC)} \times \frac{1 + CC\_R(or\ CC\_G\ or\ CC\_B)}{256}$$

(3) Line regulation is calculated by the following equation. (X = R or G or B, n = 0-15):

$$\Delta(\%V) = \left[ \frac{(I_{Xn} \text{ at } V_{LED} = 5.5\text{ V}) - (I_{Xn} \text{ at } V_{LED} = 2.5\text{ V})}{(I_{Xn} \text{ at } V_{LED} = 2.5\text{ V})} \right] \times \frac{100}{5.5\text{ V} - 2.5\text{ V}}$$

(4) Load regulation is calculated by the following equation. (X = R or G or B, n = 0-15):

$$\Delta(\%V) = \left[ \frac{(I_{Xn} \text{ at } V_{Xn} = 1\text{ V}) - (I_{Xn} \text{ at } V_{Xn} = 3\text{ V})}{(I_{Xn} \text{ at } V_{Xn} = 3\text{ V})} \right] \times \frac{100}{3\text{ V} - 1\text{ V}}$$

## 5.6 Timing Requirements

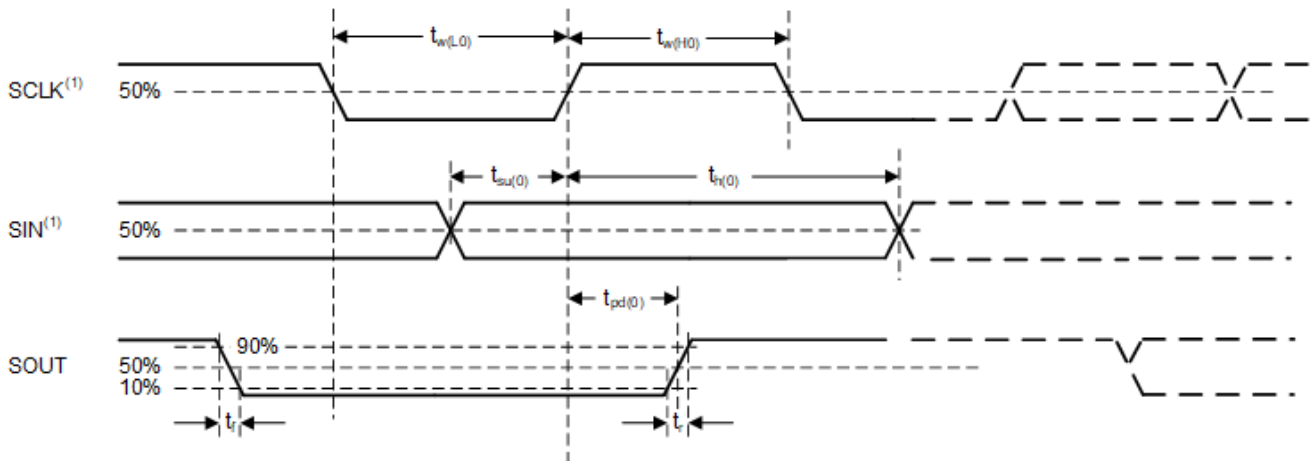
At  $V_{CC} = V_R = 2.8\text{V}$ ,  $V_{G/B} = 3.8\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; Typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

| PARAMETER          | TEST CONDITIONS                  | MIN               | TYP | MAX | UNIT |
|--------------------|----------------------------------|-------------------|-----|-----|------|
| f <sub>SCLK</sub>  | Clock frequency (SCLK)           |                   |     | 50  | MHz  |
| t <sub>w(H0)</sub> | High level pulse duration (SCLK) | 9                 |     |     | ns   |
| t <sub>w(L0)</sub> | Low level pulse duration (SCLK)  | 9                 |     |     | ns   |
| t <sub>su(0)</sub> | Set-up time                      | SIN to SCLK ↑     | 10  |     | ns   |
| t <sub>h(0)</sub>  | Hold time                        | SCLK ↑ to SIN ↑ ↓ | 2   |     | ns   |

## 5.7 Switching Characteristics

At  $V_{CC} = V_R = 2.8\text{V}$ ,  $V_{G/B} = 3.8\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; Typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

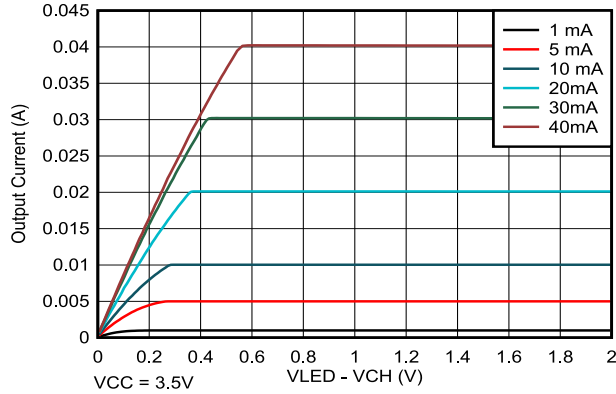
| PARAMETER          | TEST CONDITIONS   | MIN  | TYP | MAX  | UNIT |
|--------------------|-------------------|--|-----|------|------|
| t <sub>r</sub>     | Rise time (SOUT)  | V <sub>CC</sub> = 3.3 V, C <sub>SOUT</sub> = 30pF              | 2   | 10   | ns   |
| t <sub>f</sub>     | Fall time (SOUT)  | V <sub>CC</sub> = 3.3 V, C <sub>SOUT</sub> = 30pF              | 2   | 10   | ns   |
| t <sub>pd(0)</sub> | Propagation delay | SCLK ↑ to SOUT ↑ ↓, full temperature, C <sub>SOUT</sub> = 30pF | 3.5 | 14.2 | ns   |



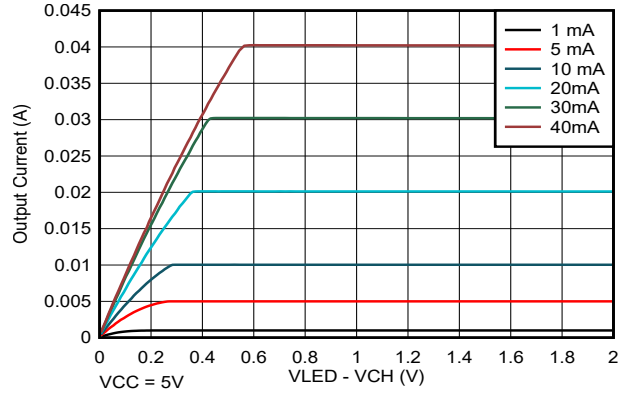
(1). Input pulse rise and fall time is 2 ns typically.

**图 5-1. Timing and Switching Diagram**

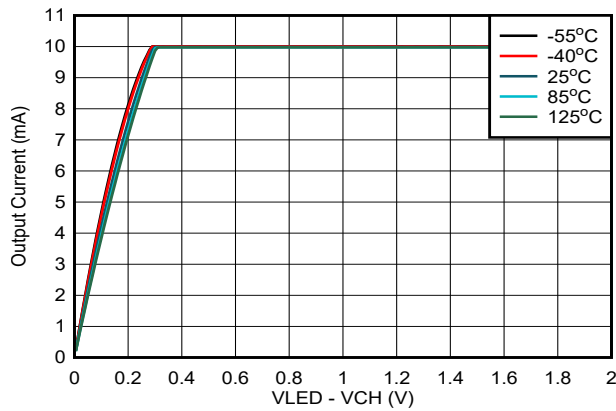
## 5.8 Typical Characteristics



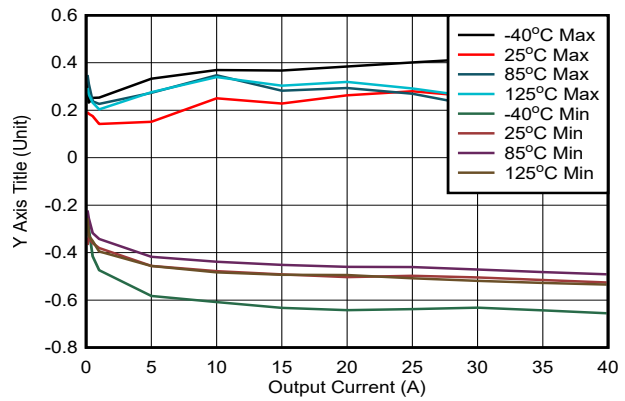
5-2. Channel Current vs (VLED-Vchannel) Voltage



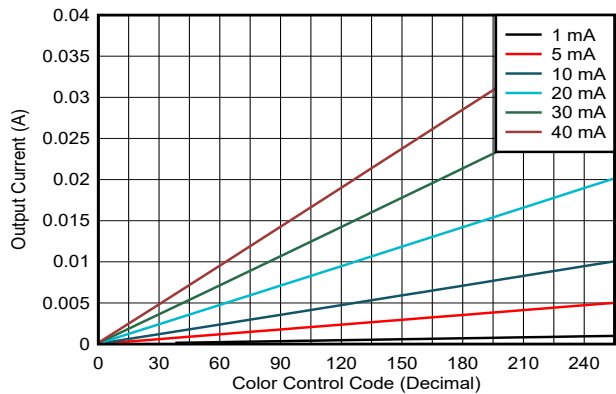
5-3. Channel Current vs (VLED-Vchannel) Voltage



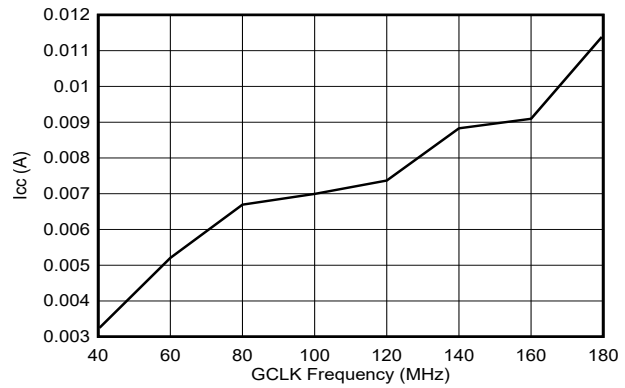
5-4. Channel Current vs (VLED-Vchannel) Voltage



5-5. Channel to Channel Accuracy vs Output Current

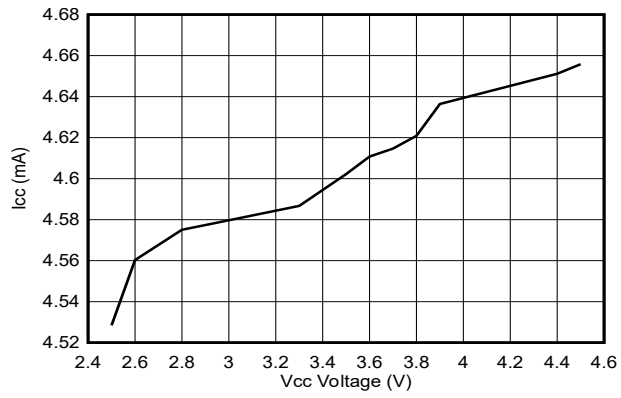


5-6. Color Control Code vs Output Current



5-7. Icc Current vs GCLK Frequency

### 5.8 Typical Characteristics (continued)



GCLK = 80 MHz

**图 5-8. Icc Current vs Vcc Voltage**

## 6 Detailed Description

### 6.1 Overview

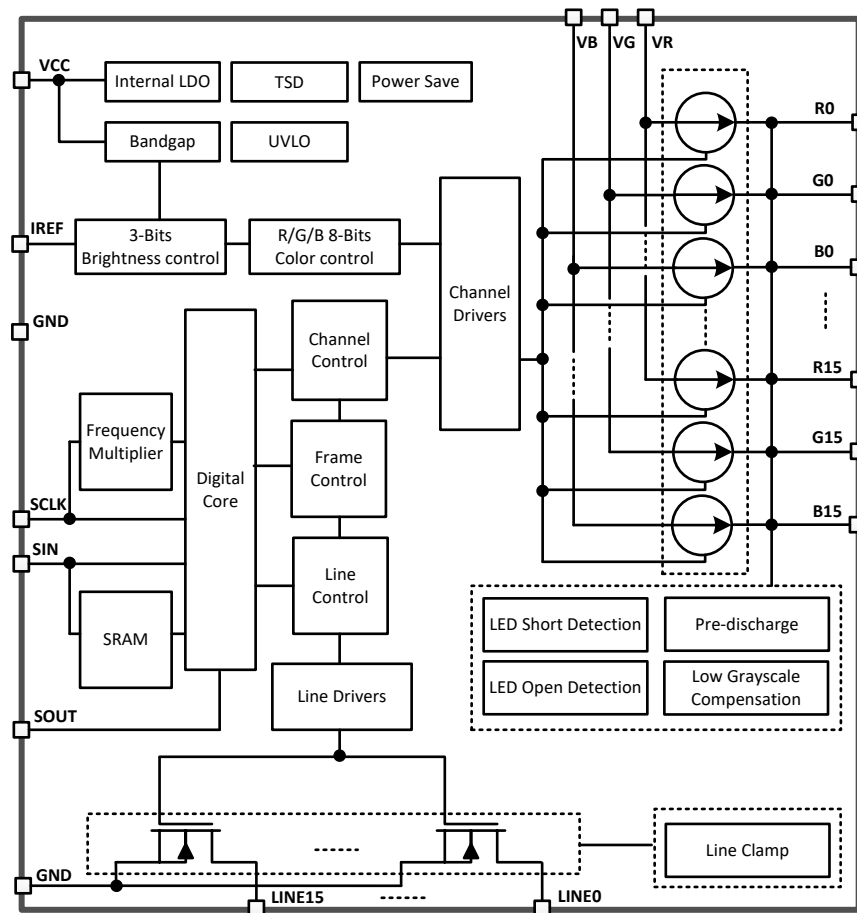
The LP5892-Q1 is a highly integrated RGB LED driver with 48 constant current sources and 16 scanning FETs. A single LP5892-Q1 is capable of driving  $16 \times 16$  RGB LED pixels while stacking two LP5892-Q1 devices can drive  $32 \times 32$  RGB LED pixels. To achieve low power consumption, the device supports separated power supplies for the red, green, and blue LEDs by its common cathode structure. Furthermore, the operation power of the LP5892-Q1 is significantly reduced by ultra-low operation voltage range ( $V_{CC}$  down to 2.5V) and ultra-low operation current ( $I_{CC}$  down to 3.6mA).

The LP5892-Q1 supports 0.2mA to 40mA per channel with typical 0.5% channel-to-channel current deviation and typical 0.5% device-to-device current deviation. The DC current value of all 48 channels is set by an external IREF resistor and can be adjusted by the 8-step global brightness control (BC) and the 256-step per-color group brightness control (CC\_R/CC\_G/CC\_B).

The LP5892-Q1 implements a high speed rising-edge transmission interface to support high device count daisy-chained and high refresh rate while minimizing electrical-magnetic interference (EMI). The LP5892-Q1 supports up to 50MHz SCLK (external) and up to 160MHz GCLK (internal).

The LP5892-Q1 also implements LED open, weak-short, and short detections and can also report this information out to the accompanying digital processor.

### 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Independent and Stackable Mode

The LP5892-Q1 can operate in two different modes: independent or stackable. In independent mode, a single LP5892-Q1 can drive a  $16 \times 16$  RGB LED matrix, while in stackable mode, two LP5892-Q1 devices can be stacked together, which means the line switches of one device can be shared to the others. Stacking two LP5892-Q1 devices can drive a  $32 \times 32$  RGB LED matrix. The mode can be configured by the MOD\_SIZE (see [FC2](#) for more details).

#### 6.3.1.1 Independent Mode

Figure 6-1 shows an implementation of a  $16 \times 32$  RGB LED matrix using two LP5892-Q1 devices in independent mode. Each device is responsible for its own  $16 \times 16$  RGB LED matrix, which means that all the data for section A is stored in device 1 and the data for section B is stored in device 2.

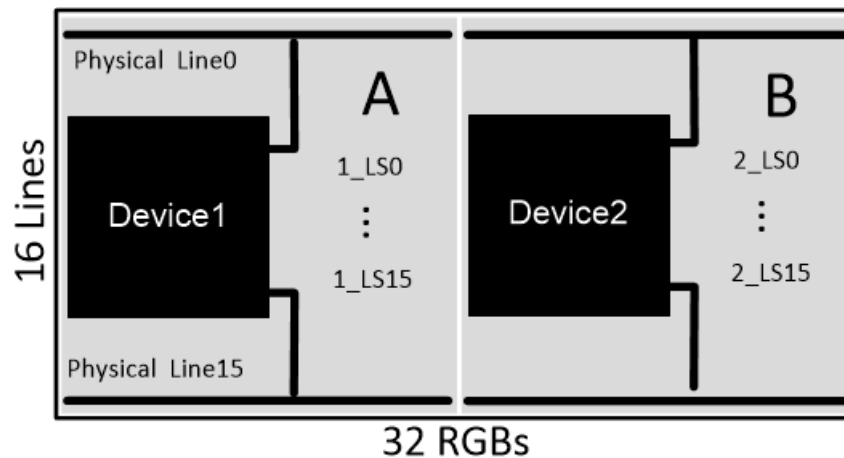


Figure 6-1. Two Devices in Independent Mode

The unused line must be assigned to the last several lines of the device. For example, if there are only 14 scanning lines, then the two unused lines must be assigned to 1\_LS14 and 1\_LS15.

### 6.3.1.2 Stackable Mode

While operating the LP5892-Q1 in stackable mode, as shown in below table.

表 6-1. Stackable Mode

| Mode  | Matrix Size | Data Sequence | Register Value |            | Scan Sequence                    |
|-------|-------------|---------------|----------------|------------|----------------------------------|
|       |             |               | FC2 Bit 43     | FC4 Bit 14 |                                  |
| Mode1 | 16x32       | D1->D2        | 0              | invalid    | D1, D2 independent               |
| Mode2 | 32x32       | D1->D2        | 1              | 1          | D1 LS0->D1 LS15->D2 LS15->D2 LS0 |

図 6-2 shows the connection between two LP5892-Q1 devices in stackable mode without scan reversed driving 32 × 32 RGB LED pixels. The MOD\_SIZE must be configured to 1b and SCAN\_REV must be configured to 1b. Device 1 supplies switches for the first 16 scan line and device 2 supplies 16 lines for physical line 17-32. The SCAN\_REV configure to 1b which reverses the scan line switching order of the second device, to make sure the scanning sequence is from physical 1<sup>st</sup> line to 32<sup>nd</sup> line. Scan sequence is shown in the table. The data for matrix sections A and C store in device 1, while matrix sections B and D data are stored in device 2.

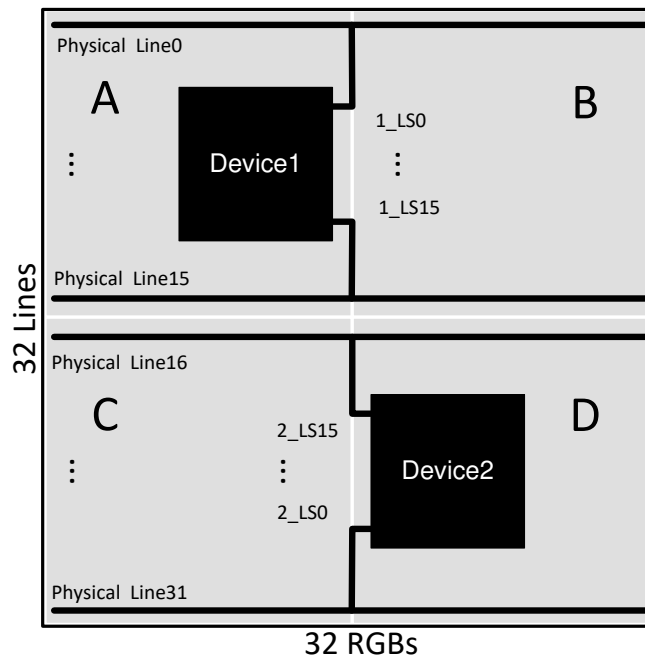


図 6-2. Mode2 Diagram

When two LP5892-Q1 devices are used in stackable mode, if there are unused line switches, these unused line switches must be the last line switches of the second device. For example, if there are only 30 scanning lines,

MOD\_SIZE = '1'b, SCAN\_REV = '1'b, the unused line switches can be below,

- D2\_LS0, D2\_LS1

MOD\_SIZE = '1'b, SCAN\_REV = '0'b, the unused line switches can be below,

- D2\_LS14, D2\_LS15

### 6.3.2 Current Setting

#### 6.3.2.1 Brightness Control (BC) Function

The LP5892-Q1 device is able to adjust the output current of all constant-current outputs simultaneously. This function is called global brightness control (BC). The global BC for all outputs is programmed with a 3-bit register, thus all output currents can be adjusted in eight steps for a given current-programming resistor,  $R_{IREF}$ . When the 3-bit BC register changes, the gain of output current,  $GAIN_{BC}$  changes as [表 6-2](#) below.

**表 6-2. Current Gain Versus BC Code**

| BC Register (BC) | Current Gain ( $GAIN_{BC}$ ) |
|------------------|------------------------------|
| 000b             | 24.17                        |
| 001b             | 30.57                        |
| 010b             | 49.49                        |
| 011b (default)   | 86.61                        |
| 100b             | 103.94                       |
| 101b             | 129.92                       |
| 110b             | 148.48                       |
| 111b             | 173.23                       |

The maximum output current per channel,  $I_{OUTSET}$ , is determined by resistor  $R_{IREF}$ , and the  $GAIN_{BC}$ . The voltage on IREF is typically 0.8 V.  $R_{IREF}$  can be calculated by [式 1](#) below. For noise immunity purpose, suggest  $R_{IREF} < 40 \text{ k}\Omega$ .

$$R_{IREF} (k\Omega) = \frac{V_{IREF} (V)}{I_{IREF} (mA)} = \frac{V_{IREF} (V)}{I_{OUTSET} (mA)} \times GAIN_{(BC)} \quad (1)$$

#### 6.3.2.2 Color Brightness Control (CC) Function

The LP5892-Q1 device is able to adjust the output current of each of the three color groups R0-R15, G0-G15, and B0-B15 separately. This function is called color brightness control (CC). For each color, it has 8-bit data register, CC\_R, CC\_G, or CC\_B. Thus, all color group output currents can be adjusted in 256 steps from 0% to 100% of the maximum output current,  $I_{OUTSET}$ . The output current of each color,  $I_{OUT\_R}$  (or G or B) can be calculated by [Equation 2](#) below.

$$I_{OUT\_R(or\ G\ or\ B)} = I_{OUTSET} \times \frac{1 + CC\_R(or\ CC\_G\ or\ CC\_B)}{256} \quad (2)$$

[表 6-3](#) shows the CC data versus the constant-current against  $I_{OUTSET}$ :

**表 6-3. CC Data vs Current Ratio**

| CC Register (CC_R or CC_G or CC_B) | Ratio of $I_{OUTSET}$ |        |
|------------------------------------|-----------------------|--------|
| 0000 0000b                         | 1/256                 | 0.39%  |
| 0000 0001b                         | 2/256                 | 0.78%  |
| ...                                | ...                   | ...    |
| 0111 1111b (default)               | 128/256               | 50%    |
| ...                                | ...                   | ...    |
| 1111 1110b                         | 255/256               | 99.61% |
| 1111 1111b                         | 256/256               | 100%   |

### 6.3.2.3 Choosing BC/CC for a Different Application

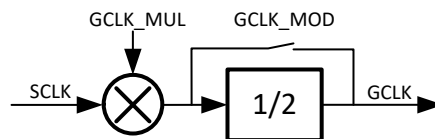
BC is mainly used for global brightness adjustment to adapt to ambient brightness, such as between day and night, indoor and outdoor.

- Suggested BC is 3h or 4h, which is in the middle of the range, allowing flexible changes in brightness up and down.
- If the current of one color group (usually R LEDs) is close to the output maximum current (40 mA), to prevent the constant output current from exceeding the upper limit in case a larger BC code is input accidentally, choose the maximum BC value, 7h.
- If the current of one color group (usually B LEDs) is close to the output minimum current (0.2 mA), to prevent the constant output current from exceeding the lower limit in case a lower BC code is input accidentally, choose the minimum BC code, 0h.

CC can be used to fine tune the brightness in 256 steps. This is suitable for white balance adjustment between RGB color group. To get a pure white color, the general requirement for the luminous intensity ratio of R, G, B LED is 5:3:2. Depending on the characteristics of the LED (Electro-Optical conversion efficiency), the current ratio of R, G, B LED is much different from this ratio. Usually, the Red LED needs the largest current. Choose 255d (the maximum value) CC code for the color group that needs the largest initial current, then choose proper CC code for the other two color groups according to the current ratio requirement of the LED used.

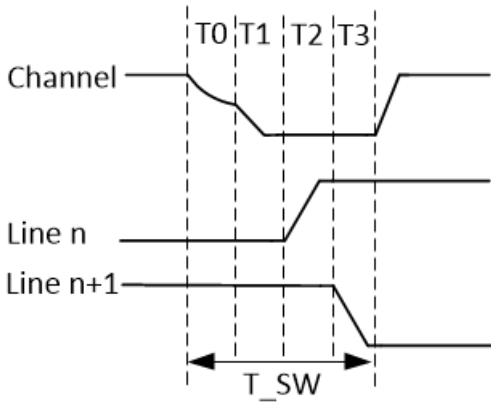
### 6.3.3 Frequency Multiplier

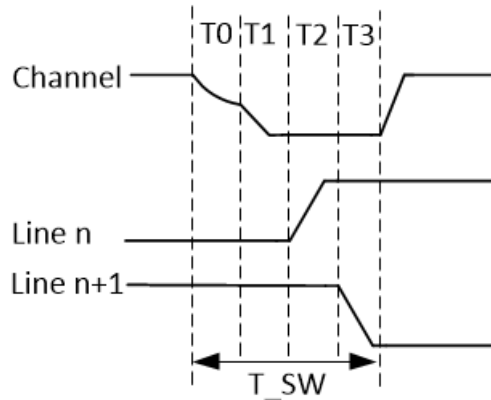
The LP5892-Q1 has an internal frequency multiplier to generate the GCLK by SCLK. The GCLK frequency can be configured by FREQ\_MOD (See [FC0](#) for more details) and FREQ\_MUL (see [FC0](#) for more details ) from 40 MHz to 160 MHz. As [Figure 6-3](#) shows, if the GCLK frequency is not higher than 80 MHz, the GCLK\_MOD is set to 1 to disable the bypass switch (enable the 1/2 divider), while the GCLK frequency is higher than 80 MHz, the GCLK\_MOD is set to 0 to enable the bypass switch (disable the 1/2 divider).



**Figure 6-3. Frequency Multiplier Block Diagram**

### 6.3.4 Line Transitioning Sequence

The LP5892-Q1 defines a timing sequence of scan line transition, shown as  6-4. T\_SW is the total transitioning time. T\_SW is broken up into four intervals: T0 is the time interval between the end of PWM time in current segment and the beginning of channel pre-discharge, T1 is the time interval between the beginning of the channel pre-discharge and the beginning of current line OFF, T2 is the time interval that the beginning of current line OFF and the beginning of next line ON, T3 is the time interval of the beginning of next line ON and the beginning of PWM time in next segment.



**図 6-4. Line Transitioning Sequence**

The line switch time T\_SW equals to T0 + T1 + T2 + T3. T\_SW can be configured by the LINE\_SWT (see FC1 register bit 40-37 in [表 6-8](#)).

[表 6-4](#) is the relation between LINE\_SWT bits and the line switch time (GCLK numbers) with different internal GCLK frequency.

**表 6-4. Line Switch Time**

| LINE_SW T | GCLK Numbers | T_SW (us, 40 MHz GCLK) | T_SW (us, 60 MHz GCLK) | T_SW (us, 100 MHz GCLK) | T_SW (us, 120 MHz GCLK) | T_SW (us, 160 MHz GCLK) |
|-----------|--------------|------------------------|------------------------|-------------------------|-------------------------|-------------------------|
| 0000b     | 45           | 1.125                  | 0.7515                 | 0.45                    | 0.3735                  | 0.2835                  |
| 0001b     | 60           | 1.5                    | 1.002                  | 0.6                     | 0.498                   | 0.378                   |
| 0010b     | 90           | 2.25                   | 1.503                  | 0.9                     | 0.747                   | 0.567                   |
| 0011b     | 120          | 3                      | 2.004                  | 1.2                     | 0.996                   | 0.756                   |
| 0100b     | 150          | 3.75                   | 2.505                  | 1.5                     | 1.245                   | 0.945                   |
| 0101b     | 180          | 4.5                    | 3.006                  | 1.8                     | 1.494                   | 1.134                   |
| 0110b     | 210          | 5.25                   | 3.507                  | 2.1                     | 1.743                   | 1.323                   |
| 0111b     | 240          | 6                      | 4.008                  | 2.4                     | 1.992                   | 1.512                   |
| 1000b     | 270          | 6.75                   | 4.509                  | 2.7                     | 2.241                   | 1.701                   |
| 1001b     | 300          | 7.5                    | 5.01                   | 3                       | 2.49                    | 1.89                    |
| 1010b     | 330          | 8.25                   | 5.511                  | 3.3                     | 2.739                   | 2.079                   |
| 1011b     | 360          | 9                      | 6.012                  | 3.6                     | 2.988                   | 2.268                   |
| 1100b     | 390          | 9.75                   | 6.513                  | 3.9                     | 3.237                   | 2.457                   |
| 1101b     | 420          | 10.5                   | 7.014                  | 4.2                     | 3.486                   | 2.646                   |
| 1110b     | 450          | 11.25                  | 7.515                  | 4.5                     | 3.735                   | 2.835                   |
| 1111b     | 480          | 12                     | 8.016                  | 4.8                     | 3.984                   | 3.024                   |

### 6.3.5 Protections and Diagnostics

#### 6.3.5.1 Thermal Shutdown Protection

The thermal shutdown (TSD) function turns off all IC constant-current outputs when the junction temperature ( $T_J$ ) exceeds 170°C (typical). The function resumes normal operation when  $T_J$  falls below 155°C (typical).

#### 6.3.5.2 IREF Resistor Short Protection

The IREF resistor short protection (ISP) function prevents unwanted large currents from flowing through the constant-current output when the IREF resistor is shorted accidentally. The LP5892-Q1 device turns off all output channels when the IREF pin voltage is lower than 0.19 V (typical). When the IREF pin voltage goes higher than 0.325 V (typical), the LP5892-Q1 device resumes normal operation.

#### 6.3.5.3 LED Open Load Detection and Removal

##### 6.3.5.3.1 LED Open Detection

The LED Open Detection (LOD) function detects faults caused by an open circuit in any LED, or a short from  $OUT_n$  to  $VLED$  with low impedance. This function was realized by comparing the  $OUT_n$  voltage to the LOD detection threshold voltage level set by  $LODVTH\_R/LODVTH\_G/LODVTH\_B$  (See [FC3](#) for more details). If the  $OUT_n$  voltage is higher than the programmed voltage, the corresponding output LOD bit is set to 1 to indicate an open LED. Otherwise, the output of that LOD bit is 0. LOD data output by the detection circuit are valid only during the  $OUT_n$  turning on period.

Figure 6-5 shows the equivalent circuit of LED open detection.

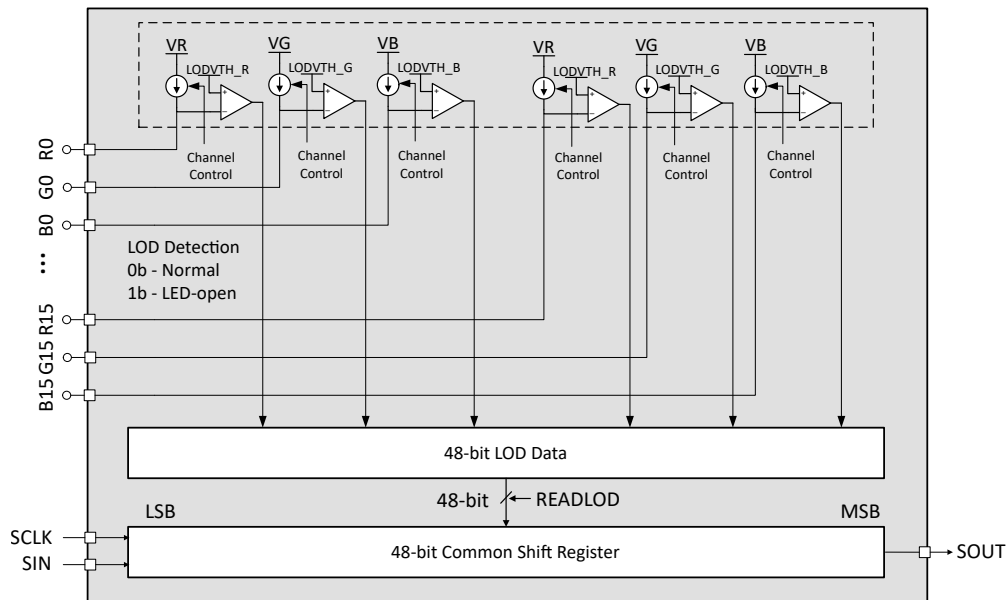

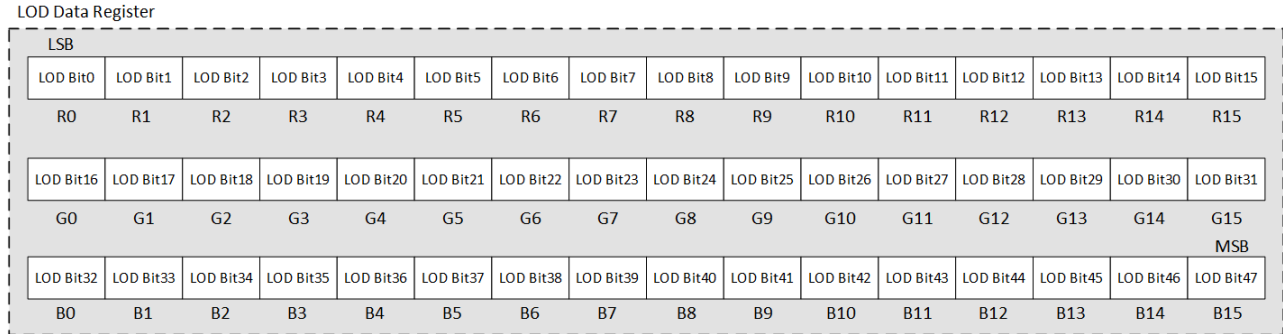


Figure 6-5. LED Open Detection Circuit


The LED open detection function records the position of the open LED, which contains the scan line number and relevant channel number. The scan line order is stored LOD\_LINE\_WARN register (see FC17 for more details), and the channel number is latched into the internal 48-bit LOD data register (see FC20 for more details) at the end of each segment.  6-6 shows the bit arrangement of the LOD data register.

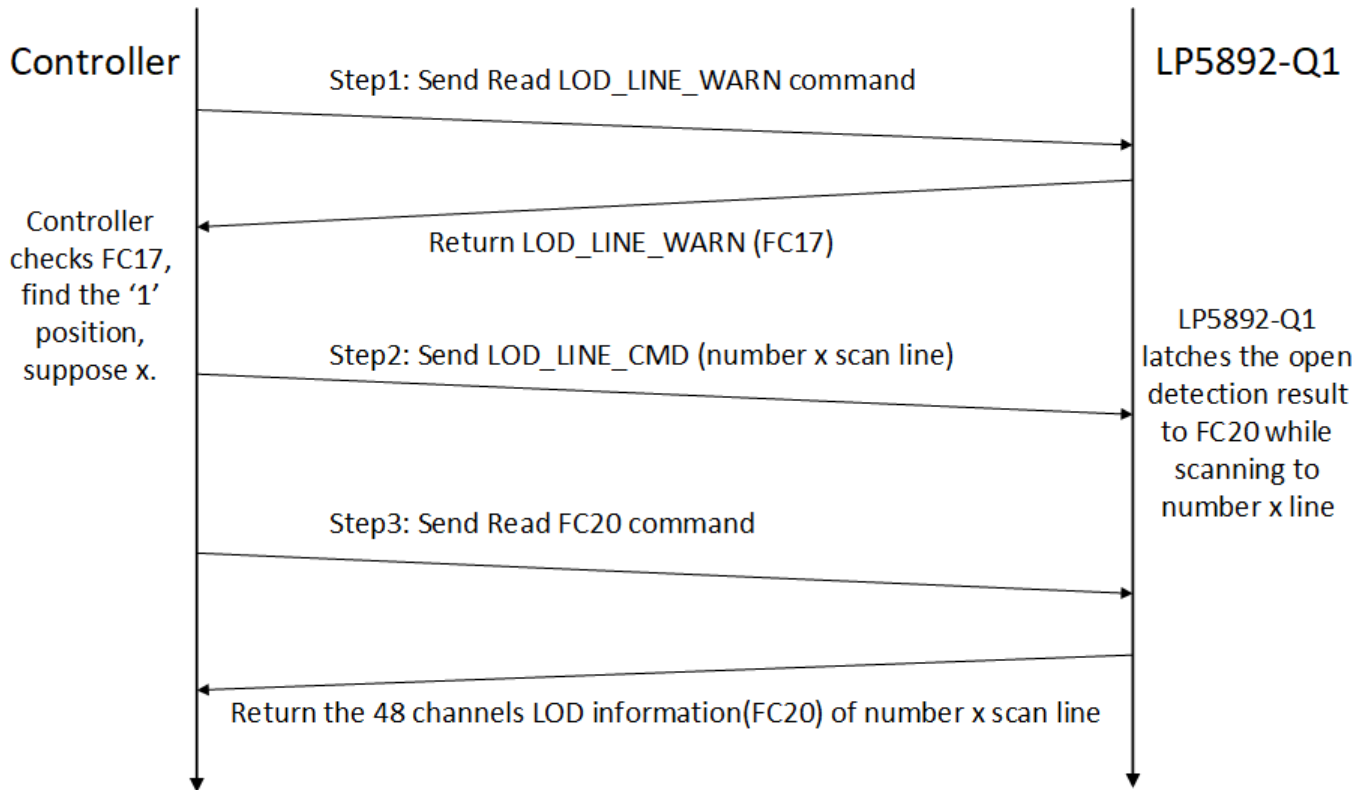


 6-6. Bit Arrangement in LOD Data Register

6.3.5.3.2 Read LED Open Information

The LOD readback function must be enabled before read LED open information. This function is enabled by LOD\_LSD\_RB (see FC3 for more details).

 6-7 shows the steps to read LED open information. Wait at least one sub-period time between Step2 and Step3 command.



 6-7. Steps to Read LED Open Information

### 6.3.5.3.3 LED Open Caterpillar Removal

Figure 6-8 shows the caterpillar issue caused by open LED. Suppose the LED0-1 is an open LED. When line 0 is chosen and the OUT1 is turned on, the OUT1 voltage is forced to approach to  $V_{LED}$  because of the broken path of the current source. However, the voltage of the un-chosen lines are below the  $V_{clamp}$  which is much lower than  $V_{LED}$ , causing all LEDs which connect to the channel OUT1, light unwanted.

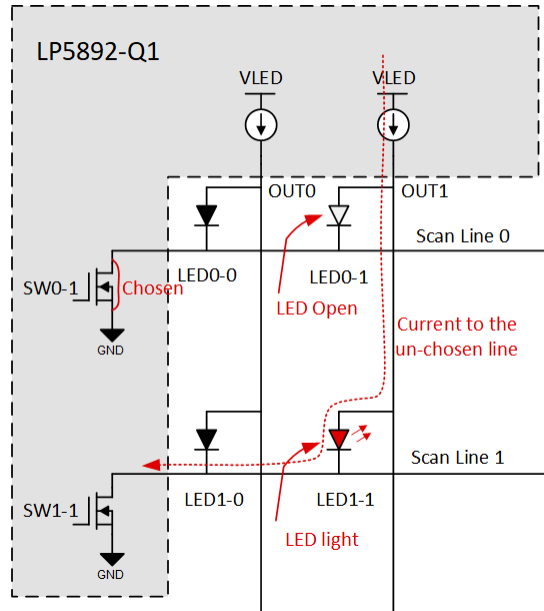


Figure 6-8. LED Open Caterpillar

The LP5892-Q1 implements circuits that can eliminate the caterpillar issue caused by open LEDs. The LED open caterpillar removal function is configured by `LOD_RM_EN` (see [FC0](#) for more details). When `LOD_RM_EN` is set to 1b, the caterpillar removal function is enabled. The corresponding channel `OUTn` is turned off when scanning to line with open LED. The caterpillar issue is eliminated until device resets or `LOD_RM_EN` is set to 0b.

The internal caterpillar elimination circuit can handle a maximum of three lines that have open LEDs fault condition. If there are open LEDs located in three or fewer lines, the LP5892-Q1 is able to handle the open LEDs all in these lines. If there are open LEDs in more than three lines, the caterpillar issue is solved for the lines where the first three open LEDs were detected, but the open LEDs in the fourth and subsequent lines still cause the caterpillar issue.

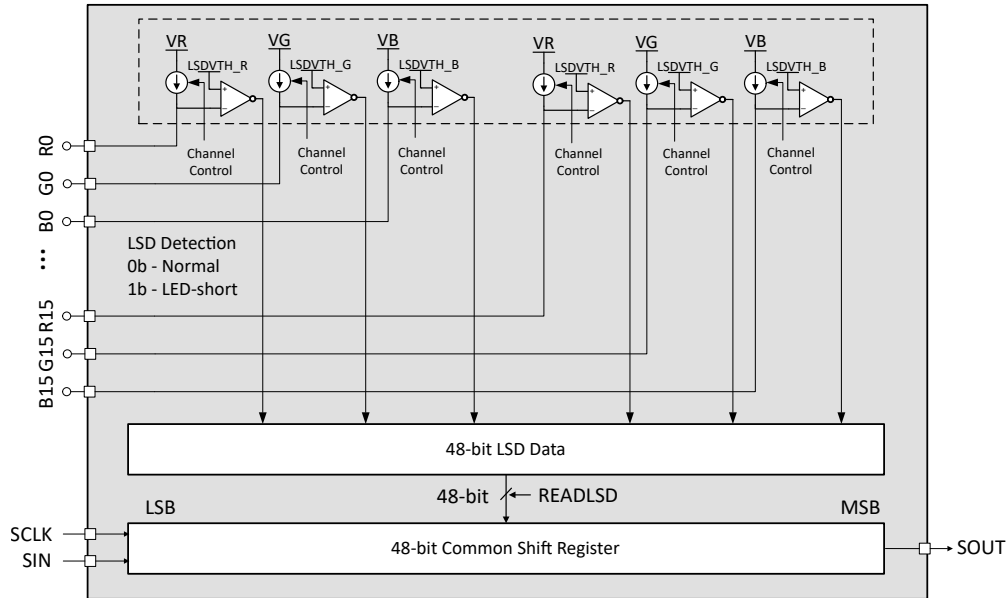
### 6.3.5.4 LED Short and Weak Short Circuitry Detection and Removal

#### 6.3.5.4.1 LED Short/Weak Short Detection

The LED short detection (LSD) function detects faults caused by a short circuit in any LED. This function was realized by comparing the OUTn voltage to the LSD threshold voltage. If the OUTn voltage is lower than the threshold voltage, the corresponding output LSD bit is set to 1 to indicate an short LED, otherwise, the output of that LSD bit is 0. LSD data output by the detection circuit are valid only during the OUTn turning on period.

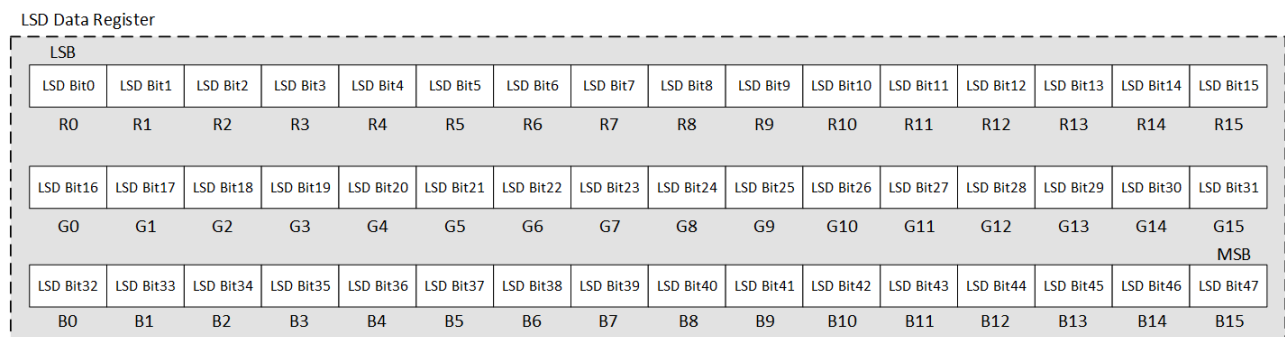
LSD weak short can be detected by adjusting threshold voltage, which level is set by LSDVTH\_R/LSDVTH\_G/LSDVTH\_B (See [FC3](#) for more details).

☒ 6-9 shows the equivalent circuit of LED short detection.



☒ 6-9. LED Short Detection Circuit

The LED short detection function records the position of the short LED, which contains the scan line order and relevant channel number. The scan line order is stored LSD\_LINE\_WARN register (see [FC19](#) for more details), and the channel number is latched into the internal 48-bit LSD data register (see [FC21](#) for more details) at the end of each segment. ☒ 6-10 shows the bit arrangement of the LSD data register.



☒ 6-10. Bit Arrangement in the LSD Data Register

### 6.3.5.4.2 Read LED Short Information

The LSD readback function must be enabled before reading LED Short information. This function is enabled by LOD\_LSD\_RB (see FC3 for more details).

Figure 6-11 shows the steps to read LED Short information. Wait at least one sub-period time between Step2 and Step3 command.

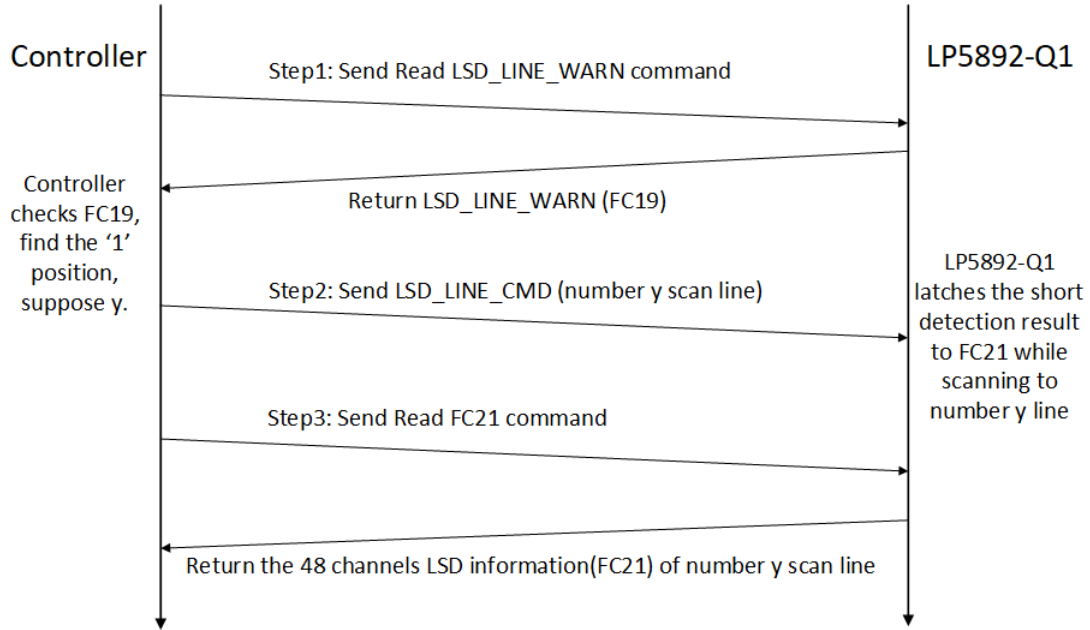
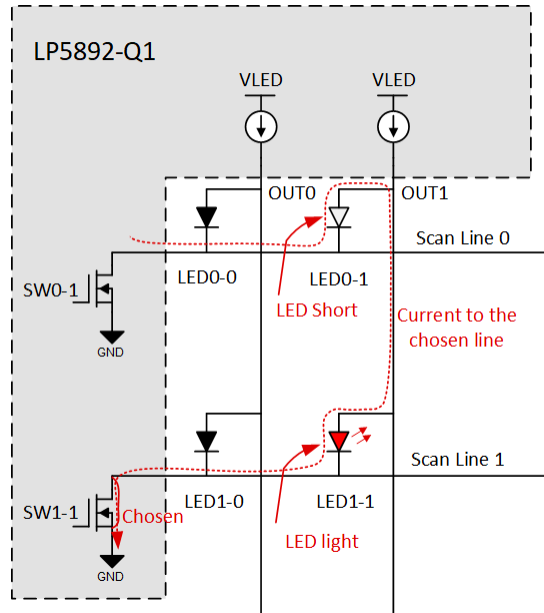


Figure 6-11. Steps to Read LED Short Information

**6.3.5.4.3 LSD Caterpillar Removal**

☒ 6-12 shows the LSD caterpillar issue caused by short LED. Suppose the LED0-1 is a short LED. When it scans to the line1 and the OUT1 is turned off, the OUT1 voltage is the same with scan line0 voltage because of the short path of the LED0-1. At this time, there is a current path from the line0 to the GND through the LED1-1 and SW1-1, which causes LED1-1 light unwanted.

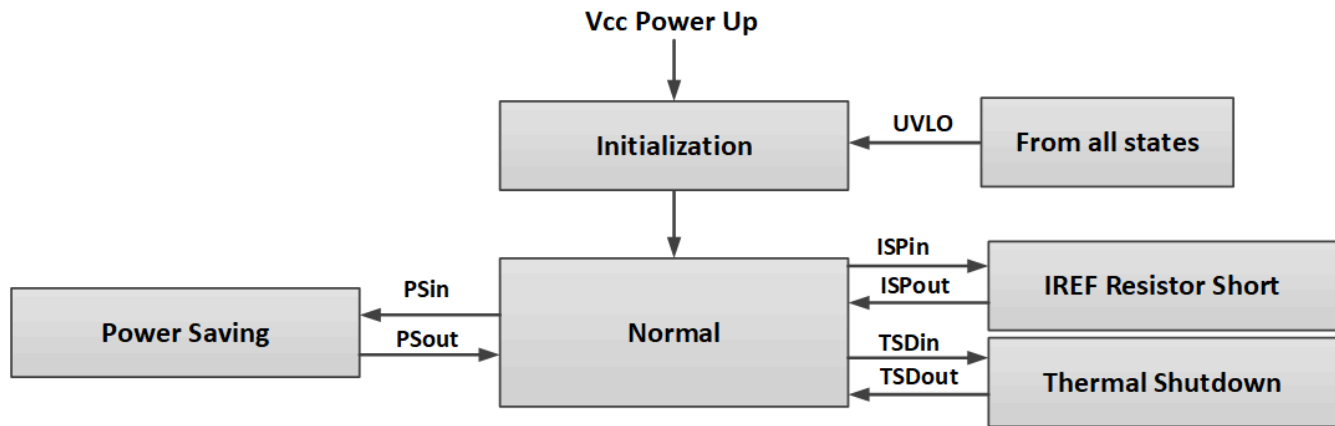


☒ 6-12. LED Short Caterpillar

The LP5892-Q1 device implements internal circuits that can eliminate the caterpillar issue by short LEDs. As is shown in ☒ 6-12, the LED short caterpillar is caused by the voltage of the Vclamp on the line. So it can be solved by adjusting the LSD\_RM\_EN (see FC3 for more details) to let the voltage drop of the LED1-1 be smaller than LED forward voltage.

## 6.4 Device Functional Modes

The device functional modes are shown in [Figure 6-13](#).



**Figure 6-13. Functional Modes**

- Initialization:** The device enters into Initialization when Vcc goes down to UVLO voltage. In this mode, all the registers are reset. Entry can also be from any state.
- Normal:** The device enters the normal mode when Vcc is higher than UVLO threshold. The display process is shown as below in normal mode.
- Power saving:** The device automatically enters and gets out from the power save mode when it detects the condition PSin and PSout. In this mode, all channels turn off. PSin: after the device detects that the display data of the next frame all equal to zero, it enters in to power save mode when the VSYNC comes. PSout: after the device detects that there is non-zero display data of the next frame, it gets out from power save mode immediately.
- IREF resistor short protection:** The device automatically enters and gets out from the IREF resistor short protection mode when it detects the condition ISPin and ISPout. In this mode, all channels turn off. ISPin: the device detects that the reference voltage is smaller than 0.195 V ISPout: the device detects that the reference voltage is larger than 0.325 V.
- Thermal shutdown:** The device automatically enters and gets out from the thermal shutdown mode when it detects the condition TSDin and TSDout. In this mode, all channels turn off. TSDin: the device detects that the junction temperature exceeds 170°C TSDout: the device detects that the junction temperature is below 155°C.

## 6.5 Continuous Clock Series Interface

The continuous clock series interface (CCSI) provides access to the programmable functions and registers, SRAM data of the device. The interface contains two input digital pins, they are the serial data input (SIN) and serial clock (SCLK). Moreover, there is an another wire called serial data output (SOUT) as the output digital signal of the device. The SIN is set to HIGH when device is in idle status and the SCLK must be existent and continuous all the time considering as the clock source of internal Frequency Multiplier, the SOUT is used to transmit the data or read the data of internal registers.

This protocol can support up to 32 devices cascaded in a data chain. The devices receive the chip index command after power up. The chip index command configured addresses of the devices from 0x00 up to 0x1F according to the sequence that receives the command. Then the controller can communicate with all the devices through the broadcast way or particular device through non-broadcast way.

The broadcast is mainly used to transmit function control commands. All the devices in a data chain receive the same data in this way. The non-broadcast is mainly used to transmit function control commands or display data, and each device receives its own data in this way. These two ways are distinguished by the command identification.

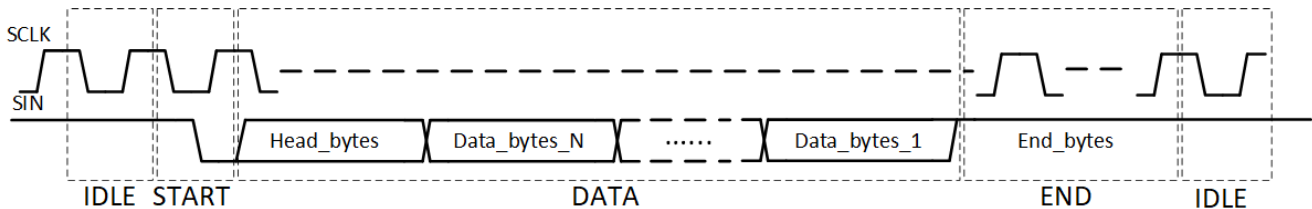
### 6.5.1 Data Validity

The data on DIN wire must be stable at rising edges of the SCLK in transmission.

### 6.5.2 CCSI Frame Format

☒ 6-14 defines the format of the command and data transmission. There are four states in one frame.

- **IDLE:** SCLK is always existent and continuous, and DIN is always HIGH.
- **START:** DIN changes from HIGH to LOW after the IDLE states.
- **DATA:**
  - **Head\_bytes:** It is the command identifier, contains one 16-bit data and one check bit. It can be WRITE COMMAND ID or READ COMMAND ID (see [Register Maps](#) for more details).
  - **Data\_bytes\_N:** The N<sup>th</sup> data-bytes, contains 3 × 17-bit data, each 17-bit data contains one 16-bit data and one check bit. N is the number of devices cascaded in a data chain.
- **END:** The device recognizes continuous 18-bit HIGH on DIN, then returns to IDLE state.
- **CHECK BIT:** The check bit (17<sup>th</sup> bit) value is the NOT of 16<sup>th</sup> bit value to avoid continuous 18-bit HIGH (to distinguish with END).



☒ 6-14. CCSI Frame

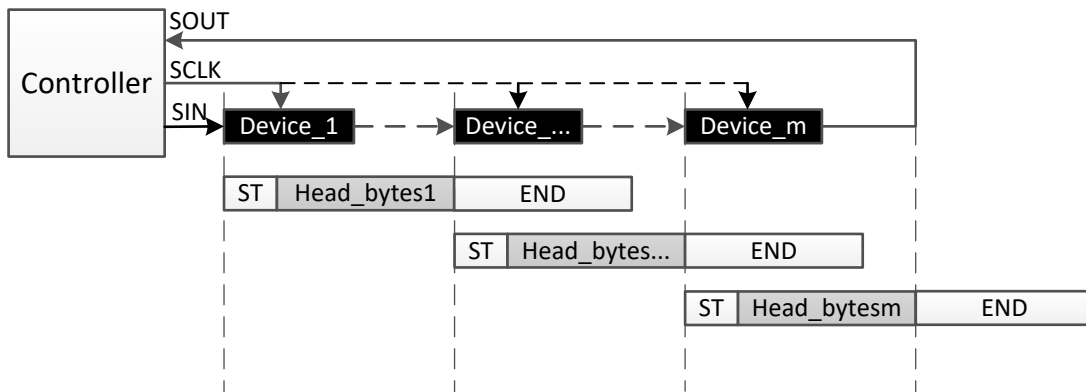
The IDLE state is not necessary, which means the START state of the next frame can connect to the END state of the current frame.

### 6.5.3 Write Command

Take m devices cascaded in a data chain for example.

#### 6.5.3.1 Chip Index Write Command

The chip index is used to set the identification of the device cascaded in a data chain. When the first device receives the chip index command Head\_bytes1, it sets the current address to 00h and meanwhile change the chip index command Head\_bytes2, then sends to the next device. When the device receives the Head\_bytes2, it sets the address to 01h and meanwhile changes the chip index command Head\_bytes3, then sends to the next device, likewise, all the cascaded devices get their unique identifications.



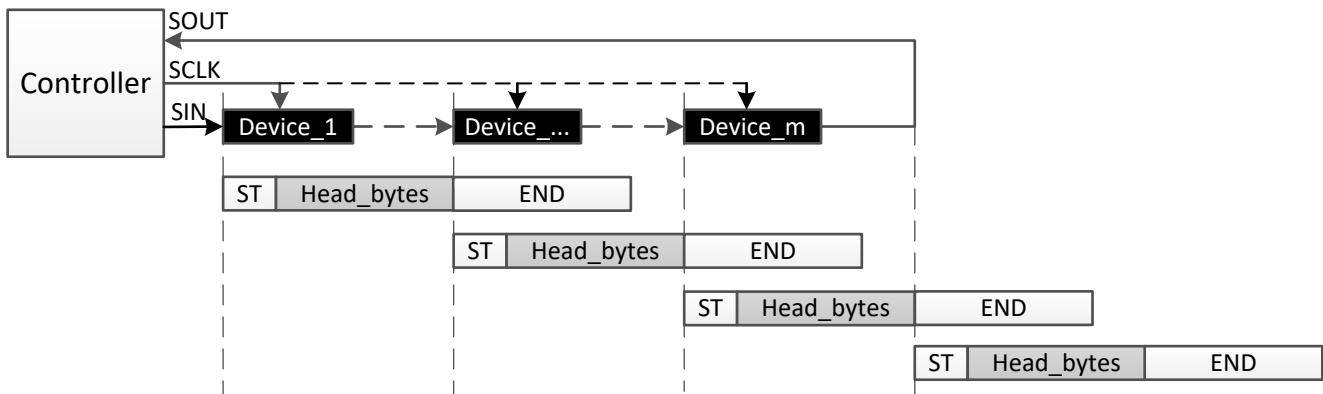
☒ 6-15. Chip Index Write Command

### 6.5.3.2 VSYNC Write Command

The VSYNC is used to sync the display of each frame for the devices in a cascaded chain. this command is a write-only command. The devices receive VSYNC command one time from the controller in each frame, and the VSYNC command needs to be active for all devices at the same time.

Because some devices receive the command earlier in the data chain, they need to wait until the last device receives the command, then all the devices are active at that time. To realize such function, each device needs to know its delay time from receiving VSYNC command to enabling VSYNC. The device uses some register bits to restore the device number in a data chain. This number minuses the device identification, and the result is the delay time of the device.

Because the sync function has been done by the device, the controller only must send the VSYNC command to the first device in a data chain.



☒ 6-16. VSYNC Write Command

### 6.5.3.3 MPSM Write Command

The MPSM command is used to control the intelligent power save mode of devices in the same matrix. The device detects all zero data in a stackable module and receives MPSM command in current frame, then when VSYNC command comes, all devices in the same matrix turn off. After the device detects that there is non-zero display data of the next frame, it gets out from intelligent power save mode until MSPM command comes in current frame.

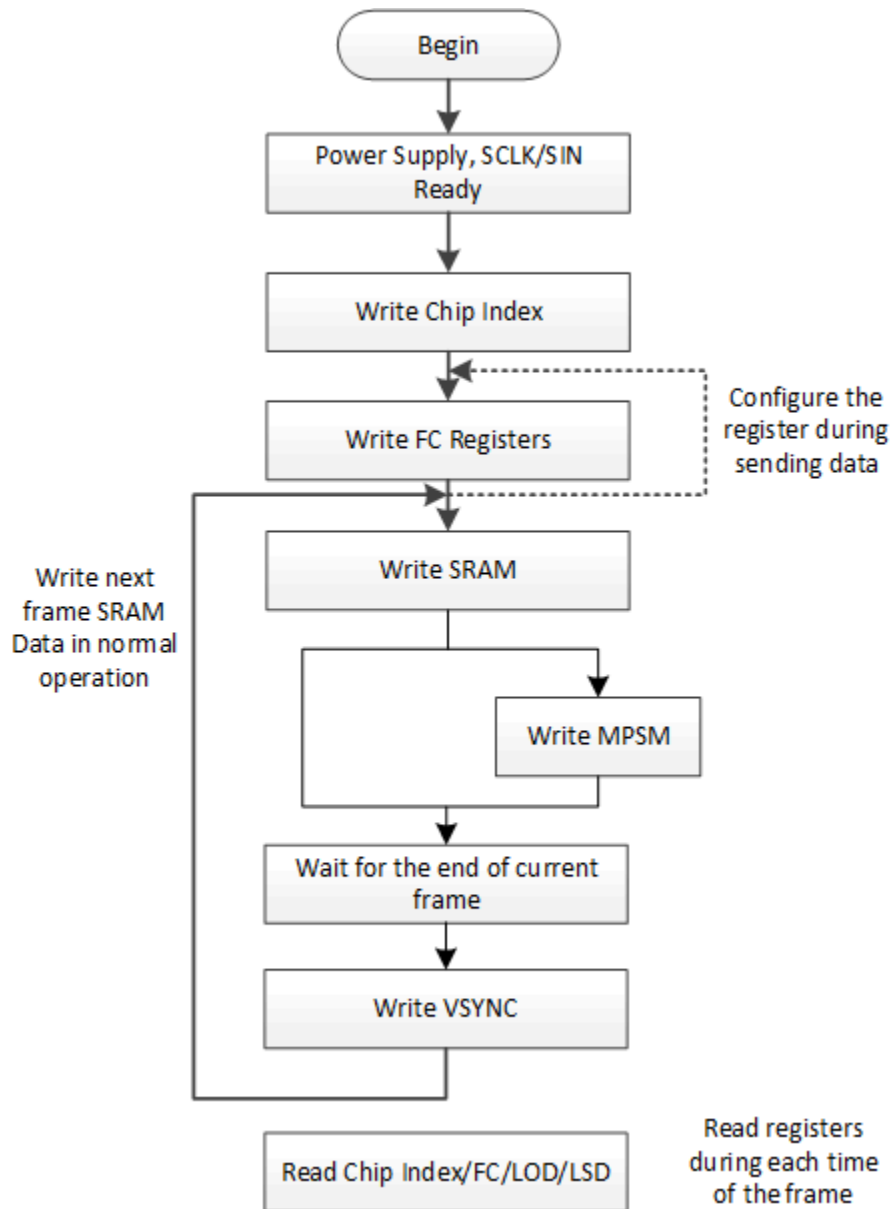


図 6-17. Design Procedure for MPSM Command

### 6.5.3.4 Standby Clear and Enable Command

Standby clear command and standby enable command are used to control intelligent power save mode of devices in the same daisy chain. When the device receives standby enable command, it enters to intelligent power save mode right away and does not have to wait for other devices in a module or daisy chain. After the device receives standby clear command, it exits from intelligent power save mode immediately and does not wait for other devices in a module or daisy chain.

### 6.5.3.5 Soft\_Reset Command

The Soft\_Reset Command is used to reset all the function registers to the default value, except for SRAM data. The format of this command is the same with VSYNC shown as [VSYNC Write Command](#). The difference is the headbytes.

### 6.5.3.6 Data Write Command

The device can receive the function control with broadcast and non-broadcast way, which depends on the configuration of the devices. If the cascaded devices have the same configuration, broadcast is used,. If the cascaded devices have the different configurations, non-broadcast is used. It is always the MSB transmitted first and the LSB transmitted last. For 48-bits RGB data, the Blue data must be transmitted first, then the Green, and last the Red data.

For broadcast, the devices receive the same data, when devices recognize the broadcast command, they copy the data to their internal registers. Generally, it is used for write FC0-FC13 command, LOD/LSD.

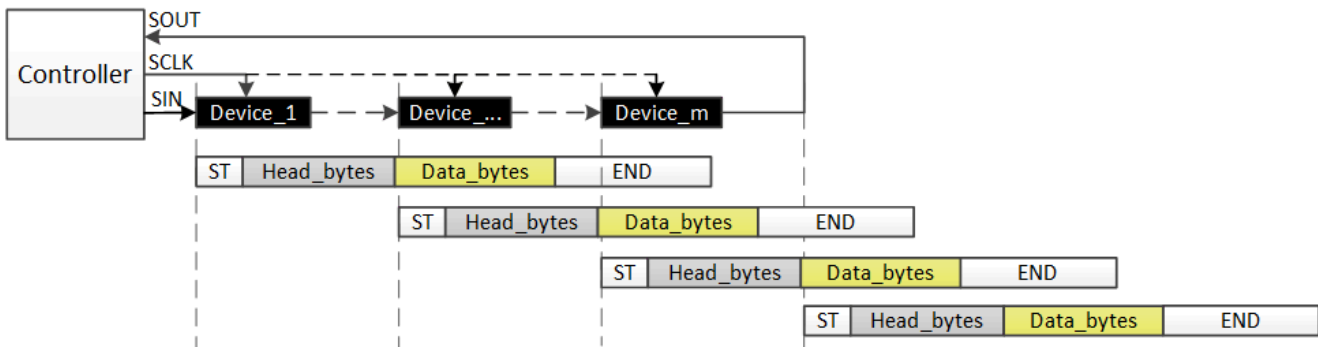


図 6-18. Data Write Command with Broadcast

図 6-19 shows the time diagram of the Data Write Command with Broadcast.

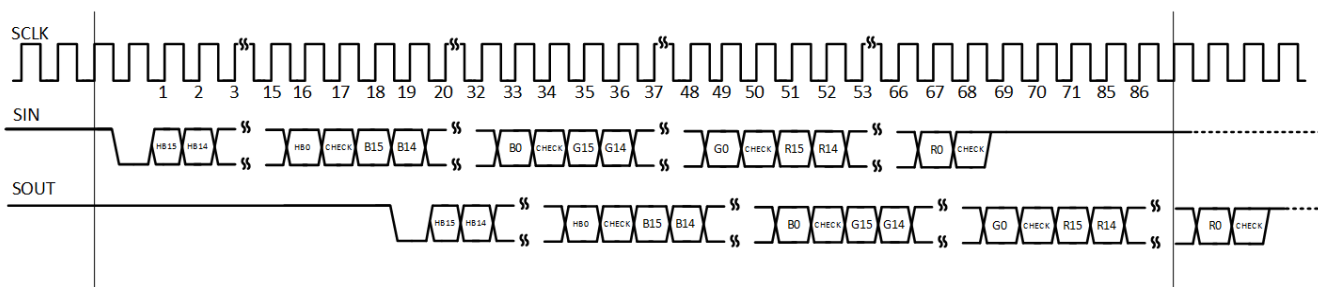


図 6-19. Data Write Command with Broadcast (Timing Diagram)



## 6.6 PWM Grayscale Control

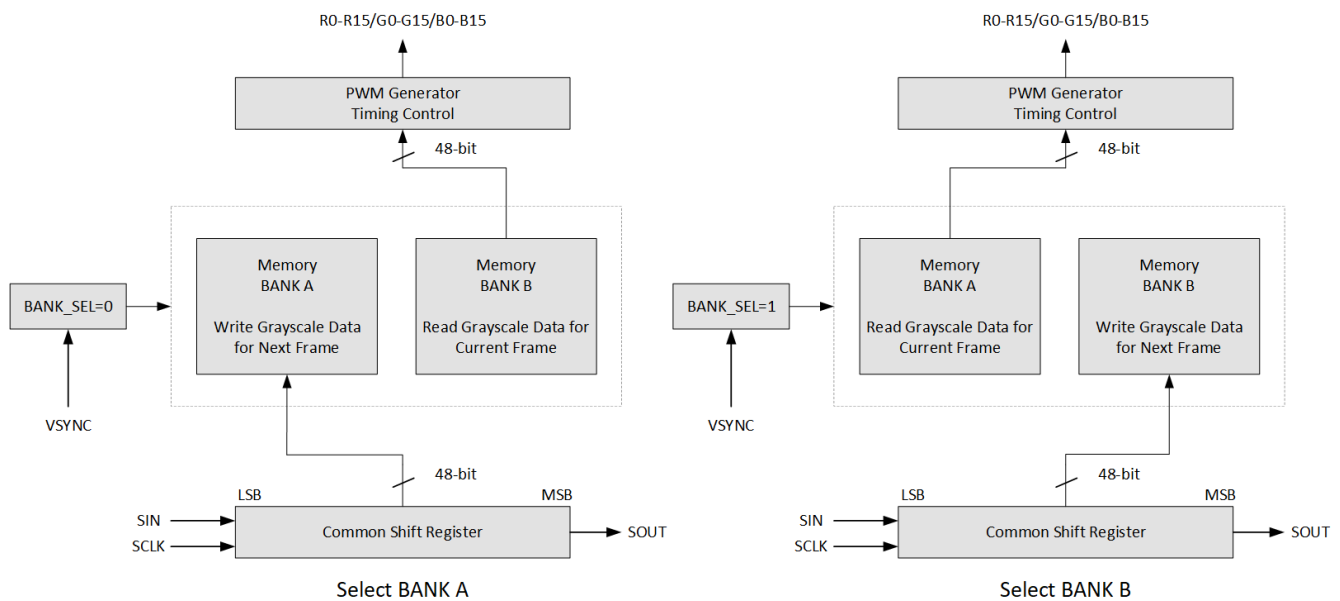
### 6.6.1 Grayscale Data Storage and Display

#### 6.6.1.1 Memory Structure Overview

The LP5892-Q1 implements a display memory unit to achieve high refresh rate and high contrast ratio in an LED display products. The internal display memory unit is divided into two BANKs: BANK A and BANK B. During the normal operation, one BANK is selected to display the data of current frame, another is used to restore the data of next frame. The BANK switcher is controlled by the BANK\_SEL bit, which is an internal flag register bit.

After power on, BANK\_SEL is initialized to 0, and BANK A is selected to restore the data of next frame. Meanwhile, the data in BANK B is read out for display. When one frame has elapsed, the controller sends the vertical synchronization (VSYNC) command to start the next frame, the BANK\_SEL bit value is toggled and the selection of the two BANKs reverses. Repeat this operation until all the frame images are displayed.

With this method, the LP5892-Q1 device can display the current frame image at a very high refresh rate. See [Figure 6-23](#) for more details about the BANK-selection exchange operation.



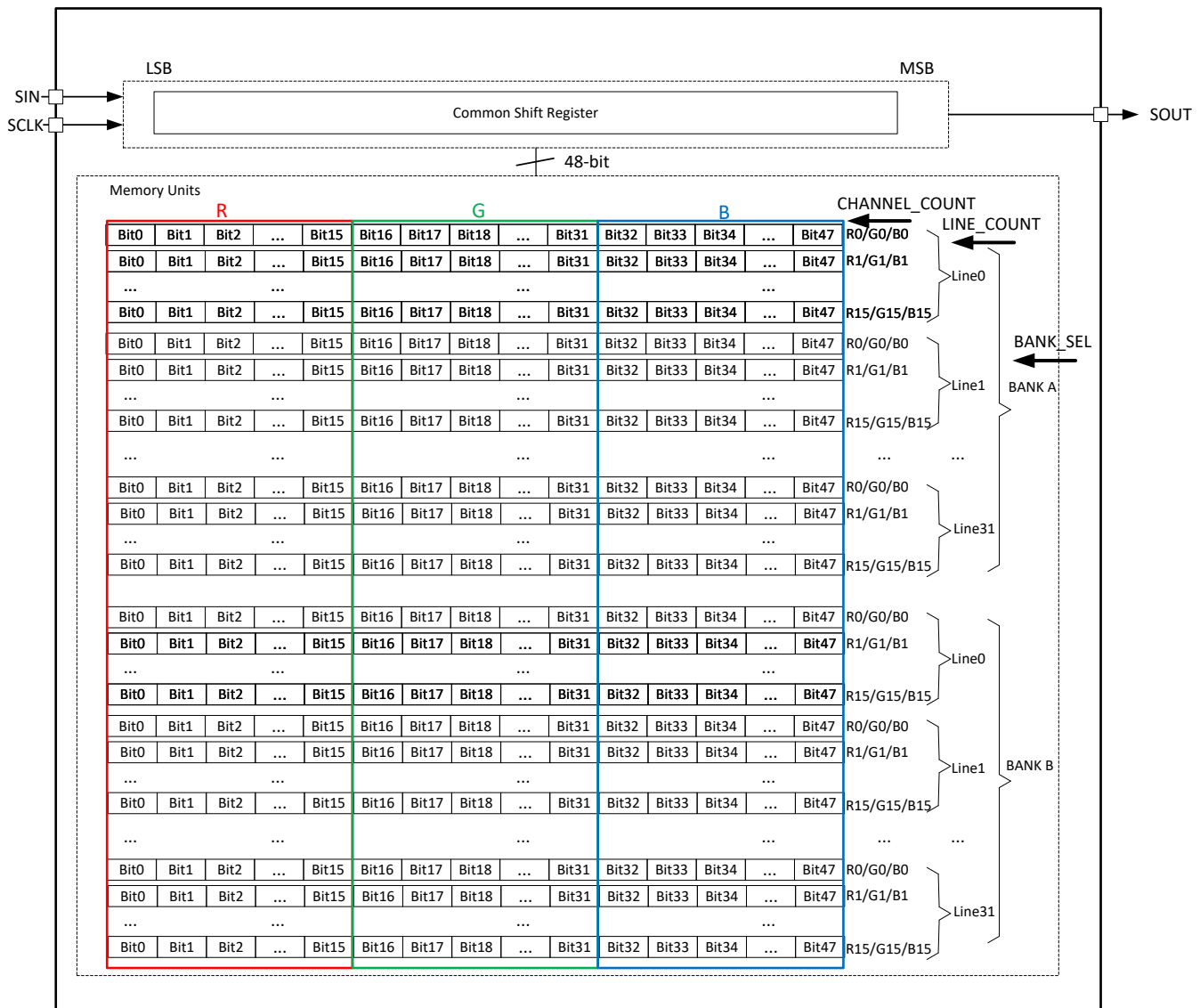
**Figure 6-23. Bank Selection Exchange Operation**

### 6.6.1.2 Details of Memory Bank

Each memory BANK contains the frame-image grayscale data of all the 32 lines. Each line comprises sixteen 48-bit-width memory units. Each memory unit contains the grayscale data of the corresponding R/G/B channels.

Depending on the number of scan lines set in SCAN\_NUM (FC0 bit 20 to bit 16), the total number of memory units that must be written in one BANK is: 48 × the number of scan lines. For example, if the number of scan lines is set to 32, then 1536 (32 × 48 = 1536) memory units must be written during each frame period.

☒ 6-24 shows the detailed memory structure of the LP5892-Q1 device.



☒ 6-24. LP5892-Q1 Memory-unit Structure

### 6.6.1.3 Write a Frame Data into Memory Bank

After power on, the LP5892-Q1 internal flag BANK\_SEL, and counters LINE\_COUNT, CHANNEL\_COUNT, are all initialized to 0. Thus, the memory unit of channel R0/G0/B0, locating in line 0 of BANK A, is selected to restore the data transmitted the first time after VSYNC command.

When the first WRTGS command is received, all the data in the common shift register is latched into the memory unit of channel R0/G0/B0, locating in line 0 of BANK A. Then CHANNEL\_COUNT increases by 1 and LINE\_COUNT stays the same. Thus, the memory unit of channel R1/G1/B1, locating in line 0 of BANK A, is selected to restore the data transmitted the second time after VSYNC command.

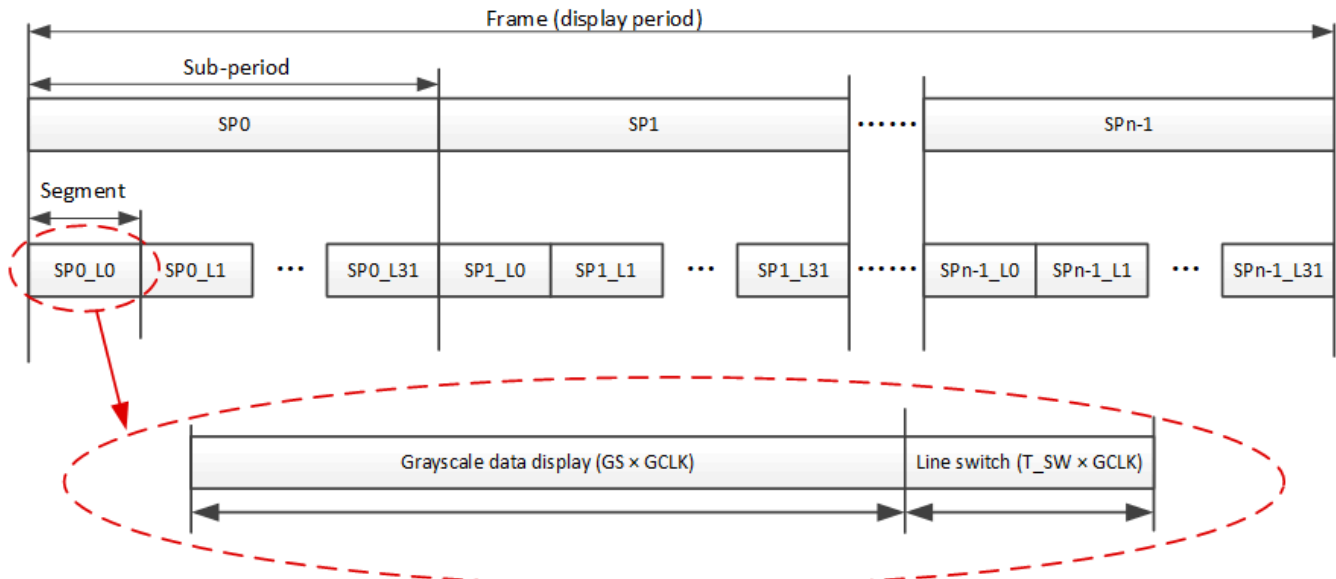
When the second WRTGS command is received, all the data in the common shift register is latched into the memory unit of channel R1/G1/B1, locating in line 0 of BANK A. Then CHANNEL\_COUNT increases by 1 and LINE\_COUNT stays the same. Thus, the memory unit of channel R2/G2/B2, locating in line 0 of BANK A, is selected to restore the data transmitted the third time after VSYNC command.

Repeat the grayscale-data-write operation until the 16<sup>th</sup> WRTGS command is received. Then CHANNEL\_COUNT is reset to 0 and LINE\_COUNT increases by 1. Thus, the memory unit of channel R0/G0/B0, locating in line 1 of BANK A, is selected to restore the data transmitted the 17<sup>th</sup> time after VSYNC command.

Repeat this operation for each line until the LINE\_COUNT exceeds the number of scan lines set in the SCAN\_NUM (See FC0 register bit20-16 ) and all scan lines have been updated with new GS data, which means one frame of GS data is restored into the memory BANK. Then the LINE\_COUNT is reset to 0.

### 6.6.2 PWM Control for Display

To increase the refresh rate in time-multiplexing display system, a DS-PWM (Dynamic Spectrum-Pulse Width Modulation) algorithm is proposed in this device. One frame is divided into many segments shown below. Note that one frame is divided into  $n$  sub-periods,  $n$  is set by SUBP\_NUM (FC0 register bit24-22), and each sub-period is divided into 32 segments for 32 scan lines. Each segment contains GS GCLKs time for grayscale data display and  $T_{SW}$  GCLKs time for switching lines. GS is configured by the SEG\_LENGTH (FC1 register bit9-0 in 表 6-8), and  $T_{SW}$  is the line switch time, which is configured by the LINE\_SWT (see FC1 register bit 40-37 in 表 6-8).



Note that, SP0: Sub-period 0, L0: Scan line 0

**图 6-25. DS-PWM Algorithm with 32 Scan Lines**

The DS-PWM can not only increase the refresh rate meanwhile keep the same frame rate, but also decrease the brightness loss in low grayscale, which can smoothly increase the sub-period number when the grayscale data increases.

To achieve ultra-low luminance, the LED driver must have the ability to output a very short current pulse (1 GCLK time), however, because of the parasitic capacitor of the LEDs, such pulse can not turn on the LEDs. The larger GCLK frequency is, the harder to turn on LEDs.

DS-PWM algorithm have a parameter called subperiod threshold, which is used to calculate when to change subperiod number according to the giving grayscale data. Subperiod threshold defines the LED minimum turn-on time, so as to conquer the current loss caused by LED parasitic capacitor. Subperiod threshold is configured by the LG\_STEP\_R/G/B (FC1 register bit24-10 in 表 6-8).

With DS-PWM algorithm, the brightness has smoothly increased with the gradient grayscale data.

## 6.7 Register Maps

表 6-5. Register Maps

| REGISTER NAME | TYPE         | WRITE COMMAND ID | READ COMMAND ID | DESCRIPTION                                       |
|---------------|--------------|------------------|-----------------|---|
| FC0           | R/ $\bar{W}$ | AA00h            | AA60h           | Common configuration                              |
| FC1           | R/ $\bar{W}$ | AA01h            | AA61h           | Common configuration                              |
| FC2           | R/ $\bar{W}$ | AA02h            | AA62h           | Common configuration                              |
| FC3           | R/ $\bar{W}$ | AA03h            | AA63h           | Common configuration                              |
| FC4           | R/ $\bar{W}$ | AA04h            | AA64h           | Common configuration                              |
| FC14          | R/ $\bar{W}$ | AA0Eh            | AA6Eh           | Locate the line for LOD                           |
| FC15          | R/ $\bar{W}$ | AA0Fh            | AA6Fh           | Locate the line for LSD                           |
| FC17          | R            |                  | AAA1h           | Read the lines' warning of LOD from 32th~1st line |
| FC19          | R            |                  | AAA3h           | Read the lines' warning of LSD from 32th~1st line |
| FC20          | R            |                  | AAA4h           | Read the channel's warning of LOD                 |
| FC21          | R            |                  | AAA5h           | Read the channel's warning of LSD                 |
| Chip Index    | R/ $\bar{W}$ | AA10h            | AA70h           | Read/Write chip index                             |
| VSYNC         | $\bar{W}$    | AAF0h            |                 | Write VSYNC command                               |
| MPSM          | $\bar{W}$    | AA90h            |                 | Write matrix PSM command                          |
| SBY_CLR       | $\bar{W}$    | AAB0h            |                 | Write standby clear command                       |
| SBY_EN        | $\bar{W}$    | AAB1h            |                 | Write standby enable command                      |
| Soft_Reset    | $\bar{W}$    | AA80h            |                 | Reset the all the registers expect the SRAM       |
| SRAM          | $\bar{W}$    | AA30h            |                 | Write or read the SRAM data                       |

表 6-6. Access Type Codes

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Write Type             |      |  |
| W                      | W    | Write                                  |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 6.7.1 FC0

FC0 is shown in [FC0 Register](#) and described in [FC0 Register Field Descriptions](#).

図 6-26. FC0 Register

|               |          |    |              |          |    |           |          |    |           |              |           |          |    |              |    |
|---------------|----------|----|--------------|----------|----|-----------|----------|----|-----------|--------------|-----------|----------|----|--------------|----|
| 47            | 46       | 45 | 44           | 43       | 42 | 41        | 40       | 39 | 38        | 37           | 36        | 35       | 34 | 33           | 32 |
| LSD_R<br>M_EN | RESERVED |    | GRP_DLY_B    |          |    | GRP_DLY_G |          |    | GRP_DLY_R |              |           | RESERVED |    | FREQ_<br>MUL |    |
| R/<br>W-0b    | R-01b    |    | R/W-000b     |          |    | R/W-000b  |          |    | R/W-000b  |              |           | R-000b   |    |              |    |
| 31            | 30       | 29 | 28           | 27       | 26 | 25        | 24       | 23 | 22        | 21           | 20        | 19       | 18 | 17           | 16 |
| FREQ_MUL      |          |    | FREQ_<br>MOD | RESERVED |    |           | SUBP_NUM |    |           | RESE<br>RVED | SCAN_NUM  |          |    |              |    |
| R/W-0111b     |          |    | R/<br>W-0b   | R-000b   |    |           | R/W-000b |    |           | R-0b         | R/W-00000 |          |    |              |    |
| 15            | 14       | 13 | 12           | 11       | 10 | 9         | 8        | 7  | 6         | 5            | 4         | 3        | 2  | 1            | 0  |

図 6-26. FC0 Register (続き)

|              |         |            |          |            |          |            |
|--------------|---------|------------|----------|------------|----------|------------|
| LODR<br>M_EN | PSP_MOD | PS_EN      | RESERVED | PDC_E<br>N | RESERVED | CHIP_NUM   |
| R/<br>W-0b   | R/W-00b | R/<br>W-0b | R-000b   | R/<br>W-1b | R-000b   | R/W-00111b |

表 6-7. FC0 Register Field Descriptions

| Bit   | Field    | Type | Reset  | Description   |
|-------|----------|------|--------|---|
| 4-0   | CHIP_NUM | R/W  | 00111b | Set the device number<br>00000b: 1 device<br>...<br>01111b: 16 devices<br>...<br>11111b: 32 devices   |
| 7-5   | RESERVED | R    | 000b   |   |
| 8     | PDC_EN   | R/W  | 1b     | Enable or disable pre-discharge function<br>0b: disable<br>1b: enable   |
| 11-9  | RESERVED | R    | 000b   |   |
| 12    | PS_EN    | R/W  | 0b     | Enable or disable the power saving mode<br>0b: disable<br>1b: enable  |
| 14-13 | PSP_MOD  | R/W  | 00b    | Set the powering saving plus mode<br>00b: disable<br>01b: save power at high level<br>10b: save power at middle level<br>11b: save power at low level |
| 15    | LODRM_EN | R/W  | 0b     | Enable or disable the LED open load removal function<br>0b: disable<br>1b: enable   |
| 20-16 | SCAN_NUM | R/W  | 00000b | Set the scan line number<br>00000b: 1 line<br>...<br>01111b: 16 lines<br>...<br>11111b: 32 lines  |
| 21    | RESERVED | R    | 0b     |   |
| 24-22 | SUBP_NUM | R/W  | 000b   | Set the subperiod number<br>000b: 16<br>001b: 32<br>010b: 48<br>011b: 64<br>100b: 80<br>101b: 96<br>110b: 112<br>111b: 128                            |
| 27-25 | RESERVED | R    | 000b   |   |
| 28    | FREQ_MOD | R/W  | 0b     | Set the GCLK multiplier mode<br>0b: high frequency mode, 80MHz to 160MHz<br>1b: low frequency mode, 40MHz to 80MHz                                    |
| 32-29 | FREQ_MUL | R/W  | 0111b  | Set the GCLK multiplier frequency<br>0000b: 1 x SCLK frequency<br>...<br>0111b: 8 x SCLK frequency<br>...<br>1111b: 16 x SCLK frequency               |
| 35-33 | RESERVED | R    | 000b   |   |

**表 6-7. FC0 Register Field Descriptions (続き)**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 38-36 | GRP_DLY_R | R/W  | 000b  | Set the Red group delay, forward PWM mode only<br>000b: no delay<br>001b: 1 GCLK<br>010b: 2 GCLK<br>011b: 3 GCLK<br>100b: 4 GCLK<br>101b: 5 GCLK<br>110b: 6 GCLK<br>111b: 7 GCLK   |
| 41-39 | GRP_DLY_G | R/W  | 000b  | Set the Green group delay, forward PWM mode only<br>000b: no delay<br>001b: 1 GCLK<br>010b: 2 GCLK<br>011b: 3 GCLK<br>100b: 4 GCLK<br>101b: 5 GCLK<br>110b: 6 GCLK<br>111b: 7 GCLK |
| 44-42 | GRP_DLY_B | R/W  | 000b  | Set the Blue group delay, forward PWM mode only<br>000b: no delay<br>001b: 1 GCLK<br>010b: 2 GCLK<br>011b: 3 GCLK<br>100b: 4 GCLK<br>101b: 5 GCLK<br>110b: 6 GCLK<br>111b: 7 GCLK  |
| 46-45 | RESERVED  | R    | 01b   |  |
| 47    | LSD_RM_EN | R/W  | 0b    | Enable or disable short LED caterpillar<br>0b: disable<br>1b: enable   |

6.7.2 FC1

FC1 is shown in [FC1 Register](#) and described in [FC1 Register Field Descriptions](#).

図 6-27. FC1 Register

|               |             |    |           |    |    |    |                    |    |    |    |            |    |    |    |              |
|---------------|-------------|----|-----------|----|----|----|--------------------|----|----|----|------------|----|----|----|--------------|
| 47            | 46          | 45 | 44        | 43 | 42 | 41 | 40                 | 39 | 38 | 37 | 36         | 35 | 34 | 33 | 32           |
| RESE<br>RVED  | BLK_ADJ     |    |           |    |    |    | LINE_SWT           |    |    |    | LG_ENH_B   |    |    |    | LG_EN<br>H_G |
| R-0b          | R/W-000000b |    |           |    |    |    | R/W-0111b          |    |    |    | R/W-0000b  |    |    |    |              |
| 31            | 30          | 29 | 28        | 27 | 26 | 25 | 24                 | 23 | 22 | 21 | 20         | 19 | 18 | 17 | 16           |
| LG_ENH_G      |             |    | LG_ENH_R  |    |    |    | LG_STEP_B          |    |    |    | LG_STEP_G  |    |    |    |              |
| R/W-0000b     |             |    | R/W-0000b |    |    |    | R/W-01001b         |    |    |    | R/W-01001b |    |    |    |              |
| 15            | 14          | 13 | 12        | 11 | 10 | 9  | 8                  | 7  | 6  | 5  | 4          | 3  | 2  | 1  | 0            |
| LG_ST<br>EP_G | LG_STEP_R   |    |           |    |    |    | SEG_LENGTH         |    |    |    |            |    |    |    |              |
|               | R/W-01001b  |    |           |    |    |    | R/W-0'000'000'000b |    |    |    |            |    |    |    |              |

表 6-8. FC1 Register Field Descriptions

| Bit   | Field      | Type | Reset          | Description   |
|-------|------------|------|----------------|---|
| 9-0   | SEG_LENGTH | R/W  | 0'000'000'000b | Set the GCLK number in each segment<br>127d: 128 GCLK<br>...<br>1023d: 1024 GCLK<br>others: 128 GCLK                          |
| 14-10 | LG_STEP_R  | R/W  | 01001b         | Adjust the smooth of the brightness in low grayscale<br>00000b: level 1<br>...<br>01111b: level 16<br>...<br>11111b: level 32 |
| 19-15 | LG_STEP_G  | R/W  | 01001b         | Adjust the smooth of the brightness in low grayscale<br>00000b: level 1<br>...<br>01111b: level 16<br>...<br>11111b: level 32 |
| 24-20 | LG_STEP_B  | R/W  | 01001b         | Adjust the smooth of the brightness in low grayscale<br>00000b: level 1<br>...<br>01111b: level 16<br>...<br>11111b: level 32 |
| 28-25 | LG_ENH_R   | R/W  | 0000b          | Adjust low grayscale enhancement of red channels<br>0000b: level 0<br>...<br>0111b: level 7<br>...<br>1111b: level 15         |
| 32-29 | LG_ENH_G   | R/W  | 0000b          | Adjust low grayscale enhancement of green channels<br>0000b: level 0<br>...<br>0111b: level 7<br>...<br>1111b: level 15       |

表 6-8. FC1 Register Field Descriptions (続き)

| Bit   | Field    | Type | Reset   | Description   |
|-------|----------|------|---------|---|
| 36-33 | LG_ENH_B | R/W  | 0000b   | Adjust low grayscale enhancement of blue channels<br>0000b: level 0<br>...<br>0111b: level 7<br>...<br>1111b: level 15      |
| 40-37 | LINE_SWT | R/W  | 0111b   | Set the scan line switch time.<br>0000b: 45 GCLK<br>0001b: 2x30 GCLK<br>...<br>0111b: 8x30 GCLK<br>...<br>1111b: 16x30 GCLK |
| 46-41 | BLK_ADJ  | R/W  | 000000b | Set the black field adjustment<br>000000b: 0 GCLK<br>...<br>011111b: 31 GCLK<br>...<br>111111b: 63 GCLK                     |
| 47    | RESERVED | R    | 0b      | Reserved bit.   |

### 6.7.3 FC2

FC2 is shown in [FC2 Register](#) and described in [FC2 Register Field Descriptions](#).

図 6-28. FC2 Register

| 47           | 46       | 45 | 44 | 43         | 42           | 41            | 40            | 39            | 38       | 37 | 36 | 35           | 34 | 33 | 32 |
|--------------|----------|----|----|------------|--------------|---------------|---------------|---------------|----------|----|----|--------------|----|----|----|
| MPSM_EN      | RESERVED |    |    | MOD_SIZE   | SUBP_MAX_256 | CH_B_IMMUNITY | CH_G_IMMUNITY | CH_R_IMMUNITY | RESERVED |    |    | LG_COLOR_B   |    |    |    |
| R/W-0b       | R-000b   |    |    | R/W-0b     | R/W-0b       | R/W-1b        | R/W-1b        | R/W-1b        | R-000b   |    |    | R/W-0000b    |    |    |    |
| 31           | 30       | 29 | 28 | 27         | 26           | 25            | 24            | 23            | 22       | 21 | 20 | 19           | 18 | 17 | 16 |
| LG_COLOR_G   |          |    |    | LG_COLOR_R |              |               |               | DE_COUPLE1_B  |          |    |    | DE_COUPLE1_G |    |    |    |
| R/W-0000b    |          |    |    | R/W-0000b  |              |               |               | R/W-0000b     |          |    |    | R/W-0000b    |    |    |    |
| 15           | 14       | 13 | 12 | 11         | 10           | 9             | 8             | 7             | 6        | 5  | 4  | 3            | 2  | 1  | 0  |
| DE_COUPLE1_R |          |    |    | V_PDC_B    |              |               |               | V_PDC_G       |          |    |    | V_PDC_R      |    |    |    |
| R/W-0000b    |          |    |    | R/W-0110b  |              |               |               | R/W-0110b     |          |    |    | R/W-0110b    |    |    |    |

表 6-9. FC2 Register Field Descriptions

| Bit   | Field        | Type | Reset | Description   |
|-------|--------------|------|-------|---|
| 3-0   | V_PDC_R      | R/W  | 0110b | Set the Red pre_discharge voltage (typical), the voltage value must not be higher than (VR-1.3V).<br>0000b: 0.1V<br>0001b: 0.2V<br>0010b: 0.3V<br>0011b: 0.4V<br>0100b: 0.5V<br>0101b: 0.6V<br>0110b: 0.7V<br>0111b: 0.8V<br>1000b: 0.9V<br>1001b: 1.0V<br>1010b: 1.1V<br>1011b: 1.3V<br>1100b: 1.5V<br>1101b: 1.7V<br>1110b: 1.9V<br>1111b: 2.1V   |
| 7-4   | V_PDC_G      | R/W  | 0110b | Set the Green pre_discharge voltage (typical), the voltage value must not be higher than (VG-1.3V).<br>0000b: 0.1V<br>0001b: 0.2V<br>0010b: 0.3V<br>0011b: 0.4V<br>0100b: 0.5V<br>0101b: 0.6V<br>0110b: 0.7V<br>0111b: 0.8V<br>1000b: 0.9V<br>1001b: 1.0V<br>1010b: 1.1V<br>1011b: 1.3V<br>1100b: 1.5V<br>1101b: 1.7V<br>1110b: 1.9V<br>1111b: 2.1V |
| 11-8  | V_PDC_B      | R/W  | 0110b | Set the Blue pre_discharge voltage (typical), the voltage value must not be higher than (VB-1.3V).<br>0000b: 0.1V<br>0001b: 0.2V<br>0010b: 0.3V<br>0011b: 0.4V<br>0100b: 0.5V<br>0101b: 0.6V<br>0110b: 0.7V<br>0111b: 0.8V<br>1000b: 0.9V<br>1001b: 1.0V<br>1010b: 1.1V<br>1011b: 1.3V<br>1100b: 1.5V<br>1101b: 1.7V<br>1110b: 1.9V<br>1111b: 2.1V  |
| 15-12 | DE_COUPLE1_R | R/W  | 0000b | Set the Red decoupling level<br>0000b: level 1 (lowest)<br>...<br>0111b: level 8 (middle)<br>...<br>1111b: level 16(highest)  |

表 6-9. FC2 Register Field Descriptions (続き)

| Bit       | Field         | Type | Reset | Description  |
|-----------|---------------|------|-------|--|
| 19-16     | DE_COUPLE1_G  | R/W  | 0000b | Set the Green decoupling level<br>0000b: level 1 (lowest)<br>...<br>0111b: level 8 (middle)<br>...<br>1111b: level 16(highest)                                 |
| 23-20     | DE_COUPLE1_B  | R/W  | 0000b | Set the Blue decoupling level<br>0000b: level 1 (lowest)<br>...<br>0111b: level 8 (middle)<br>...<br>1111b: level 16(highest)                                  |
| 27-24     | LG_COLOR_R    | R/W  | 0000b | Set the Red brightness compensation level of the low grayscale<br>0000b: level 1 (lowest)<br>...<br>0111b: level 8 (middle)<br>...<br>1111b: level 16(highest) |
| 31-28     | LG_COLOR_G    | R/W  | 0000b | Set the Red brightness compensation level of the low grayscale<br>0000b: level 1 (lowest)<br>...<br>0111b: level 8 (middle)<br>...<br>1111b: level 16(highest) |
| 35-32     | LG_COLOR_B    | R/W  | 0000b | Set the Red brightness compensation level of the low grayscale<br>0000b: level 1 (lowest)<br>...<br>0111b: level 8 (middle)<br>...<br>1111b: level 16(highest) |
| 38-36     | RESERVED      | R    | 000b  |  |
| 39        | CH_R_IMMUNITY | R/W  | 1b    | Set the immunity of the Red channels group<br>0b: high immunity<br>1b: low immunity  |
| 40        | CH_G_IMMUNITY | R/W  | 1b    | Set the immunity of the Green channels group<br>0b: high immunity<br>1b: low immunity  |
| 41        | CH_B_IMMUNITY | R/W  | 1b    | Set the immunity of the Blue channels group<br>0b: high immunity<br>1b: low immunity   |
| 42        | SUBP_MAX_256  | R/W  | 0b    | Set the maximum subperiod to 256.<br>0b: disable<br>1b: enable   |
| 43        | MOD_SIZE      | R/W  | 0b    | Set the module size.<br>0b: 16x16 RGB pixels<br>1b:32x32 RGB pixels  |
| 46<br>-44 | RESERVED      | R    | 000b  |  |
| 47        | MPSM_EN       | R/W  | 0b    | Enable or disable matrix power saving mode.<br>0b: disable<br>1b: enable   |

### 6.7.4 FC3

FC3 is shown in [FC3 Register](#) and described in [FC3 Register Field Descriptions](#).

図 6-29. FC3 Register

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

図 6-29. FC3 Register (続き)

|                |    |    |          |    |    |                |    |                |              |          |    |          |          |          |    |
|----------------|----|----|----------|----|----|----------------|----|----------------|--------------|----------|----|----------|----------|----------|----|
| LSDVTH_B       |    |    | LSDVTH_G |    |    | LSDVTH_R       |    |                | LSD_RM       |          |    |          | BC       |          |    |
| R/W-000b       |    |    | R/W-000b |    |    | R/W-000b       |    |                | R/W-0111b    |          |    |          | R/W-011b |          |    |
| 31             | 30 | 29 | 28       | 27 | 26 | 25             | 24 | 23             | 22           | 21       | 20 | 19       | 18       | 17       | 16 |
| CC_B           |    |    |          |    |    | CC_G           |    |                |              |          |    |          |          |          |    |
| R/W-0111 1111b |    |    |          |    |    | R/W-0111 1111b |    |                |              |          |    |          |          |          |    |
| 15             | 14 | 13 | 12       | 11 | 10 | 9              | 8  | 7              | 6            | 5        | 4  | 3        | 2        | 1        | 0  |
| CC_R           |    |    |          |    |    |                |    | LOD_L<br>SD_RB | RESE<br>RVED | LODVTH_B |    | LODVTH_G |          | LODVTH_R |    |
| R/W-0111 1111b |    |    |          |    |    |                |    | R/<br>W-0b     | R-0b         | R/W-00b  |    | R/W-00b  |          | R/W-00b  |    |

表 6-10. FC3 Register Field Descriptions

| Bit   | Field      | Type | Reset      | Description   |
|-------|------------|------|------------|---|
| 1-0   | LODVTH_R   | R/W  | 00b        | Set the Red LED open load detection threshold<br>00b: (V <sub>LEDR</sub> -0.2) V<br>01b: (V <sub>LEDR</sub> -0.5) V<br>10b: (V <sub>LEDR</sub> -0.9) V<br>11b: (V <sub>LEDR</sub> -1.2) V   |
| 3-2   | LODVTH_G   | R/W  | 00b        | Set the Green LED open load detection threshold<br>00b: (V <sub>LEDG</sub> -0.2) V<br>01b: (V <sub>LEDG</sub> -0.5) V<br>10b: (V <sub>LEDG</sub> -0.9) V<br>11b: (V <sub>LEDG</sub> -1.2) V |
| 5-4   | LODVTH_B   | R/W  | 00b        | Set the Blue LED open load detection threshold<br>00b: (V <sub>LEDB</sub> -0.2) V<br>01b: (V <sub>LEDB</sub> -0.5) V<br>10b: (V <sub>LEDB</sub> -0.9) V<br>11b: (V <sub>LEDB</sub> -1.2) V  |
| 6     | RESERVED   | R    | 0b         |   |
| 7     | LOD_LSD_RB | R/W  | 0b         | Enable or disable the LOD and LSD readback function<br>0b: disabled<br>01b: enabled   |
| 15-8  | CC_R       | R/W  | 0111 1111b | Set the Red color brightness level<br>0000 0000b: level 0 (lowest)<br>...<br>0111 1111b: level 127 (middle)<br>...<br>1111 1111b: level 255 (highest)                                       |
| 23-16 | CC_G       | R/W  | 0111 1111b | Set the Green color brightness level<br>0000 0000b: level 0 (lowest)<br>...<br>0111 1111b: level 127 (middle)<br>...<br>1111 1111b: level 255 (highest)                                     |
| 31-24 | CC_B       | R/W  | 0111 1111b | Set the Blue color brightness level<br>0000 0000b: level 0 (lowest)<br>...<br>0111 1111b: level 127 (middle)<br>...<br>1111 1111b: level 255 (highest)                                      |
| 34-32 | BC         | R/W  | 011b       | Set the global brightness level<br>000b: level 0 (lowest)<br>...<br>011b: level 3 (middle)<br>...<br>111b: level 7 (highest)  |

表 6-10. FC3 Register Field Descriptions (続き)

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 38-35 | LSD_RM   | R/W  | 0111b | Set the LED short removal level<br>0000b: level 1<br>0001b: level 2<br>0010b: level 3<br>0011b: level 4<br>0100b: level 5<br>0101b: level 6<br>0110b: level 7<br>0111b: level 8<br>1000b: level 9<br>1001b: level 10<br>1010b: level 11<br>1011b: level 12<br>1100b: level 13<br>1101b: level 14<br>1110b: level 15<br>1111b: level 16 |
| 41-39 | LSDVTH_R | R/W  | 000b  | Set the Red LED short/weak short circuitry detection threshold (typical)<br>000b: 0.2 V<br>001b: 0.4 V<br>010b: 0.8 V<br>011b: 1.0 V<br>100b: 1.2 V<br>101b: 1.4 V<br>110b: 1.6 V<br>111b: 1.8 V   |
| 44-42 | LSDVTH_G | R/W  | 000b  | Set the Green LED short/weak short circuitry detection threshold (typical)<br>000b: 0.2 V<br>001b: 0.4 V<br>010b: 0.8 V<br>011b: 1.2 V<br>100b: 1.6 V<br>101b: 2 V<br>110b: 2.4 V<br>111b: 2.8 V   |
| 47-45 | LSDVTH_B | R/W  | 000b  | Set the Blue LED short/weak short circuitry detection threshold (typical)<br>000b: 0.2 V<br>001b: 0.4 V<br>010b: 0.8 V<br>011b: 1.2 V<br>100b: 1.6 V<br>101b: 2 V<br>110b: 2.4 V<br>111b: 2.8 V  |

### 6.7.5 FC4

FC4 is shown in [FC4 Register](#) and described in [FC4 Register Field Descriptions](#).

図 6-30. FC4 Register

|          |    |    |               |            |    |         |    |            |                |          |          |          |          |          |          |
|----------|----|----|---------------|------------|----|---------|----|------------|----------------|----------|----------|----------|----------|----------|----------|
| 47       | 46 | 45 | 44            | 43         | 42 | 41      | 40 | 39         | 38             | 37       | 36       | 35       | 34       | 33       | 32       |
| RESERVED |    |    | DE_COUPLE3_EN | DE_COUPLE3 |    |         |    | DE_COUPLE2 | FIRST_LINE_DIM |          |          |          | CAURSE_B | CAURSE_G | CAURSE_R |
| R-000b   |    |    | R/W-0b        | R/W-1000b  |    |         |    | R/W-0b     | R/W-0000b      |          |          |          | R/W-0b   | R/W-0b   | R/W-0b   |
| 31       | 30 | 29 | 28            | 27         | 26 | 25      | 24 | 23         | 22             | 21       | 20       | 19       | 18       | 17       | 16       |
| RESERVED |    |    |               | SR_ON_B    |    | SR_ON_G |    | SR_ON_R    |                | SR_OFF_B | SR_OFF_G | SR_OFF_R | FINE_B   | FINE_G   | FINE_R   |
| R-0000b  |    |    |               | R/W-01b    |    | R/W-01b |    | R/W-01b    |                | R/W-0b   | R/W-0b   | R/W-0b   | R/W-0b   | R/W-0b   | R/W-0b   |
| 15       | 14 | 13 | 12            | 11         | 10 | 9       | 8  | 7          | 6              | 5        | 4        | 3        | 2        | 1        | 0        |

図 6-30. FC4 Register (続き)

|          |          |                   |        |          |
|----------|----------|-------------------|--------|----------|
| RESERVED | SCAN_REV | RESERVED          | IMAX   | RESERVED |
| R-0b     | R/W-1b   | R-0000 0000 1111b | R/W-0b | R-0b     |

表 6-11. FC4 Register Field Descriptions

| Bit   | Field    | Type | Reset              | Description  |
|-------|----------|------|--------------------|--|
| 0     | RESERVED | R    | 0b                 |  |
| 1     | IMAX     | R/W  | 0b                 | Set the maximum current of each channel<br>0b: 10mA maximum<br>01b: 40 mA maximum  |
| 13-2  | RESERVED | R    | 0000 0000<br>1111b |  |
| 14    | SCAN_REV | R/W  | 1b                 | When 2 device stackable, the scan lines PCB layout is reversed. For the proper scan and SRAM read sequence, SCAN_REV register is provided.<br>0b: the PCB layout sequence is L0-L15, L16-L31.<br>1b: the PCB layout sequence is L0-L15, L31-L16. |
| 15    | RESERVED | R    | 0b                 |  |
| 16    | FINE_R   | R/W  | 0b                 | Enable the Red brightness compensation level fine range<br>0b: disable<br>1b: enable   |
| 17    | FINE_G   | R/W  | 0b                 | Enable the Green brightness compensation level fine range<br>0b: disable<br>1b: enable   |
| 18    | FINE_B   | R/W  | 0b                 | Enable the Blue brightness compensation level fine range<br>0b: disable<br>1b: enable  |
| 19    | SR_OFF_R | R/W  | 0b                 | Slew rate control function when Red turns off operation<br>0b: slow slew rate.<br>1b: fast slew rate.  |
| 20    | SR_OFF_G | R/W  | 0b                 | Slew rate control function when Green turns off operation<br>0b: slow slew rate.<br>1b: fast slew rate.  |
| 21    | SR_OFF_B | R/W  | 0b                 | Slew rate control function when Blue turns off operation<br>0b: slow slew rate.<br>1b: fast slew rate.   |
| 23-22 | SR_ON_R  | R/W  | 01b                | Slew rate control function when Red turns on operation<br>00b: the slower slew rate.<br>01b: slow slew rate.<br>10b: fast slew rate.<br>11b: the faster slew rate.   |
| 25-24 | SR_ON_G  | R/W  | 01b                | Slew rate control function when Green turns on operation<br>00b: the slower slew rate.<br>01b: slow slew rate.<br>10b: fast slew rate.<br>11b: the faster slew rate.   |
| 27-26 | SR_ON_B  | R/W  | 01b                | Slew rate control function when Blue turns on operation<br>00b: the slower slew rate.<br>01b: slow slew rate.<br>10b: fast slew rate.<br>11b: the faster slew rate.  |
| 31-28 | RESERVED | R    | 0000b              |  |
| 32    | CAURSE_R | R/W  | 0b                 | Enable the Red brightness compensation level course range<br>0b: disable<br>1b: enable   |
| 33    | CAURSE_G | R/W  | 0b                 | Enable the Green brightness compensation level course range<br>0b: disable<br>1b: enable   |

表 6-11. FC4 Register Field Descriptions (続き)

| Bit   | Field          | Type | Reset | Description   |
|-------|----------------|------|-------|---|
| 34    | CAURSE_B       | R/W  | 0b    | Enable the Blue brightness compensation level course range<br>0b: disable<br>1b: enable               |
| 38-35 | FIRST_LINE_DIM | R/W  | 0000b | Adjust the first line dim level<br>0000b: level 1<br>...<br>0111b: level 8<br>...<br>1111b: level 16  |
| 39    | DE_COUPLE2     | R/W  | 0b    | Decoupling between ON and OFF channels<br>0b: disabled<br>1b: enabled                                 |
| 43-40 | DE_COUPLE3     | R/W  | 1000b | Set decoupling enhancement level<br>0000b: level 1<br>...<br>0111b: level 8<br>...<br>1111b: level 16 |
| 44    | DE_COUPLE3_EN  | R/W  | 0b    | Enable decoupling enhancement<br>0b: disabled<br>1b: enabled  |
| 47-45 | RESERVED       | R    | 000b  |   |

### 6.7.6 FC14

FC14 is shown in [FC14 Register](#) and described in [FC14 Register Field Descriptions](#).

図 6-31. FC14 Register

|          |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|
| 47       | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35           | 34 | 33 | 32 |
| RESERVED |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
| R-0b     |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
| R-0b     |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |    |    |    |    | LOD_LINE_CMD |    |    |    |
| R-0b     |    |    |    |    |    |    |    |    |    |    |    | R/W-00000b   |    |    |    |

表 6-12. FC14 Register Field Descriptions

| Bit  | Field        | Type | Reset  | Description  |
|------|--------------|------|--------|--|
| 4-0  | LOD_LINE_CMD | R/W  | 00000b | Locate the line with LED open load warnings:<br>00000b: Line 0<br>...<br>11111b: Line 31 |
| 47-5 | RESERVED     | R    | 0b     | Reserved bits  |

### 6.7.7 FC15

FC15 is shown in [FC15 Register](#) and described in [FC15 Register Field Descriptions](#).

図 6-32. FC15 Register

|          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 47       | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| RESERVED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

図 6-32. FC15 Register (続き)

|          |    |    |    |    |    |    |    |    |    |    |              |    |    |    |    |
|----------|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |    |    |    |              |    |    |    |    |
| R-0b     |    |    |    |    |    |    |    |    |    |    |              |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |    |    |    | LSD_LINE_CMD |    |    |    |    |
| R-0b     |    |    |    |    |    |    |    |    |    |    | R/W-00000b   |    |    |    |    |

表 6-13. FC15 Register Field Descriptions

| Bit  | Field        | Type | Reset  | Description  |
|------|--------------|------|--------|--|
| 4-0  | LSD_LINE_CMD | R/W  | 00000b | Locate the line with LED short circuitry warnings:<br>00000b: Line 0<br>...<br>11111b: Line 31 |
| 47-5 | RESERVED     | R    | 0b     | Reserved bits  |

### 6.7.8 FC17

FC17 is shown in [FC17 Register](#) and described in [FC17 Register Field Descriptions](#).

図 6-33. FC17 Register

|                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 47                   | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| RESERVED             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOD_LINE_WARN[31:16] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOD_LINE_WARN[15:0]  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

表 6-14. FC17 Register Field Descriptions

| Bit  | Field               | Type | Reset | Description   |
|------|---------------------|------|-------|---|
| 47-0 | LOD_LINE_WARN[47:0] | R    | 0b    | Read the line with LED open load warnings:<br>Bit 0 = 0, Line 0 has no warning; Bit 0 = 1, Line 0 has warning<br>...<br>Bit 31 = 0, Line 31 has no warning; Bit 31 = 1, Line 31 has warning |

### 6.7.9 FC19

FC19 is shown in [FC19 Register](#) and described in [FC19 Register Field Descriptions](#).

図 6-34. FC19 Register

|                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 47                   | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| RESERVED             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LSD_LINE_WARN[31:16] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LSD_LINE_WARN[15:0]  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

図 6-34. FC19 Register (続き)

R-0b

表 6-15. FC19 Register Field Descriptions

| Bit  | Field               | Type | Reset | Description   |
|------|---------------------|------|-------|---|
| 47-0 | LSD_LINE_WARN[47:0] | R    | 0b    | Read the line with LED short circuitry warnings:<br>Bit 0 = 0, Line 0 has no warning; Bit 0 = 1, Line 0 has warning<br>...<br>Bit 31 = 0, Line 31 has no warning; Bit 31 = 1, Line 31 has warning |

### 6.7.10 FC20

FC20 is shown in [FC20 Register](#) and described in [FC20 Register Field Descriptions](#).

図 6-35. FC20 Register

|        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 47     | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| LOD_CH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOD_CH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOD_CH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

表 6-16. FC20 Register Field Descriptions

| Bit  | Field  | Type | Reset | Description  |
|------|--------|------|-------|--|
| 47-0 | LOD_CH | R    | 0b    | Locate the LED open load channel:<br>Bit 0 = 0, CH 0 is normal; Bit 0 = 1, CH 0 is short circuitry<br>...<br>Bit 47 = 0, CH 47 is normal; Bit 47 = 1, CH 47 is short circuitry |

### 6.7.11 FC21

FC21 is shown in [FC21 Register](#) and described in [FC21 Register Field Descriptions](#).

図 6-36. FC21 Register

|        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 47     | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| LSD_CH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LSD_CH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LSD_CH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| R-0b   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

表 6-17. FC21 Register Field Descriptions

| Bit  | Field  | Type | Reset | Description  |
|------|--------|------|-------|--|
| 47-0 | LSD_CH | R    | 0b    | Locate the LED short circuitry channel:<br>Bit 0 = 0, CH 0 is normal; Bit 0 = 1, CH 0 is short circuitry<br>...<br>Bit 47 = 0, CH 47 is normal; Bit 47 = 1, CH 47 is short circuitry |

## 7 Application and Implementation

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### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 7.1 Application Information

The LP5892-Q1 integrates 48 constant current sources and 16 scanning FETs. A single LP5892-Q1 is capable of driving  $16 \times 16$  RGB LED pixels while stacking two LP5892-Q1 devices can drive  $32 \times 32$  RGB LED pixels. To achieve low power consumption, the LP5892-Q1 supports separated power supplies for the red, green, and blue LEDs by its common cathode structure.

The LP5892-Q1 implements a high speed rising edge transmission interface (up to 50 MHz) to support high device count daisy-chained and high refresh rate while minimizing electrical-magnetic interference (EMI). SCLK must be continuous, no matter there is data on SIN or not, because SCLK is not only used to sample the data on SIN, but also used as a clock source to generate GCLK by internal frequency multiplier. Based on rising-edge CCSI protocol, all the commands/FC registers/SRAM data are written from the SIN input terminal, and all the FC registers/ LED open and short flag can be read out from the SOUT output terminal. Moreover, the device supports up to 160-MHz GCLK frequency and can achieve 16-bit PWM resolution, with 3840 Hz or even higher refresh rate.

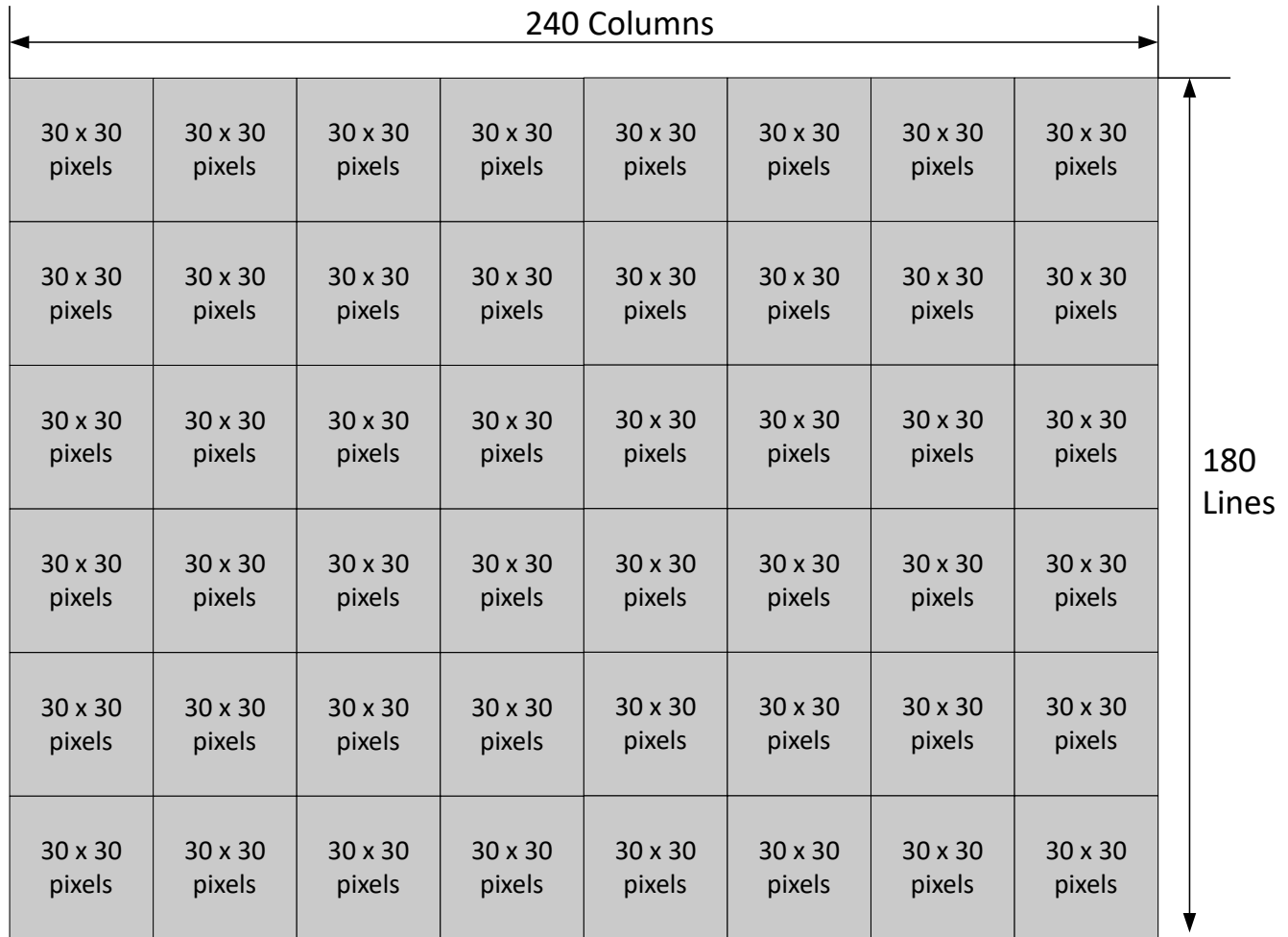
Meanwhile, the LP5892-Q1 integrates enhanced circuits and intelligent algorithms to solve the various display challenges in Narrow Pixel Pitch (NPP) LED display applications and mini and micro-LED products: dim at the first scan line, upper and downside ghosting, non-uniformity in low grayscale, coupling, caterpillar caused by open or short LEDs, which make the LP5892-Q1 a perfect choice in such applications.

The LP5892-Q1 also implements LED open, weak short, short detections and removals during operations and can also report this information out to the accompanying digital processor.



### 7.2.1.1 System Structure

To build an LED display module with 240 × 180 pixels, 96 LP5892-Q1 devices are required.



**図 7-2. LED Display Module**

As shown in [図 7-2](#), the total module can be divided into 48 32 × 32 matrix. Each matrix includes two devices with stackable connection.

注

To achieve the best performance, distribute the redundant channels and lines to each 32 × 32 matrix. For this case, two Red/Green/Blue channels and two lines are not used in each matrix. And these unused pins can be floated. For the software, TI suggests zero data to send to the unused channels. There is no need to send the zero data to unused lines.

### 7.2.1.2 SCLK Frequency

The SCLK frequency is determined by the data volume of one frame and frame rate. In this application, the data volume  $V_{Data}$  is  $30 \times 32 \times 48 \text{ bits} \times 4 = 184.32 \text{ Kb}$ , the frame rate is 120 Hz. Suppose the data transmission efficiency is 0.8, the minimum frequency of SCLK must be:  $f_{SCLK} = V_{Data} \times f_{frame} / 0.8$ . So the minimum SCLK frequency is 27.65 MHz with rising-edge transmission.

### 7.2.1.3 Internal GCLK Frequency

The internal GCLK frequency is configured by the Frequency Multiplier (FREQ\_MUL), and is determined by the PWM resolution. The GCLK frequency can be calculated by the below equations:

$$N_{sub\_period} = \frac{f_{refresh\_rate}}{f_{frame\_rate}}$$

$$GS_{max} = 2^K$$

$$GS_{max} = N_{GCLK\_Seg} \times N_{sub\_period}$$

$$\frac{1}{f_{frame\_rate}} = \left( \frac{N_{GCLK\_Seg}}{f_{GCLK}} + T_{SW} \right) \times N_{scan\_line} \times N_{sub\_period} + T_{Blank} \quad (3)$$

where

- $f_{refresh\_rate}$  means the refresh rate
- $f_{frame\_rate}$  means the frame rate
- $K$  means the PWM resolution
- $N_{sub\_period}$  means the sub-period numbers within one frame
- $N_{GCLK\_seg}$  means the GCLK number per segment (line switch time excluded)
- $f_{GCLK}$  means GCLK frequency
- $T_{SW}$  means line switching time
- $N_{scan\_line}$  means the scan line number
- $T_{blank}$  means the blank time in one frame, equals to 0 in ideal configuration
- $GS_{max}$  means the maximum grayscale that the device can output in one frame

表 7-2 gives the values based on the system configuration and equation.

**表 7-2. LP5892-Q1 Design Parameters for GCLK Frequency Calculation**

| DESIGN PARAMETER  | EXAMPLE VALUE |
|-------------------|---------------|
| $N_{sub\_period}$ | 32            |
| $N_{scan\_line}$  | 30            |
| $T_{SW}$          | 1.5 $\mu$ s   |
| $T_{blank}$       | 0             |
| $N_{GCLK\_seg}$   | 512           |
| $GS_{max}$        | 16383         |
| $f_{GCLK}$        | 71.3 MHz      |

Considering SCLK frequency and FREQ\_MUL, the SCLK can be 27.7 MHz, and FREQ\_MUL can be 0010b. So the GCLK is 83.1 MHz.

#### 7.2.1.4 Line Switch Time

The line switch time is digitalized with the GCLK number and can be set by the LINE\_SWT (Bit 40-37 in FC1 register). In this application, it is  $1.5 \text{ us} \times 83.1 \text{ MHz} = 125 \text{ GCLKs}$ , so the LINE\_SWT equals to 0011b (120 GCLKs), the actual line switch time is 1.44 us.

#### 7.2.1.5 Blank Time Removal

The LP5892-Q1 has an algorithm to distribute the blank time into each sub-period to prevent the black field when taking photos or video.

From Equation 3, 83.1-MHz GCLK frequency and 1.44-us line switch time, the calculated blank time is 1.0361 ms ( 86100 GCLK ), which is too long and brings black field.

Here are detailed steps of the algorithm.

#### Step 1: Distribute blank time into each segment

When the blank GCLK number is larger than  $N_{sub\_period} \times N_{scan\_line}$ , it can be distributed into each segment.

In this application, the blank GCLK number is 86100, and  $N_{sub\_period} \times N_{scan\_line}$  is 960, so the distributed GCLK number in each segment is  $86100/960 = 89...660$ . These 89 GCLKs can be used to increase PWM length or extend line switch time. If used to increase PWM length, the GCLK number in each segment will be  $512 + 89 = 601$ , so the SEG\_LENGTH ( Bit9-0 in FC1 register) is 1001011001b.

#### Step 2: Distribute blank time into each sub-period

If the left GCLK number is larger than  $N_{sub\_period}$ , it can be distributed into each sub-period.

In this application, the left GCLK is 660, the distributed GCLK number in each sub-period is  $660/32=20$ . The BLK\_ADJ (Bit46-41 in FC1 register) is 010100b.

After distributing into each sub-period, the left GCLK number is 0.

#### 7.2.1.6 BC and CC

Select the reference current-setting resistor  $R_{IREF}$  and configure a proper BC value to set the maximum current of the RGB LEDs (see [Brightness Control \(BC\) Function](#) for more details). Here the maximum current is 3 mA, BC value is 03h, according to equation 式 1, the reference resistor value is  $0.8 \text{ V}/3 \text{ mA} \times 86.61 = 23 \text{ k}\Omega$ .

Configure the CC\_R/CC\_G/CC\_B registers to set the current of Red/Green/Blue LED current to 3 mA/2 mA/1 mA (see [Color Brightness Control \(CC\) Function](#) for more details).

表 7-3 shows the reference current setting resistor  $R_{IREF}$ , BC and CC\_R/CC\_G/CC\_B register value.

表 7-3. Current Setting Value

| DESIGN PARAMETER | EXAMPLE VALUE |
|------------------|---------------|
| $R_{IREF}$       | 23 k $\Omega$ |
| BC               | 011 b         |
| CC_R             | 11111110 b    |
| CC_G             | 10101001 b    |
| CC_B             | 01010100 b    |

### 7.2.2 Detailed Design Procedure

Figure 7-3 gives a detail design procedure for LED display. After power on and digital signals are ready, the first step for the controller is to send the chip index command to let the devices know their identifications. Then, the command sends the configuration data to the FC registers. After this, it sends the VSYNC at the beginning of each frame and also sends the data to each device. The devices displays the data of last frame when the VSYNC comes and meanwhile receive the data of current frame transmitted from controller. The registers can be read at anytime of the frame.

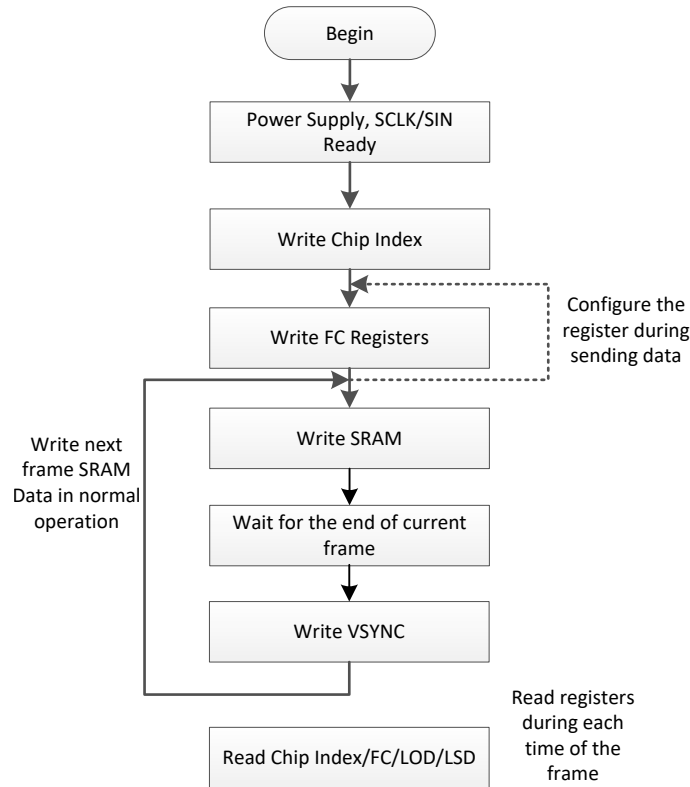


Figure 7-3. Design Procedure for LED Display

#### 7.2.2.1 Chip Index Command

The chip index is used to distribute the address of the devices in a data chain,. Each device gets its unique address by this command. Details can be found in [Chip Index Write Command](#).

#### 7.2.2.2 FC Registers Settings

Some bits of FC0, FC1, FC2, FC3 registers must be configured properly before the devices work normally. In this application, the registers value can be:

Table 7-4. FC Registers Value

| FC Registers | Register Value(BIN)   | Register Value(HEX) |
|--------------|---|---------------------|
| FC0          | 0001 0000 0000 0000 0101 1000 0011 1111 0000 0001 0000 0111 b | 1000 583F 0107 h    |
| FC1          | 0010 1010 1110 0000 0000 0000 1001 0100 1010 0110 0011 0001 b | 2AE0 0094 A631 h    |
| FC2          | 0000 1000 0000 0000 0000 0000 0000 1111 0000 0110 0110 0110 b | 0800 000F 0666 h    |
| FC3          | 0000 0000 0011 1011 0101 0100 1010 1001 1111 1111 0000 0000 b | 003B 54A9 FF00 h    |

The controller can configure the FC by the data write command with broadcast mode (see [Data Write Command](#) for more detail), the FC0, FC1 registers are updated after the VSYNC command comes, and the other FC registers are updated right away regardless the VSYNC command.

### 7.2.2.3 Grayscale Data Write

The channel grayscale data is written to SRAM of the device by the data write command with non-broadcast way, details can be found in [Data Write Command](#) and [Write a Frame Data into Memory Book](#).

[Data Write Flow](#) is the data write flow for this application,  $P(i, j)$  is the data of pixel locating in  $i + 1$  row and  $j + 1$  column. Suppose channel R15/G15/B15 of each device is not used and not connected, the channel R14/G14/B14 is connected to  $P(i, 0)$ , the channel R13/G13/B13 is connected to  $P(i, 1)$ , ..., and channel R0/G0/B0 is connected to  $P(i, 14)$ . The data of unused channel must be zero noting  $D\_Zero$  in below figure, and  $D\_Zero = 00000000000000001\ 00000000000000001\ 00000000000000001b$ .

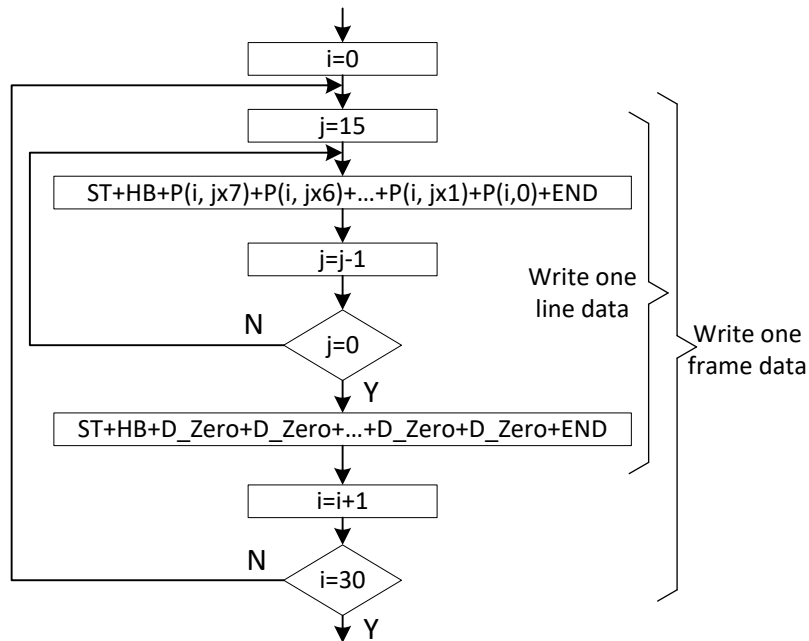


图 7-4. Data Write Flow

### 7.2.2.4 VSYNC Command

The VSYNC is used to sync the display of each frame for the devices in a cascaded chain. Details can be found in [VSYNC Write Command](#).

### 7.2.2.5 LED Open, Short Read

FC14, FC15, FC17, FC19, FC20, FC21 are the read command for LOD/LSD information. Details can be found in [Read LED-open Information](#) and [Read LED-short Information](#).

### 7.2.3 Application Curves

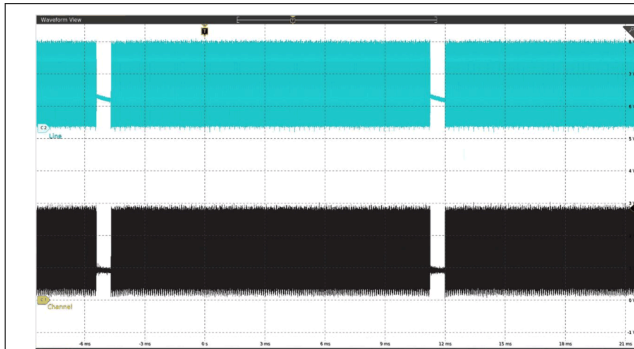


図 7-5. Line and Channel Waveform in One Frame (GSn = 0xFFFFh)

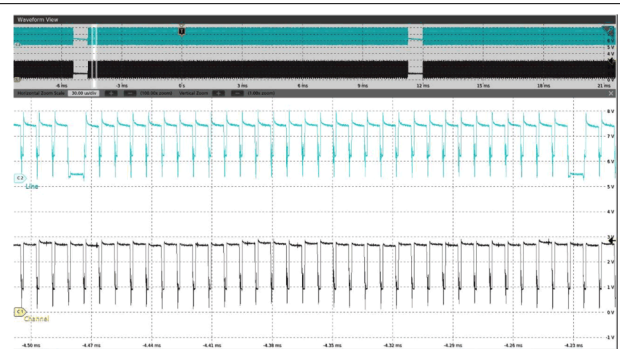


図 7-6. Line and Channel Waveform in One Subperiod (GSn = 0xFFFFh)

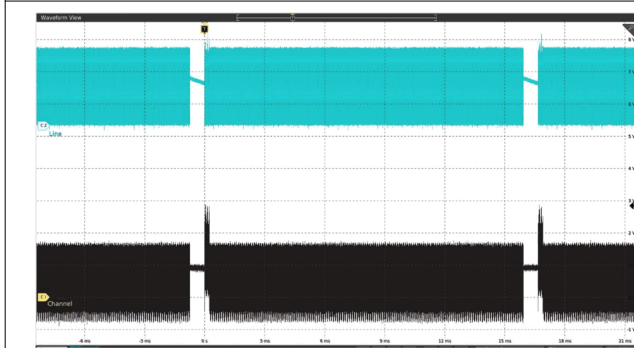


図 7-7. Line and Channel Waveform in One Frame (GSn = 0x0001h)

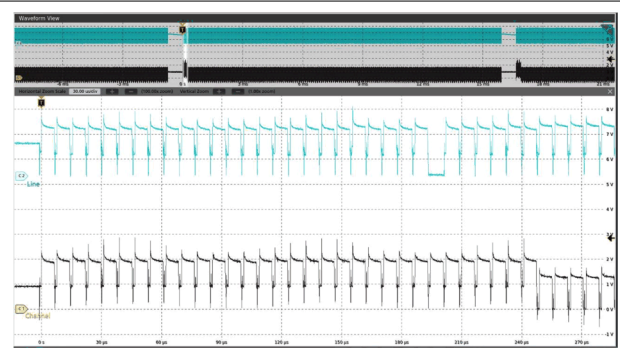


図 7-8. Line and Channel Waveform in One Frame (GSn = 0x0001h)

### 7.3 Power Supply Recommendations

Decouple the VCC power supply voltage by placing a 0.1μF ceramic capacitor close to VCC pin and GND plane. Depending on panel size, several electrolytic capacitors must be placed on the board equally distributed to get well regulated LED supply voltage VR/VG/VB. The ripple of the LED supply voltage must be less than 5% of their nominal value. Generally, the green and blue LEDs have the similar forward voltage, they can be supplied by the same power rail.

Furthermore, the  $VR > Vf(R) + 0.35V$  (10mA constant current example), the  $VG = VB > Vf(G/B) + 0.35V$  (10mA constant current example), here  $Vf(R)$ ,  $Vf(G/B)$  are representative for the maximum forward voltage of red, green/blue LEDs.

To simplify the power design, VCC can be connected to the VR power rail.

## 7.4 Layout

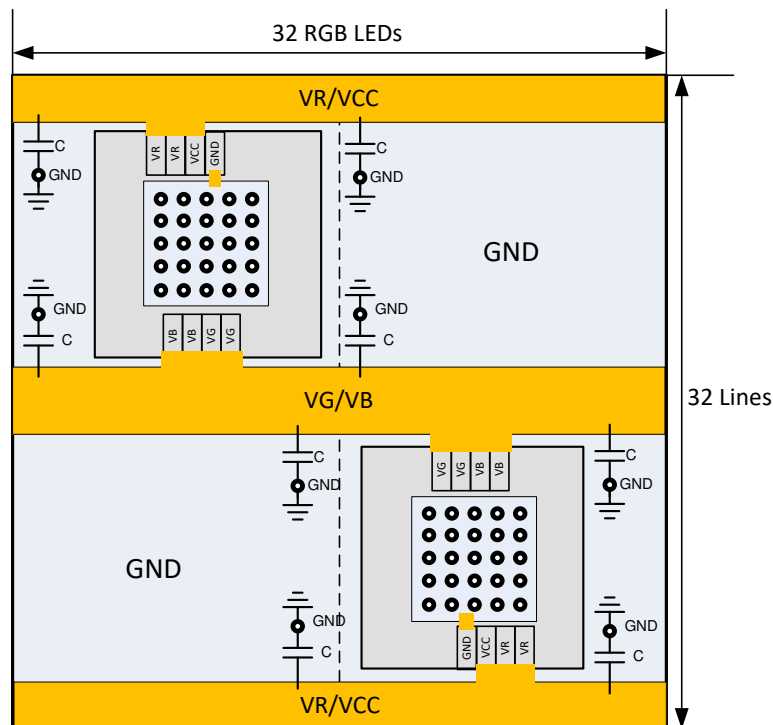
### 7.4.1 Layout Guidelines

- Place the decoupling capacitor near the VCC/VR, VG/VB pins and GND plane.
- Place the current programming resistor RIREF close to IREF pin and GND plane.
- Route the GND thermal pad as widely as possible for large GND currents. Maximum GND current is approximately 2A for one device ( $48\text{-CH} \times 40\text{mA} = 1.92\text{A}$ ).
- The Thermal Pad must be connected to GND plane because the pad is used as power ground pin internally. There is a large current flow through this pad when all channels turn on. Furthermore, this pad must be connected to a heat sink layer by thermal via to reduce device temperature. For more information about suggested thermal via pattern and via size, see [PowerPAD™ Thermally Enhanced Package application note](#).
- Routing between the LED Anode side and the device OUTXn pin must be as short and straight as possible to reduce wire inductance.
- The line switch pins must be located in the middle of the matrix, which must be laid out as symmetrically as possible.

### 7.4.2 Layout Example

To simplify the system power rails design, VR, VCC must use one power rail and VG, VB use another power rail. The image below gives an example for power rails routing.

Connect the GND pin to the thermal pad on the board with the shortest wire and the thermal pad is connected to GND plane with the vias, as many as possible to help the power dissipation.



☒ 7-9. Power Rails Routing Suggestion

The image below gives an example for line routing. Connect the line switch to the center of the line bus, so as to uniform the current flowing from the line switch to the left side and right side LEDs in white grayscale. With this connection, the unbalance of the parasitic inductor from the routing is the smallest and the display performance is better, especially in low grayscale condition.

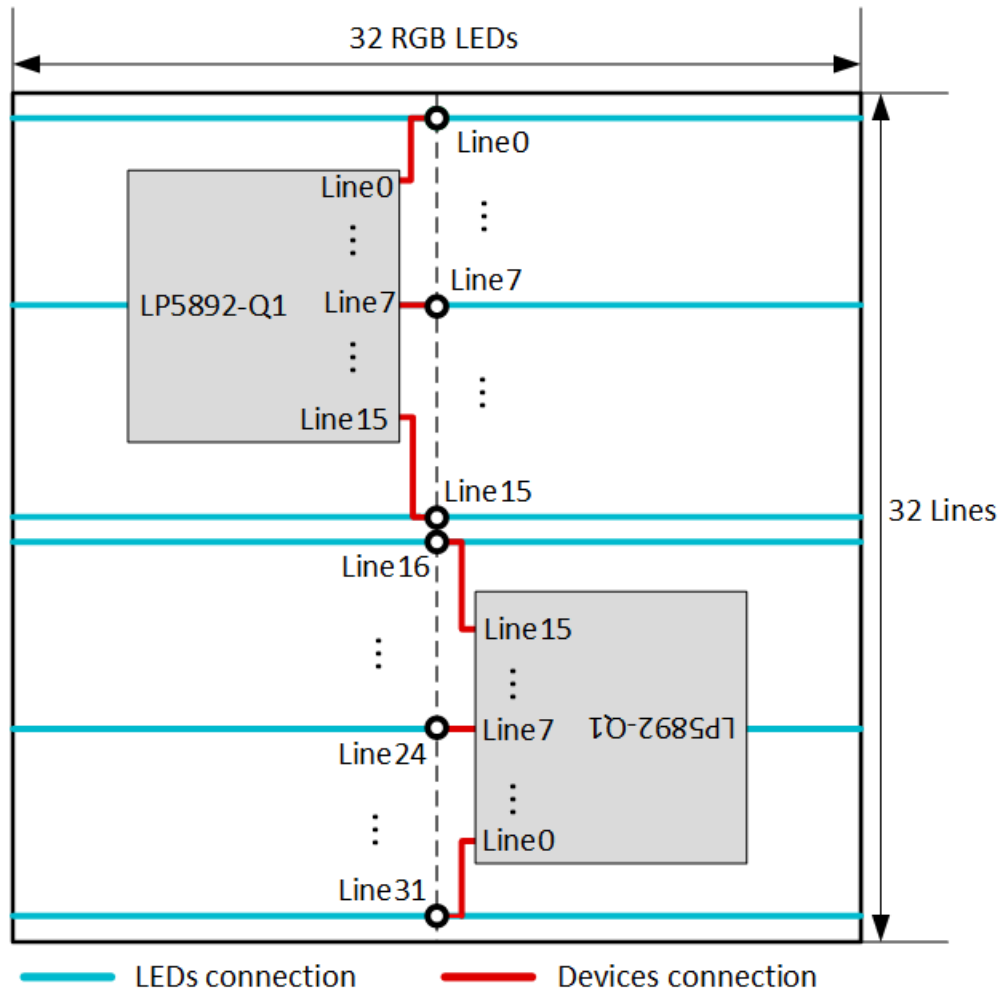


図 7-10. Line Routing Suggestion

The image below gives an example for channel routing with the shortest wire. With this connection, the channel to the LED path is the shortest, which can reduce the wire inductance, and be a benefit to the performance. However, the data transmission sequence must be adjusted to follow the pins routing map. For example, R0 connects to column 15 (LED15 ). The first data must be column 15 (LED15) rather than column 0 (LED0).

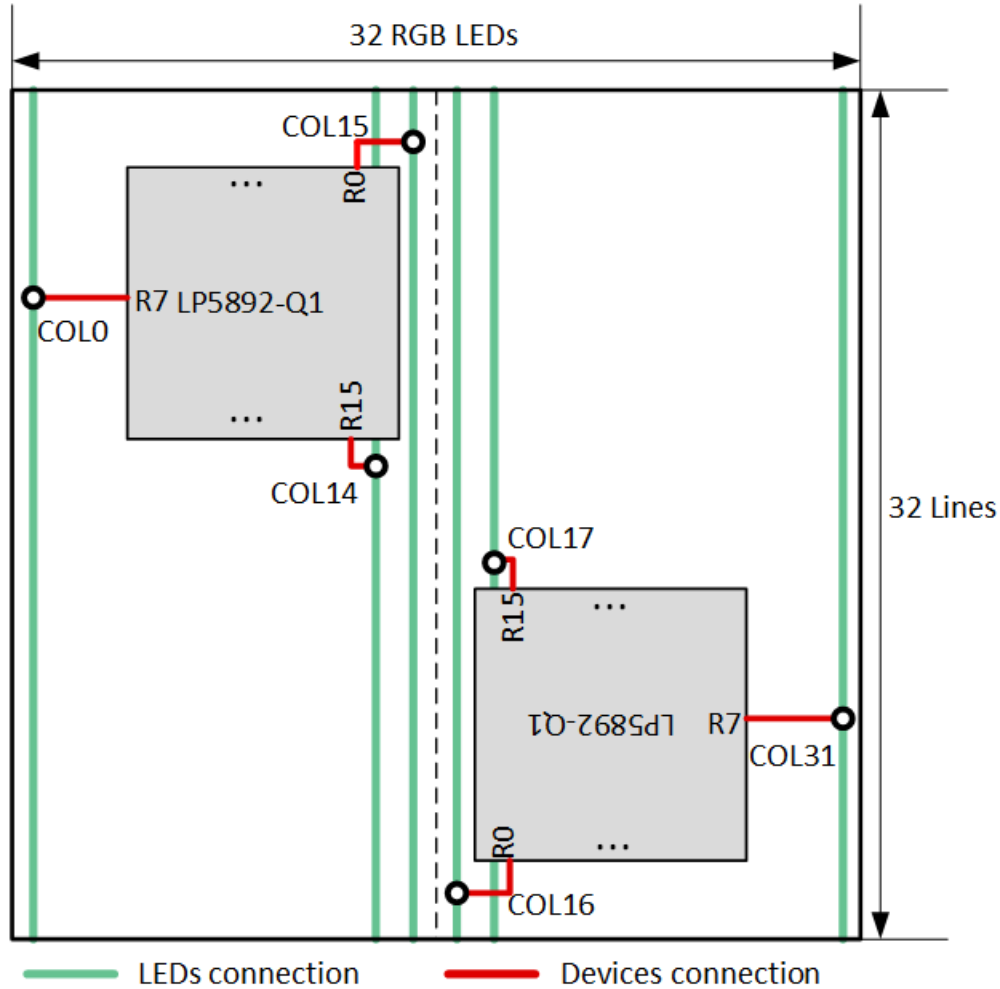


図 7-11. Channel Routing Suggestion with Shortest Wire

The image below gives an example for channel routing with pin number sequence. With this connection, the data transmission sequence is the same with pin number sequence. For example, R0 connects to column 0 (LED0). The first data is column 0 (LED0). However, with this connection, the inductance for each channel can be different, which can bring a slight difference for the worst case.

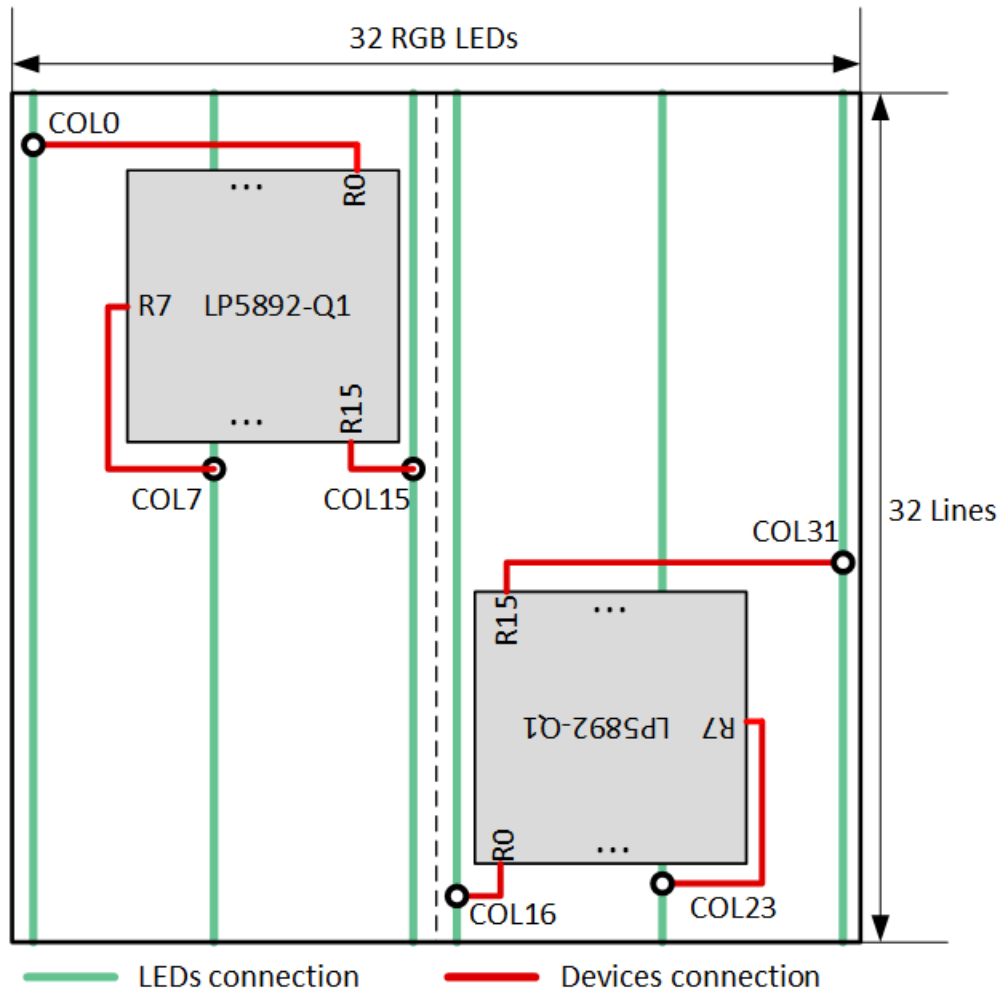


図 7-12. Channel Routing Suggestion with Channel Order Sequence

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

Texas Instruments, [PowerPAD™ Thermally Enhanced Package application note](#)

### 8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE          | REVISION | NOTES                       |
|---------------|----------|-----------------------------|
| February 2025 | *        | Advance Information release |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LP5892QRRFRQ1</a> | Active        | Production           | VQFN (RRF)   76 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | LP5892Q             |
| LP5892QRRFRQ1.A               | Active        | Production           | VQFN (RRF)   76 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | LP5892Q             |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

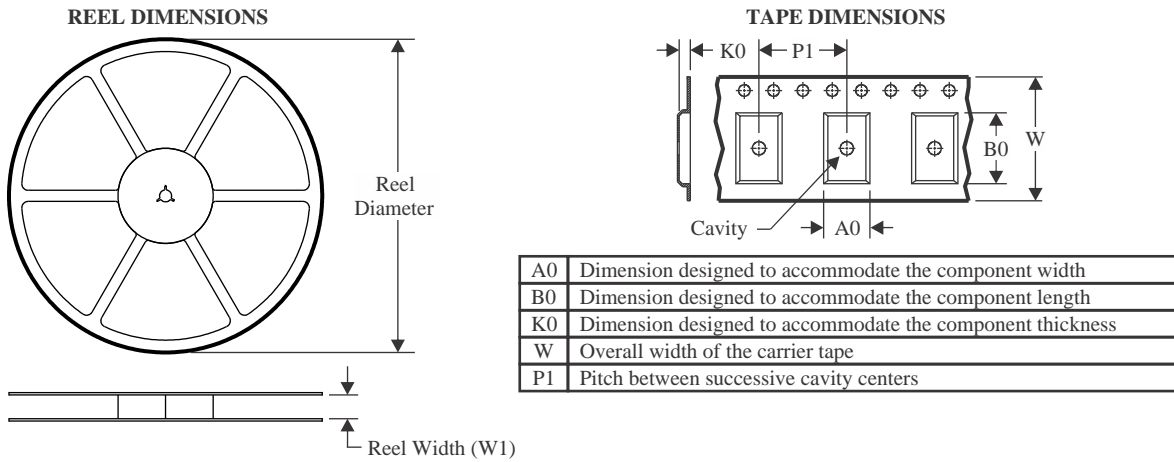
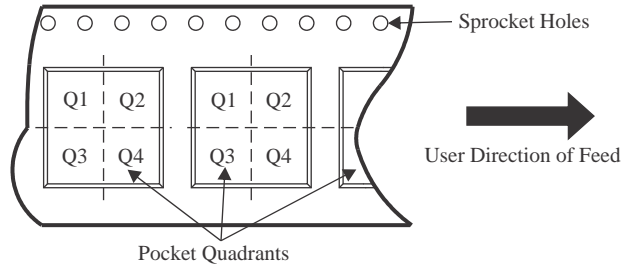
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP5892QRRFRQ1 | VQFN         | RRF             | 76   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.1     | 12.0    | 16.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP5892QRRFRQ1 | VQFN         | RRF             | 76   | 2000 | 367.0       | 367.0      | 35.0        |

## GENERIC PACKAGE VIEW

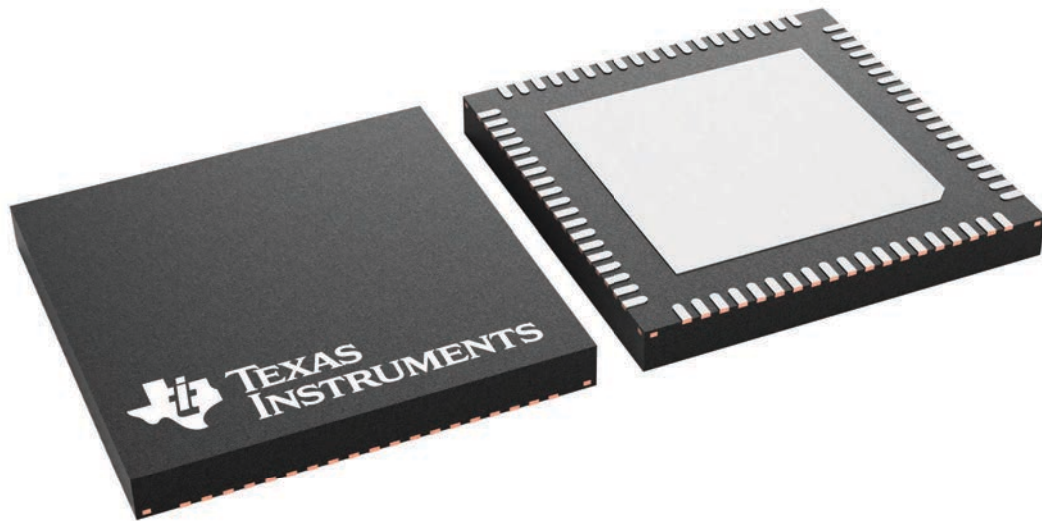
**RRF 76**

**VQFN - 1 mm max height**

9 x 9, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4232009/A

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