TEXAS INSTRUMENTS
LP5910
JAJSLM3F – SEPTEMBER 2015 – REVISED APRIL 2021

LP5910：低ノイズ、低静止時電流 (I_Q) の 300mA 出力 LDO

1 特長

- 入力電圧範囲：1.3V～3.3V
- 出力電圧範囲：0.8V～2.3V
- 出力電流：300mA
- PSRR：1kHz 時に 75dB
- 出力電圧許容誤差：±2%
- 低ドロップアウト：120mV (標準値)
- 超低 I_Q (イネーブル、無負荷時)：12µA
- 低出力電圧ノイズ：12µV_{RMS}
- セラミック入出力コンデンサで安定動作
- 熱的過負荷保護機能
- 短絡保護
- 逆電流保護
- 自動出力放電による高速なターンオフ

2 アプリケーション

- 携帯電話およびタブレット
- デジタル・カメラおよびオーディオ機器
- 携帯型およびバッテリ駆動の機器
- 携帯医療機器
- 仮想現実
- RF、PLL、VCO、およびクロック電源
- IP カメラ

3 概要

LP5910 は、最大 300mA の出力電流を供給できる低ノイズ LDO です。RF / アナログ回路の要件を満たすよう設計されたこのデバイスは、低ノイズ、高 PSRR、低静止電流、優れたライン / 負荷過渡応答といった特長を備えています。新しい革新的な設計手法の採用により、ノイズ・バイパス用コンデンサなしでクラス最高レベルの優れたノイズ特性を実現し、出力コンデンサのリモート配置も選択できます。

本デバイスは、入力電圧が出力電圧よりも下がった際に LDO を通って IN ピンへ逆電流が流れるのを防止する逆電流保護回路を内蔵しています。

イネーブル (EN) ピンを LOW にして、出力をオフ状態にすると、自動出力放電回路が出力容量を放電してターンオフを速めます。

LP5910 は低い入出力電圧範囲で動作するため、ポスト DC/DC レギュレータ (ポスト BUCK レギュレータ) またはシングル / デュアル・セル・アプリケーションに適しています。

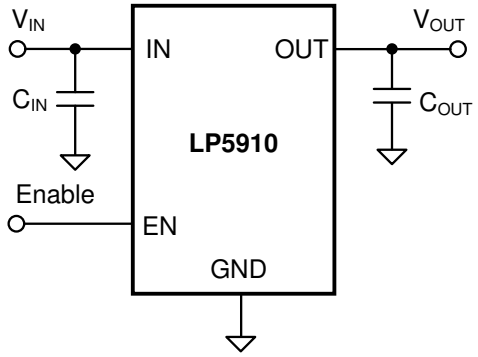
このデバイスは、入力および出力に 1µF のセラミック・コンデンサを使用して動作するよう設計されています。独立したノイズ・バイパス・コンデンサは不要です。

このデバイスでは、0.8V～2.3V (25mV ステップ) の固定出力電圧を使用できます。具体的な電圧オプションについては、テキサス・インスツルメンツの販売部門までお問い合わせください。

製品情報(1)

部品番号	パッケージ	本体サイズ
LP5910	WSON (6)	2.00mm × 2.00mm (公称値)
	DSBGA (4)	0.742mm × 0.742mm (最大値)

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (July 2017) to Revision F (April 2021) **Page**

- *文書全体にわたって表、図、相互参照の採番方法を更新*.....1
- ドキュメントから WEBENCH のリンクを削除.....1
- 「*特長*」セクションの最後の箇条書き項目を削除.....1
- Changed Dropout Voltage specifications for 1.5V ≤ V_{IN} < 1.8V; added new rows in Dropout Voltage specifications for this voltage range.....5
- Deleted *Custom Design With WEBENCH® Tools* section from *Detailed Design Procedure*.....13
- Deleted *Custom Design With WEBENCH® Tools* section from *Documentation Support*.....19

Changes from Revision D (August 2016) to Revision E (July 2017) **Page**

- 発注型名 LP5910-1.1BYKAR および LP5910-1.1BYKAT に関連する新しいパッケージ YKA0004-C01 を追加。WEBENCH のリンクを追加.....1

5 Pin Configuration and Functions

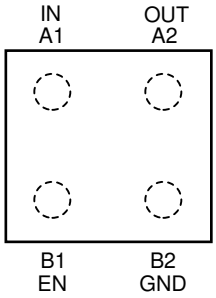


図 5-1. YKA Package, 4-Pin Ultra-Thin DSBGA, Top View

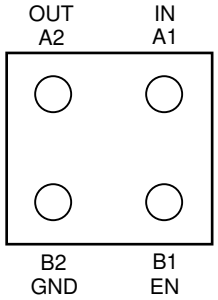


図 5-2. YKA Package, 4-Pin Ultra-Thin DSBGA, Bottom View

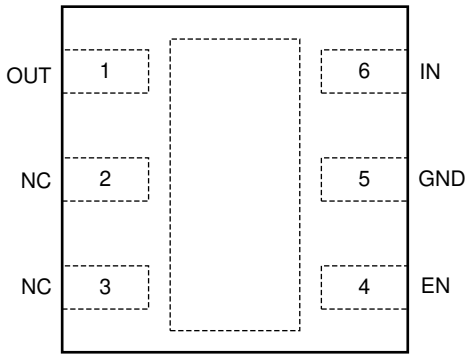


図 5-3. DRV Package, 6-Pin WSON With Thermal Pad, Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSBGA	WSON		
EN	B1	4	I	Enable input; disables the regulator when logic low. Enables the regulator when logic high. An internal 1-MΩ pull down resistor connects this input to ground.
GND	B2	5	—	Common ground
IN	A1	6	I	Voltage supply input. A 1-µF capacitor must be connected at this input.
NC	—	2, 3	—	No internal connection. Connect to ground or leave open.
OUT	A2	1	O	Voltage output. A 1-µF low-ESR capacitor must be connected from this pin to the GND pin. Connect this output to the load circuit.
Exposed Pad	—	Thermal Pad	—	The exposed thermal pad on the bottom of the package must be connected to a copper area under the package on the PCB. Connect to ground potential or leave floating. Do not connect to any potential other than the same ground potential seen at device pin 5 (GND). See the *Power Dissipation* section for more information.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
Input voltage, V_{IN}	–0.3	3.6	V
Output voltage, V_{OUT}	–0.3	3.6	V
Enable input voltage, V_{EN}	–0.3	3.6	V
Continuous power dissipation(3)	Internally limited		W
Junction temperature, $T_{J(MAX)}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage, V_{IN}	1.3	3.3	V
Output voltage, V_{OUT}	0.8	2.3	V
Enable input voltage, V_{EN}	0	3.3	V
Output current, I_{OUT}	0	300	mA
Junction temperature, T_J (1)	–40	125	°C
Ambient temperature, T_A (1)	–40	85	°C

(1) The maximum ambient temperature, ($T_{A(MAX)}$) is a recommended value only and can vary depending on device power dissipation and $R_{\theta JA}$. For reliable operation, the junction temperature (T_J) must be limited to a maximum of 125°C. Ambient temperature (T_A), thermal resistance ($R_{\theta JA}$) , V_{IN}, V_{OUT}, and I_{OUT} all define T_J : $T_J = T_A + (R_{\theta JA} \times ((V_{IN} – V_{OUT}) \times I_{OUT})$.

6.4 Thermal Information

THERMAL METRIC[1]		LP5910		UNIT
		YKA (DSBGA)	DRV (WSON)	
		4 PINS	6 PINS	
$R_{\theta JA}$ [2]	Junction-to-ambient thermal resistance, High-K	202.8	79.2[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.3	110.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.0	48.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.0	49.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	18.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(3) The PCB for the WSON/DRV package $R_{\theta JA}$ includes two (2) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)[1] [2] [3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to 3.3 V, I_{OUT} = 1 mA to 300 mA		–2		2	$\%V_{OUT}$
	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to 3.3 V, I_{OUT} = 1 mA			0.01		%/V
	Load regulation	I_{OUT} = 1 mA to 300 mA			0.002		%/mA
I_{LOAD}	Load current	See[4]		0		300	mA
I_Q	Quiescent current[5]	V_{EN} = 1 V, I_{OUT} = 0 mA			12	25	µA
		V_{EN} = 1 V, I_{OUT} = 300 mA			230	350	
$I_{Q(SD)}$	Quiescent current in shutdown[5]	V_{EN} = 0.3 V, –40°C ≤ T_J ≤ 85°C			0.02	2	µA
I_{RO}	Output reverse current[7] V_{OUT} > V_{IN}	V_{OUT} = 3.3 V, V_{IN} = V_{EN} = 0 V		–20		0	µA
		V_{OUT} = 3.3 V, V_{IN} = V_{EN} = 1.3 V		0		50	µA
I_G	Ground current[6]	I_{OUT} = 0 mA (V_{OUT} = 2.3 V)			15		µA
V_{DO}	Dropout voltage[8]	1.3 V ≤ V_{OUT} < 1.5 V, I_{OUT} = 300 mA	DSBGA only		200	300	mV
		1.5 V ≤ V_{OUT} <1.8V, I_{OUT} = 300 mA	DSBGA only		160	235	
		1.8 V ≤ V_{OUT} ≤ 2.3 V, I_{OUT} = 300 mA	DSBGA only		120	180	
		1.3 V ≤ V_{OUT} < 1.5 V, I_{OUT} = 300 mA	WSON only		245	370	
		1.5 V ≤ V_{OUT} < 1.8V, I_{OUT} = 300 mA	WSON only		195	270	
		1.8 V ≤ V_{OUT} ≤ 2.3 V, I_{OUT} = 300 mA	WSON only		145	220	
I_{LIMIT}	Output current limit	V_{OUT} = $V_{OUT(NOM)}$ – 0.1 V, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V			450		mA

6.5 Electrical Characteristics (continued)

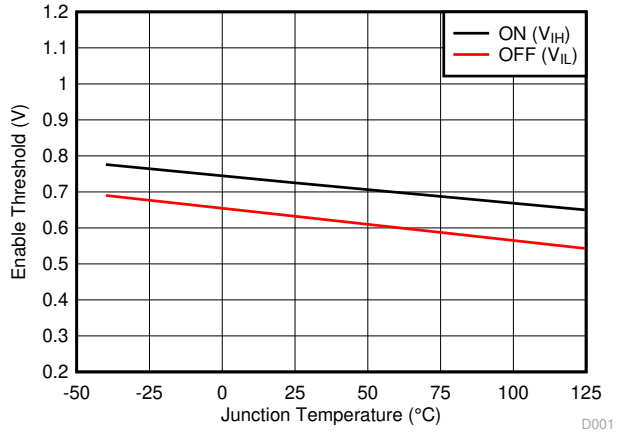
V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{EN} = 1 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio(10)	f = 100 Hz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			80		dB
		f = 1 kHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			75		
		f = 10 kHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			65		
		f = 100 kHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			40		
		f = 2 MHz, I_{OUT} = 20 mA, V_{OUT} ≥ 1 V			25		
		f = 100 Hz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			65		
		f = 1 kHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			65		
		f = 10 kHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			65		
		f = 100 kHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			40		
		f = 2 MHz, I_{OUT} = 20 mA, 0.8 V < V_{OUT} < 1 V			25		
e_N	Output noise voltage(10)	BW = 10 Hz to 100 kHz	I_{OUT} = 1 mA		12		$µV_{RMS}$
			I_{OUT} = 300 mA		12		
T_{SD}	Thermal shutdown	T_J rising until output is OFF			160		°C
	Thermal hysteresis	T_J falling from shutdown			15		
LOGIC INPUT THRESHOLDS							
V_{IL}	EN low threshold (Off)	V_{IN} = 1.3 V to 3.3 V				0.3	V
V_{IH}	EN high threshold (On)			1			
I_{EN}	EN pin current(9)	V_{EN} = 3.3 V, V_{IN} = 3.3 V			3.3		µA
		V_{EN} = 0 V, V_{IN} = 3.3 V			0.001		
TRANSIENT CHARACTERISTICS(9)							
$ΔV_{OUT}$	Line transient(10)	V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 µs, I_{OUT} = 1 mA			0	1	mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 0.5 V) in 30 µs, I_{OUT} = 1 mA		–1	0		
	Load transient(10)	I_{OUT} = 1 mA to 100 mA in 10 µs		–45			mV
		I_{OUT} = 100 mA to 1 mA in 10 µs				45	
	Overshoot on start-up(10)					5%	
t_{ON}	Turnon time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$			80	200	µs
OUTPUT DISCHARGE							
R_{AD}	Output discharge pulldown resistance	V_{EN} = 0 V, V_{IN} = 2.3 V			160		Ω

(1) All voltages are with respect to the device GND pin.
(2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the T_J range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) C_{IN}, C_{OUT}: Low-ESR Surface-Mount-Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) The device maintains a stable, regulated output voltage without a load current.
(5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}. I_Q = (I_{IN} – I_{OUT})
(6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(7) Output reverse current (I_{RO}) is measured at the IN pin.
(8) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value. Dropout voltage is not a valid condition for output voltages less than 1.3 V as compliance with the minimum operating input voltage can not be ensured.
(9) There is a 1-MΩ resistor between EN and ground on the device.
(10) This specification is verified by design.

6.6 Typical Characteristics

V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C (unless otherwise noted)



V_{IN} = 2.3 V V_{OUT} = 1.8 V

図 6-1. V_{EN} Threshold vs Temperature

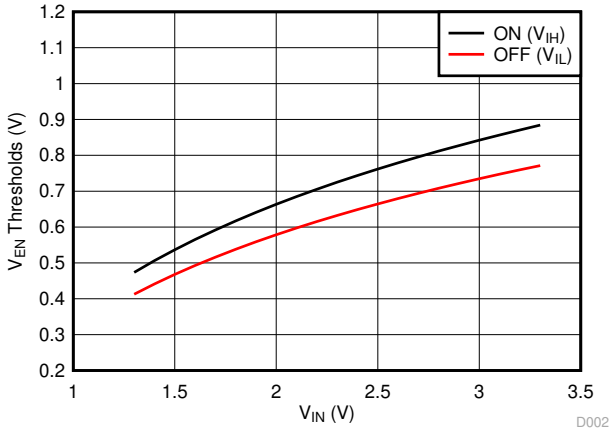
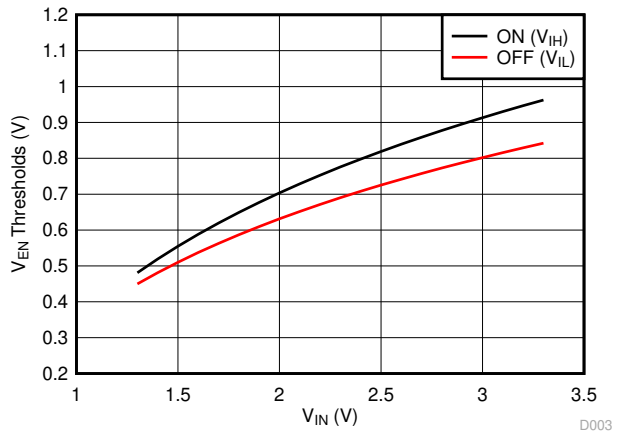
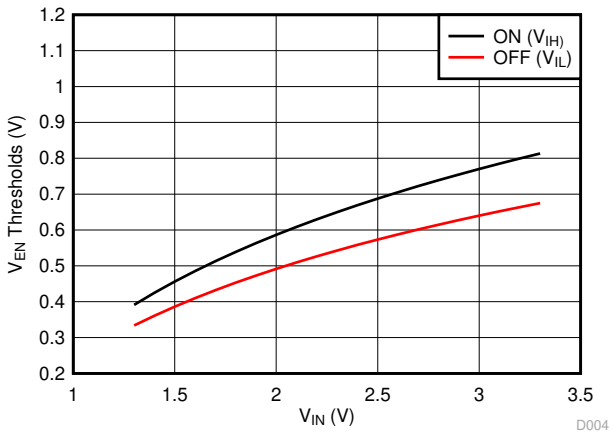


図 6-2. V_{EN} Thresholds vs V_{IN}



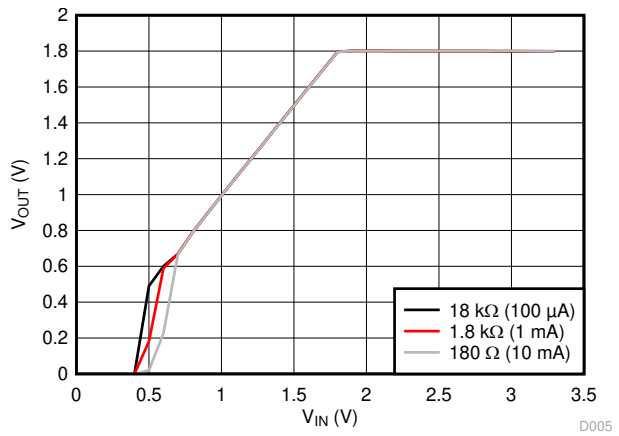
T_J = –40°C

図 6-3. V_{EN} Thresholds vs V_{IN}



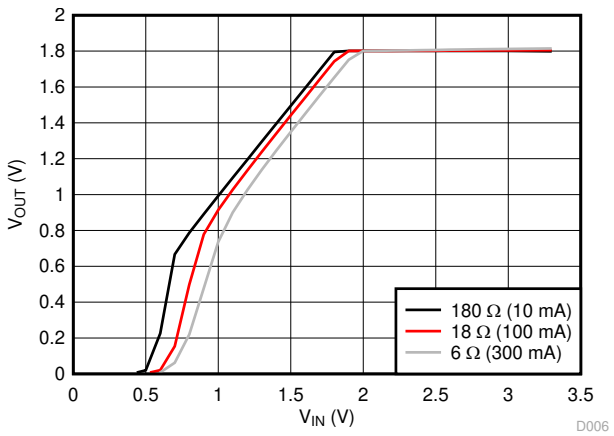
T_J = 125°C

図 6-4. V_{EN} Thresholds vs V_{IN}



V_{EN} = V_{IN}

図 6-5. V_{OUT} vs V_{IN}

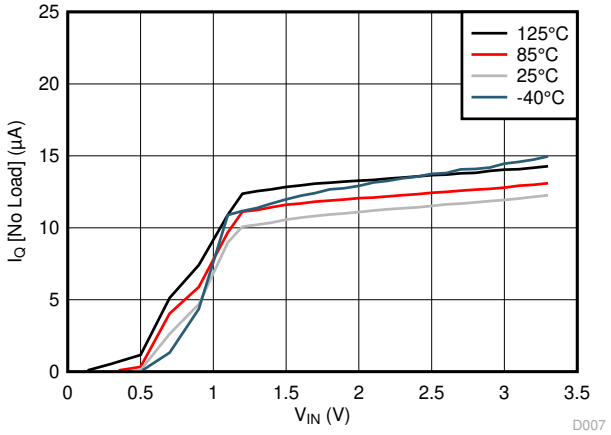


V_{EN} = V_{IN}

図 6-6. V_{OUT} vs V_{IN}

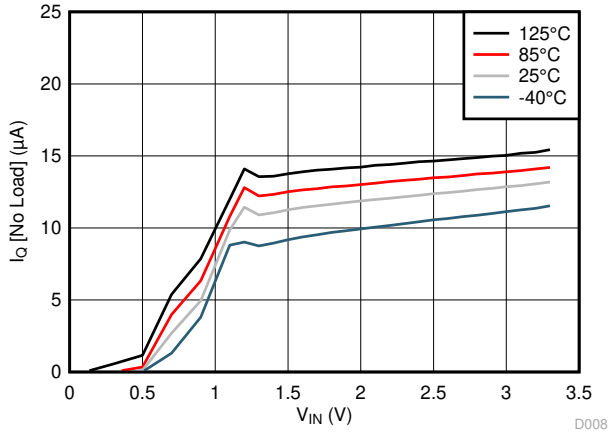
6.6 Typical Characteristics (continued)

V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C (unless otherwise noted)



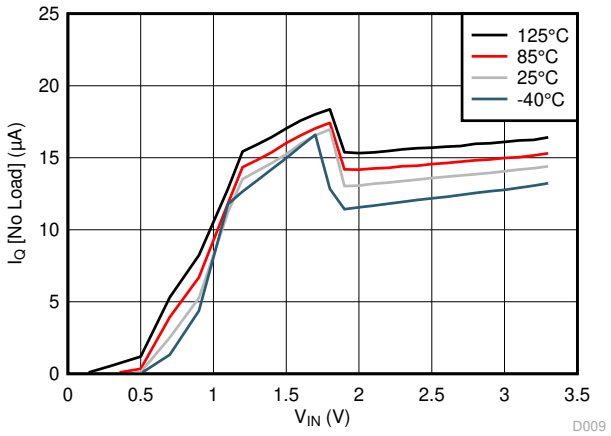
V_{OUT} = 0.8 V V_{EN} = V_{IN} No load

図 6-7. I_Q vs V_{IN}



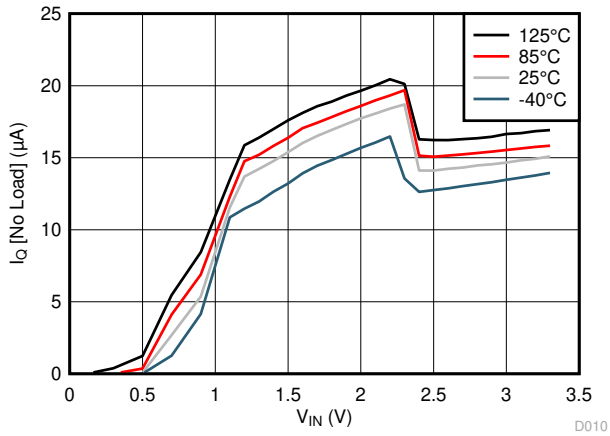
V_{OUT} = 1.2 V V_{EN} = V_{IN} No load

図 6-8. I_Q vs V_{IN}



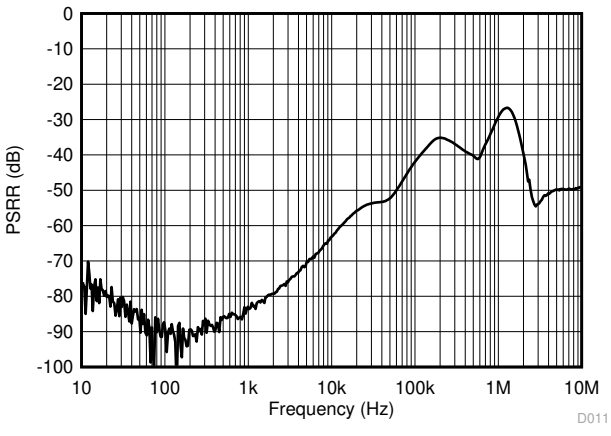
V_{OUT} = 1.8 V V_{EN} = V_{IN} No load

図 6-9. I_Q vs V_{IN}



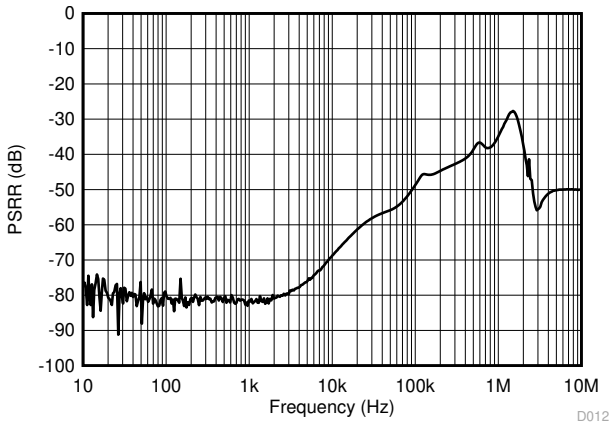
V_{OUT} = 2.3 V V_{EN} = V_{IN} No load

図 6-10. I_Q vs V_{IN}



V_{OUT} = 0.8 V V_{IN} = 1.3 V I_{OUT} = 20 mA

図 6-11. PSRR vs Frequency

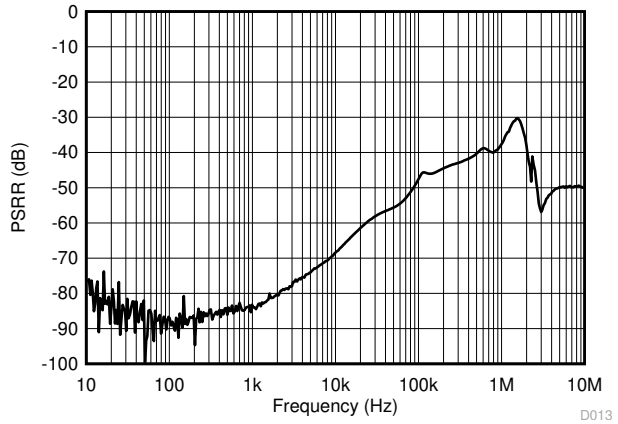


V_{OUT} = 1.8 V V_{IN} = 2.3 V I_{OUT} = 20 mA

図 6-12. PSRR vs Frequency

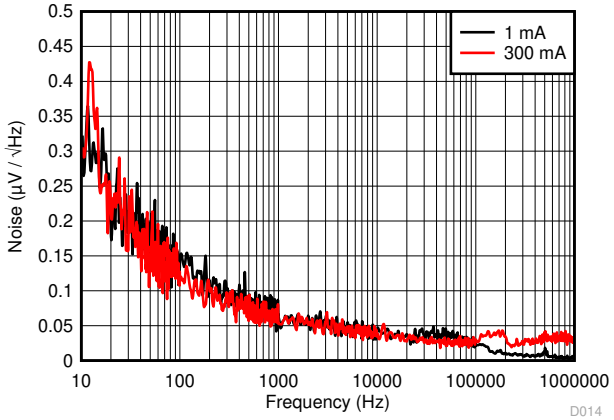
6.6 Typical Characteristics (continued)

V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C (unless otherwise noted)



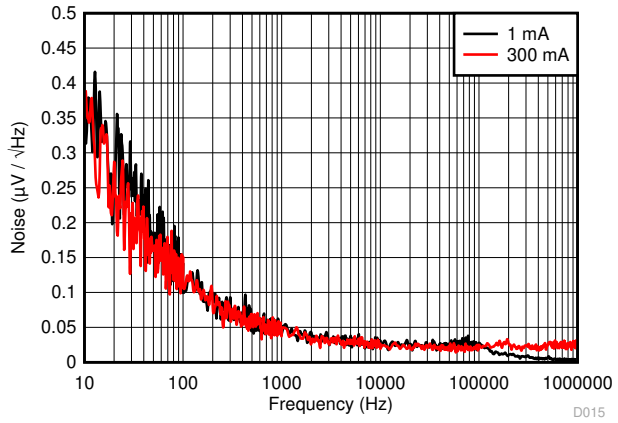
V_{OUT} = 2.3 V V_{IN} = 2.8 V I_{OUT} = 20 mA

図 6-13. PSRR vs Frequency



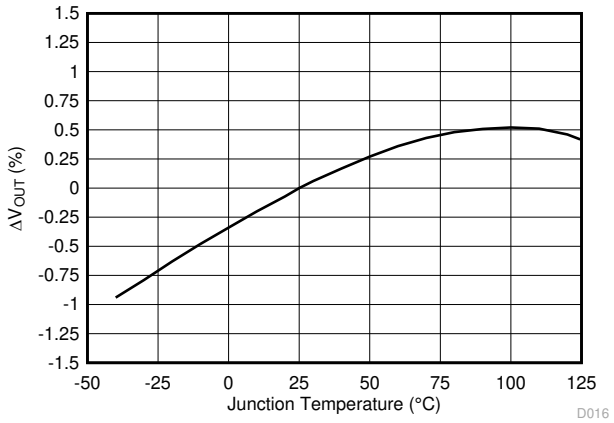
V_{OUT} = 0.8 V V_{IN} = 1.3 V

図 6-14. Noise Density



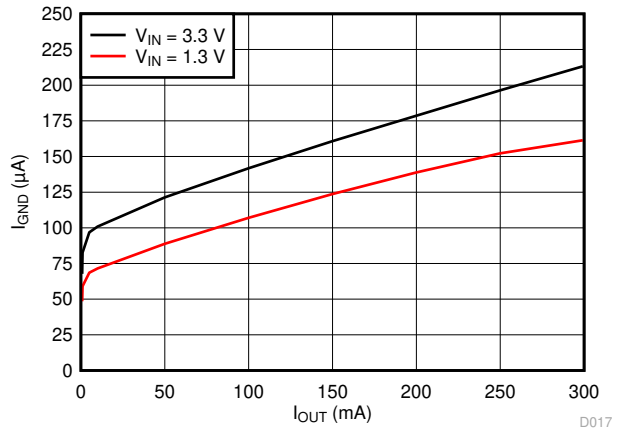
V_{OUT} = 2.3 V V_{IN} = 2.8 V

図 6-15. Noise Density



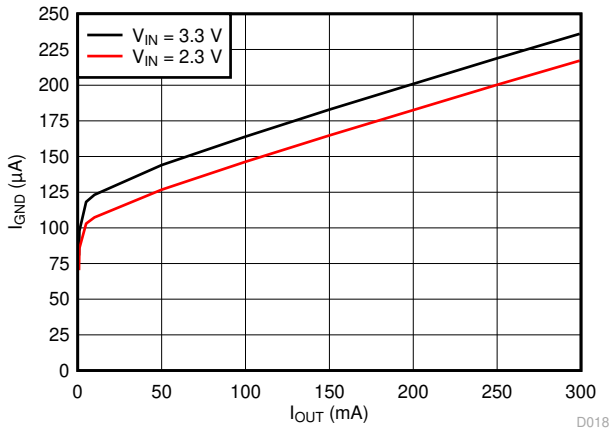
V_{IN} = V_{OUT} + 0.5 V I_{OUT} = 1 mA

図 6-16. ΔV_{OUT} vs Temperature



V_{OUT} = 0.8 V

図 6-17. I_{GND} vs I_{OUT}

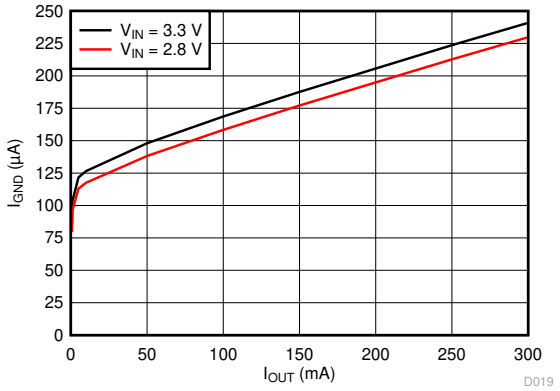


V_{OUT} = 1.8 V

図 6-18. I_{GND} vs I_{OUT}

6.6 Typical Characteristics (continued)

V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_J = 25°C (unless otherwise noted)



V_{OUT} = 2.3 V

図 6-19. I_{GND} vs I_{OUT}

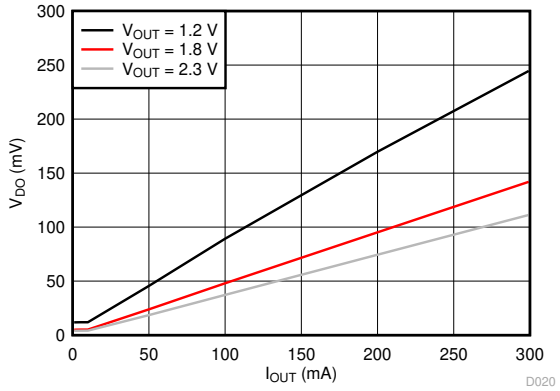
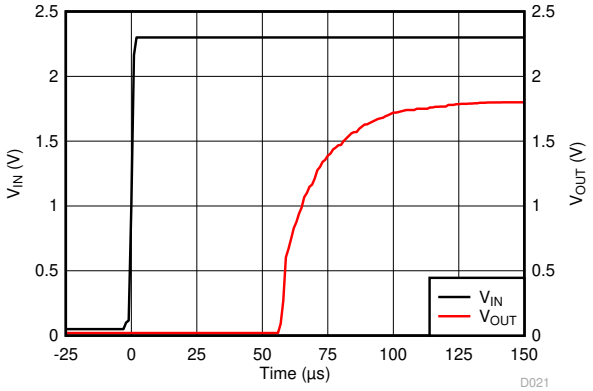
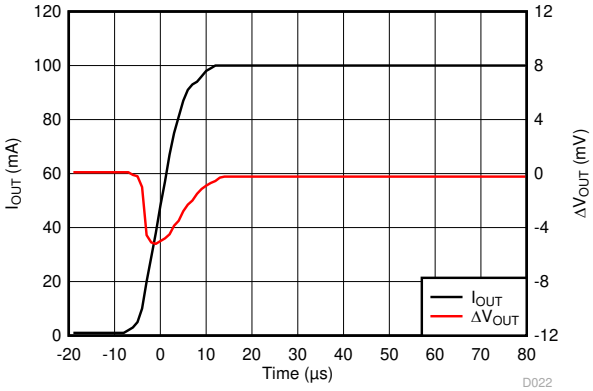


図 6-20. Dropout Voltage vs I_{OUT}



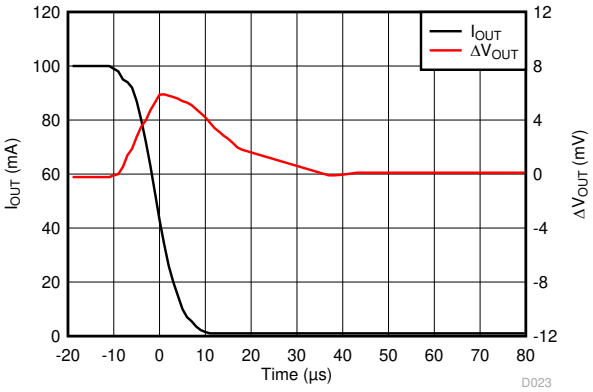
V_{EN} = V_{IN} V_{OUT} = 1.8 V C_{OUT} = 1 µF

図 6-21. Turnon Time



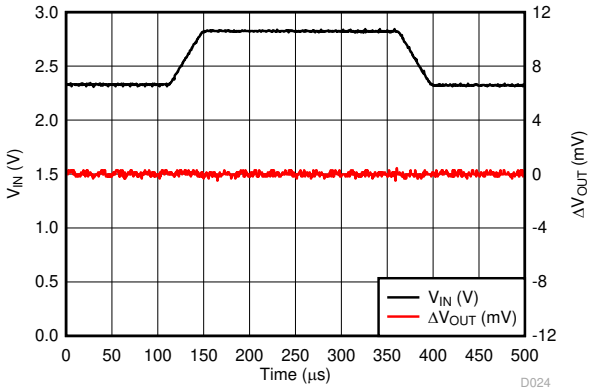
V_{IN} = 2.3 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
I_{OUT} = 1 mA to 100 mA t_{RISE} = 10 µs

図 6-22. Load Transient Response



V_{IN} = 2.3 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
I_{OUT} = 100 mA to 1 mA t_{FALL} = 10 µs

図 6-23. Load Transient Response



ΔV_{IN} = 0.5 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
t_{RISE} = t_{FALL} = 30 µs I_{OUT} = 1 mA

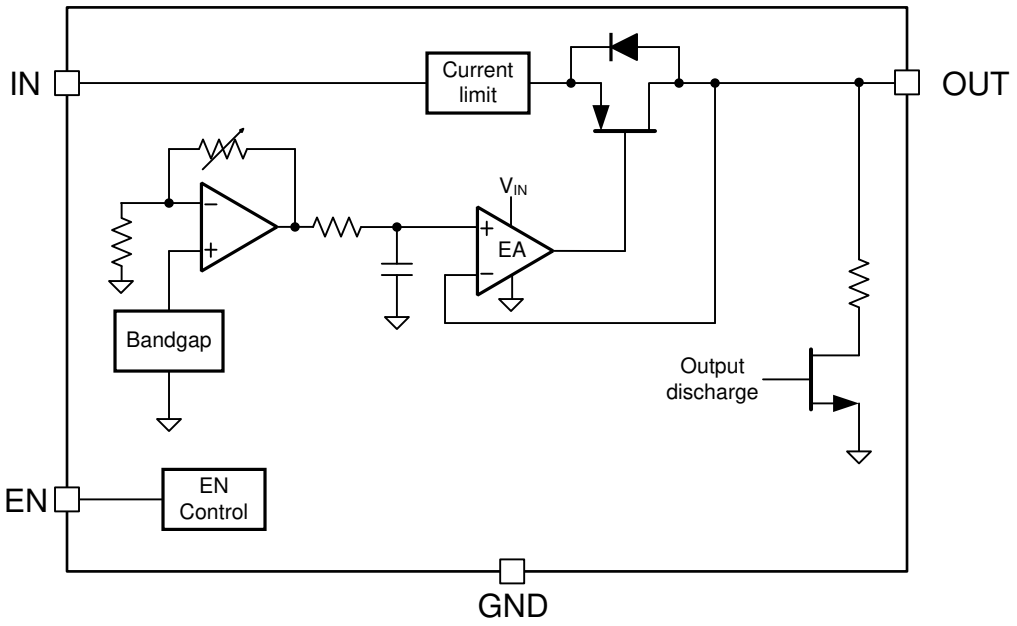
図 6-24. Line Transient Response

7 Detailed Description

7.1 Overview

The LP5910 is a linear regulator capable of supplying 300-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5910 device provides low noise, high PSRR, low quiescent current, and low line/load transient response figures. Using new innovative design techniques the LP5910 offers class-leading noise performance without a noise bypass capacitor and the option for remote output capacitor placement.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 No-Load Stability

The LP5910 remains stable and in regulation with no external load.

7.3.2 Thermal Overload Protection

The LP5910 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 160°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to 145°C (typical).

7.3.3 Short-Circuit Protection

The LP5910 contains internal current limit which reduces output current to a safe value if the output is overloaded or shorted. Depending upon the value of V_{IN}, thermal limiting may also become active as the average power dissipated causes the die temperature to increase to the limit value (about 160°C). The hysteresis of the thermal shutdown circuitry can result in a *cyclic* behavior on the output as the die temperature heats and cools.

7.3.4 Output Automatic Discharge

The LP5910 output employs an internal 160-Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

7.3.5 Reverse Current Protection

The device contains a reverse current protection circuit that prevents a backward current flowing through the LDO from the OUT pin to the IN pin.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5910 may be switched to the ON or OFF state by logic input at the EN pin. A logic-high voltage on the EN pin turns the device to the ON state. A logic-low voltage on the EN pin turns the device to the OFF state. If the application does not require the shutdown feature, the EN pin must be tied to VIN to keep the regulator output permanently in the ON state when power is applied

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the *Electrical Characteristics* section under V_{IL} and V_{IH}.

A 1-MΩ pulldown resistor ties the EN input to ground. If the EN pin is left open, the internal 1-MΩ pulldown resistor ensures that the device is turned into an OFF state by default.

When the EN pin is low, and the output is in an OFF state, the output activates an internal pulldown resistance to discharge the output capacitance for fast turnoff.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LP5910 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The LP5910 delivers this performance in an industry-standard DSBGA package which, for this device, is specified with a T_J of –40°C to +125°C.

8.2 Typical Application

図 8-1 shows the typical application circuit for the LP5910. Input and output capacitances may need to be increased above 1-µF minimum for some applications.

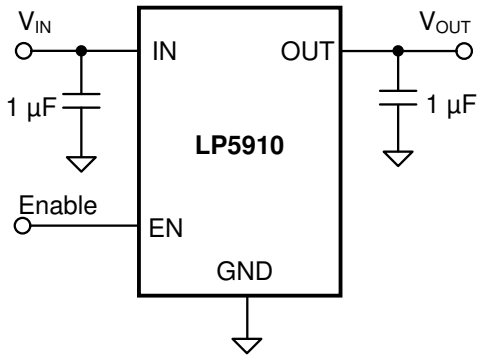


図 8-1. LP5910 Typical Application

8.2.1 Design Requirements

For typical LP5910 applications, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	1.3 V to 3.3 V
Output voltage	0.8 V to 2.3 V
Output current	300 mA
Output capacitor range	1 µF to 10 µF

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like most low-dropout regulators, the LP5910 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.2 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected from the LP5910 IN pin to ground. (This capacitance value may be increased without limit.) The input capacitor must be

located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Note

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains 1 µF ±30% over the entire operating temperature range.

8.2.2.3 Output Capacitor

For capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5910. The temperature performance of ceramic capacitors varies by type. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

8.2.2.4 Capacitor Characteristics

The LP5910 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5910.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 10-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. Also, the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.5 Remote Capacitor Operation

The LP5910 requires at least a 1-µF capacitor at the OUT pin, but there is no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the OUT pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, keep the wiring parasitic inductance at a minimum, using as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many vias as possible between the connection layers. It is recommended to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, an input capacitor is recommended, equal to or larger to the sum of the capacitance at the output node, for the best load-transient performance.

8.2.2.6 No-Load Stability

The LP5910 remains stable, and in regulation, with no external load.

8.2.2.7 Enable Control

The LP5910 may be switched to an ON or OFF state by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 µA. Additionally, an output pulldown circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-MΩ pulldown resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* under V_{IL} and V_{IH}.

表 8-2. Recommended Output Capacitor Specification

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Output capacitor, C_{OUT}	Capacitance for stability	0.7	1	10	µF
	ESR	5		500	mΩ

8.2.2.8 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with 式 1.

$$P_{D(MAX)} = (V_{IN(MAX)} – V_{OUT}) \times I_{OUT(MAX)} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (DRV) package, the primary conduction path for heat is through the exposed power pad to the PCB. To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area .

On the DSBGA (YKA) package, the primary conduction path for heat is through the four bumps to the PCB.

The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to 式 2 or 式 3:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.9 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with 式 4 or 式 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)}) \quad (4)$$

where

- $P_{D(MAX)}$ is explained in 式 1.
- T_{TOP} is the temperature measured at the center-top of the device package.

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)}) \quad (5)$$

where

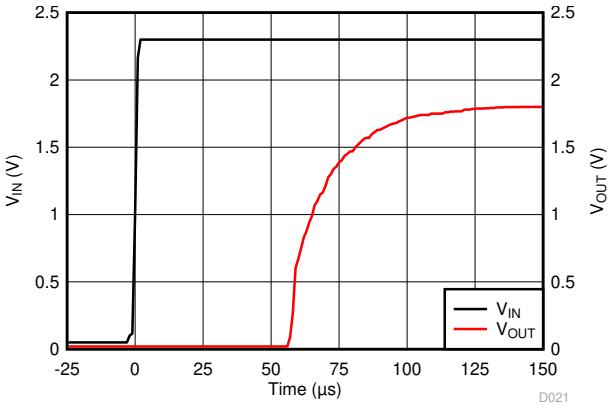
- $P_{D(MAX)}$ is explained in 式 1.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge.

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see the *Semiconductor and IC Package Thermal Metrics* application report, available for download at www.ti.com.

For more information about measuring T_{TOP} and T_{BOARD}, see the *Using New Thermal Metrics* application report, available for download at www.ti.com.

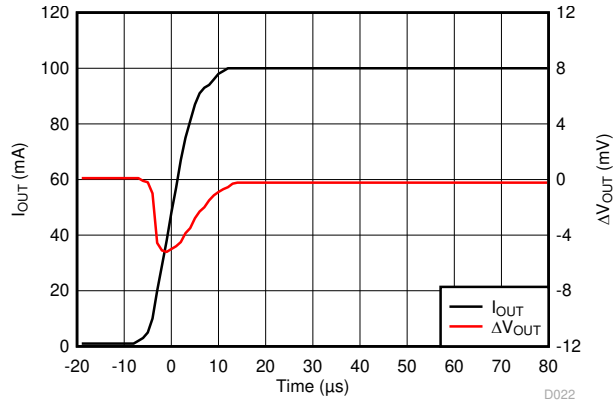
For more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application report, available for download at www.ti.com.

8.2.3 Application Curves



$V_{EN} = V_{IN}$ V_{OUT} = 1.8 V C_{OUT} = 1 µF

図 8-2. Turnon Time



V_{IN} = 2.3 V V_{OUT} = 1.8 V C_{OUT} = 1 µF
I_{OUT} = 1 mA to 100 mA t_{RISE} = 10 µs

図 8-3. Load Transient Response

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.3 V to 3.3 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5910 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 0.5 V.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5910 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5910.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5910 device, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP5910 GND pin using as wide and as short of a copper trace as is practical.

Avoid connections using long trace lengths, narrow trace widths, and/or connections through vias. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

10.1.1 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in the *DSBGA Wafer Level Chip Scale Package* application note. For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.1.2 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. High intensity light sources such as halogen lamps can affect electrical performance if they are situated in close proximity to the device. The wavelengths that have the most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has little effect on performance.

10.2 Layout Examples

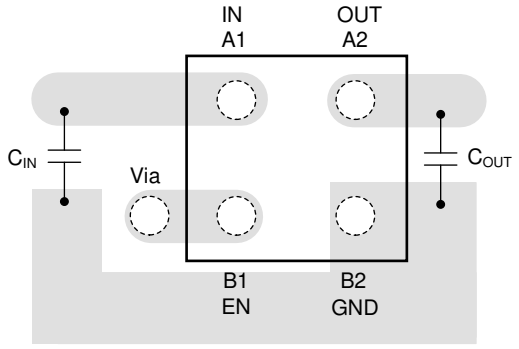


図 10-1. LP5910 Typical DSBGA Layout

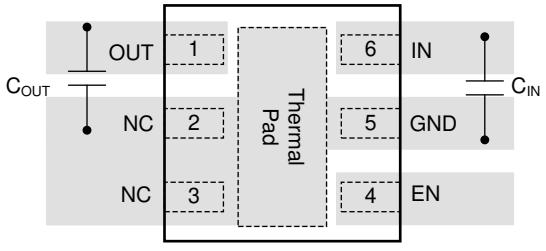


図 10-2. LP5910 Typical WSON Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5910-0.9YKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D
LP5910-0.9YKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D
LP5910-1.0DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59A
LP5910-1.0DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59A
LP5910-1.0YKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A
LP5910-1.0YKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A
LP5910-1.1BYKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
LP5910-1.1BYKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
LP5910-1.1BYKAT	Active	Production	DSBGA (YKA) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
LP5910-1.1BYKAT.B	Active	Production	DSBGA (YKA) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
LP5910-1.1YKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E
LP5910-1.1YKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E
LP5910-1.2YKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
LP5910-1.2YKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
LP5910-1.725YKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	N
LP5910-1.725YKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	N
LP5910-1.825YKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O
LP5910-1.825YKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O
LP5910-1.825YKAT	Active	Production	DSBGA (YKA) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O
LP5910-1.825YKAT.B	Active	Production	DSBGA (YKA) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O
LP5910-1.8DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C
LP5910-1.8DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C
LP5910-1.8DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C
LP5910-1.8DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C
LP5910-1.8DRVTG4	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C
LP5910-1.8DRVTG4.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	59C
LP5910-1.8YKAR	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
LP5910-1.8YKAR.B	Active	Production	DSBGA (YKA) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
LP5910-1.8YKAT	Active	Production	DSBGA (YKA) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5910-1.8YKAT.B	Active	Production	DSBGA (YKA) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

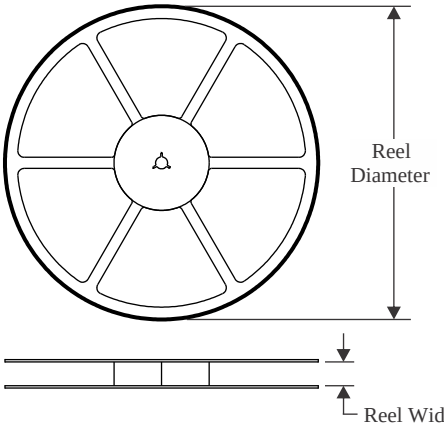
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

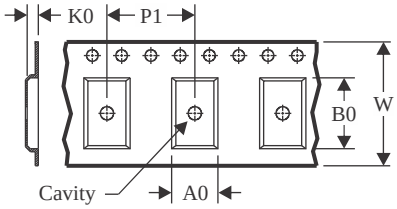
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

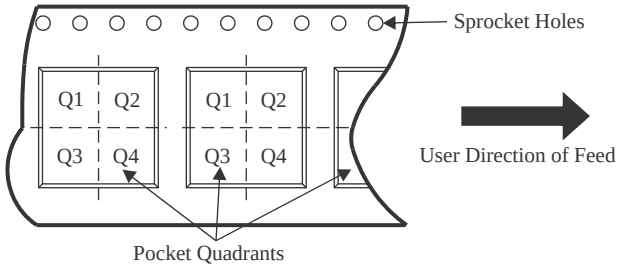


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

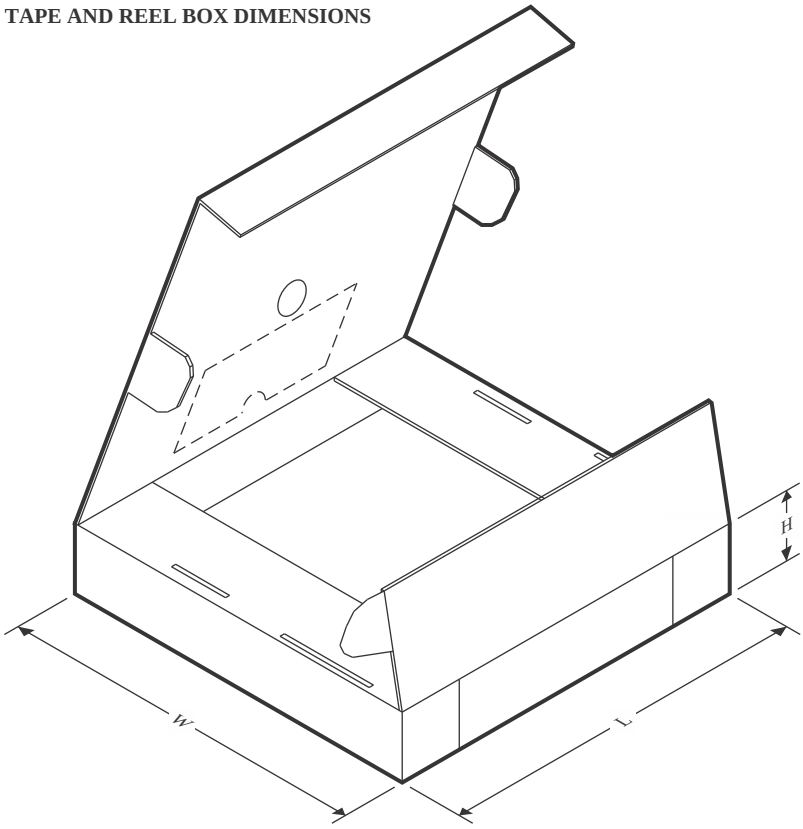
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5910-0.9YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	2.0	8.0	Q1
LP5910-1.0DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5910-1.0YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	2.0	8.0	Q1
LP5910-1.1BYKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.1BYKAT	DSBGA	YKA	4	250	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	2.0	8.0	Q1
LP5910-1.725YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.825YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.825YKAT	DSBGA	YKA	4	250	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.8DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5910-1.8DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5910-1.8DRVTG4	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LP5910-1.8YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1
LP5910-1.8YKAT	DSBGA	YKA	4	250	180.0	8.4	0.8	0.8	0.47	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

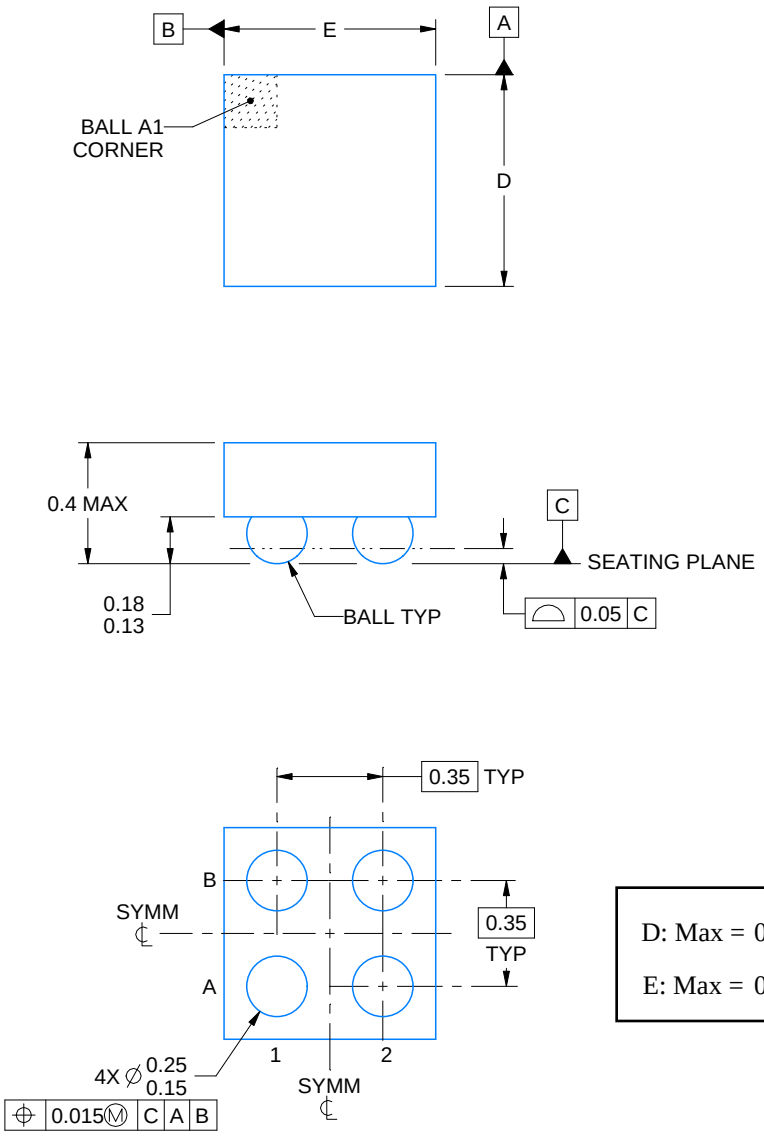
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5910-0.9YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.0DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
LP5910-1.0YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.1BYKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.1BYKAT	DSBGA	YKA	4	250	182.0	182.0	20.0
LP5910-1.1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.725YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.825YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.825YKAT	DSBGA	YKA	4	250	182.0	182.0	20.0
LP5910-1.8DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
LP5910-1.8DRVT	WSON	DRV	6	250	182.0	182.0	20.0
LP5910-1.8DRVTG4	WSON	DRV	6	250	182.0	182.0	20.0
LP5910-1.8YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
LP5910-1.8YKAT	DSBGA	YKA	4	250	182.0	182.0	20.0

PACKAGE OUTLINE

YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



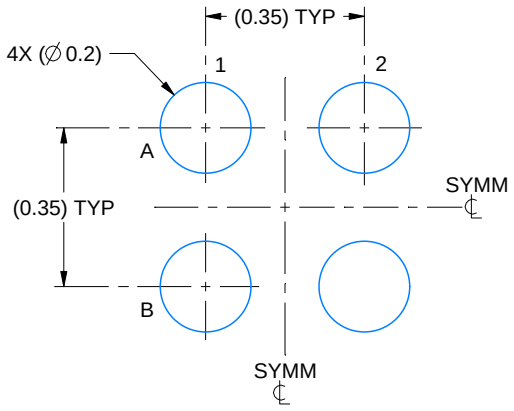
D: Max = 0.742 mm, Min =0.682 mm

E: Max = 0.742 mm, Min =0.682 mm

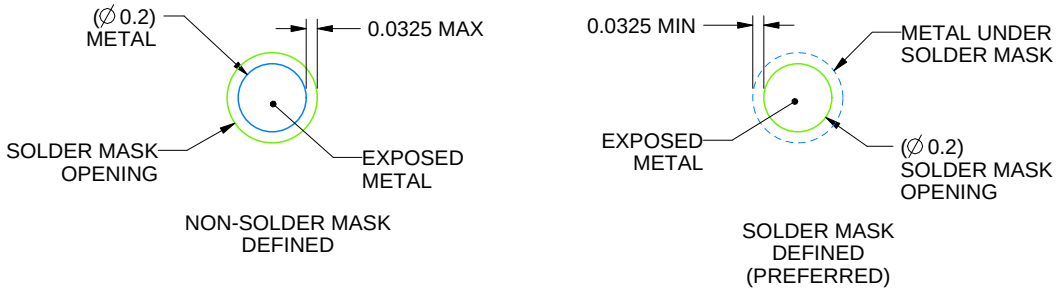
4221909/B 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

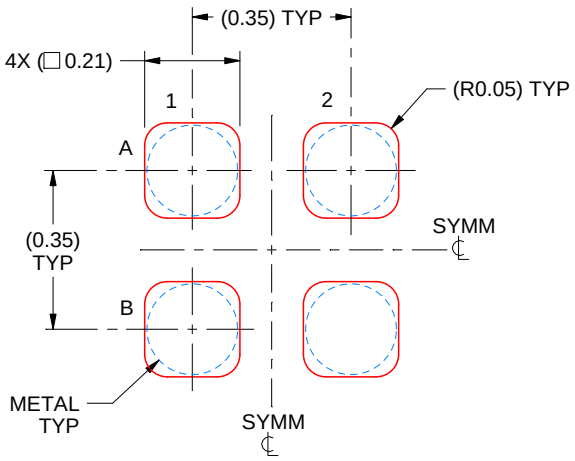


SOLDER MASK DETAILS
NOT TO SCALE

4221909/B 08/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

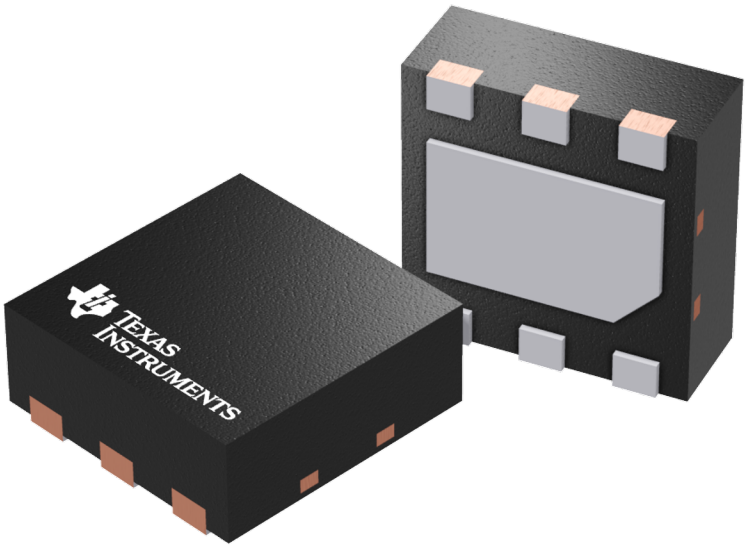
4221909/B 08/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

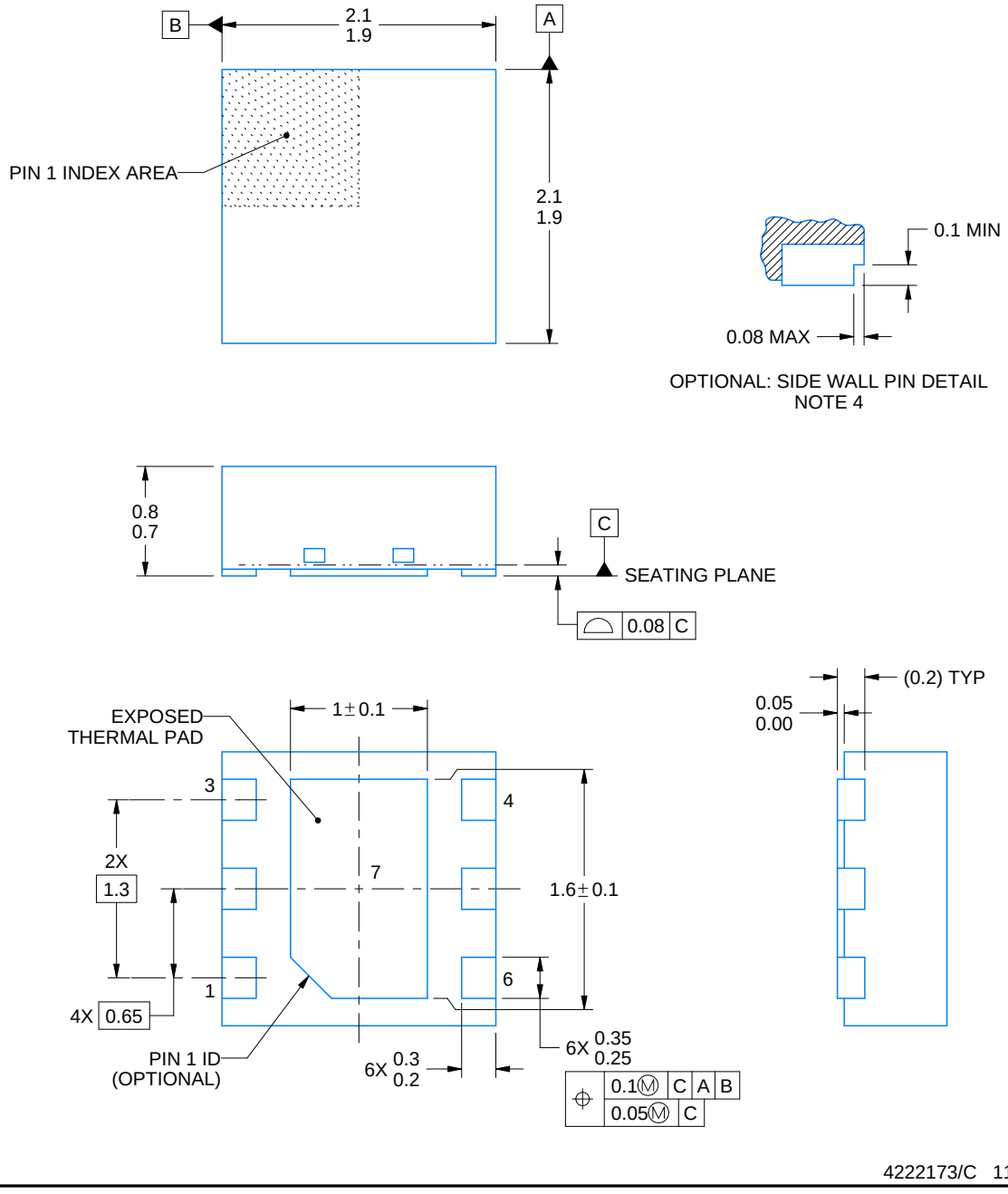
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



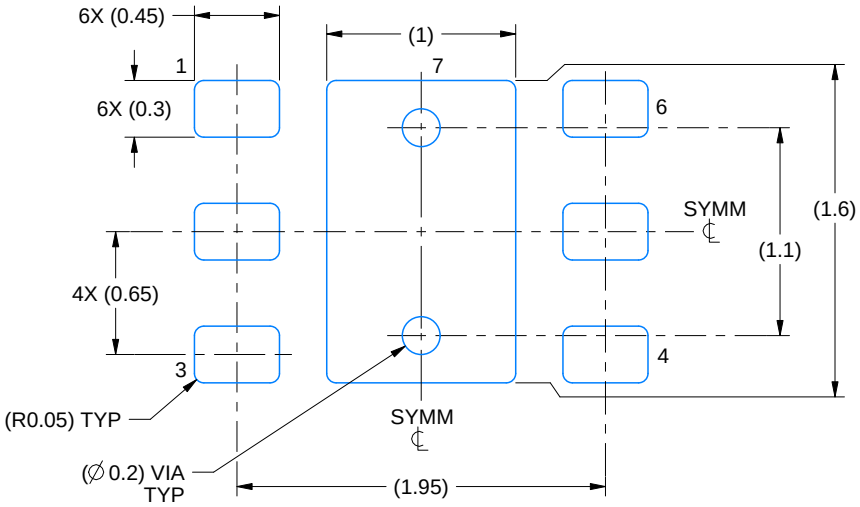
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

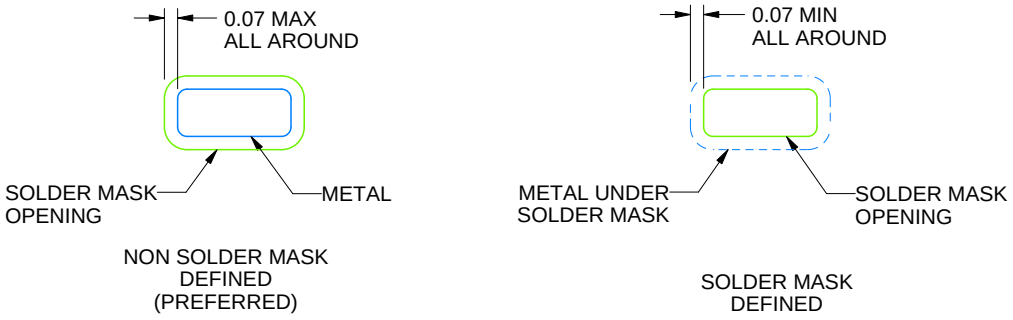


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

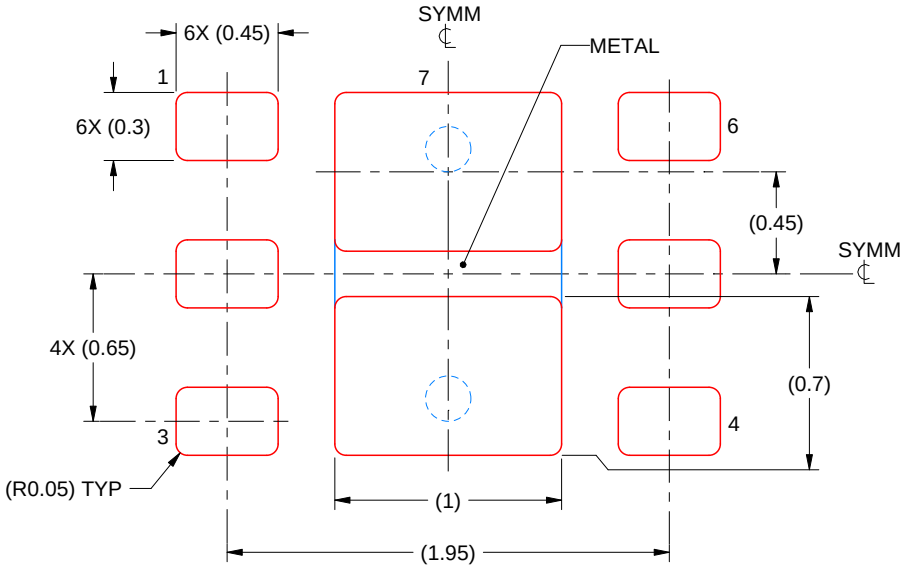


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月