LPV811/LPV812 高精度425nA Nanopowerオペアンプ

1 特長

- ナノパワー消費電流: チャネルごとに425nA
- オフセット電圧: 300µV (最大値)
- TcVos: 1µV/℃
- ゲイン帯域幅: 8kHz
- ユニティ・ゲインで安定
- 低い入力バイアス電流: 100fA
- 広い電源電圧範囲: 1.6V～5.5V
- レール・ツー・レール出力
- 出力反転なし
- EMI保護
- 温度範囲: -40℃～+125℃
- 業界標準パッケージ:
  - シングル: 5ピンSOT-23
  - デュアル: 8ピンVSSOP

2 アプリケーション

- COおよびO_2ガスの検出器(TIDA-0756)
- PIR動作検出器
- 電流検出
- サーモスタット
- IoTリモート・センサ
- アクティブRFIDリーダーおよびタグ
- 携帯型医療機器

3 概要

LPV811 (シングル)およびLPV812 (デュアル)は、バッテリ駆動のワイヤレスおよび低消費電力の有線機器における「常時オン」センシング・アプリケーションを対象とした、超低消費電力の高精度オペアンプ・ファミリです。425nAの静止電流からの8kHz帯域幅、および300µV未満にトリムされたオフセット電圧により、LPV81xアンプはガス検出器や携帯用電子機器など、バッテリ動作時間が重要な機器において、要求される精度を実現しながら、消費電力を最小化できます。

超低消費電力に加えて、LPV81xアンプにはCMOS入力段があり、インピーダンス源のアプリケーションについてバイアス電流がフェムトアンペア単位です。またLPV81xアンプには、負のレール・センシング入力段とレール・ツー・レール出力段が搭載されており、レールから数mVの範囲内までスイング可能で、可能な限り最も広いダイナミック・レンジを維持できます。LPV81xの設計には、携帯電話、WiFi、ラジオ送信機、タグ・リーダーからの不要なRF信号に対するシステムの感受性を低下させるため、EMI保護が組み込まれています。

製品情報(1)

型番	パッケージ	本体サイズ
LPV811	SOT-23 (5)	2.90mm×1.60mm
LPV812	VSSOP (8)	3.00mm×3.00mm

LPV8xxファミリのNanopowerアンプ

型番	チャネル	消費電流 (標準値 /チャネル)	オフセット 電圧 (最大値)
LPV801	1	500nA	3.5mV
LPV802	2	320nA	3.5mV
LPV811	1	450nA	370µV
LPV812	2	425nA	300µV

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

図 1. NanoPower COセンサ

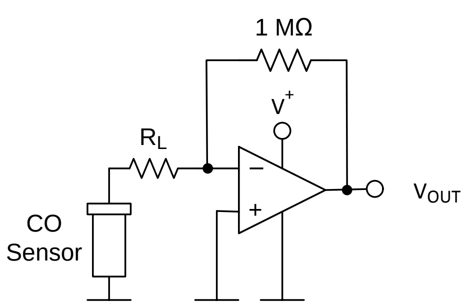
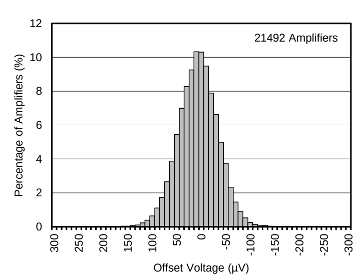


図 2. LPV812のオフセット電圧分布



English Data Sheet: SNOSD33

目次

4 改訂履歴

Revision A (October 2016) から **Revision B** に変更 — **Page**

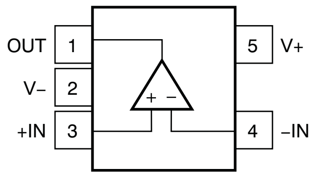
- 表紙にファミリのアップセル表を 追加 ... 1
- 表紙のO2センシング回路をオフセット電圧分布のグラフに 変更 ... 1
- 大きなファミリのアップセル表を 削除 ... 2
- Deleted LPV811 preview "preliminary spec" table note. ... 5
- Added separate LPV811 CMRR Specification. ... 5
- Added offset distribution graphs ... 6

2016年8月発行のものから更新 — **Page**

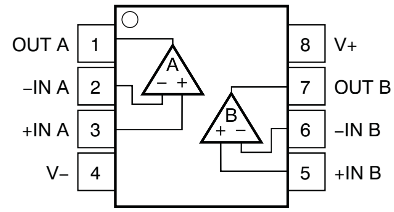
- 製品プレビューから量産データへ 変更 ... 1

5 Pin Configuration and Functions

LPV811 5-Pin SOT-23
DBV Package
Top View



LPV812 8-Pin VSSOP
DGK Package
Top View



Pin Functions: LPV811 DBV

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Output
-IN	4	I	Inverting Input
+IN	3	I	Non-Inverting Input
V-	2	P	Negative (lowest) power supply
V+	5	P	Positive (highest) power supply

Pin Functions: LPV812 DGK

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_s = (V+) - (V-)			–0.3	6	V
Input pins	Voltage (2) (3)	Common mode	(V-) - 0.3	(V+) + 0.3	V
		Differential	(V-) - 0.3	(V+) + 0.3	V
Input pins	Current		-10	10	mA
Output short current (4)			Continuous	Continuous	
Storage temperature, T_{stg}			–65	150	°C
Junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not to exceed -0.3V or +6.0V on ANY pin, referred to V-
(3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(4) Short-circuit to Vs/2, one amplifier per package. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage (V+ – V–)	1.6	5.5	V
Specified temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LPV811 DBV (SOT-23) 5 PINS	LPV812 DGK (VSSOP) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	177.4	177.6	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	133.9	68.8	
θ_{JB}	Junction-to-board thermal resistance	36.3	98.2	
ψ_{JT}	Junction-to-top characterization parameter	23.6	12.3	
ψ_{JB}	Junction-to-board characterization parameter	35.7	96.7	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

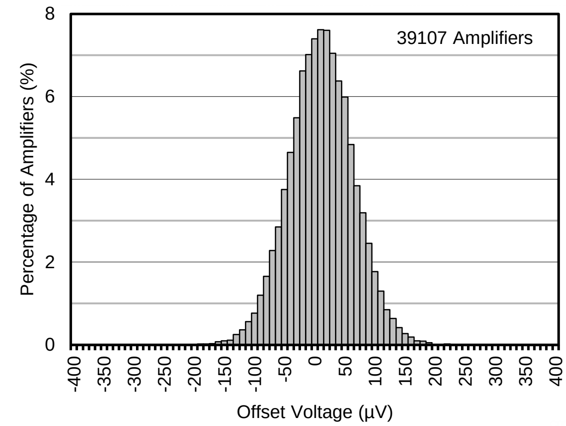
6.5 Electrical Characteristics

T_A = 25°C, V_S = 1.8 V to 5 V, V_{CM} = V_{OUT} = V_S/2, and R_L≥ 10 MΩ to V_S / 2, unless otherwise noted .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage, LPV811	V_S = 1.8V and 3.3V, V_{CM} = V-		±60	±370	µV
	Input offset voltage, LPV812	V_S = 1.8V and 3.3V, V_{CM} = V-		±55	±300	µV
$\Delta V_{OS}/\Delta T$	Input offset drift	V_{CM} = V-, T_A = –40°C to 125°C		±1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8V to 3.3V, V_{CM} = V-		±1.6	±60	µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 3.3V	0		2.4	V
CMRR	Common-mode rejection ratio, LPV811	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S = 3.3V	77	95		dB
	Common-mode rejection ratio, LPV812	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S = 3.3V	80	98		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 1.8V		±100		fA
I_{OS}	Input offset current	V_S = 1.8V		±100		fA
INPUT IMPEDANCE						
	Differential			7		pF
	Common mode			3		pF
NOISE						
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz		6.5		µVp-p
e_n	Input voltage noise density	f = 100 Hz		340		nV/√Hz
		f = 1 kHz		420		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V ≤ V_O ≤ (V+) – 0.3 V, R_L = 100 kΩ		120		dB
OUTPUT						
V_{OH}	Voltage output swing from positive rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2	10	3.5		mV
V_{OL}	Voltage output swing from negative rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2		2.5	10	
I_{SC}	Short-circuit current	V_S = 3.3V, Short to V_S/2		4.7		mA
Z_O	Open loop output impedance	f = 1 KHz, I_O = 0 A		90		kΩ
FREQUENCY RESPONSE						
GBP	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ, V_S = 5V		8		kHz
SR	Slew rate (10% to 90%)	G = 1, Rising Edge, C_L = 20 pF, V_S = 5V		2		V/ms
		G = 1, Falling Edge, C_L = 20 pF, V_S = 5V		2.1		
POWER SUPPLY						
I_Q	Quiescent Current, LPV811	V_{CM} = V-, I_O = 0, V_S = 3.3V		450	540	nA
	Quiescent Current, Per Channel, LPV812	V_{CM} = V-, I_O = 0, V_S = 3.3V		425	495	

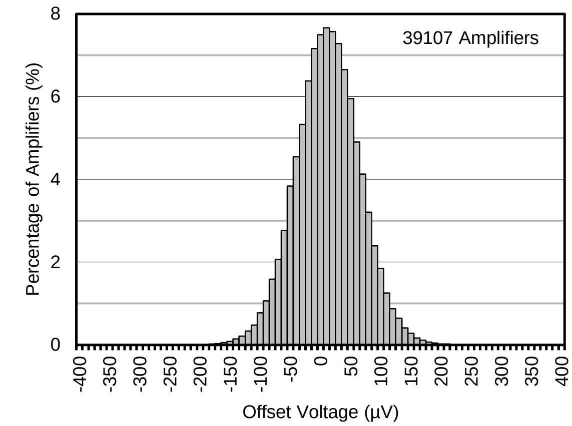
6.6 Typical Characteristics

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



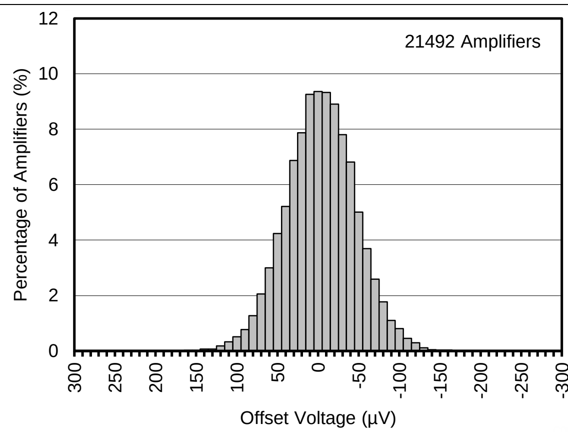
V_S = 1.8V LPV811
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 3. Offset Distribution of LPV811



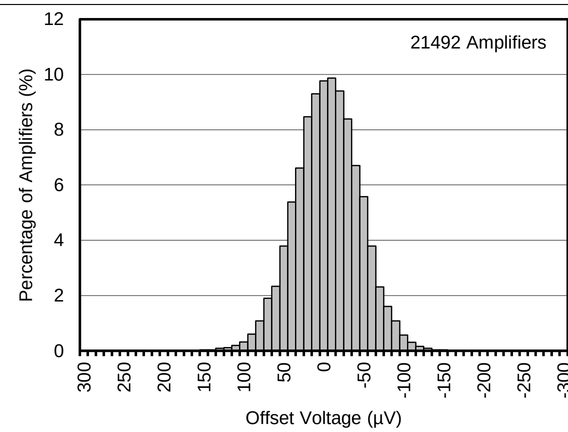
V_S = 3.3V LPV811
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 4. Offset Distribution of LPV811



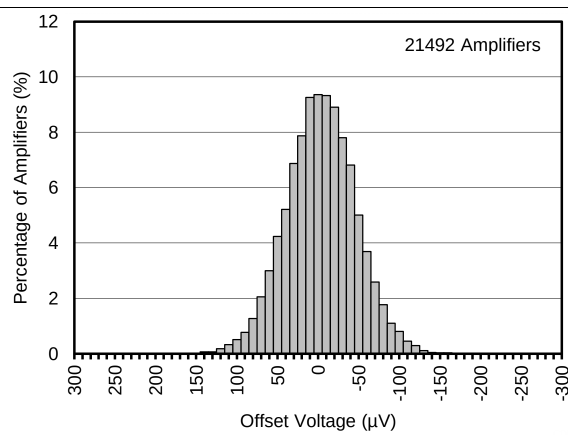
V_S = 1.8V LPV812, Channel A
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 5. Offset Distribution of LPV812, CH A



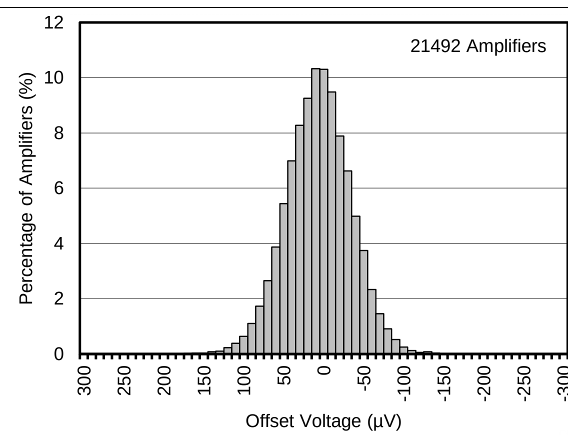
V_S = 3.3V LPV812, Channel A
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 6. Offset Distribution of LPV812, CH A



V_S =1.8V LPV812, Channel B
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 7. Offset Distribution of LPV812, CH B



V_S = 3.3V LPV812, Channel B
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 8. Offset Distribution of LPV812, CH B

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.

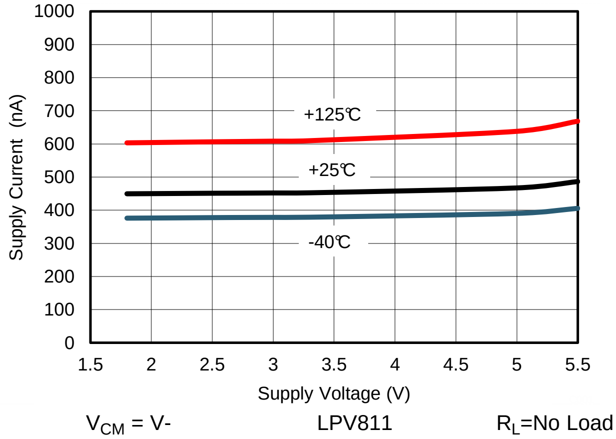


Figure 9. Supply Current vs. Supply Voltage, LPV811

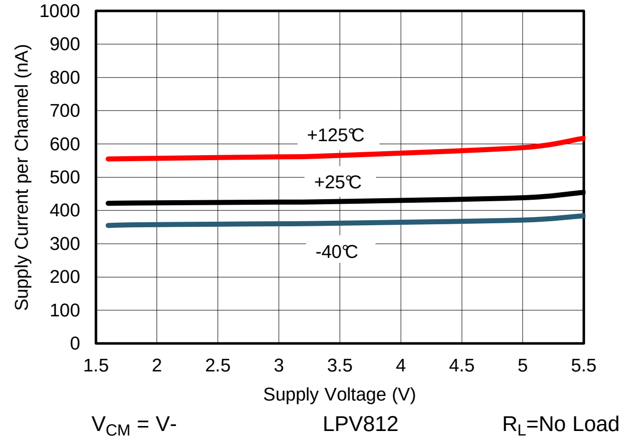


Figure 10. Supply Current vs. Supply Voltage, LPV812

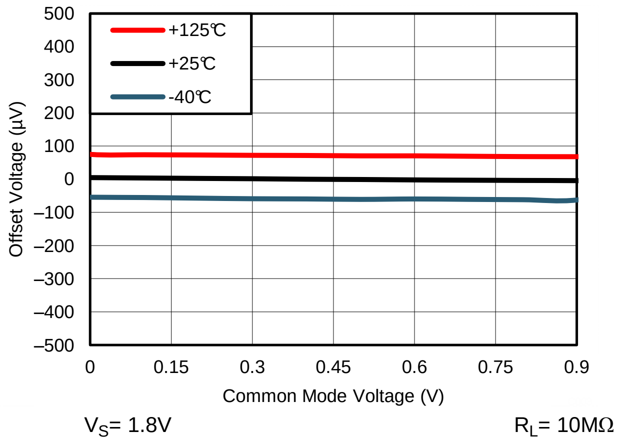


Figure 11. Typical Offset Voltage vs. Common Mode Voltage

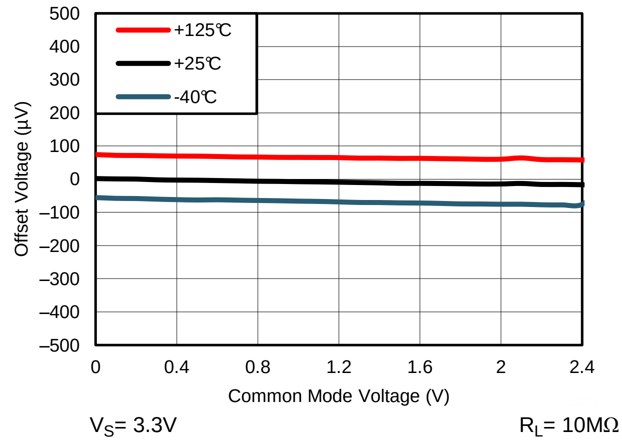


Figure 12. Typical Offset Voltage vs. Common Mode Voltage

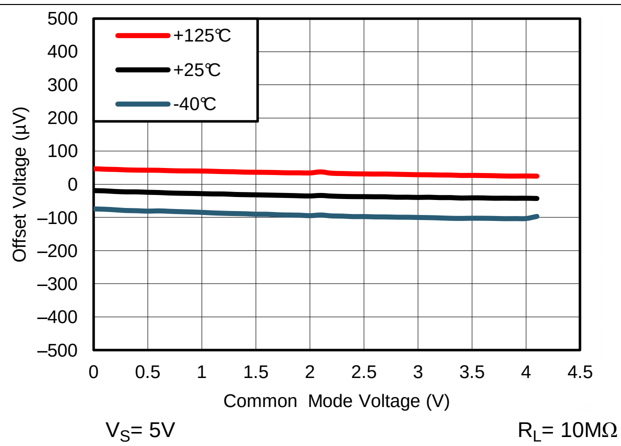


Figure 13. Typical Offset Voltage vs. Common Mode Voltage

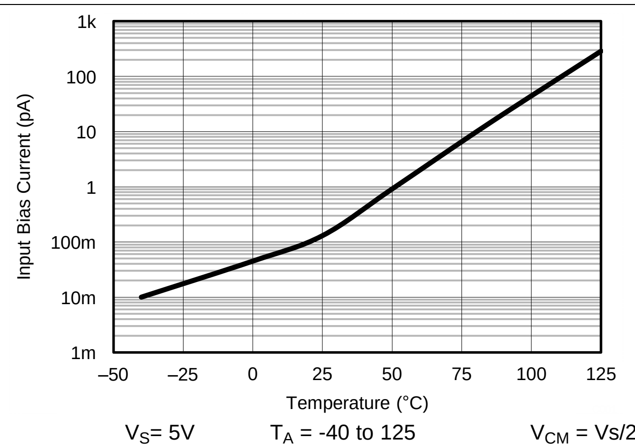
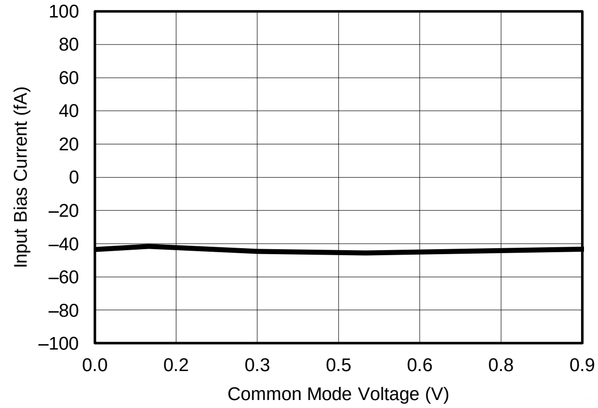


Figure 14. Input Bias Current vs. Temperature

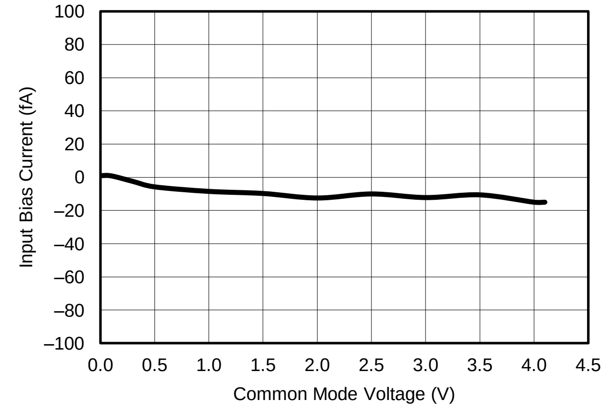
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



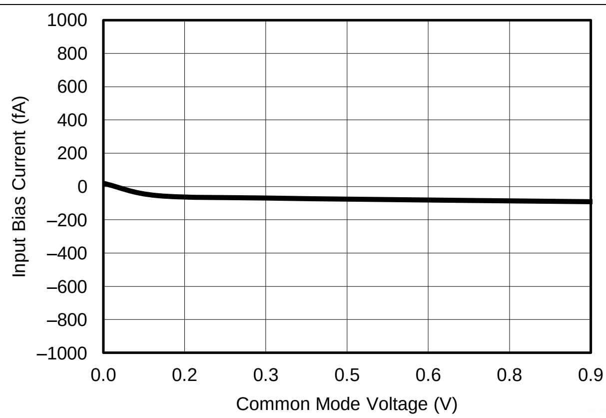
V_S= 1.8V T_A = -40°C

Figure 15. Input Bias Current vs. Common Mode Voltage



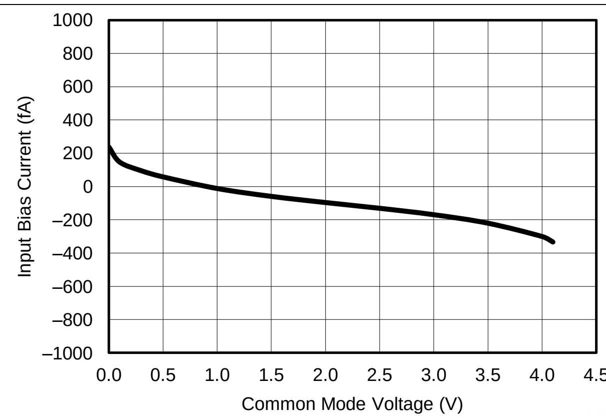
V_S= 5V T_A = -40°C

Figure 16. Input Bias Current vs. Common Mode Voltage



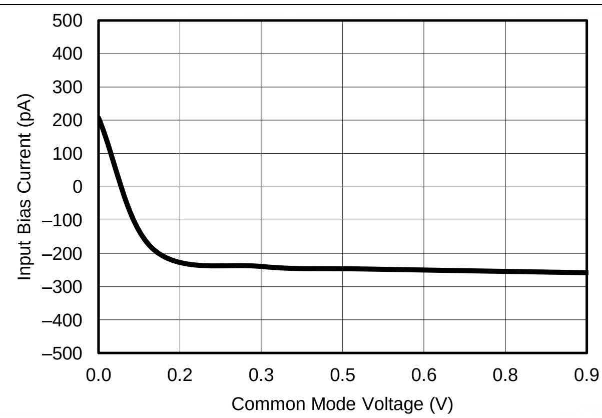
V_S= 1.8V T_A = 25°C

Figure 17. Input Bias Current vs. Common Mode Voltage



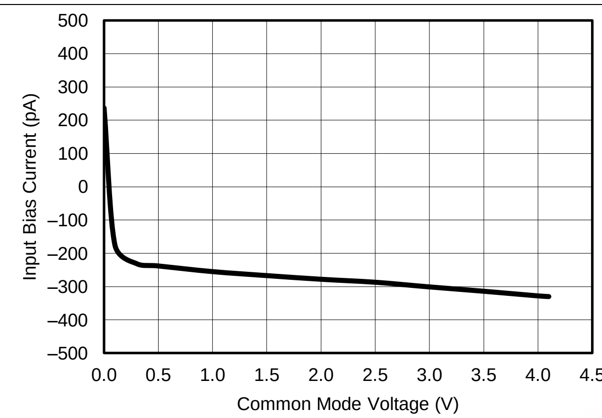
V_S= 5V T_A = 25°C

Figure 18. Input Bias Current vs. Common Mode Voltage



V_S= 1.8V T_A = 125°C

Figure 19. Input Bias Current vs. Common Mode Voltage



V_S= 5V T_A = 125°C

Figure 20. Input Bias Current vs. Common Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.

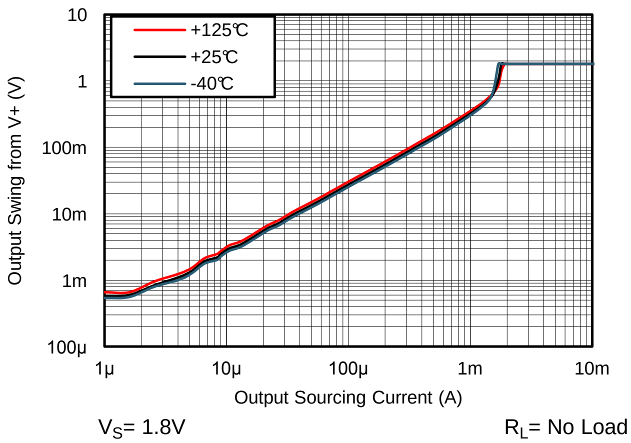


Figure 21. Output Swing vs. Sourcing Current, 1.8V

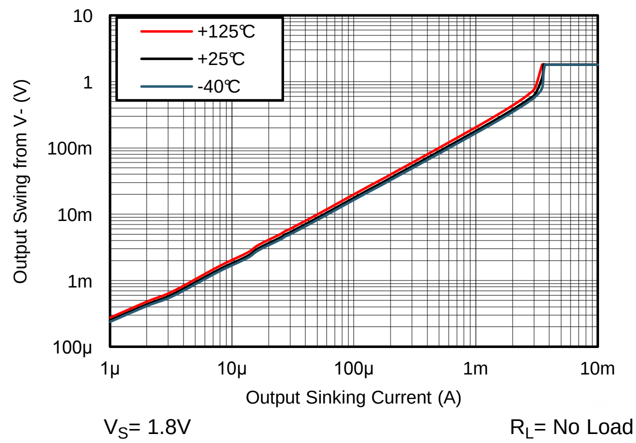


Figure 22. Output Swing vs. Sinking Current, 1.8V

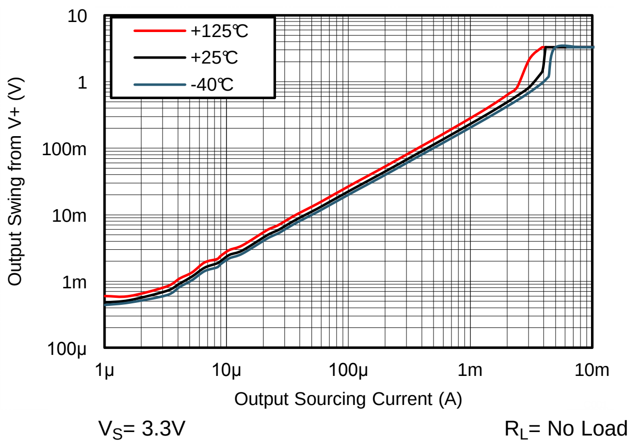


Figure 23. Output Swing vs. Sourcing Current, 3.3V

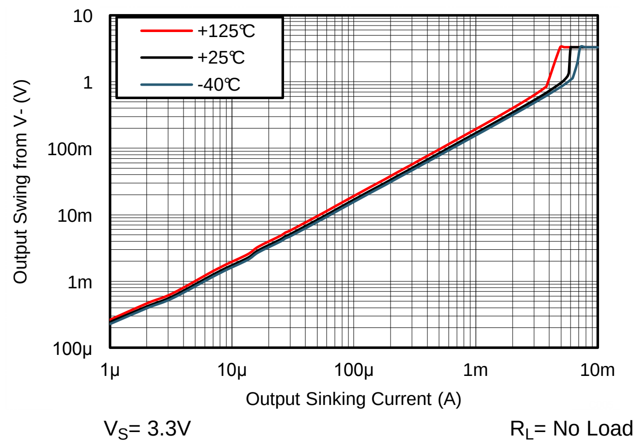


Figure 24. Output Swing vs. Sinking Current, 3.3V

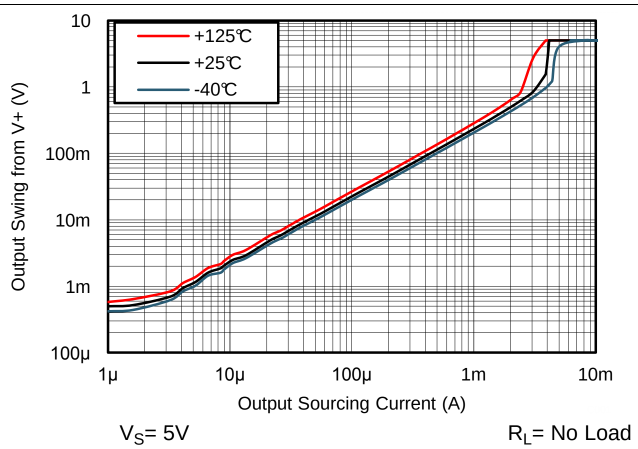


Figure 25. Output Swing vs. Sourcing Current, 5V

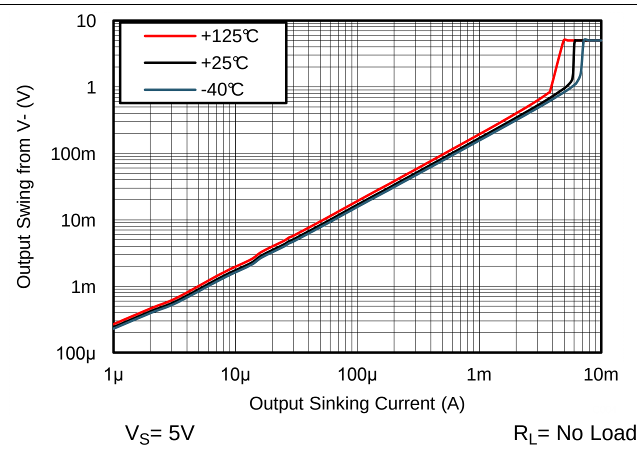


Figure 26. Output Swing vs. Sinking Current, 5V

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.

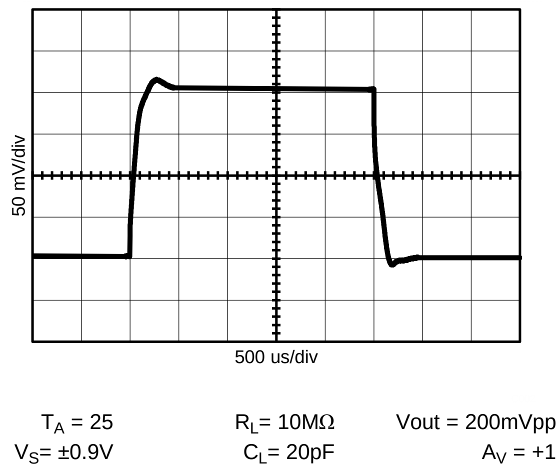


Figure 27. Small Signal Pulse Response, 1.8V

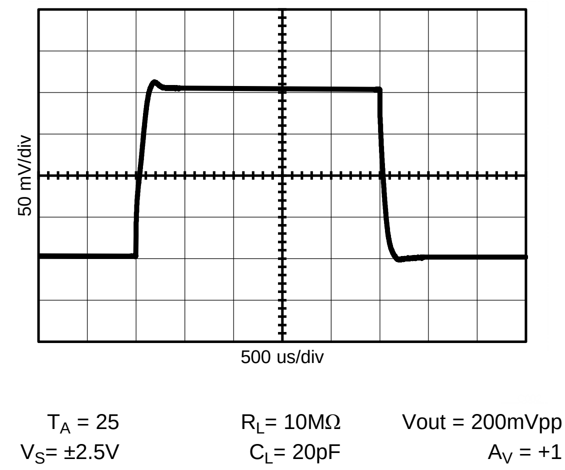


Figure 28. Small Signal Pulse Response, 5V

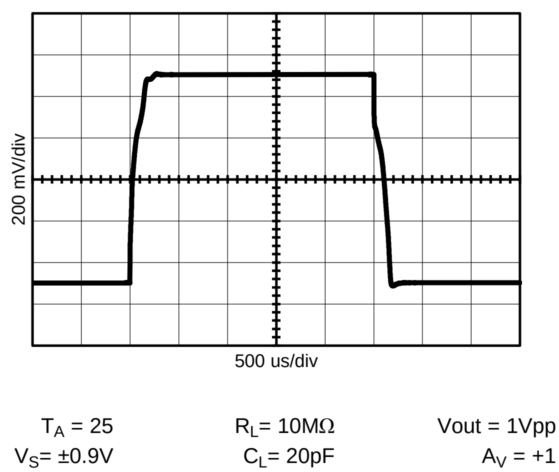


Figure 29. Large Signal Pulse Response, 1.8V

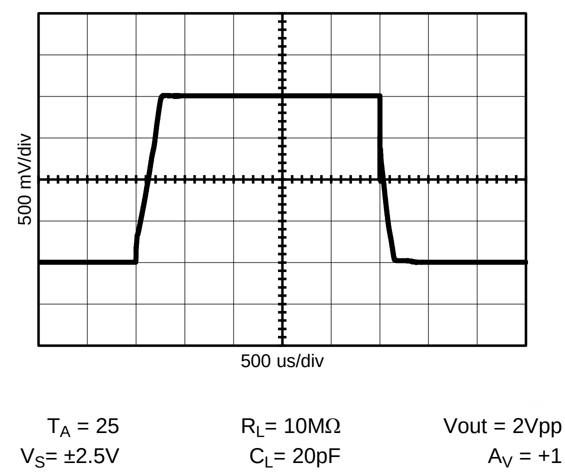


Figure 30. Large Signal Pulse Response, 5V

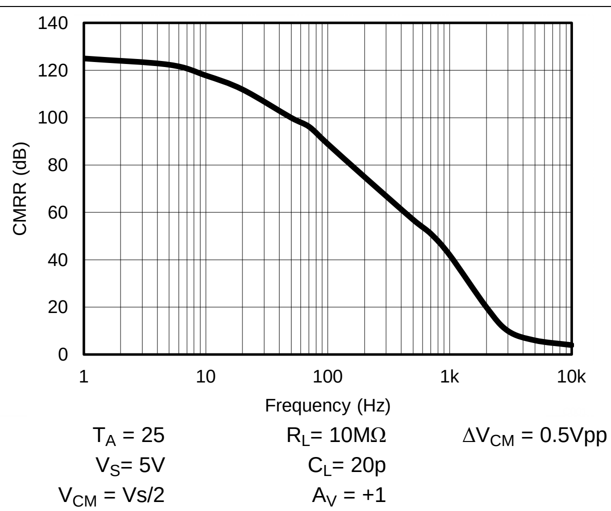


Figure 31. CMRR vs Frequency

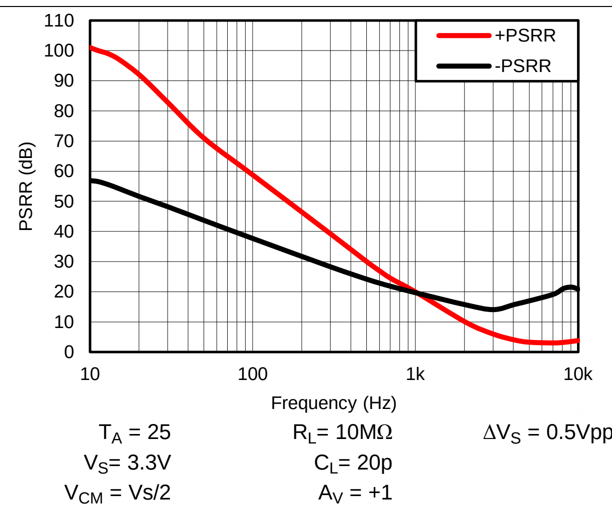
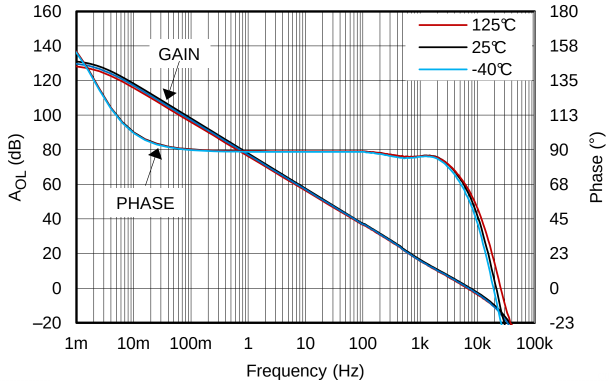


Figure 32. ±PSRR vs Frequency

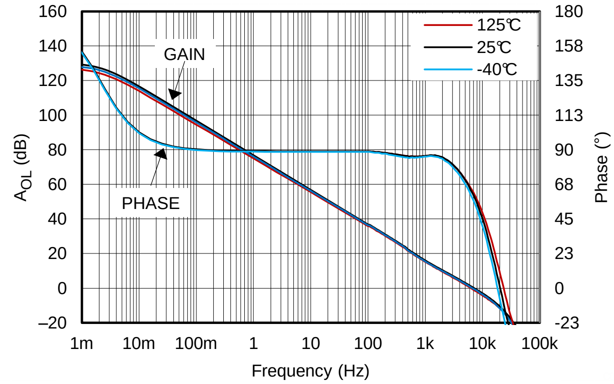
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



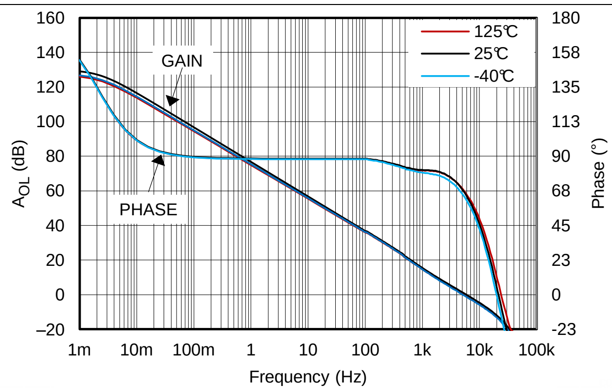
T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV$_{PP}$
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 33. Open Loop Gain and Phase, 5V, 10 MΩ Load



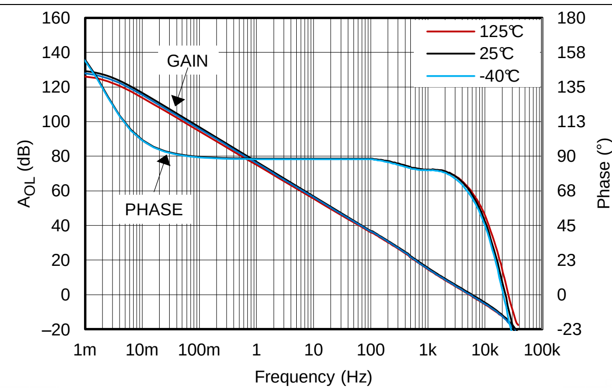
T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV$_{PP}$
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 34. Open Loop Gain and Phase, 3.3V, 10 MΩ Load



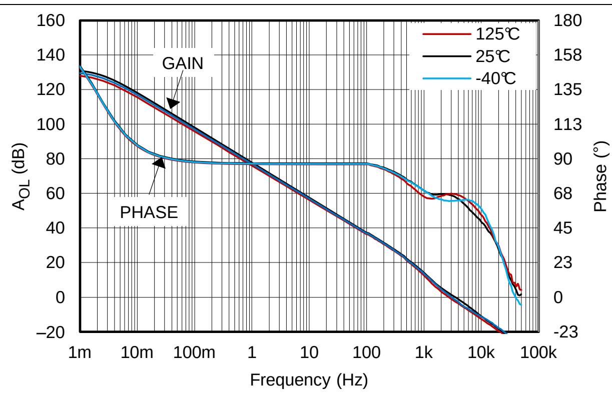
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV$_{PP}$
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 35. Open Loop Gain and Phase, 5V, 1 MΩ Load



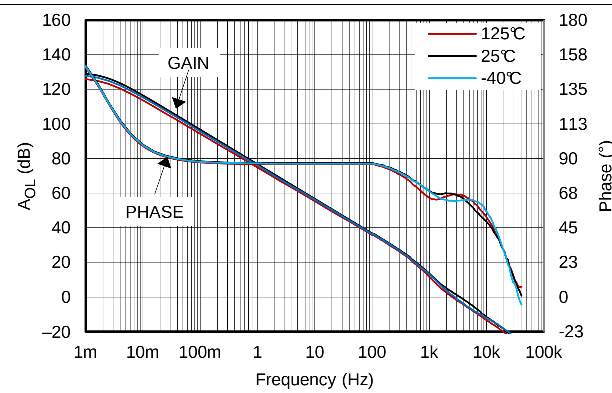
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV$_{PP}$
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 36. Open Loop Gain and Phase, 3.3V, 1 MΩ Load



T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV$_{PP}$
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 37. Open Loop Gain and Phase, 5V, 100kΩ Load

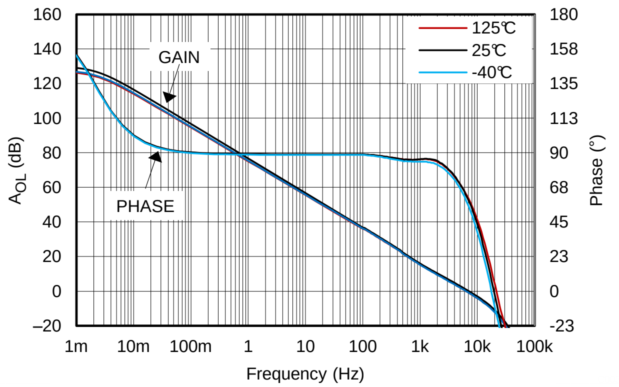


T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV$_{PP}$
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 38. Open Loop Gain and Phase, 3.3V, 100kΩ Load

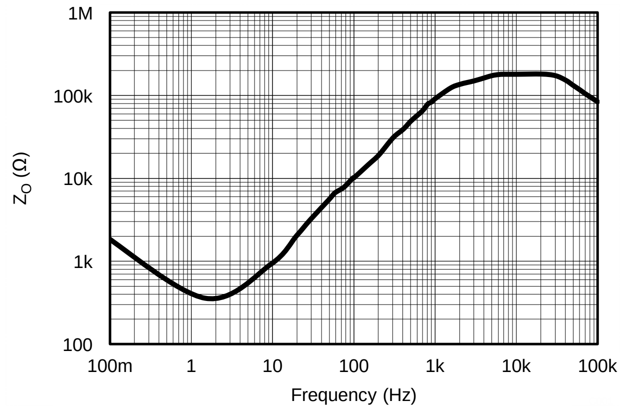
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



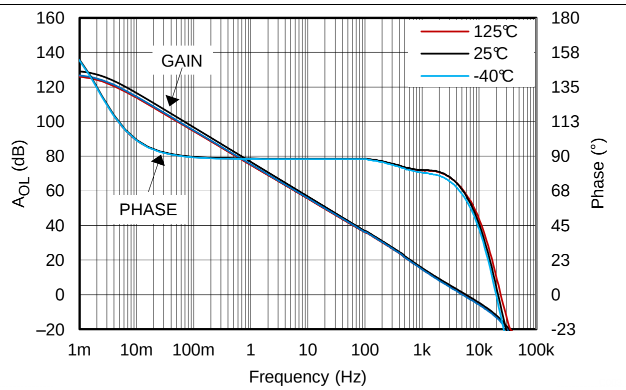
T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV$_{PP}$
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 39. Open Loop Gain and Phase, 1.8V, 10 MΩ Load



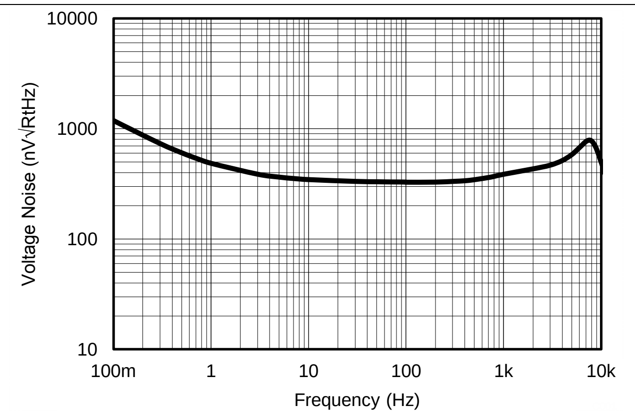
T_A = 25°C V_S= 5 V R_L= 10MΩ

Figure 40. Open Loop Output Impedance



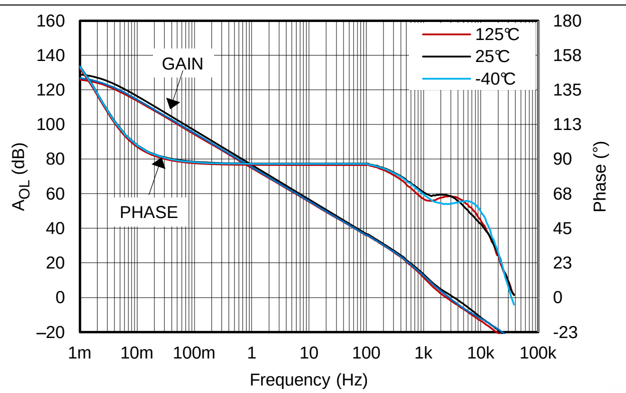
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV$_{PP}$
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 41. Open Loop Gain and Phase, 1.8V, 1 MΩ Load



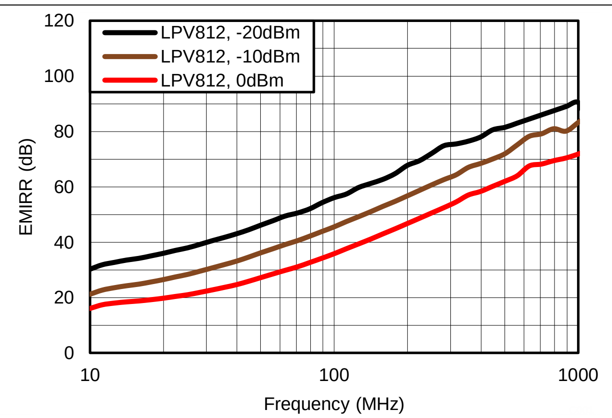
T_A = 25 R_L= 1MΩ V_{CM} = Vs/2
V_S= 5V C_L= 20pF A_V = +1

Figure 42. Input Voltage Noise vs Frequency



T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV$_{PP}$
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 43. Open Loop Gain and Phase, 1.8V, 100kΩ Load



T_A = 25 R_L= 1MΩ V_{CM} = Vs/2
V_S= 3.3V C_L= 20pF A_V = +1

Figure 44. EMIRR Performance

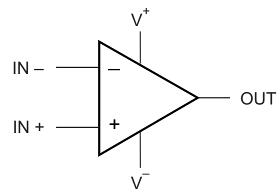
7 Detailed Description

7.1 Overview

The LPV811 (single) and LPV812 (dual) series of nanoPower CMOS operational amplifiers are designed for long-life battery-powered and energy harvested applications. They operate on a single supply with operation as low as 1.6V. The Input Offset is trimmed to less than 300uV and the output is rail-to-rail and swings to within 3.5mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply making it ideal for single-supply applications. EMI protection has been employed internally to reduce the effects of EMI.

Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^{+} - IN^{-})$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 120 dB (1,000,000x, or 1,000,000 Volts per microvolt). (1)

7.4 Device Functional Modes

7.4.1 Negative-Rail Sensing Input

The input common-mode voltage range of the LPV81x extends from (V-) to (V+) – 0.9 V. In this range, low offset can be expected with a minimum of 77dB CMRR. The LPV81x is protected from output "inversions" or "reversals".

7.4.2 Rail to Rail Output Stage

The LPV81x output voltage swings 3.5 mV from rails at 1.8 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV81x Maximum Output Voltage Swing graph defines the maximum swing possible under a particular output load.

7.4.3 Design Optimization for Nanopower Operation

When designing for ultra-low power, choose system feedback components carefully. To minimize quiescent current consumption, select large-value feedback resistors. Any large resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electrolytics may have large static leakage currents in the nanoamps.

Device Functional Modes (continued)

7.4.4 Driving Capacitive Load

The LPV81x is internally compensated for stable unity gain operation, with a 8 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (>50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 45. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive. The recommended value for R_{ISO} is 30-50kΩ.

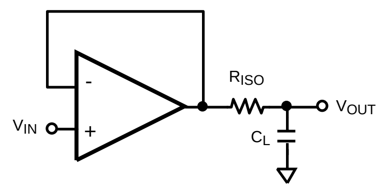


Figure 45. Resistive Isolation Of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV81x is a ultra-low power operational amplifier that provides 8 kHz bandwidth with only 425nA typical quiescent current, trimmed input offset voltage and precision drift specifications. These rail-to-rail output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the negative supply rail and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

8.2 Typical Application: Three Terminal CO Gas Sensor Amplifier

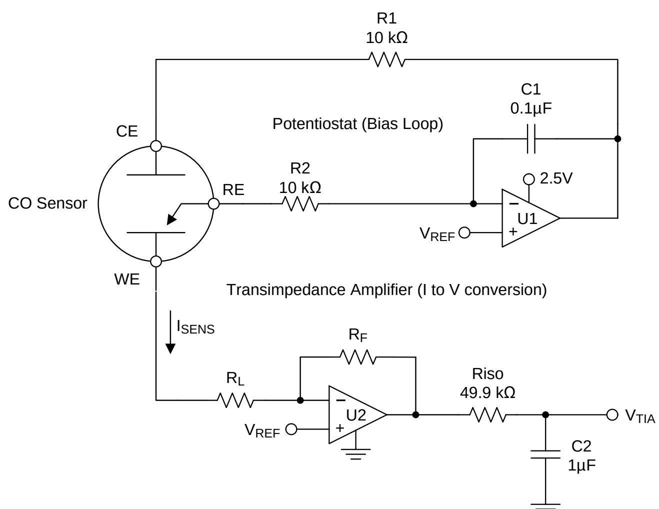


Figure 46. Three Terminal Gas Sensor Amplifier Schematic

8.2.1 Design Requirements

Figure 46 shows a simple micropower potentiostat circuit for use with three terminal unbiased CO sensors, though it is applicable to many other type of three terminal gas sensors or electrochemical cells.

The basic sensor has three electrodes; The Sense or Working Electrode ("WE"), Counter Electrode ("CE") and Reference Electrode ("RE"). A current flows between the CE and WE proportional to the detected concentration.

The RE monitors the potential of the internal reference point. For an unbiased sensor, the WE and RE electrodes must be maintained at the same potential by adjusting the bias on CE. Through the Potentiostat circuit formed by U1, the servo feedback action will maintain the RE pin at a potential set by V_{REF}.

R1 is to maintain stability due to the large capacitance of the sensor. C1 and R2 form the Potentiostat integrator and set the feedback time constant.

U2 forms a transimpedance amplifier ("TIA") to convert the resulting sensor current into a proportional voltage. The transimpedance gain, and resulting sensitivity, is set by R_F according to Equation 2.

$$V_{TIA} = (-I * R_F) + V_{REF} \tag{2}$$

R_L is a load resistor of which the value is normally specified by the sensor manufacturer (typically 10 ohms). The potential at WE is set by the applied $V_{REF.}$ Riso provides capacitive isolation and, combined with C2, form the output filter and ADC reservoir capacitor to drive the ADC.

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.2 Detailed Design Procedure

For this example, we will be using a CO sensor with a sensitivity of 69nA/ppm. The supply voltage and maximum ADC input voltage is 2.5V, and the maximum concentration is 300ppm.

First the V_{REF} voltage must be determined. This voltage is a compromise between maximum headroom and resolution, as well as allowance for "footroom" for the minimum swing on the CE terminal, since the CE terminal generally goes negative in relation to the RE potential as the concentration (sensor current) increases. Bench measurements found the difference between CE and RE to be 180mV at 300ppm for this particular sensor.

To allow for negative CE swing "footroom" and voltage drop across the 10k resistor, 300mV was chosen for V_{REF}.

Therefore +300mV will be used as the minimum V_{ZERO} to add some headroom.

$V_{ZERO} = V_{REF} = +300mV$

where

- V_{ZERO} is the zero concentration voltage
- V_{REF} is the reference voltage (300mV) (3)

Next we calculate the maximum sensor current at highest expected concentration:

$I_{SENSMAX} = I_{PERPPM} * ppmMAX = 69nA * 300ppm = 20.7uA$

where

- $I_{SENSMAX}$ is the maximum expected sensor current
- I_{PERPPM} is the manufacturer specified sensor current in Amps per ppm
- ppmMAX is the maximum required ppm reading (4)

Now find the available output swing range above the reference voltage available for the measurement:

$V_{SWING} = V_{OUTMAX} – V_{ZERO} = 2.5V – 0.3V = 2.2V$

where

- V_{SWING} is the expected change in output voltage
- V_{OUTMAX} is the maximum amplifier output swing (usually near V+) (5)

Now we calculate the transimpedance resistor ®$_F$) value using the maximum swing and the maximum sensor current:

$R_F = V_{SWING} / I_{SENSMAX} = 2.2V / 20.7µA = 106.28 kΩ$ (we will use 110 kΩ for a common value) (6)

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.3 Application Curve

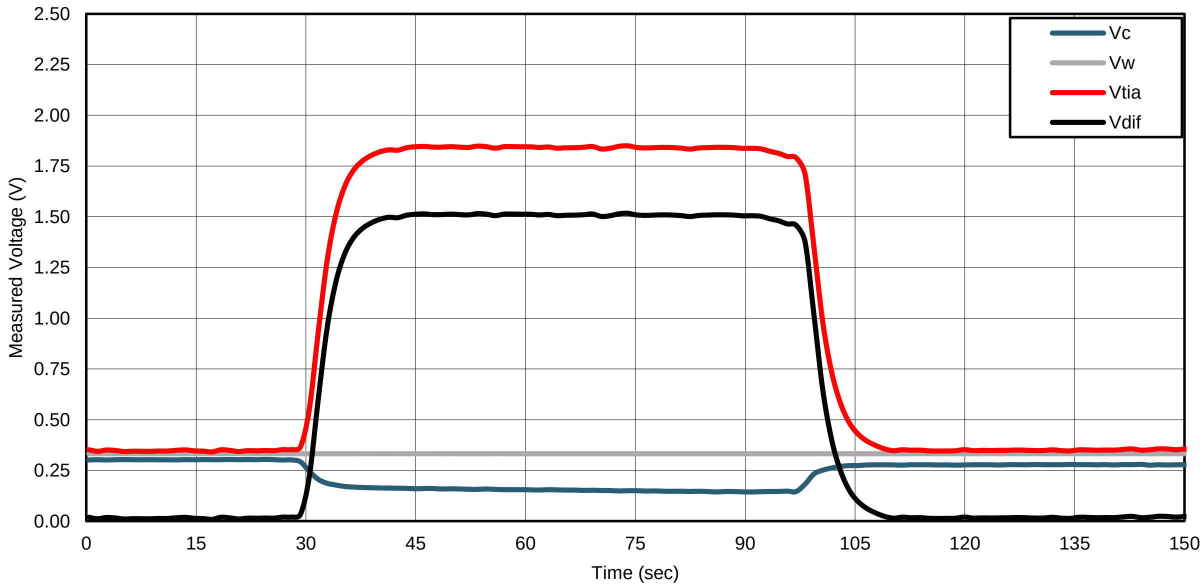


Figure 47. Monitored Voltages when exposed to 200ppm CO

Figure 47 shows the resulting circuit voltages when the sensor was exposed to 200ppm step of carbon monoxide gas. V_C is the monitored CE pin voltage and clearly shows the expected CE voltage dropping below the WE voltage, V_W, as the concentration increases.

V_{TIA} is the output of the transimpedance amplifier U2. V_{DIFF} is the calculated difference between V_{REF} and V_{TIA}, which will be used for the ppm calculation.

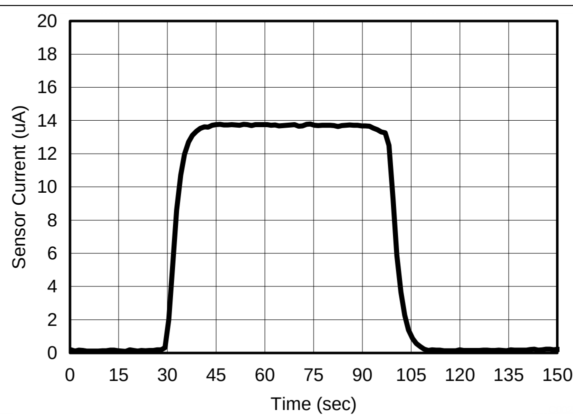


Figure 48. Calculated Sensor Current

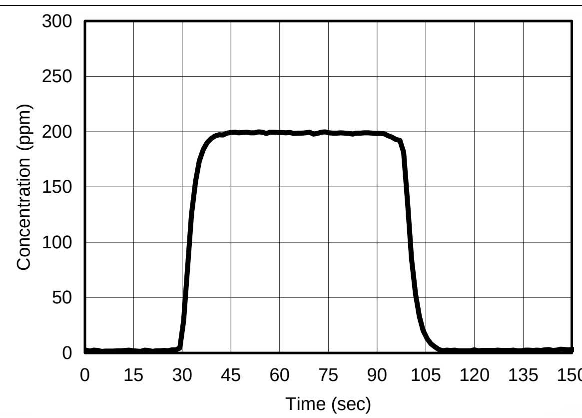


Figure 49. Calculated ppm

Figure 48 shows the calculated sensor current using the formula in Equation 7 :

$$I_{SENSOR} = V_{DIFF} / R_F = 1.52V / 110\ k\Omega = 13.8uA \quad (7)$$

Equation 8 shows the resulting conversion of the sensor current into ppm.

$$ppm = I_{SENSOR} / I_{PERPPM} = 13.8\mu A / 69nA = 200 \quad (8)$$

Total supply current for the amplifier section is less than 700 nA, minus sensor current. Note that the sensor current is sourced from the amplifier output, which in turn comes from the amplifier supply voltage. Therefore, any continuous sensor current must also be included in supply current budget calculations.

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1mA or less (1KΩ per volt).

9 Power Supply Recommendations

The LPV81x is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize strays.

10.2 Layout Example

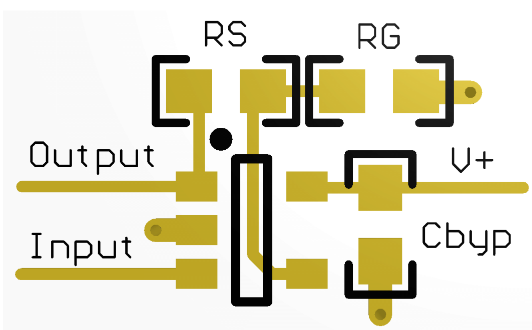


Figure 50. SOT-23 Layout Example (Top View)

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

TINA-TI SPICEベースのアナログ・シミュレーション・プログラム

DIP アダプタ評価モジュール

TIユニバーサル・オペアンプ評価モジュール

TI FilterProフィルタ設計ソフトウェア

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『AN-1798 電気化学的センサを使用した設計』*
- *『AN-1803 トランスインピーダンス・アンプ設計の考慮事項』*
- *『AN-1852 pH電極を使用した設計』*
- *『トランスインピーダンス・アンプの直感的な補正』*
- *『高速オペアンプのトランスインピーダンスの考慮事項』*
- *『FETトランスインピーダンス・アンプのノイズ解析』*
- *『基板のレイアウト技法』*
- *『オペアンプ・アプリケーション・ハンドブック』*

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LPV811	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LPV812	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LPV811DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	15TM
LPV811DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	15TM
LPV811DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	15TM
LPV811DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	15TM
LPV812DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(L812, LPV) 812
LPV812DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(L812, LPV) 812
LPV812DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(L812, LPV) 812
LPV812DGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(L812, LPV) 812

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

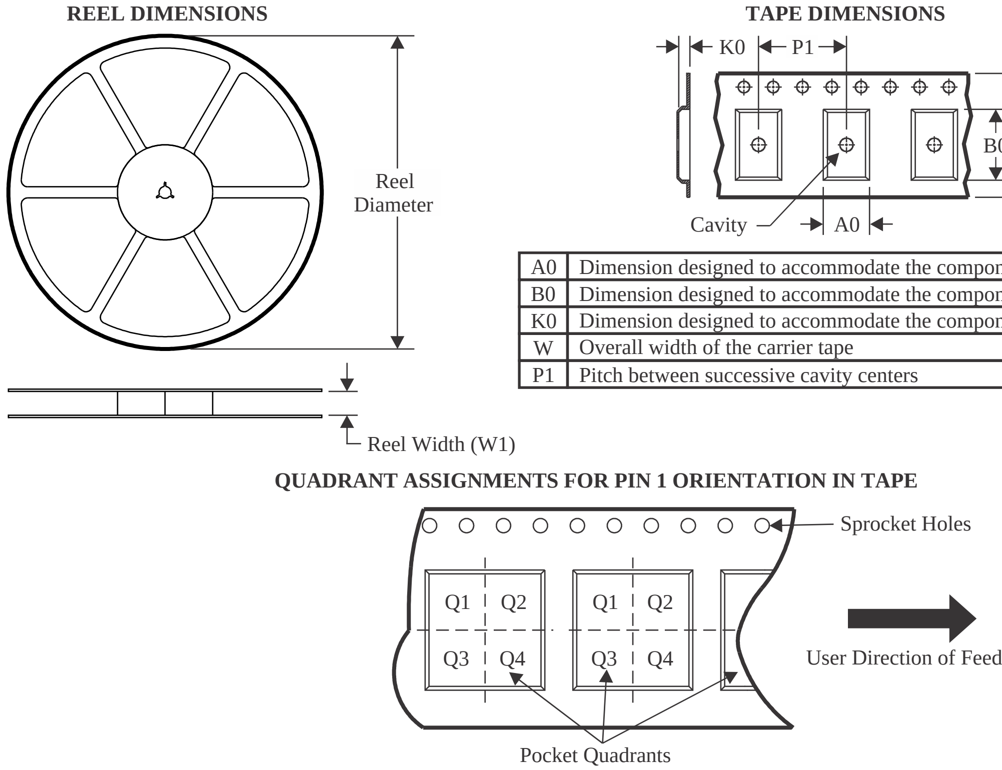
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

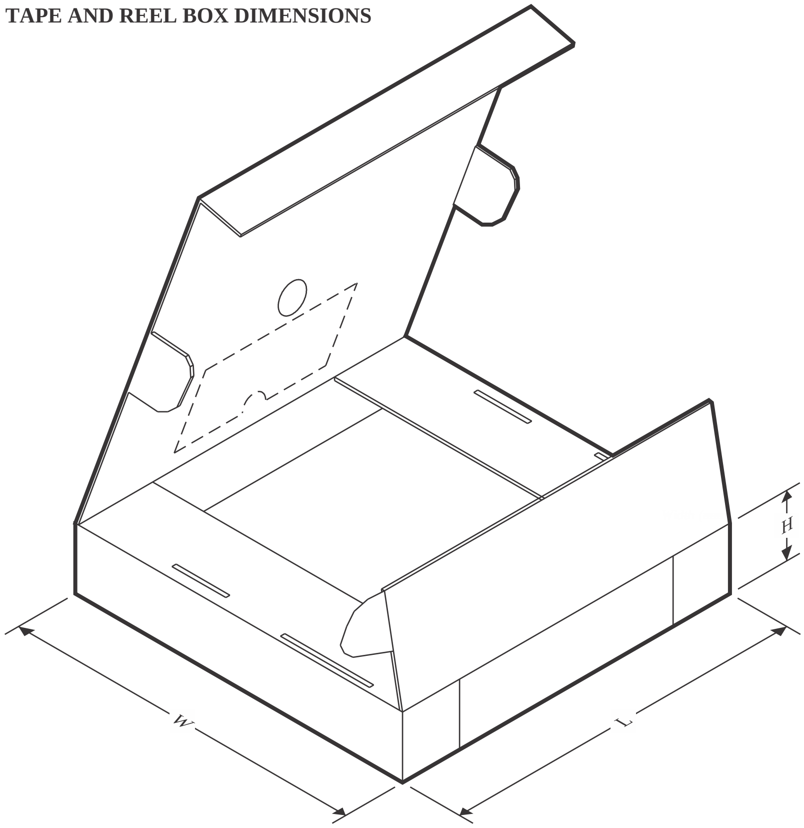


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

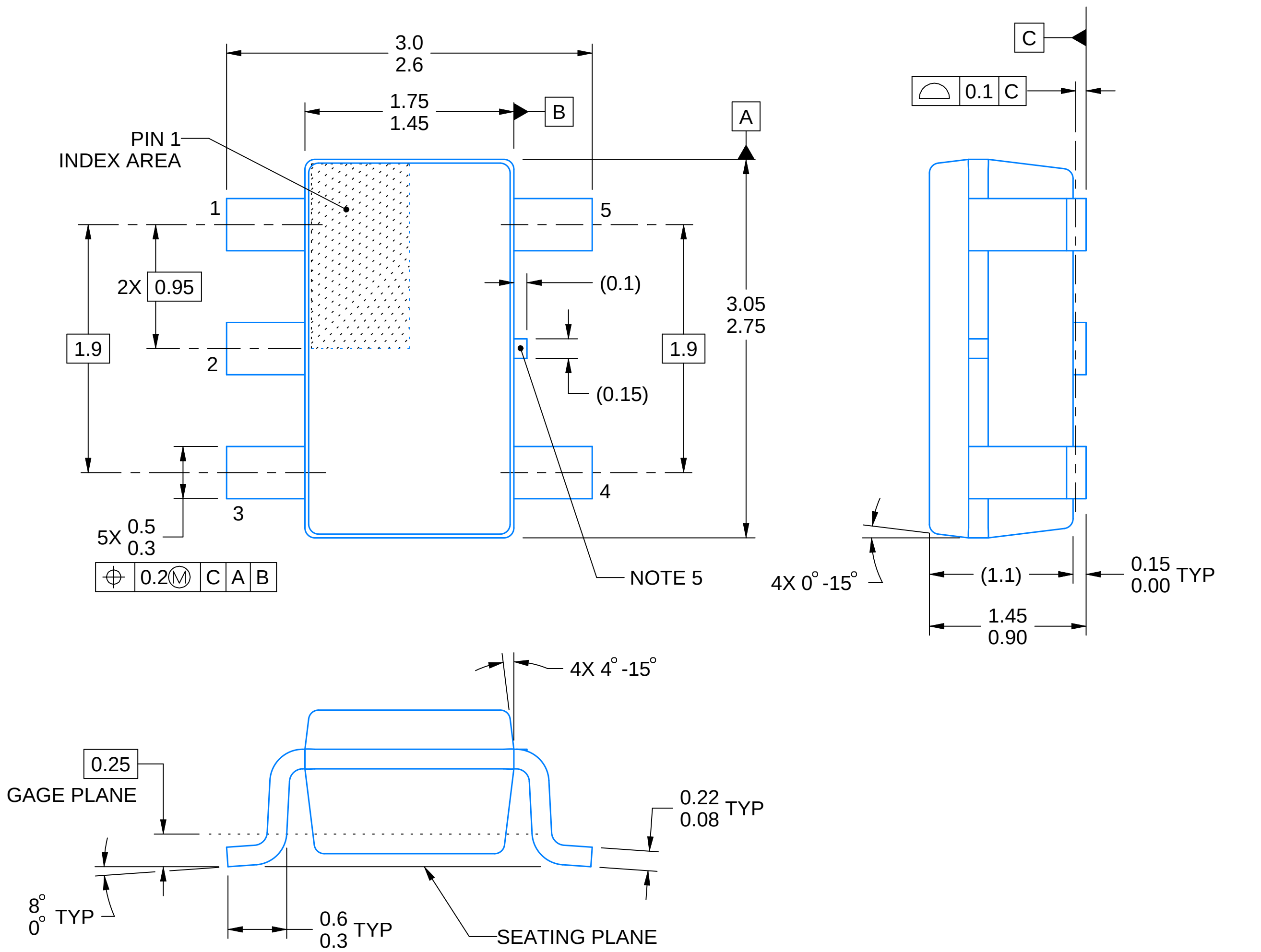
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV811DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV811DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV811DBVT	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV811DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV812DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV812DGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LPV812DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

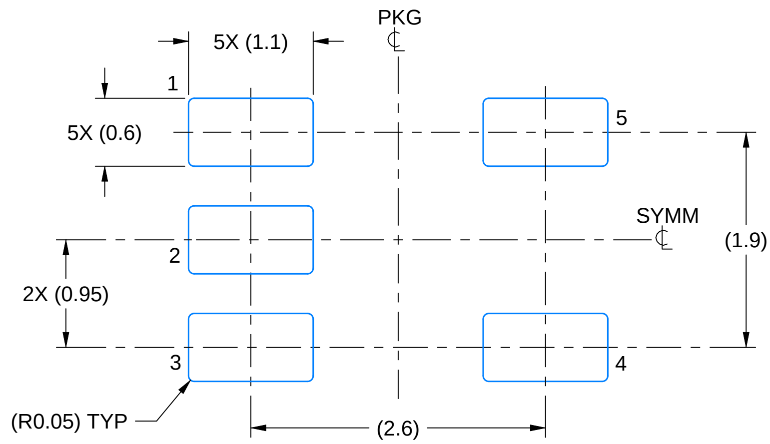
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV811DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LPV811DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LPV811DBVT	SOT-23	DBV	5	250	208.0	191.0	35.0
LPV811DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
LPV812DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
LPV812DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
LPV812DGKT	VSSOP	DGK	8	250	353.0	353.0	32.0



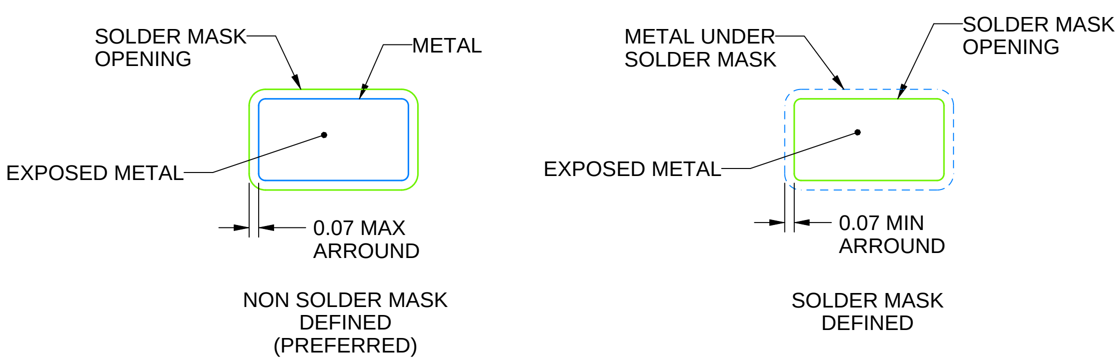
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

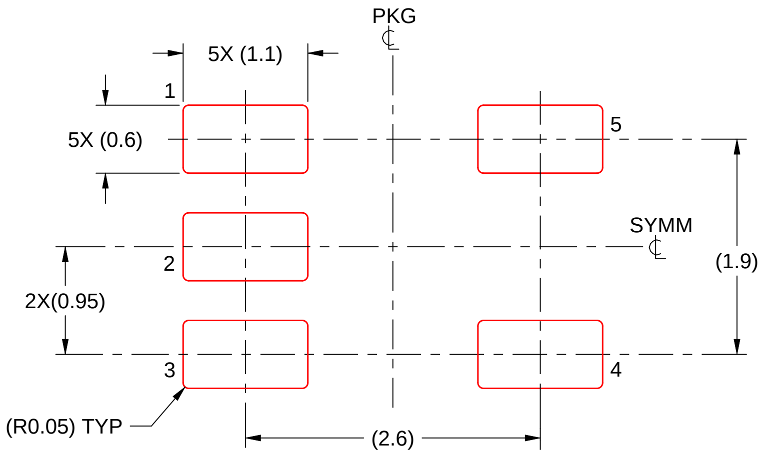


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

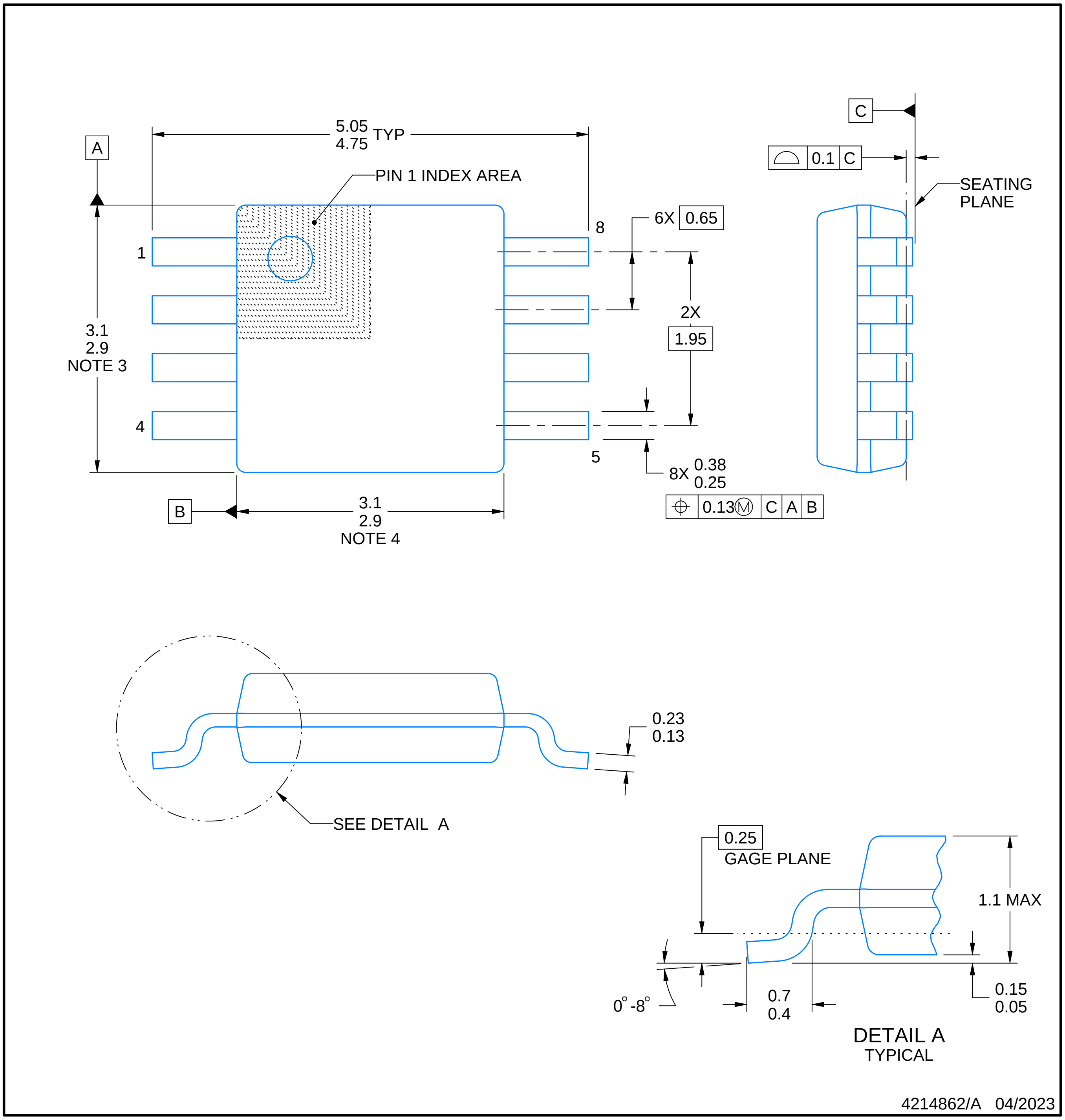


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

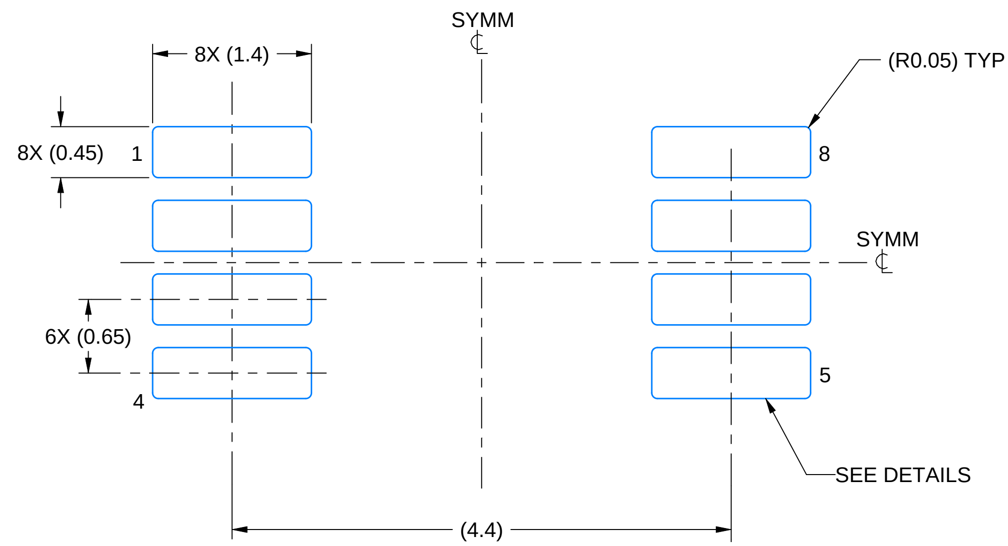


4214862/A 04/2023

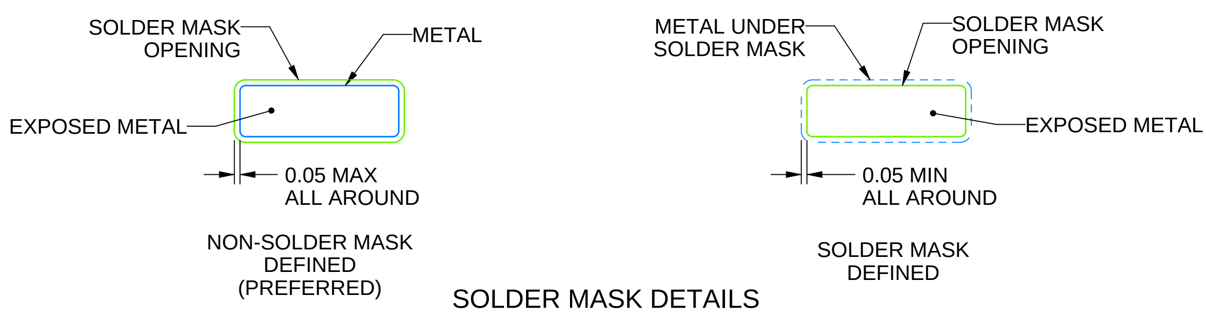
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

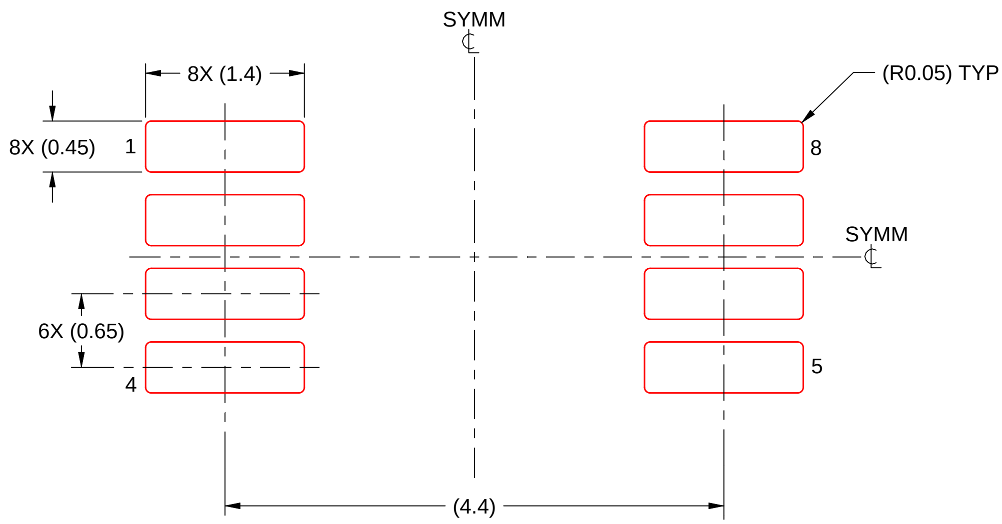


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。