MAX3243E ±15kV IEC ESD 保護機能搭載、3V～5.5V 1ch RS-232 ライン・ドライバ / レシーバ

1 特長

- IBM™ PC/AT™ シリアル・ポート用のシングルチップおよび単一電源インターフェイス
- RS-232 バス・ピン用 ESD 保護機能
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2、接触放電
  - ±15kV IEC 61000-4-2、気中放電
- TIA/EIA-232-F および ITU V.28 規格の要件に適合またはそれを上回る性能
- 3V～5.5V の V_{CC} 電源で動作
- 常時アクティブの非反転レシーバ出力 (ROUT2B)
- 最大 500kbit/s のデータ・レートでの送信に対応
- 小さいスタンバイ電流:1µA (標準値)
- 外付けコンデンサ:4 × 0.1µF
- 3.3V 電源で 5V ロジック入力を許容
- Maxim の MAX3243E と交換可能
- シリアルマウス駆動可能
- 有効な RS-232 信号が検出されない場合、自動パワー・ダウン機能によりドライバ出力をディスエーブル
- プラスチック・スモール・アウトライン (DW)、シュリンク・スモール・アウトライン (DB)、シン・シュリンク・スモール・アウトライン (PW) パッケージを選択可能

2 アプリケーション

- バッテリ駆動システム
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリ駆動システム
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

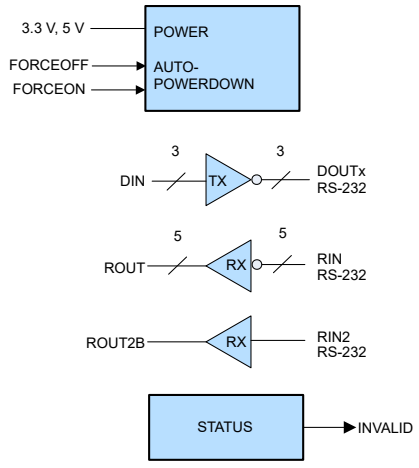
3 概要

MAX3243E デバイスは、3 つのライン・ドライバ、5 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、シリアル・ポート接続ピンには、±15kV ESD (HBM および IEC61000-4-2、気中放電) および ±8kV ESD (IEC61000-4-2、接触放電) の保護を備えています。このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポート・コネクタの間の電気的インターフェイスとして機能します。このドライバとレシーバの組み合わせは、IBM PC/AT で使用される標準的なシリアル・ポートまたはその互換シリアル・ポートの要件を満たしています。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V～5.5V の単一電源で動作できます。さらに、本デバイスには常時アクティブな非反転出力 (ROUT2B) があり、リング・インジケータを使用するアプリケーションが、デバイスの電源がオフのときにもデータを送信できるようになっています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
MAX3243E	SSOP (DB) (28)	10.20mm × 5.30mm
	SOIC (DW) (28)	17.90mm × 7.50mm
	TSSOP (PW) (28)	9.70mm × 4.40mm
	VQFN (RHB) (32)	5.00mm × 5.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2011) to Revision E (October 2022)	Page
• *「製品情報」表、「ESD 定格 」、「ESD 定格 - IEC 仕様 」、「熱に関する情報」、「詳細説明」、「電源に関する推奨事項」、「レイアウト」、「デバイスおよびドキュメントのサポート 」、「メカニカル、パッケージ、および注文情報」を追加*	1
• 「注文情報」表を削除	1
• 「概要」の 250kbit/s を 500kbit/s に変更	1
• Changed the I_{CC} Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the *Electrical Characteristics*	7

Changes from Revision C (February 2009) to Revision D (September 2011)	Page
• Deleted "VALID RIN RS-232 LEVEL" from INPUTS	13
• Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs	13
• Added table "Outputs ROUT2B and $\overline{\text{INVALID}}$" defining truth for ROUT2B and INVALID outputs.	13

5 概要 (続き)

本デバイスは最大 250kbit/s のデータ信号速度、最大 30V/µs のドライバ出力スルーレートで動作します。

MAX3243EC デバイスは 0℃～70℃、MAX3243EI デバイスは -40℃～85℃で動作が規定されています。

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6 Pin Configuration and Functions

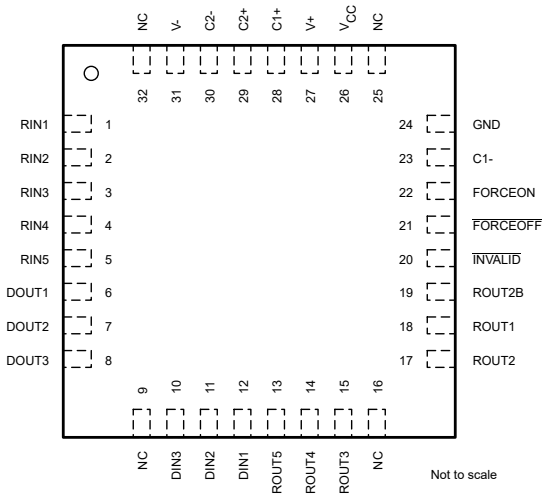


図 6-1. RHB Package, 32 Pin (VQFN), Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RIN1	I	RS-232 receiver inputs
2	RIN2		
3	RIN3		
4	RIN4		
5	RIN5		
6	DOUT1	O	RS-232 driver outputs
7	DOUT2		
8	DOUT3		
9	NC	—	Not connected internally
10	DIN3	I	Driver inputs
11	DIN2		
12	DIN1		
13	ROUT5	O	Receiver outputs
14	ROUT4		
15	ROUT3		
16	NC	—	Not connected internally
17	ROUT2	O	Receiver outputs
18	ROUT1		
19	ROUT2B	O	Always-active noninverting receiver output
20	$\overline{\text{INVALID}}$	O	Invalid Output Pin
21	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
22	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
23	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
24	GND	—	Ground
25	NC	—	Not connected internally
26	V_{CC}	—	3-V to 5.5-V supply voltage

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表 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminals of the voltage-doubler charge-pump capacitors
29	C2+	—	
30	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
31	V-	—	Negative charge pump output voltage
32	NC	—	Not connected internally

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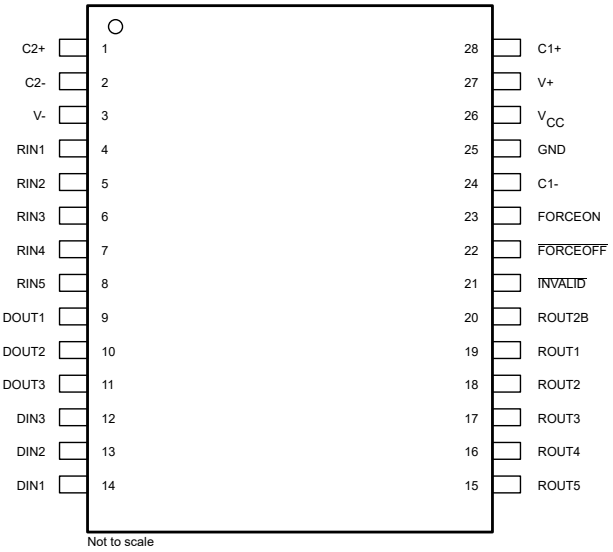


図 6-2. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP), Top View

表 6-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-		Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	$\overline{\text{INVALID}}$	O	Invalid Output Pin
22	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V_{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Output supply voltage difference(2)			13	V
V_I	Input voltage range	Driver ($\overline{FORCEOFF}$, FORCEON)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver ($\overline{INVALID}$)	–0.3	V_{CC} + 0.3	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 DOUT1/2/3, RIN1/2/3/4/5 pins(1)	±15,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge (1)	RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins	±8,000	V
		IEC 61000-4-2 Air-gap Discharge (1)		±15,000	

(1) For DB, PW and RHB package only: A minimum of 1-µF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating.

7.4 Recommended Operating Conditions

See 図 10-1 (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		MAX3243EC	0		70	°C
			MAX3243EI	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

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7.5 Thermal Information

THERMAL METRIC[1]		{DB} (SSOP) 28 PINS	{DW} (SOIC) 28 PINS	{PW} (TSSOP) 28 PINS	{RHB} (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.1	59.0	70.3	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	25.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	30.3	29.2	14.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	7.8	1.3	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.0	30.0	28.8	14.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	5.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see 図 10-1)

PARAMETER			TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±1	µA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC} For DB, PW and RHB package		0.3	1.2	mA
		Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC} For DW package		0.3	1	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	µA
		Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded, All DIN are grounded		1	10	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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7.7 Driver Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 図 10-1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND			–5	–5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$				±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	μA
V_{hys}	Input hysteresis						±1	V
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V				±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V					
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND,	V_O = ±12 V,	V_{CC} = 0 to 5.5 V			±25	μA

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

7.8 Receiver, Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 図 10-1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	μA
r_i	Input resistance	V_I = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

7.9 Auto-Powerdown Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	$\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{IT–(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	$\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	$\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = -1 mA, $\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, $\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

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7.10 Driver Switching Characteristics

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 図 10-1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ See 図 8-1	250	500		kbit/s
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See 図 8-2		100		ns
SR(tr)	Slew rate, transition region (see 図 8-1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ, PRR = 250 kbit/s	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V + 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

7.11 Receiver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 図 8-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output		150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 図 8-4	200	ns
t_{dis}	Output disable time		200	ns
$t_{sk(p)}$	Puse skew(3)	See 図 8-3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

7.12 Auto-Powerdown Switching Characteristics

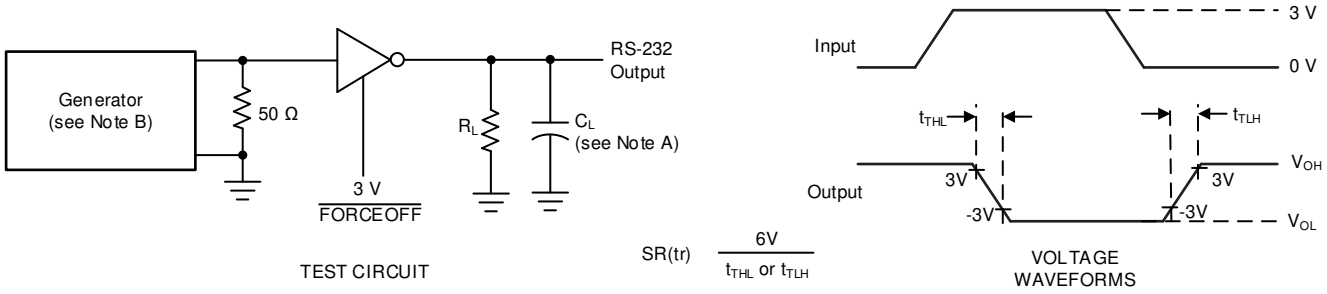
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-5)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	V_{CC} = 5 V	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	V_{CC} = 5 V	30	µs
t_{en}	Supply enable time	V_{CC} = 5 V	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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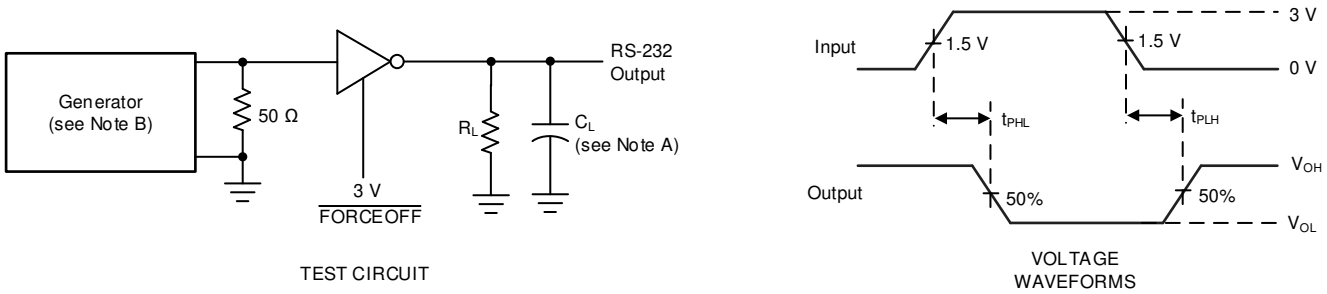
8 Parameter Measurement Information



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

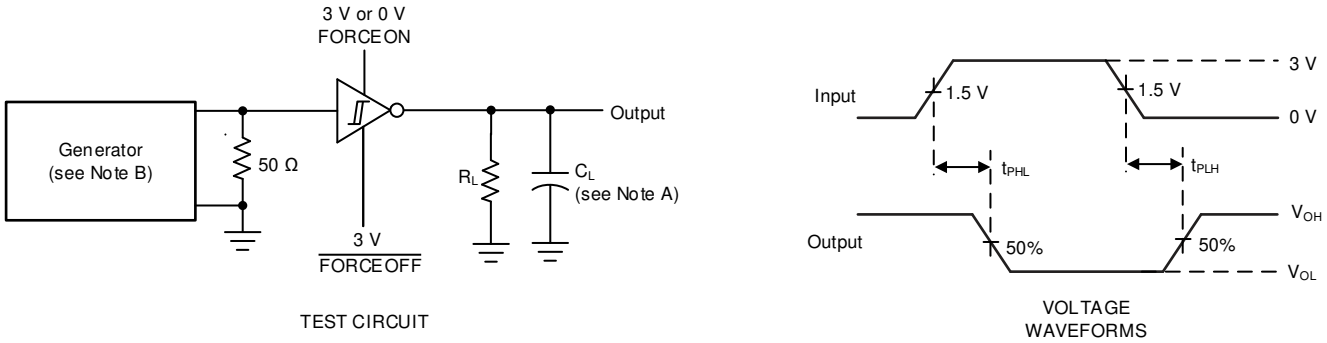
図 8-1. Driver Slew Rate



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

図 8-2. Driver Pulse Skew

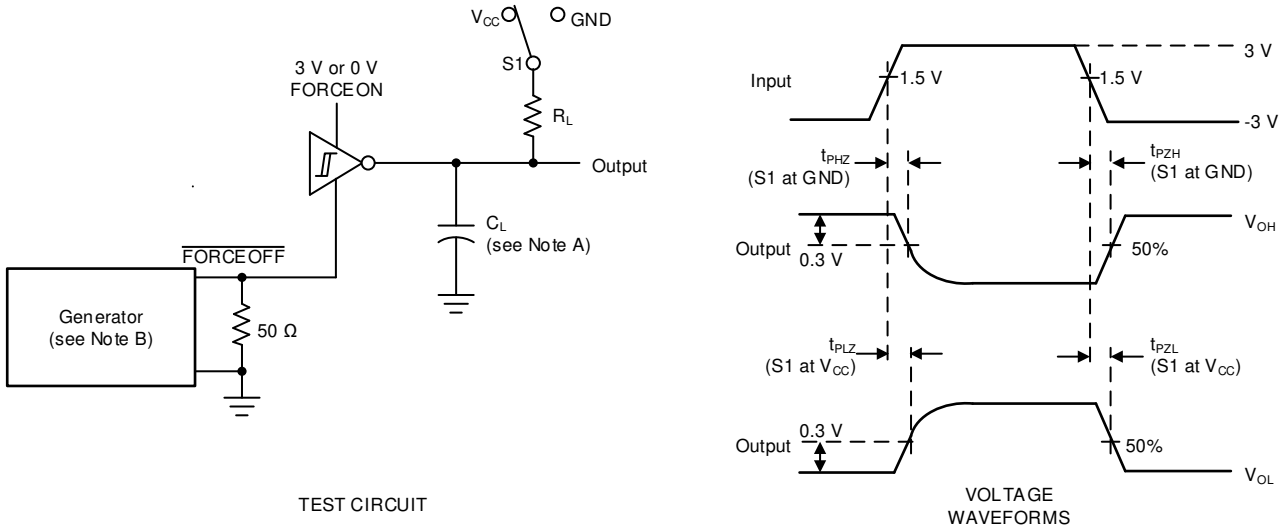


A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

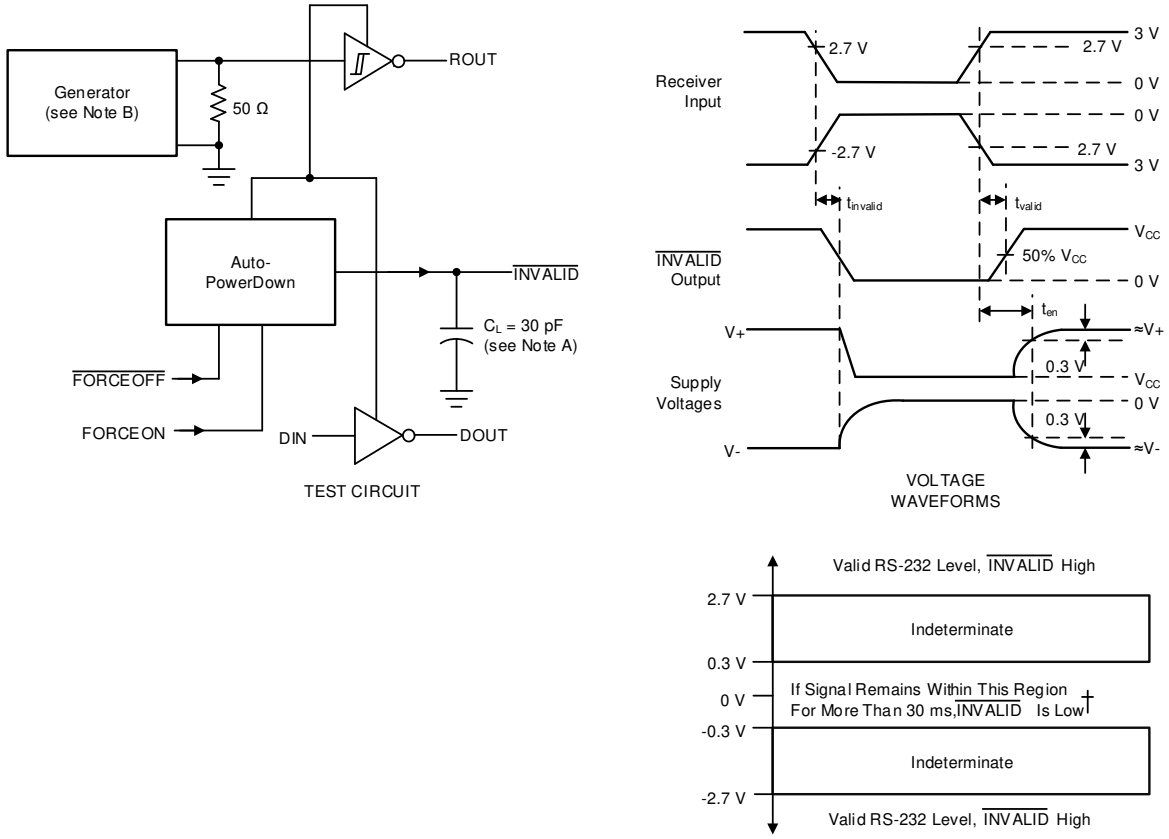
図 8-3. Receiver Propagation Delay Times

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A. C_L includes probe and jig capacitance
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

図 8-4. Receiver Enable and Disable Times



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

図 8-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

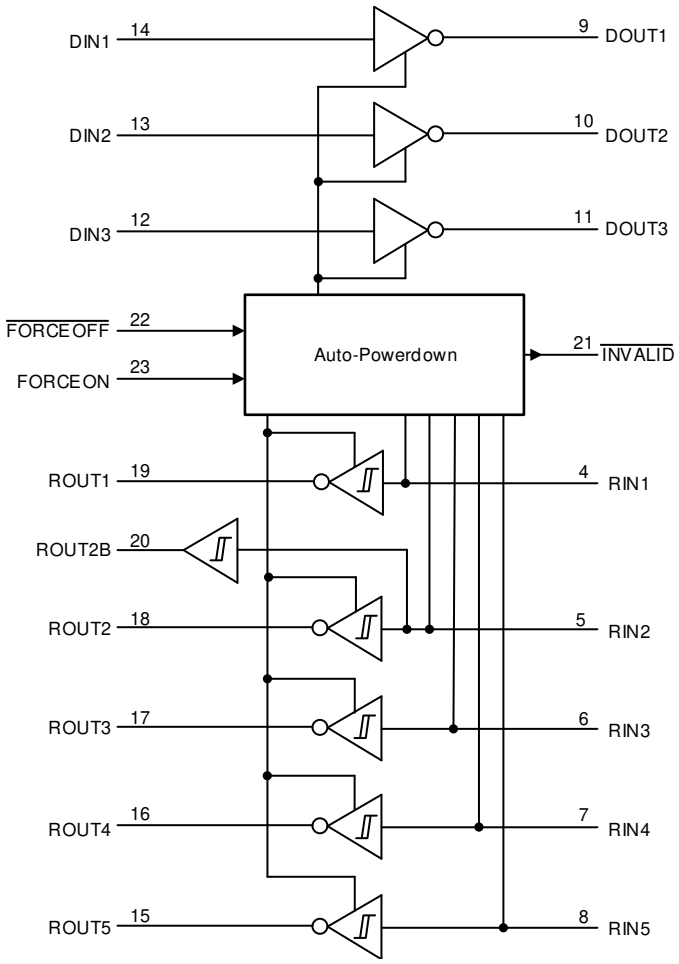
9 Detailed Description

9.1 Overview

The MAX3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector.

The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

9.2 Functional Block Diagram



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9.3 Feature Description

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 µA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs. Refer to Figure 8-5 for receiver input levels.

9.4 Device Functional Modes

Figure 9-1 through 9-3 show the device functional modes.

表 9-1. Each Driver

INPUTS(1)				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
X	L	H	No	Z	Powered off by auto-powerdown feature

表 9-2. Each Receiver

INPUTS(1)			OUTPUT	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation with auto-powerdown disabled/enabled
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 9-3. Outputs ROUT2B and $\overline{\text{INVALID}}$

INPUTS(1)				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

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10 Application and Implementation

注

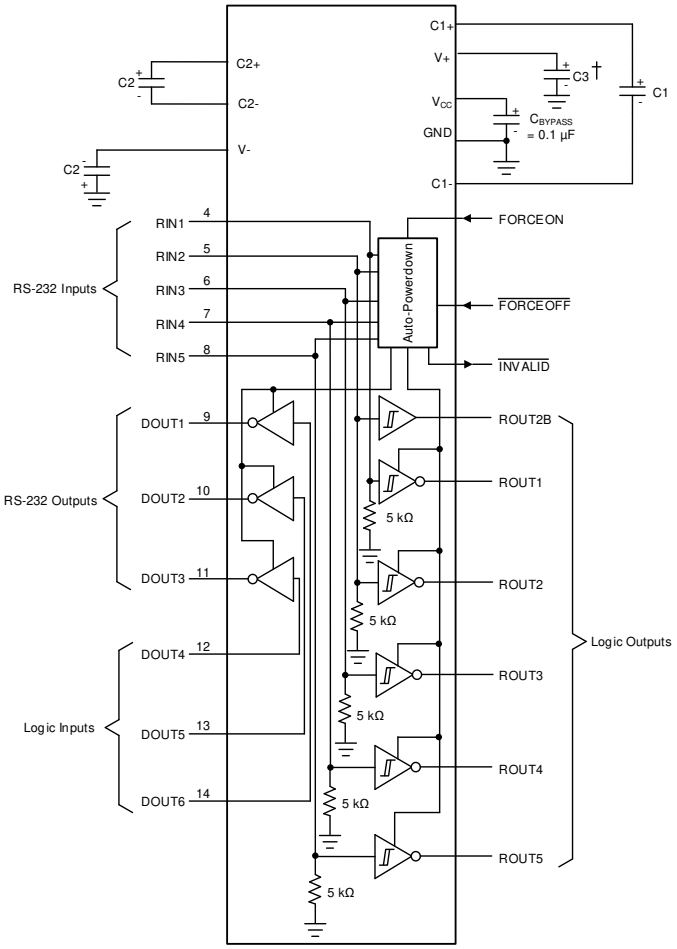
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10.1 Application Information

For proper operation, add capacitors as shown in 図 10-1. Pins 12 through 23 connect to UART or general purpose logic lines. RS-232 lines on Pins 4 through 11 connect to a connector or cable.

10.2 Typical Application

Three driver and five receiver channels are supported for full duplex transmission with hardware flow control. The five 5-kΩ resistors are internal to the MAX3243E.



† C3 can be connected to V_{CC} or GND

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

図 10-1. Typical Operating Circuit and Capacitor Values

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10.2.1 Design Requirements

For this design example, use the values in 表 10-1.

- V_{CC} minimum is 3 V and maximum is 5.5 V.
- Maximum recommended bit rate is 250 kbps.

表 10-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

10.2.2 Detailed Design Procedure

MAX3243E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors.

10.2.2.1 ESD Protection

TI MAX3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV in all states: normal operation, shutdown, and powered down. The MAX3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The MAX3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

- ±15-kV Human Body Model (HBM)
- ±15-kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- ±8-kV IEC61000-4-2, Contact Discharge

10.2.2.1.1 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

10.2.2.1.2 Human Body Model (HBM)

The Human Body Model of ESD testing is shown in 図 10-2, while 図 10-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5k-Ω resistor.

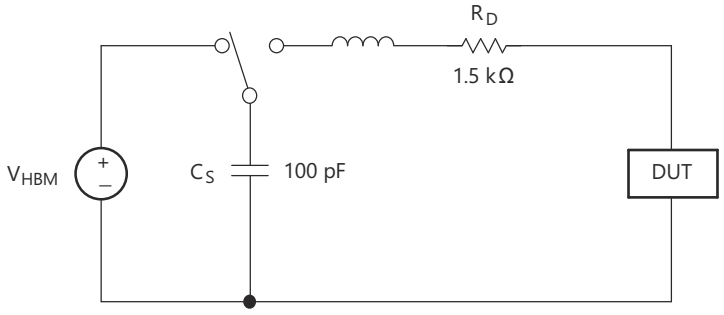


図 10-2. HBM ESD Test Circuit

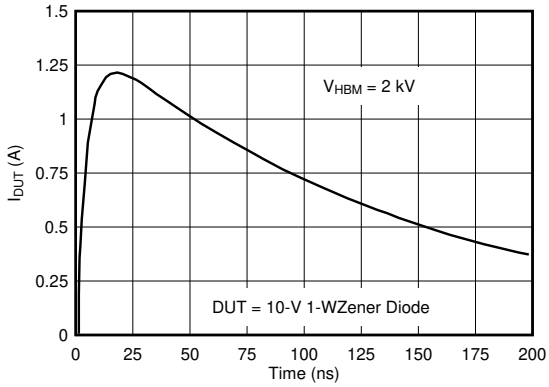


図 10-3. Typical HBM Current Waveform

10.2.2.1.3 IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM, ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The MAX3243E device is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

図 10-4 shows the IEC61000-4-2 model, and 図 10-5 shows the current waveform for the corresponding ±8-kV Contact-Discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding ±15-kV (Level 4) Air-Gap Discharge test involves approaching the DUT with an already energized probe.

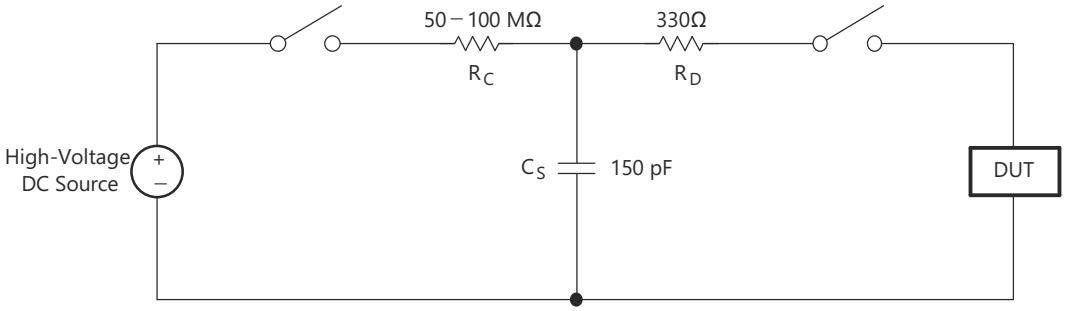


図 10-4. Simplified IEC61000-4-2 ESD Test Circuit

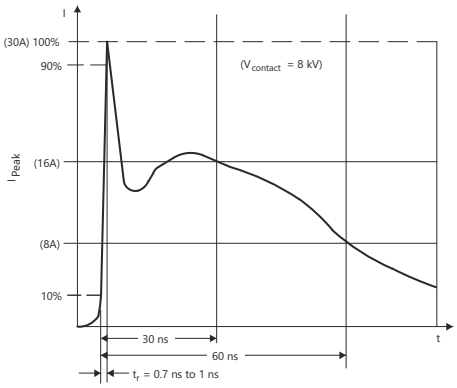


図 10-5. Typical Current Waveform of IEC61000-4-2 ESD Generator

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10.2.2.1.4 Machine Model

The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test is no longer as pertinent to the RS-232 pins.

10.3 Power Supply Recommendations

The V_{CC} voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} must be between 3 V and 5.5 V.

10.4 Layout

As shown in Layout Example, charge-pump and supply voltage capacitors must be located very close to device pins. Non-polarized ceramic capacitors are recommended. If polarized tantalum or electrolytic capacitors are used, they should be connected as per Typical Operating Circuit and Capacitor Values.

10.4.1 Layout Example

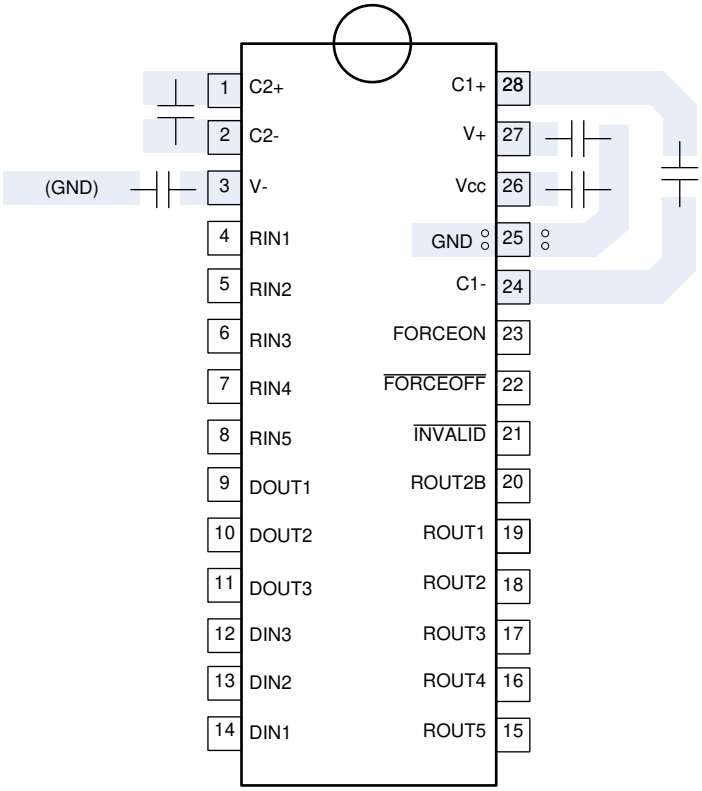


図 10-6. Example Layout

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Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3243ECDB	Obsolete	Production	SSOP (DB) | 28	-	-	Call TI	Call TI	0 to 70	MAX3243EC
MAX3243ECDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC
MAX3243ECDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC
MAX3243ECDW	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	0 to 70	MAX3243EC
MAX3243ECDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC
MAX3243ECDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC
MAX3243ECPW	Obsolete	Production	TSSOP (PW) | 28	-	-	Call TI	Call TI	0 to 70	MP243EC
MAX3243ECPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP243EC
MAX3243ECPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP243EC
MAX3243ECPWRG4	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP243EC
MAX3243ECRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	MP243E
MAX3243ECRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	MP243E
MAX3243ECRHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MP243E
MAX3243ECRHBRG4.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MP243E
MAX3243EIDB	Obsolete	Production	SSOP (DB) | 28	-	-	Call TI	Call TI	-40 to 85	MAX3243EI
MAX3243EIDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI
MAX3243EIDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI
MAX3243EIDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI
MAX3243EIDBRG4.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI
MAX3243EIDW	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	-40 to 85	MAX3243EI
MAX3243EIDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI
MAX3243EIDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI
MAX3243EIDWRG4	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI
MAX3243EIPW	Obsolete	Production	TSSOP (PW) | 28	-	-	Call TI	Call TI	-40 to 85	MP243EI
MAX3243EIPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI
MAX3243EIPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI
MAX3243EIPWRE4	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI
MAX3243EIPWRG4	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI
MAX3243EIRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MR243E

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3243EIRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MR243E
MAX3243EIRHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MR243E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

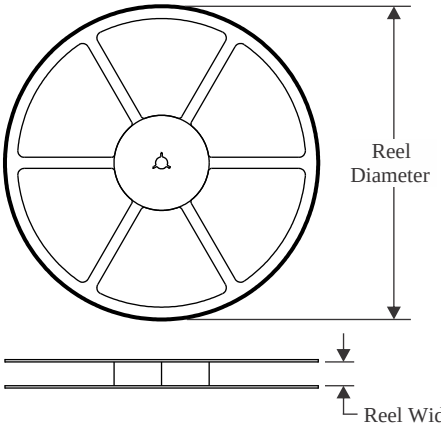
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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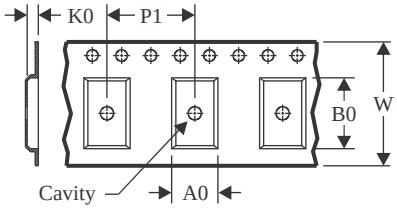
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

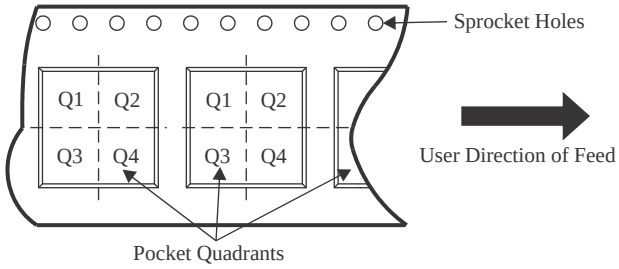


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

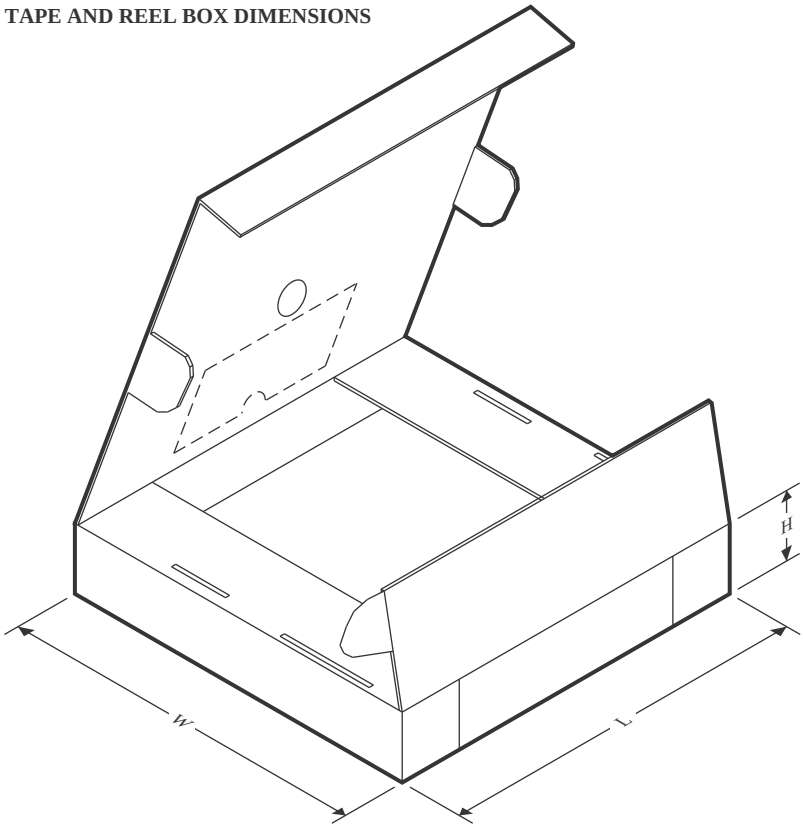
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
MAX3243ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
MAX3243ECRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MAX3243ECRHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MAX3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
MAX3243EIDBRG4	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
MAX3243EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
MAX3243EIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

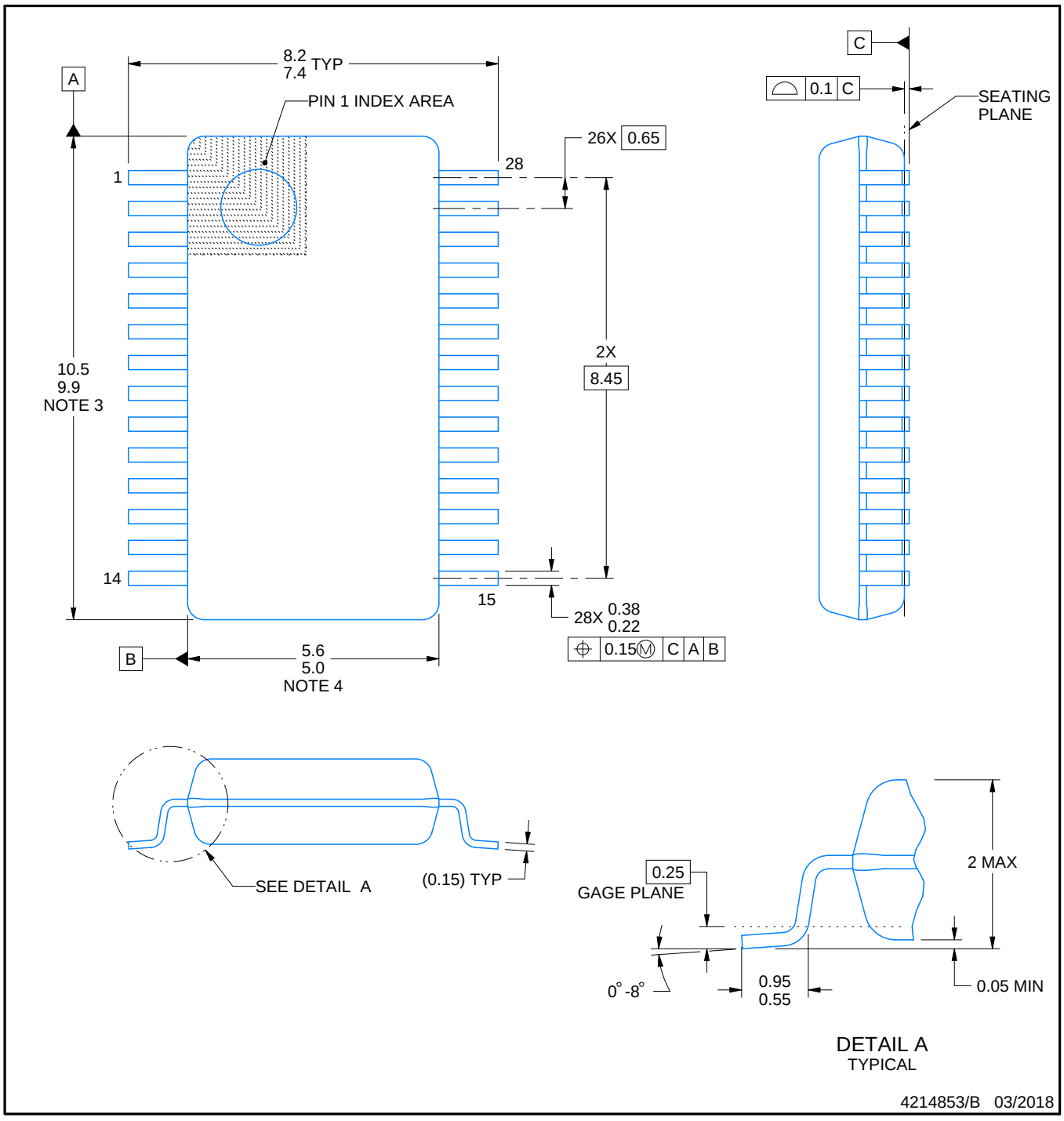
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3243ECDBR	SSOP	DB	28	2000	353.0	353.0	32.0
MAX3243ECDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243ECPWR	TSSOP	PW	28	2000	353.0	353.0	32.0
MAX3243ECRHBR	VQFN	RHB	32	3000	360.0	360.0	36.0
MAX3243ECRHBRG4	VQFN	RHB	32	3000	367.0	367.0	35.0
MAX3243EIDBR	SSOP	DB	28	2000	353.0	353.0	32.0
MAX3243EIDBRG4	SSOP	DB	28	2000	353.0	353.0	32.0
MAX3243EIDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243EIPWR	TSSOP	PW	28	2000	353.0	353.0	32.0
MAX3243EIRHBR	VQFN	RHB	32	3000	360.0	360.0	36.0

PACKAGE OUTLINE

DB0028A

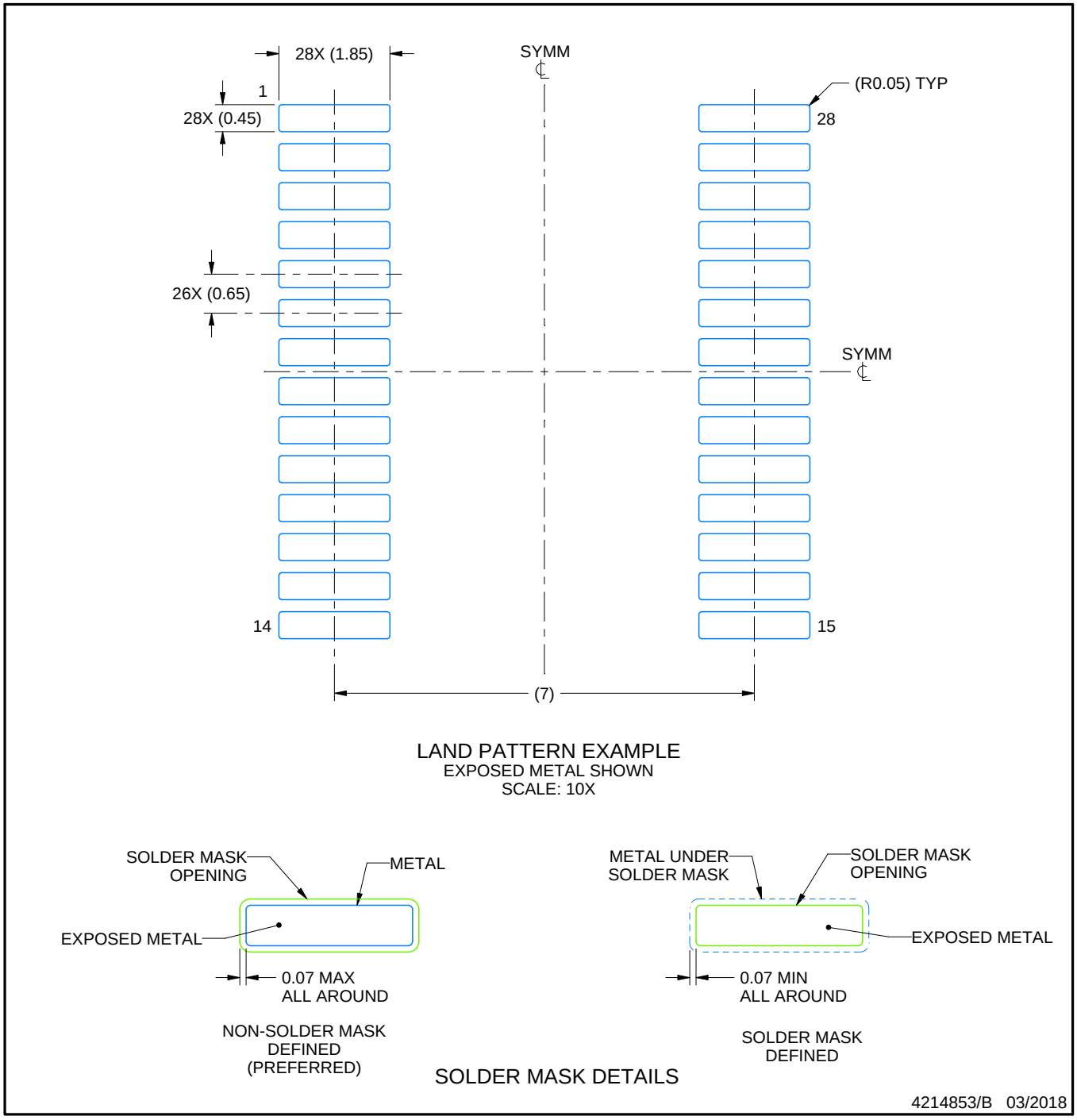
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



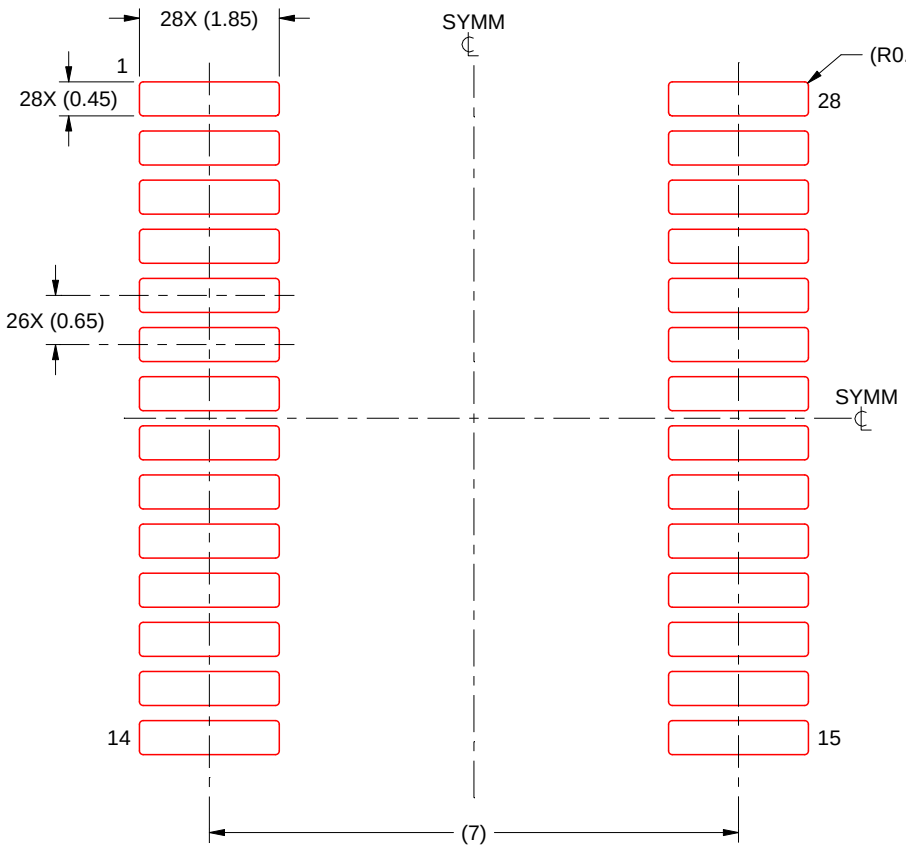
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

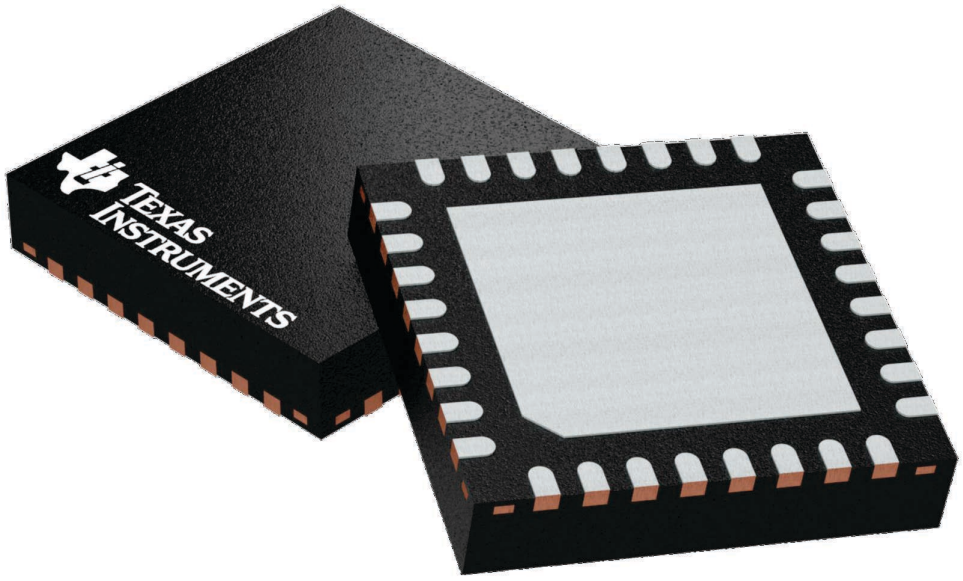
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

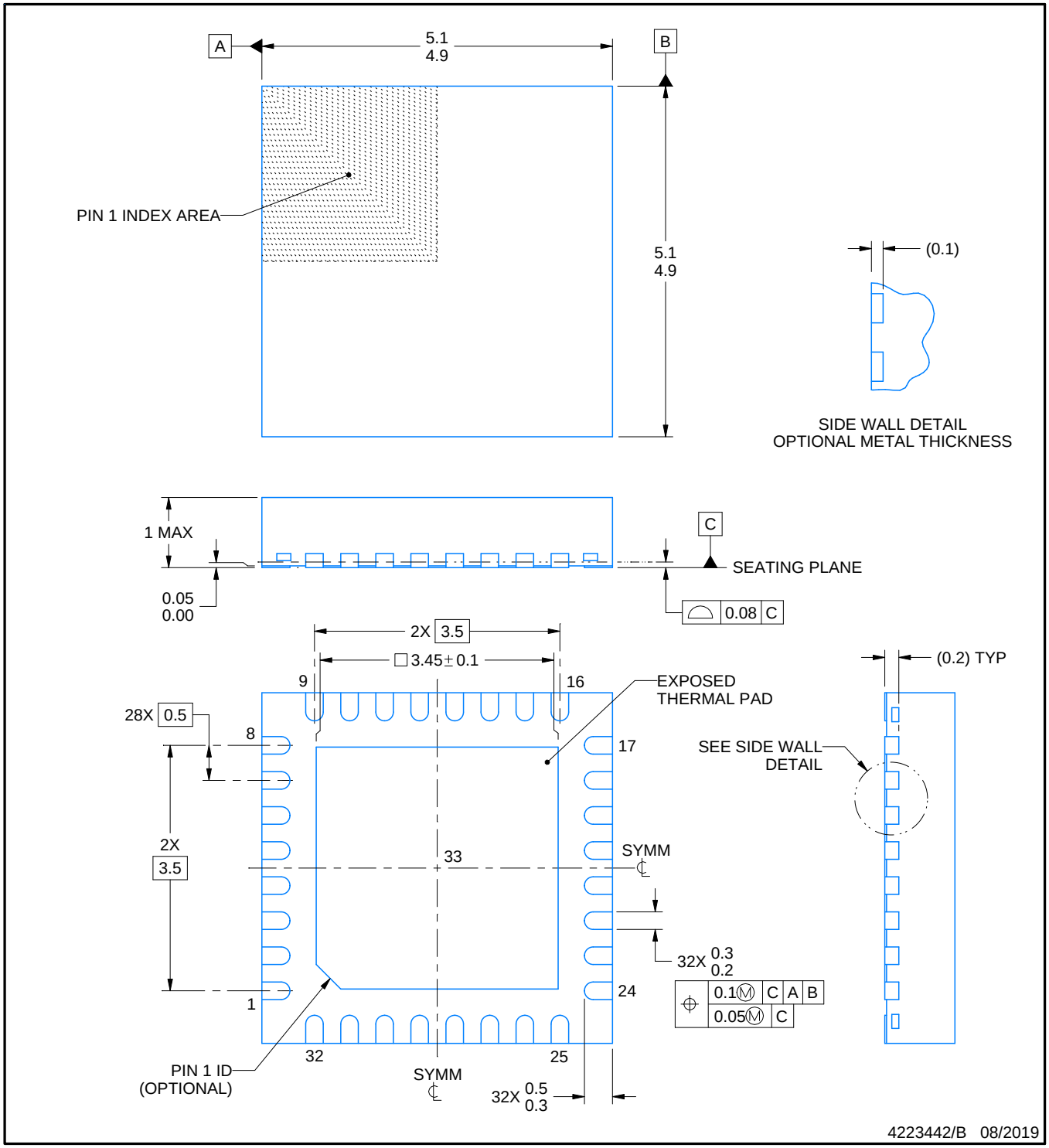
4224745/A

RHB0032E

PACKAGE OUTLINE

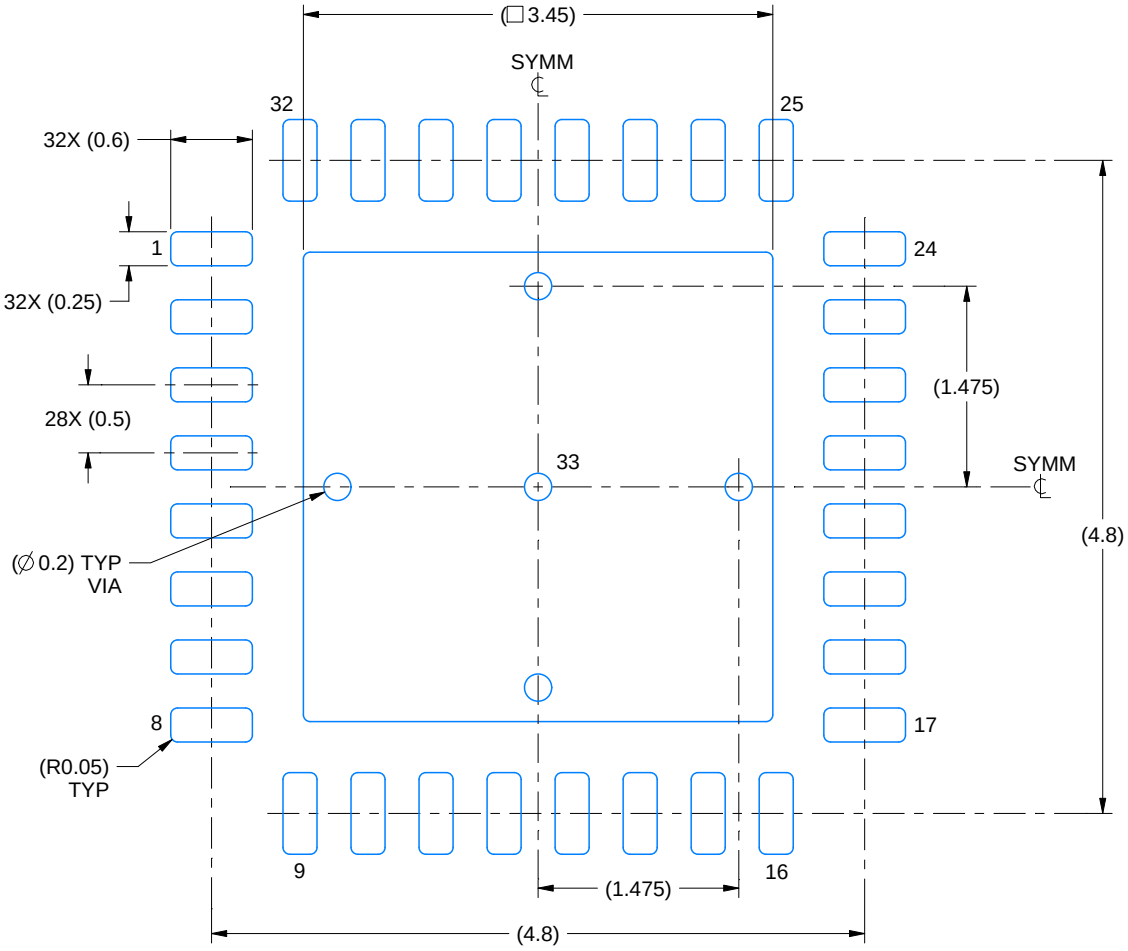
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

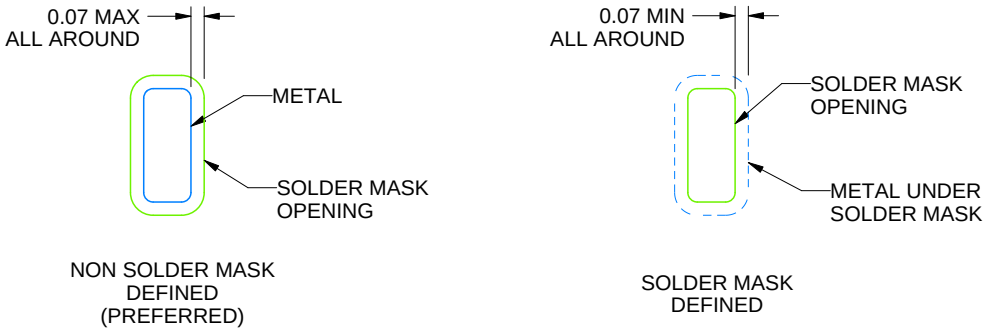


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

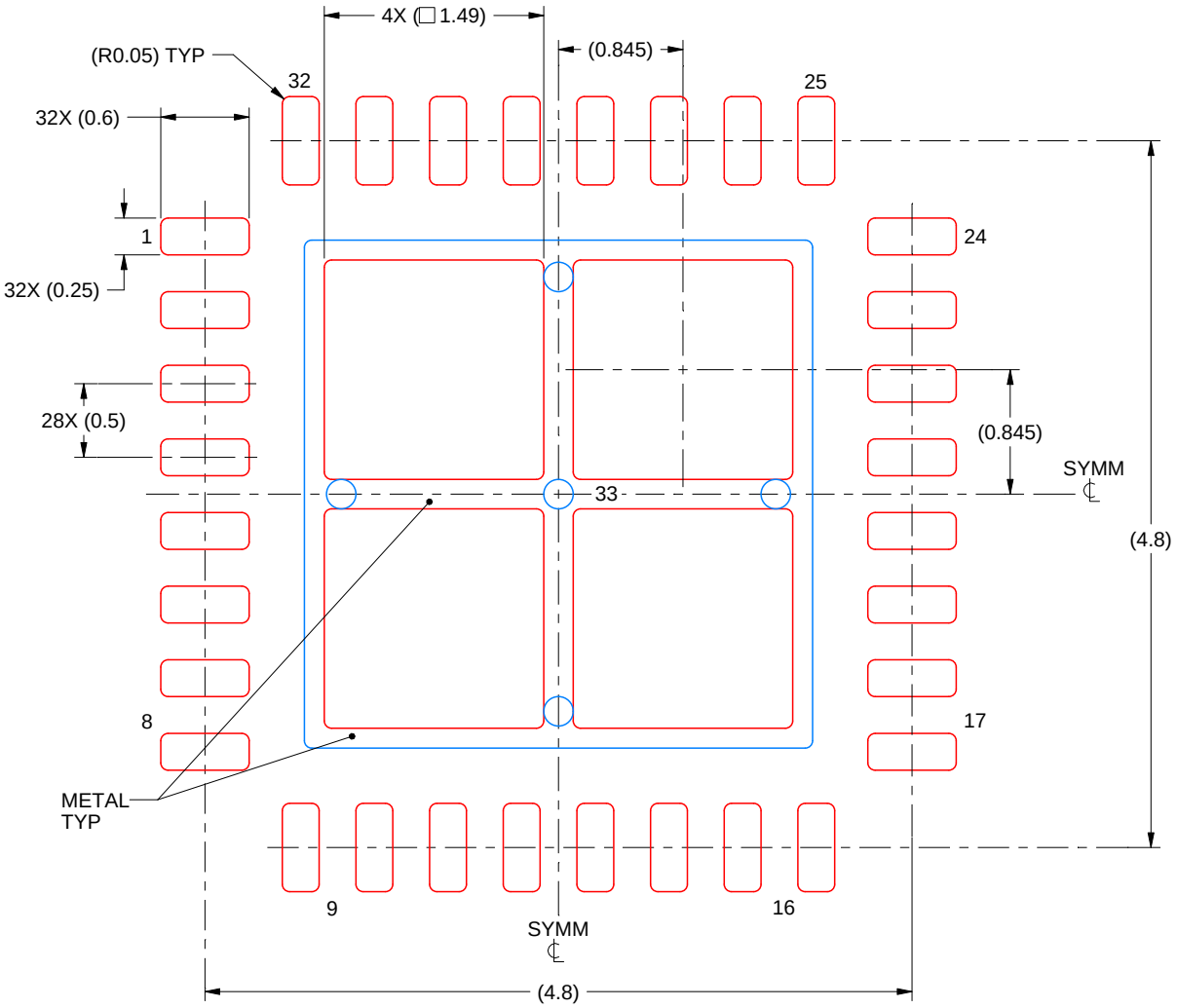


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

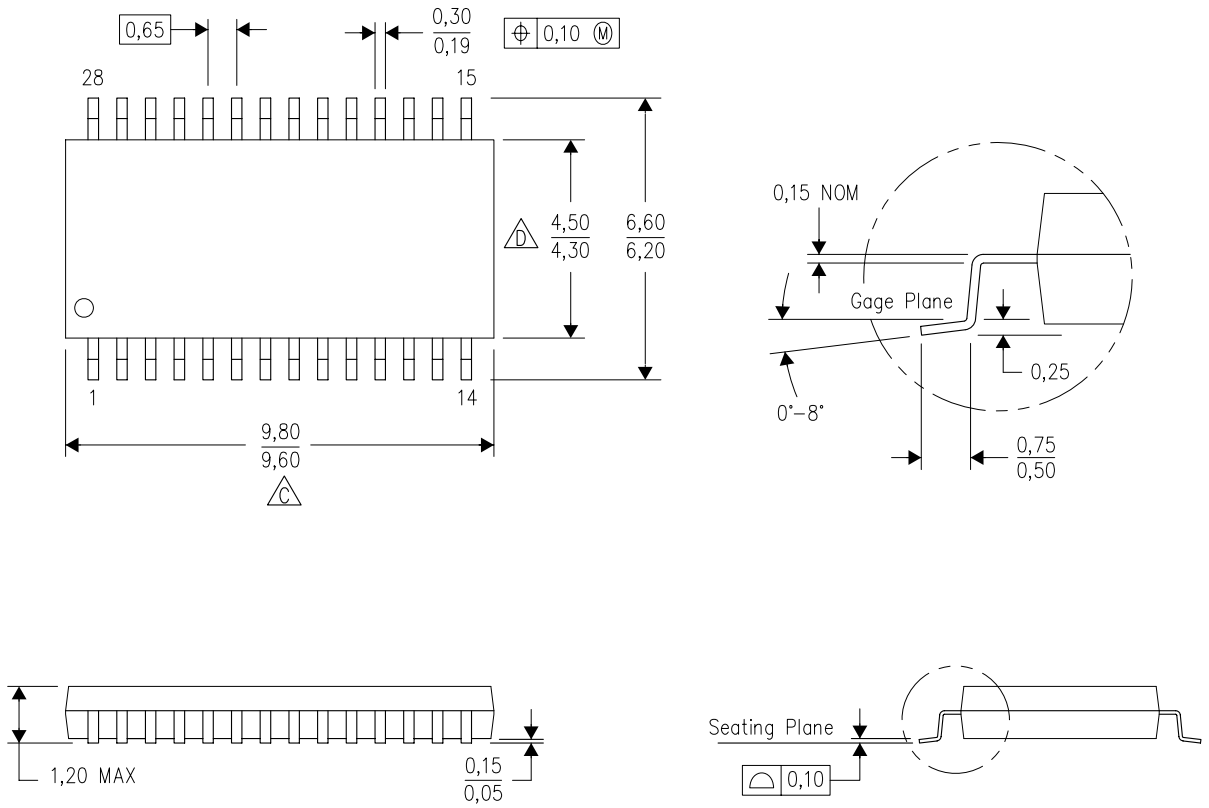
EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

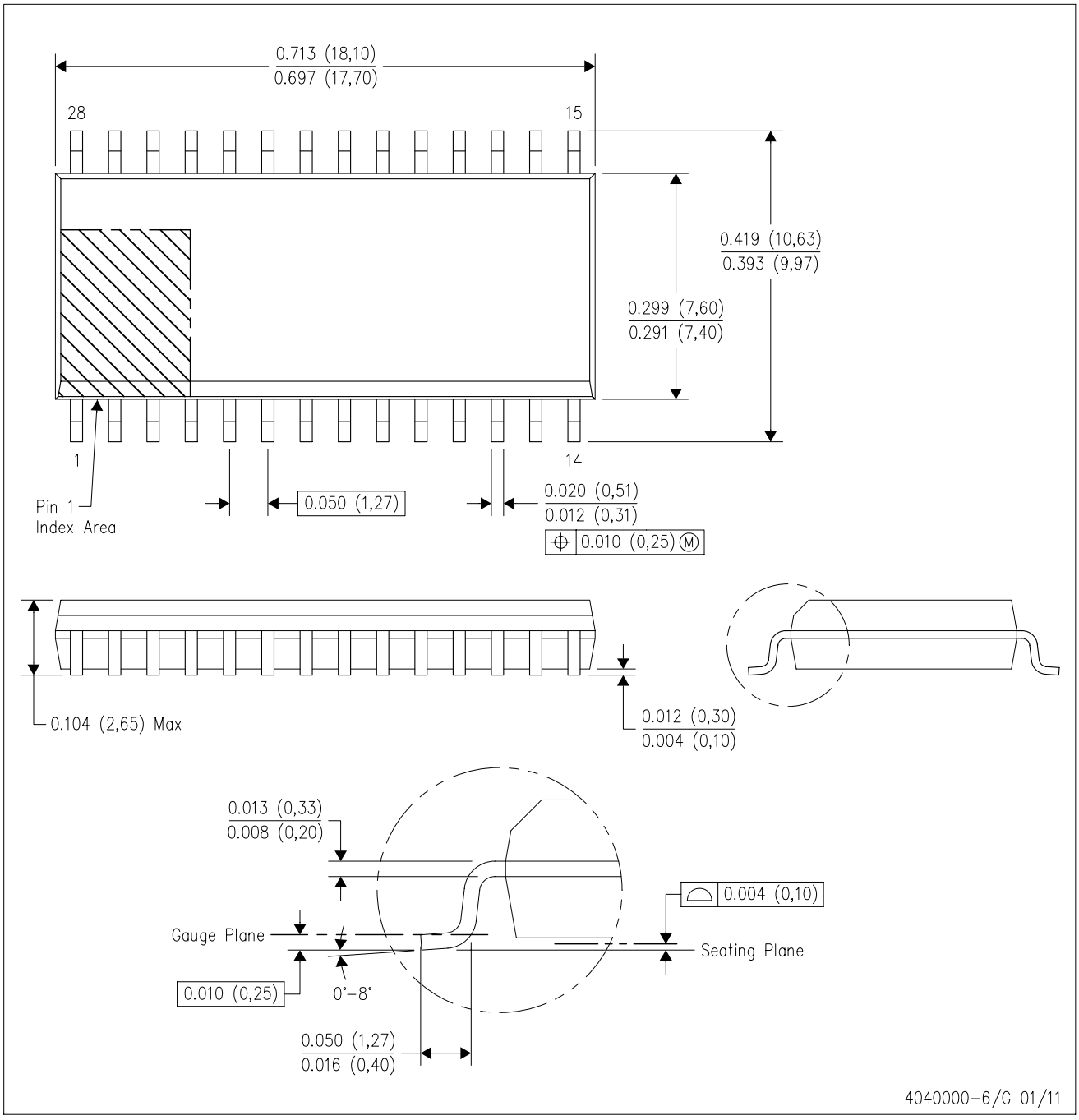
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

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