TEXAS INSTRUMENTS

MC33063A, MC34063A

SLLS636N –DECEMBER 2004–REVISED JANUARY 2015

MC3x063A 1.5-A Peak Boost/Buck/Inverting Switching Regulators

1 Features

- Wide Input Voltage Range: 3 V to 40 V
- High Output Switch Current: Up to 1.5 A
- Adjustable Output Voltage
- Oscillator Frequency Up to 100 kHz
- Precision Internal Reference: 2%
- Short-Circuit Current Limiting
- Low Standby Current

2 Applications

- Blood Gas Analyzers: Portable
- Cable Solutions
- HMIs (Human Machine Interfaces)
- Telecommunications
- Portable Devices
- Consumer & Computing
- Test & Measurement

3 Description

The MC33063A and MC34063A devices are easy-to-use ICs containing all the primary circuitry needed for building simple DC-DC converters. These devices primarily consist of an internal temperature-compensated reference, a comparator, an oscillator, a PWM controller with active current limiting, a driver, and a high-current output switch. Thus, the devices require minimal external components to build converters in the boost, buck, and inverting topologies.
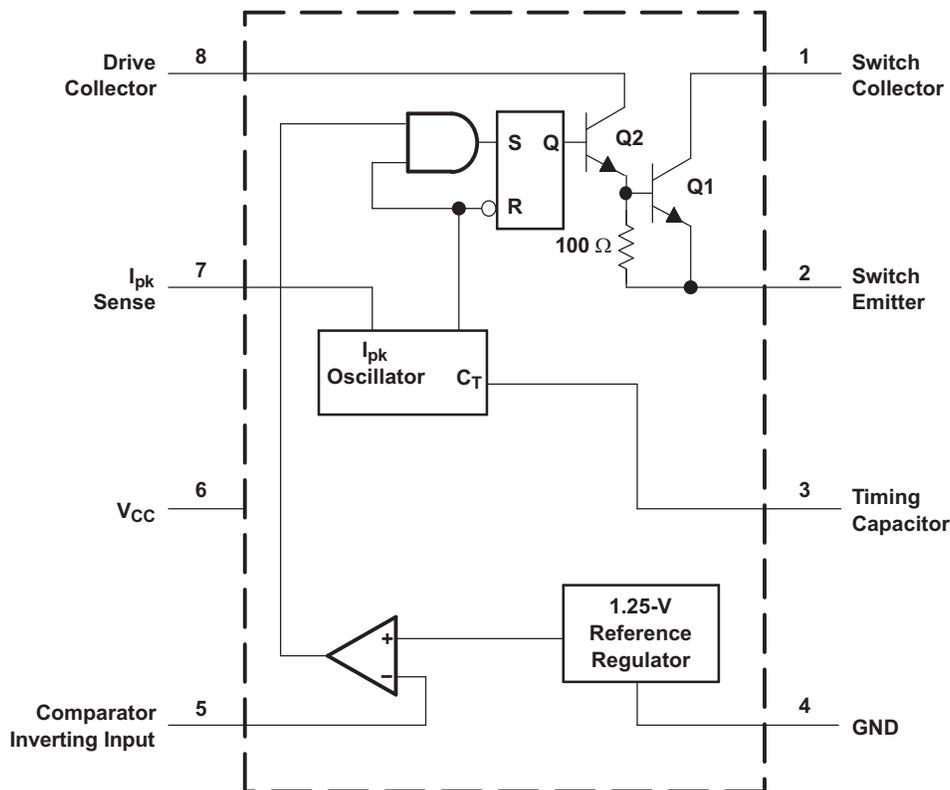
The MC33063A device is characterized for operation from –40°C to 85°C, while the MC34063A device is characterized for operation from 0°C to 70°C.

Device Information[(1)]

PART NUMBER	PACKAGE (PIN)	BODY SIZE
MC3x063A	SOIC (8)	4.90 mm × 3.91 mm
	SON (8)	4.00 mm × 4.00 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

Table of Contents

5 Revision History

Changes from Revision M (January 2011) to Revision N   **Page**

* Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
* Deleted *Ordering Information* table. 1

6 Pin Configuration and Functions

D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)

Switch Collector	1	8	Driver Collector
Switch Emitter	2	7	I_{pk}
Timing Capacitor	3	6	V_{CC}
GND	4	5	Comparator Inverting Input

DRJ (QFN) PACKAGE
(TOP VIEW)

Switch Collector	1	8	Driver Collector
Switch Emitter	2	7	I_{pk}
Timing Capacitor	3	6	V_{CC}
GND	4	5	Comparator Inverting Input
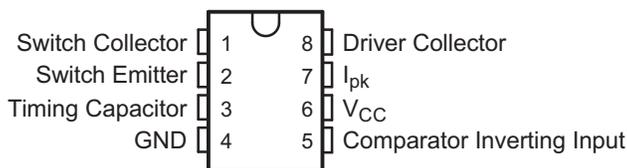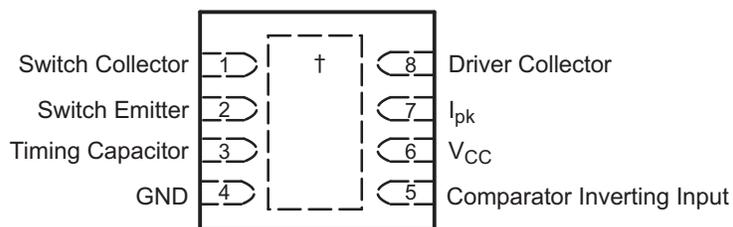
† The exposed thermal pad is electrically bonded internally to pin 4 (GND) .

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Switch Collector	1	I/O	High-current internal switch collector input.
Switch Emitter	2	I/O	High-current internal switch emitter output.
Timing Capacitor	3	—	Attach a timing capacitor to change the switching frequency.
GND	4	—	Ground
Comparator Inverting Input	5	I	Attach to a resistor divider network to create a feedback loop.
V_{CC}	6	I	Logic supply voltage. Tie to V_{IN}.
I_{PK}	7	I	Current-limit sense input.
Driver Collector	8	I/O	Darlington pair driving transistor collector input.

Product Folder Links: *MC33063A MC34063A*

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage			40	V
V_{IR}	Comparator inverting input voltage range		−0.3	40	V
$V_{C(switch)}$	Switch collector voltage			40	V
$V_{E(switch)}$	Switch emitter voltage	$V_{PIN1} = 40$ V		40	V
$V_{CE(switch)}$	Switch collector to switch emitter voltage			40	V
$V_{C(driver)}$	Driver collector voltage			40	V
$I_{C(driver)}$	Driver collector current			100	mA
I_{SW}	Switch current			1.5	A
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	40	V
T_A	Operating free-air temperature	MC33063A	−40	85	°C
		MC34063A	0	70	

7.4 Thermal Information

		MC33063A			UNIT
THERMAL METRIC[1]		D	DRJ	P	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	41	85	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics—Oscillator

$V_{CC} = 5$ V, T_A = full operating range (unless otherwise noted) (see block diagram)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
f_{osc}	Oscillator frequency	$V_{PIN5} = 0$ V, $C_T = 1$ nF	25°C	24	33	42	kHz
I_{chg}	Charge current	$V_{CC} = 5$ V to 40 V	25°C	24	35	42	µA
I_{dischg}	Discharge current	$V_{CC} = 5$ V to 40 V	25°C	140	220	260	µA
I_{dischg}/I_{chg}	Discharge-to-charge current ratio	$V_{PIN7} = V_{CC}$	25°C	5.2	6.5	7.5	—
V_{Ipk}	Current-limit sense voltage	$I_{dischg} = I_{chg}$	25°C	250	300	350	mV

Product Folder Links: *MC33063A MC34063A*

7.6 Electrical Characteristics—Output Switch

V_{CC} = 5 V, T_A = full operating range (unless otherwise noted) (see block diagram)[1]

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$V_{CE(sat)}$	Saturation voltage – Darlington connection	I_{SW} = 1 A, pins 1 and 8 connected	Full range		1	1.3	V
$V_{CE(sat)}$	Saturation voltage – non-Darlington connection[2]	I_{SW} = 1 A, R_{PIN8} = 82 Ω to V_{CC}, forced β ~ 20	Full range		0.45	0.7	V
h_{FE}	DC current gain	I_{SW} = 1 A, V_{CE} = 5 V	25°C	50	75		—
$I_{C(off)}$	Collector off-state current	V_{CE} = 40 V	Full range		0.01	100	µA

(1) Low duty-cycle pulse testing is used to maintain junction temperature as close to ambient temperature as possible.
(2) In the non-Darlington configuration, if the output switch is driven into hard saturation at low switch currents (≤300 mA) and high driver currents (≥30 mA), it may take up to 2 µs for the switch to come out of saturation. This condition effectively shortens the off time at frequencies ≥30 kHz, becoming magnified as temperature increases. The following output drive condition is recommended in the non-Darlington configuration:
Forced β of output switch = $I_{C,SW}$ / ($I_{C,driver}$ − 7 mA) ≥ 10, where ~7 mA is required by the 100-Ω resistor in the emitter of the driver to forward bias the V_{be} of the switch.

7.7 Electrical Characteristics—Comparator

V_{CC} = 5 V, T_A = full operating range (unless otherwise noted) (see block diagram)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{th}	Threshold voltage		25°C	1.225	1.25	1.275	V
			Full range	1.21		1.29	
ΔV_{th}	Threshold-voltage line regulation	V_{CC} = 5 V to 40 V	Full range		1.4	5	mV
I_{IB}	Input bias current	V_{IN} = 0 V	Full range		−20	−400	nA

7.8 Electrical Characteristics—Total Device

V_{CC} = 5 V, T_A = full operating range (unless otherwise noted) (see block diagram)

PARAMETER		TEST CONDITIONS	T_A	MIN	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5 V to 40 V, C_T = 1 nF, V_{PIN7} = V_{CC}, V_{PIN5} > V_{th}, V_{PIN2} = GND, All other pins open	Full range		4	mA

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Product Folder Links: *MC33063A MC34063A*

7.9 Typical Characteristics

Figure 1. Output Switch On-Off Time vs Oscillator Timing Capacitor

V_{CC} = 5 V
Pin 7 = V_{CC}
Pin 5 = GND
T_A = 25°C

t_{ON}
t_{OFF}

Figure 2. Output Switch Saturation Voltage vs Emitter Current (Emitter-Follower Configuration)

V_{CC} = 5 V
Pin 1, 7, 8 = V_{CC}
Pin 3, 5 = GND
T_A = 25°C

Figure 3. Output Switch Saturation Voltage vs Collector Current (Common-Emitter Configuration)

Darlington Connection

Force Beta = 20

V_{CC} = 5 V
Pin 7 = V_{CC}
Pin 2, 3, 5 = GND
T_A = 25°C

Figure 4. Standby Supply Current vs Supply Voltage

C_T = 1 nF
Pin 7 = V_{CC}
Pin 2 = GND
T_A = 25°C

Product Folder Links: *MC33063A   MC34063A*

8 Detailed Description

8.1 Overview

The MC33063A and MC34063A devices are easy-to-use ICs containing all the primary circuitry needed for building simple DC-DC converters. These devices primarily consist of an internal temperature-compensated reference, a comparator, an oscillator, a PWM controller with active current limiting, a driver, and a high-current output switch. Thus, the devices require minimal external components to build converters in the boost, buck, and inverting topologies.

The MC33063A device is characterized for operation from –40°C to 85°C, while the MC34063A device is characterized for operation from 0°C to 70°C.

8.2 Functional Block Diagram
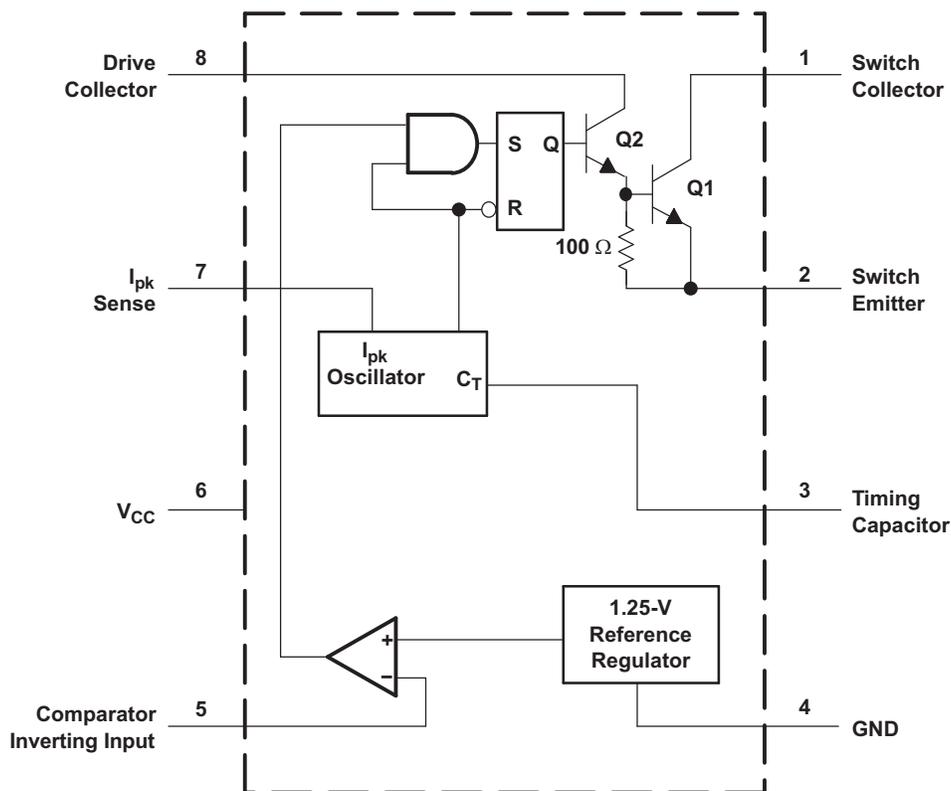
8.3 Feature Description

- Wide Input Voltage Range: 3 V to 40 V
- High Output Switch Current: Up to 1.5 A
- Adjustable Output Voltage
- Oscillator Frequency Up to 100 kHz
- Precision Internal Reference: 2%
- Short-Circuit Current Limiting
- Low Standby Current

8.4 Device Functional Modes

8.4.1 Standard operation

Based on the application, the device can be configured in multiple different topologies. See the *Application and Implementation* section for how to configure the device in several different operating modes.

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 External Switch Configurations for Higher Peak Current
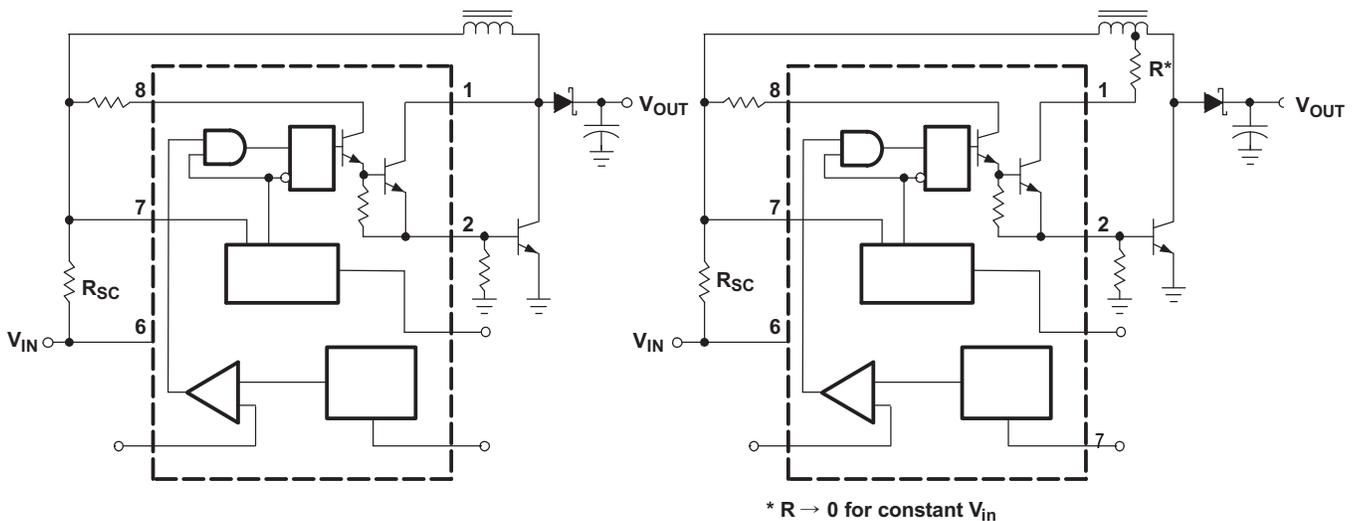
a) EXTERNAL npn SWITCH

b) EXTERNAL npn SATURATED SWITCH (see Note A)

* R → 0 for constant V$_{in}$

A. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300 mA) and high driver currents (≥30 mA), it may take up to 2 µs to come out of saturation. This condition will shorten the off time at frequencies ≥30 kHz and is magnified at high temperatures. This condition does not occur with a Darlington configuration because the output switch cannot saturate. If a non-Darlington configuration is used, the output drive configuration in Figure 7b is recommended.

Figure 5. Boost Regulator Connections for I$_C$ Peak Greater Than 1.5 A

Application Information (continued)

a) EXTERNAL npn SWITCH

b) EXTERNAL pnp SATURATED SWITCH
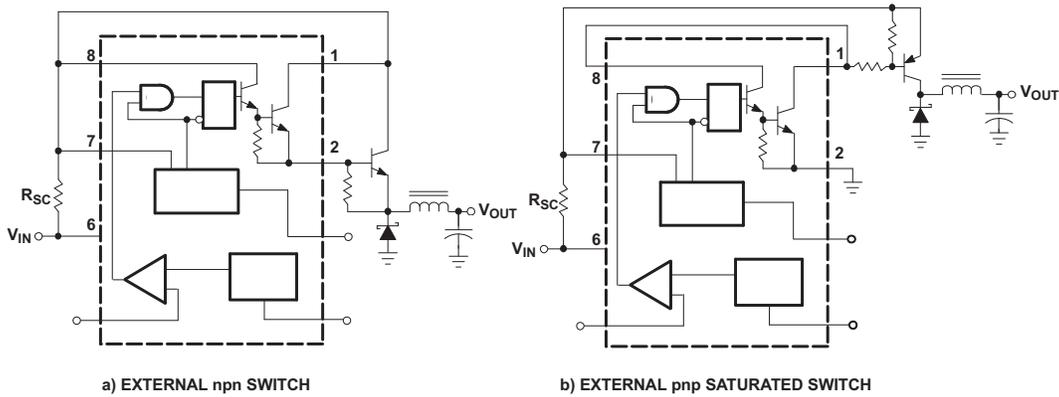
Figure 6. Buck Regulator Connections for I_C Peak Greater Than 1.5 A

a) External NPN Switch

b) External PNP Saturated Switch
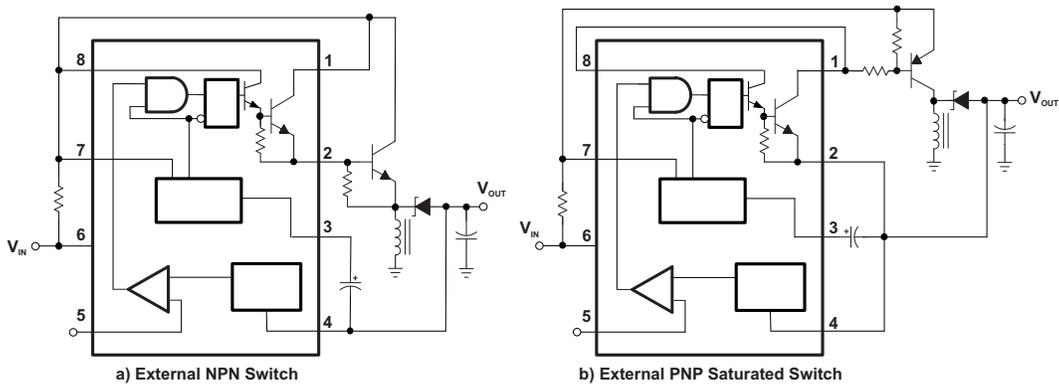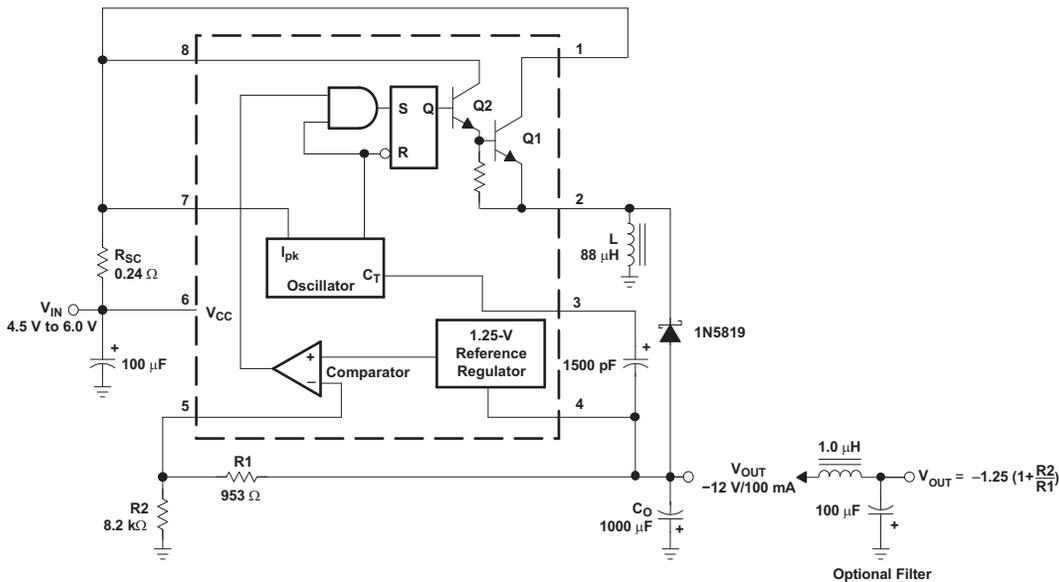
Figure 7. Inverting Regulator Connections for I_C Peak Greater Than 1.5 A

9.2 Typical Application

9.2.1 Voltage-Inverting Converter Application

$$V_{OUT} = -1.25 \left(1 + \frac{R2}{R1}\right)$$

Product Folder Links: *MC33063A MC34063A*

Typical Application (continued)

Figure 8. Voltage-Inverting Converter

Product Folder Links: *MC33063A MC34063A*

Typical Application (continued)

9.2.1.1 Design Requirements

The user must determine the following desired parameters:

V_{sat} = Saturation voltage of the output switch

V_F = Forward voltage drop of the chosen output rectifier

The following power-supply parameters are set by the user:

V_{in} = Nominal input voltage

V_{out} = Desired output voltage

I_{out} = Desired output current

f_{min} = Minimum desired output switching frequency at the selected values of V_{in} and I_{out}

V_{ripple} = Desired peak-to-peak output ripple voltage. The ripple voltage directly affects the line and load regulation and, thus, must be considered. In practice, the actual capacitor value should be larger than the calculated value, to account for the capacitor's equivalent series resistance and board layout.

9.2.1.2 Detailed Design Procedure

CALCULATION	VOLTAGE INVERTING
t_{on}/t_{off}	$\dfrac{\lvert V_{out} \rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\dfrac{1}{f}$
t_{off}	$\dfrac{t_{on} + t_{off}}{\dfrac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$
C_T	$4 \times 10^{-5} \, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\dfrac{t_{on}}{t_{off}} + 1 \right)$
R_{SC}	$\dfrac{0.3}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\dfrac{\left(V_{in(min)} - V_{sat} \right)}{I_{pk(switch)}} \right) t_{on(max)}$
C_O	$9 \dfrac{I_{out} t_{on}}{V_{ripple(pp)}}$
V_{out}	$-1.25 \left(1 + \dfrac{R2}{R1} \right)$ See Figure 8

9.2.1.3 Application Performance

Figure 9. Current-Limit Sense Voltage vs Temperature
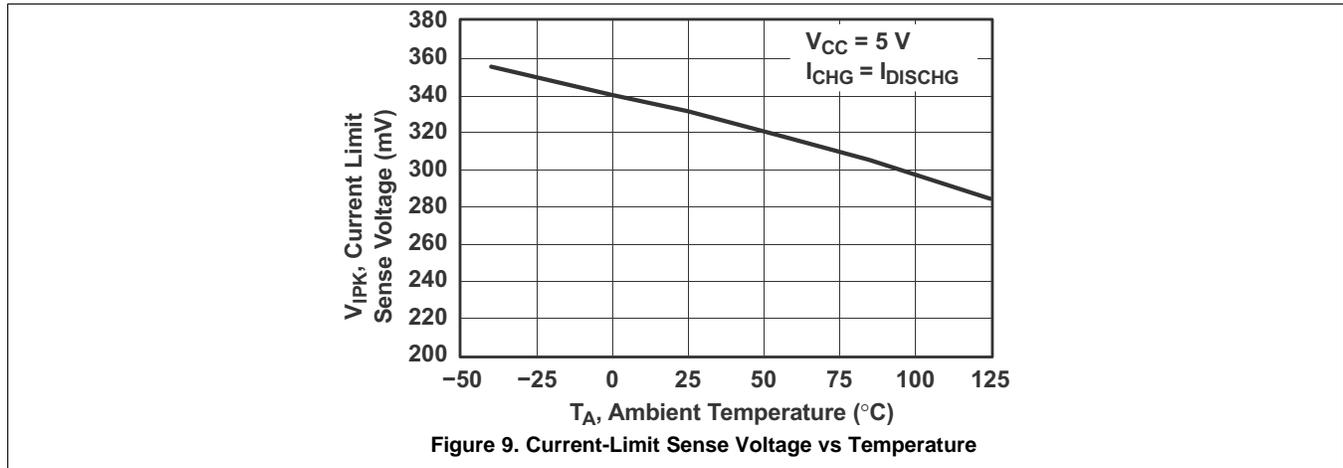
TEST	CONDITIONS	RESULTS
Line regulation	V_{IN} = 4.5 V to 6 V, I_O = 100 mA	3 mV ± 0.12%
Load regulation	V_{IN} = 5 V, I_O = 10 mA to 100 mA	0.022 V ± 0.09%
Output ripple	V_{IN} = 5 V, I_O = 100 mA	500 mV$_{PP}$
Short-circuit current	V_{IN} = 5 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{IN} = 5 V, I_O = 100 mA	62.2%
Output ripple with optional filter	V_{IN} = 5 V, I_O = 100 mA	70 mV$_{PP}$

Product Folder Links: *MC33063A MC34063A*

9.2.2 Step-Up Converter Application
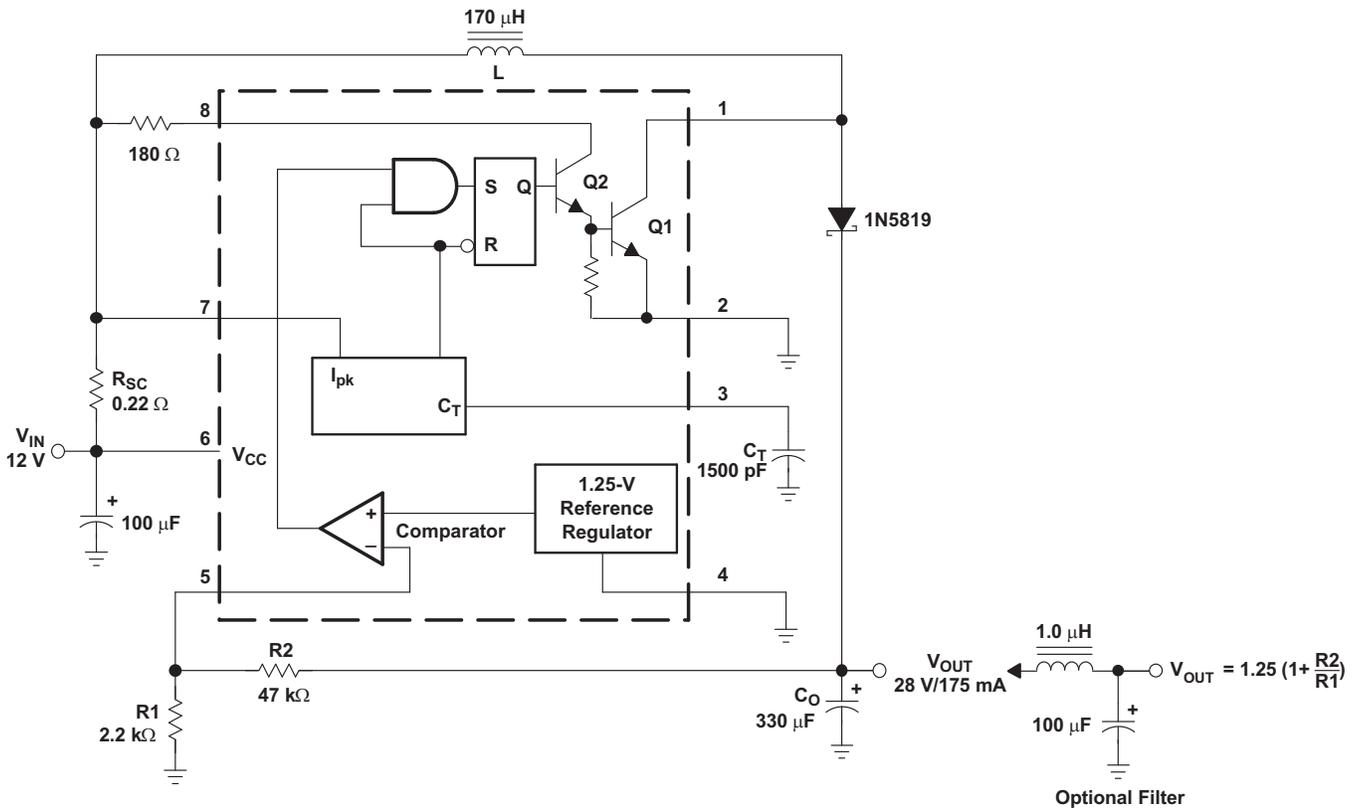
Figure 10. Step-Up Converter

9.2.2.1 Design Requirements

The user must determine the following desired parameters:

V_{sat} = Saturation voltage of the output switch

V_F = Forward voltage drop of the chosen output rectifier

The following power-supply parameters are set by the user:

V_{in} = Nominal input voltage

V_{out} = Desired output voltage

I_{out} = Desired output current

f_{min} = Minimum desired output switching frequency at the selected values of V_{in} and I_{out}

V_{ripple} = Desired peak-to-peak output ripple voltage. The ripple voltage directly affects the line and load regulation and, thus, must be considered. In practice, the actual capacitor value should be larger than the calculated value, to account for the capacitor's equivalent series resistance and board layout.

9.2.2.2 Detailed Design Procedure

CALCULATION	STEP UP
t_{on}/t_{off}	$$\dfrac{V_{out} + V_{F-Vin(min)}}{V_{in(min)} - V_{sat}}$$
$(t_{on} + t_{off})$	$$\dfrac{1}{f}$$
t_{off}	$$\dfrac{t_{on} + t_{off}}{\dfrac{t_{on}}{t_{off}} + 1}$$
t_{on}	$$\left(t_{on} + t_{off}\right) - t_{off}$$
C_T	$$4 \times 10^{-5}\, t_{on}$$
$I_{pk(switch)}$	$$2 I_{out(max)}\left(\dfrac{t_{on}}{t_{off}} + 1\right)$$
R_{SC}	$$\dfrac{0.3}{I_{pk(switch)}}$$
$L_{(min)}$	$$\left(\dfrac{\left(V_{in(min)} - V_{sat}\right)}{I_{pk(switch)}}\right) t_{on(max)}$$
C_O	$$9\,\dfrac{I_{out}\, t_{on}}{V_{ripple(pp)}}$$
V_{out}	$$1.25\left(1 + \dfrac{R2}{R1}\right)$$ See Figure 10

9.2.2.3 Application Performance

| TEST	CONDITIONS	RESULTS
Line regulation	V_{IN} = 8 V to 16 V, I_O = 175 mA	30 mV ± 0.05%
Load regulation	V_{IN} = 12 V, I_O = 75 mA to 175 mA	10 mV ± 0.017%
Output ripple	V_{IN} = 12 V, I_O = 175 mA	400 mV$_{PP}$
Efficiency	V_{IN} = 12 V, I_O = 175 mA	87.7%
Output ripple with optional filter	V_{IN} = 12 V, I_O = 175 mA	40 mV$_{PP}$

9.2.3 Step-Down Converter Application
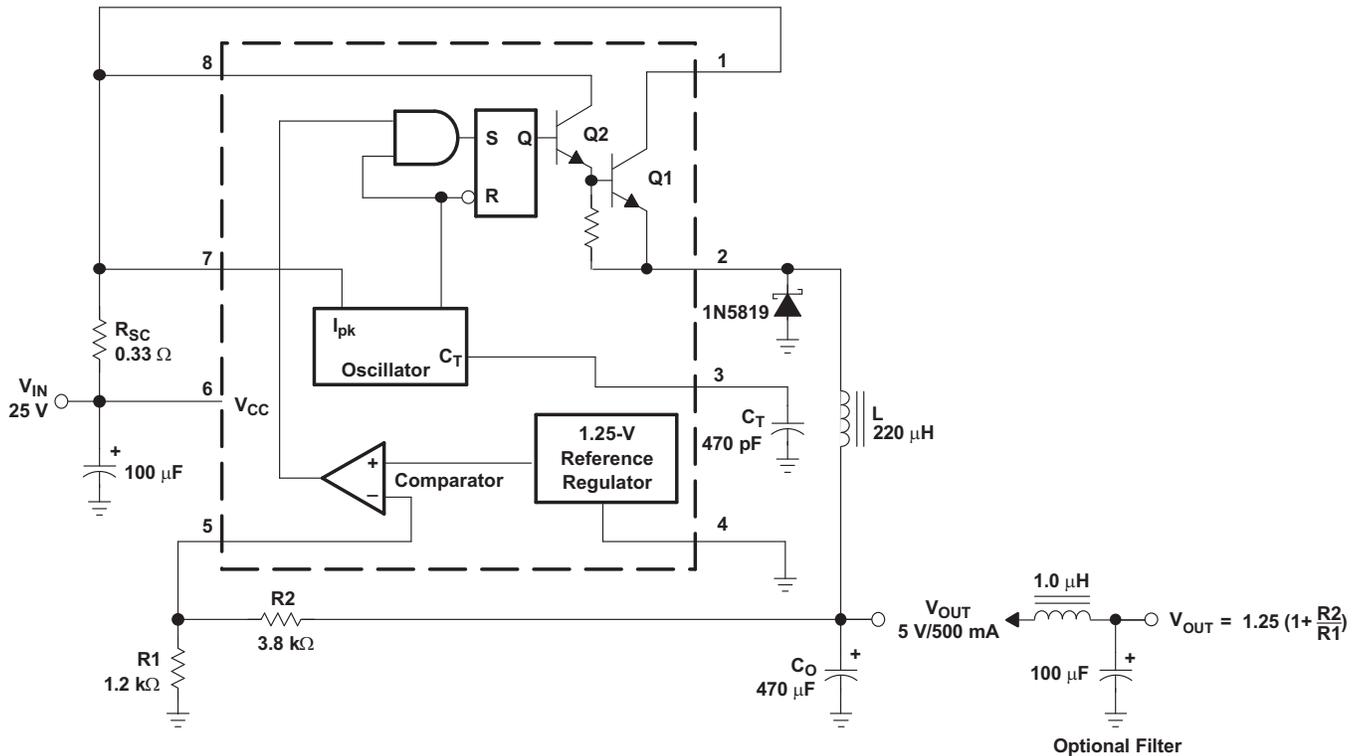
Figure 11. Step-Down Converter

9.2.3.1 Design Requirements

The user must determine the following desired parameters:

V_{sat} = Saturation voltage of the output switch

V_F = Forward voltage drop of the chosen output rectifier

The following power-supply parameters are set by the user:

   V_{in} = Nominal input voltage
   V_{out} = Desired output voltage
   I_{out} = Desired output current
   f_{min} = Minimum desired output switching frequency at the selected values of V_{in} and I_{out}

   V_{ripple} = Desired peak-to-peak output ripple voltage. The ripple voltage directly affects the line and load regulation and, thus, must be considered. In practice, the actual capacitor value should be larger than the calculated value, to account for the capacitor's equivalent series resistance and board layout.

9.2.3.2 Detailed Design Procedure

CALCULATION	STEP DOWN
t_{on}/t_{off}	$\dfrac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$
$(t_{on} + t_{off})$	$\dfrac{1}{f}$
t_{off}	$\dfrac{t_{on} + t_{off}}{\dfrac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$
C_T	$4 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}$
R_{SC}	$\dfrac{0.3}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\dfrac{\left(V_{in(min)} - V_{sat} - V_{out} \right)}{I_{pk(switch)}} \right) t_{on(max)}$
C_O	$\dfrac{I_{pk(switch)} \left(t_{on} + t_{off} \right)}{8 V_{ripple(pp)}}$
V_{out}	$1.25 \left(1 + \dfrac{R2}{R1} \right)$ See Figure 11

9.2.3.3 Application Performance

TEST	CONDITIONS	RESULTS
Line regulation	V_{IN} = 15 V to 25 V, I_O = 500 mA	12 mV ± 0.12%
Load regulation	V_{IN} = 25 V, I_O = 50 mA to 500 mA	3 mV ± 0.03%
Output ripple	V_{IN} = 25 V, I_O = 500 mA	120 mV$_{PP}$
Short-circuit current	V_{IN} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{IN} = 25 V, I_O = 500 mA	83.7%
Output ripple with optional filter	V_{IN} = 25 V, I_O = 500 mA	40 mV$_{PP}$

Product Folder Links: *MC33063A   MC34063A*

10 Power Supply Recommendations

This device accepts 3 V to 40 V on the input. It is recommended to have a 1000-µF decoupling capacitor on the input.

11 Layout

11.1 Layout Guidelines

Keep feedback loop layout trace lengths to a minimum to avoid unnecessary IR drop. In addition, the loop for the decoupling capacitor at the input should be as small as possible. The trace from V_{IN} to pin 1 of the device should be thicker to handle the higher current.

11.2 Layout Example
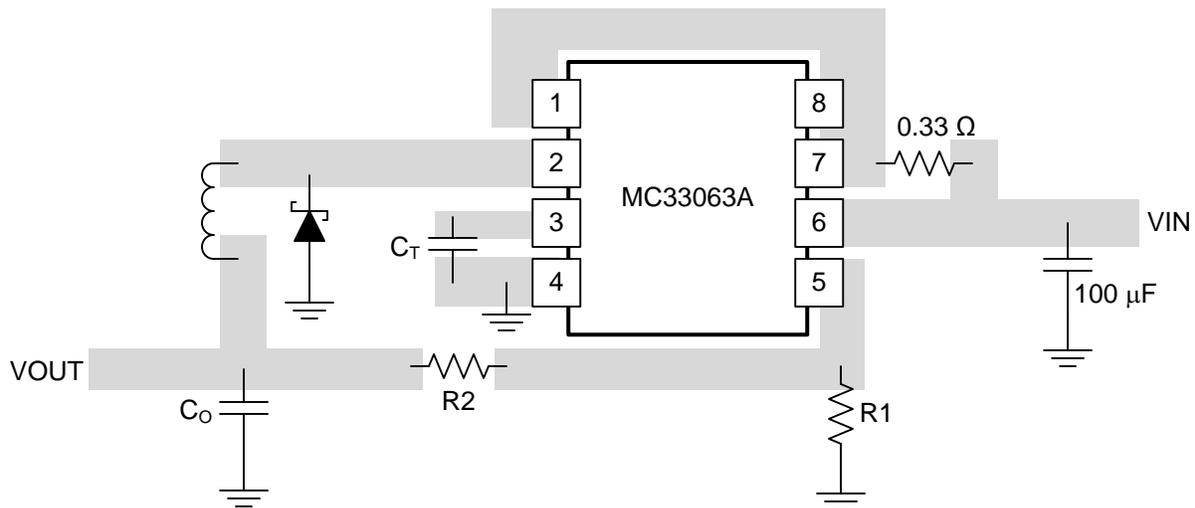
Figure 12. Layout Example for a Step-Down Converter

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MC33063A	Click here	Click here	Click here	Click here	Click here
MC34063A	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *MC33063A MC34063A*

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MC33063AD	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063AD.A	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063ADE4	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063ADG4	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063ADRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063ADRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33063A
MC33063ADRJR	Last Time Buy	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ZYF
MC33063ADRJR.A	Last Time Buy	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ZYF
MC33063AP	Last Time Buy	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MC33063AP
MC33063AP.A	Last Time Buy	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MC33063AP
MC33063APE4	Last Time Buy	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MC33063AP
MC34063AD	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	M34063A
MC34063AD.A	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	M34063A
MC34063ADE4	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	M34063A
MC34063ADG4	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	M34063A
MC34063ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	M34063A
MC34063ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	M34063A

Orderable part number (1)	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MC34063ADRJR	Last Time Buy	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	ZYF
MC34063ADRJR.A	Last Time Buy	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	ZYF
MC34063ADRJRG4	Last Time Buy	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	ZYF
MC34063AP	Last Time Buy	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MC34063AP
MC34063AP.A	Last Time Buy	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MC34063AP
MC34063APE4	Last Time Buy	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MC34063AP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF MC33063A :

● Automotive : MC33063A-Q1

NOTE: Qualified Version Definitions:

     ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants
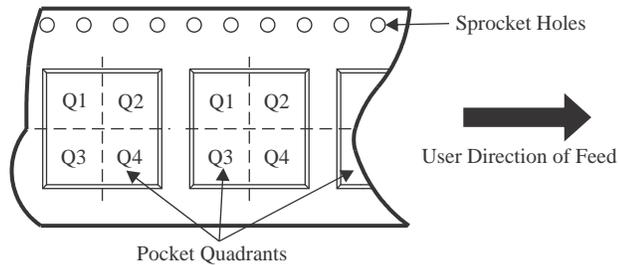
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC33063ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC33063ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC33063ADRJR	SON	DRJ	8	1000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MC34063ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC33063ADR	SOIC	D	8	2500	340.5	338.1	20.6
MC33063ADR	SOIC	D	8	2500	353.0	353.0	32.0
MC33063ADRJR	SON	DRJ	8	1000	353.0	353.0	32.0
MC34063ADR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE
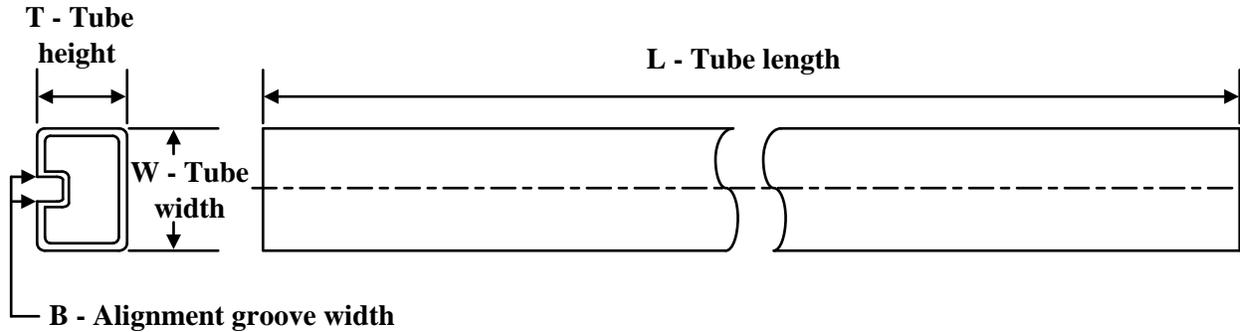
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MC33063AD	D	SOIC	8	75	507	8	3940	4.32
MC33063AD	D	SOIC	8	75	506.6	8	3940	4.32
MC33063AD.A	D	SOIC	8	75	507	8	3940	4.32
MC33063AD.A	D	SOIC	8	75	506.6	8	3940	4.32
MC33063ADE4	D	SOIC	8	75	507	8	3940	4.32
MC33063ADE4	D	SOIC	8	75	506.6	8	3940	4.32
MC33063ADG4	D	SOIC	8	75	507	8	3940	4.32
MC33063ADG4	D	SOIC	8	75	506.6	8	3940	4.32
MC33063AP	P	PDIP	8	50	506	13.97	11230	4.32
MC33063AP.A	P	PDIP	8	50	506	13.97	11230	4.32
MC33063APE4	P	PDIP	8	50	506	13.97	11230	4.32
MC34063AD	D	SOIC	8	75	507	8	3940	4.32
MC34063AD.A	D	SOIC	8	75	507	8	3940	4.32
MC34063ADE4	D	SOIC	8	75	507	8	3940	4.32
MC34063ADG4	D	SOIC	8	75	507	8	3940	4.32
MC34063AP	P	PDIP	8	50	506	13.97	11230	4.32
MC34063AP.A	P	PDIP	8	50	506	13.97	11230	4.32
MC34063APE4	P	PDIP	8	50	506	13.97	11230	4.32

DRJ (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

$\frac{4,10}{3,90}$ [A]

[B]

8   5

$\frac{4,10}{3,90}$

Pin 1 Index Area
Top and Bottom

1   4

0,20 Nominal
Lead Frame

$\frac{0,80}{0,70}$

Seating Plane

[⌒] 0,08 [C]

$\frac{0,05}{0,00}$ [C]

[0,80]

8X $\frac{0,60}{0,40}$

1   4

Exposed Thermal Die Pad

[D]

8   5

8X $\frac{0,35}{0,25}$

| ⊕ | 0,10 Ⓜ | C | A | B |
| | 0,05 Ⓜ | C | | |

Bottom View

4205439/C 12/10
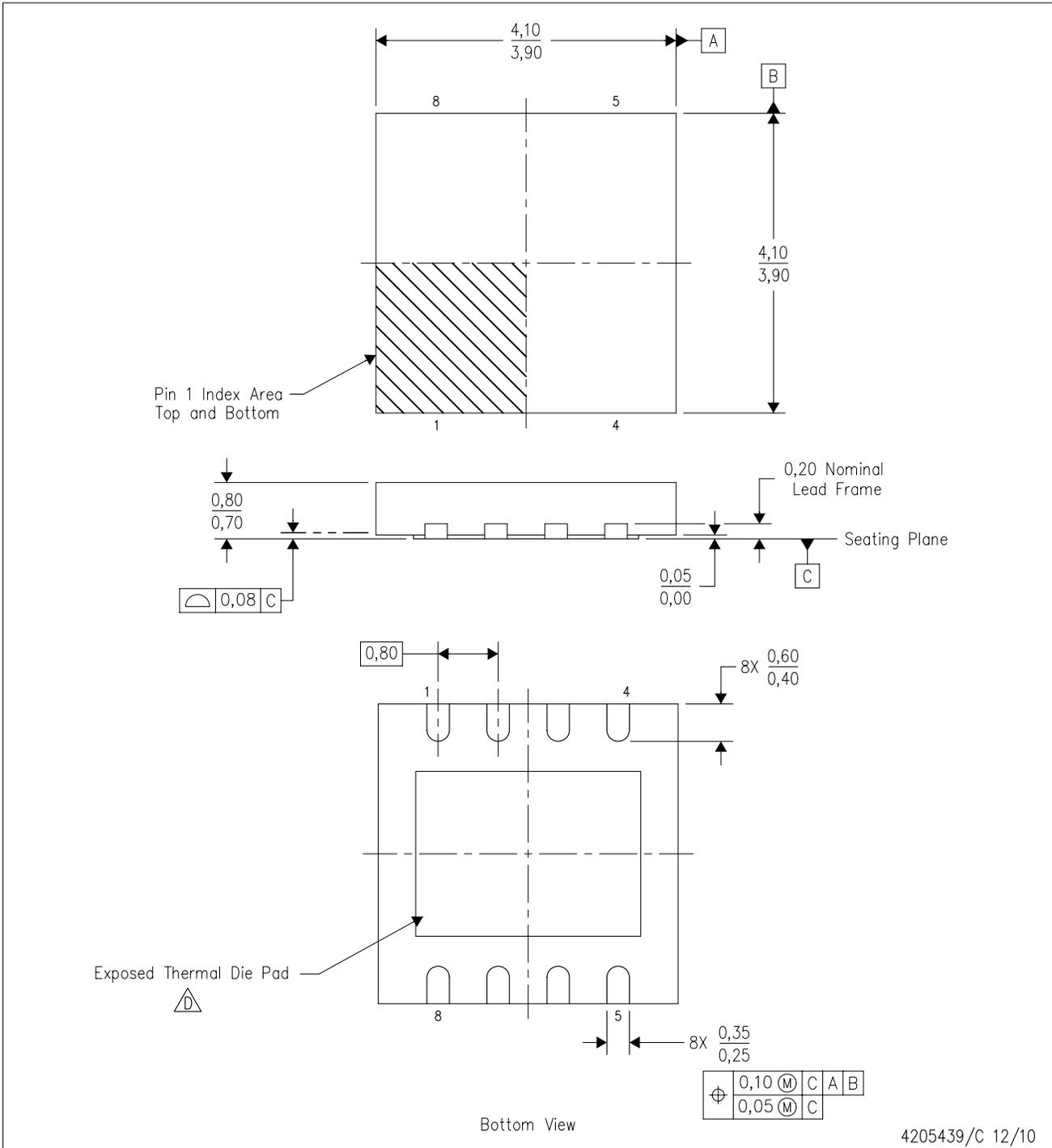
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. SON (Small Outline No−Lead) package configuration.

         [D] The package thermal pad must be soldered to the board for thermal and mechanical performance.
              See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E. Package complies to JEDEC MO−229 variation WGGB.

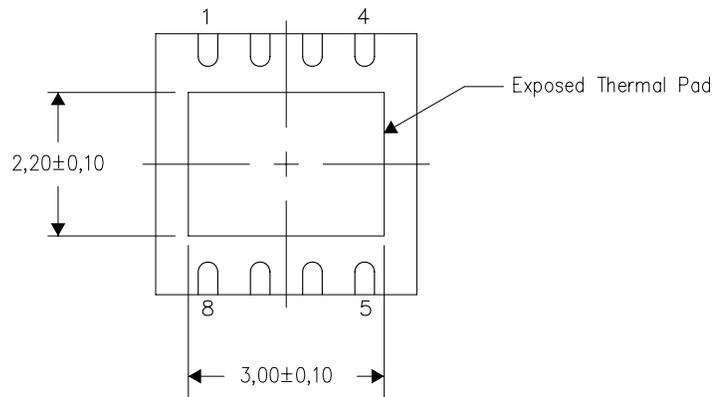DRJ (S−PWSON−N8)   PLASTIC SMALL OUTLINE NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external
heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the
PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached
directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be
attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the
integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report,
QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

2,20±0,10

3,00±0,10

Bottom View

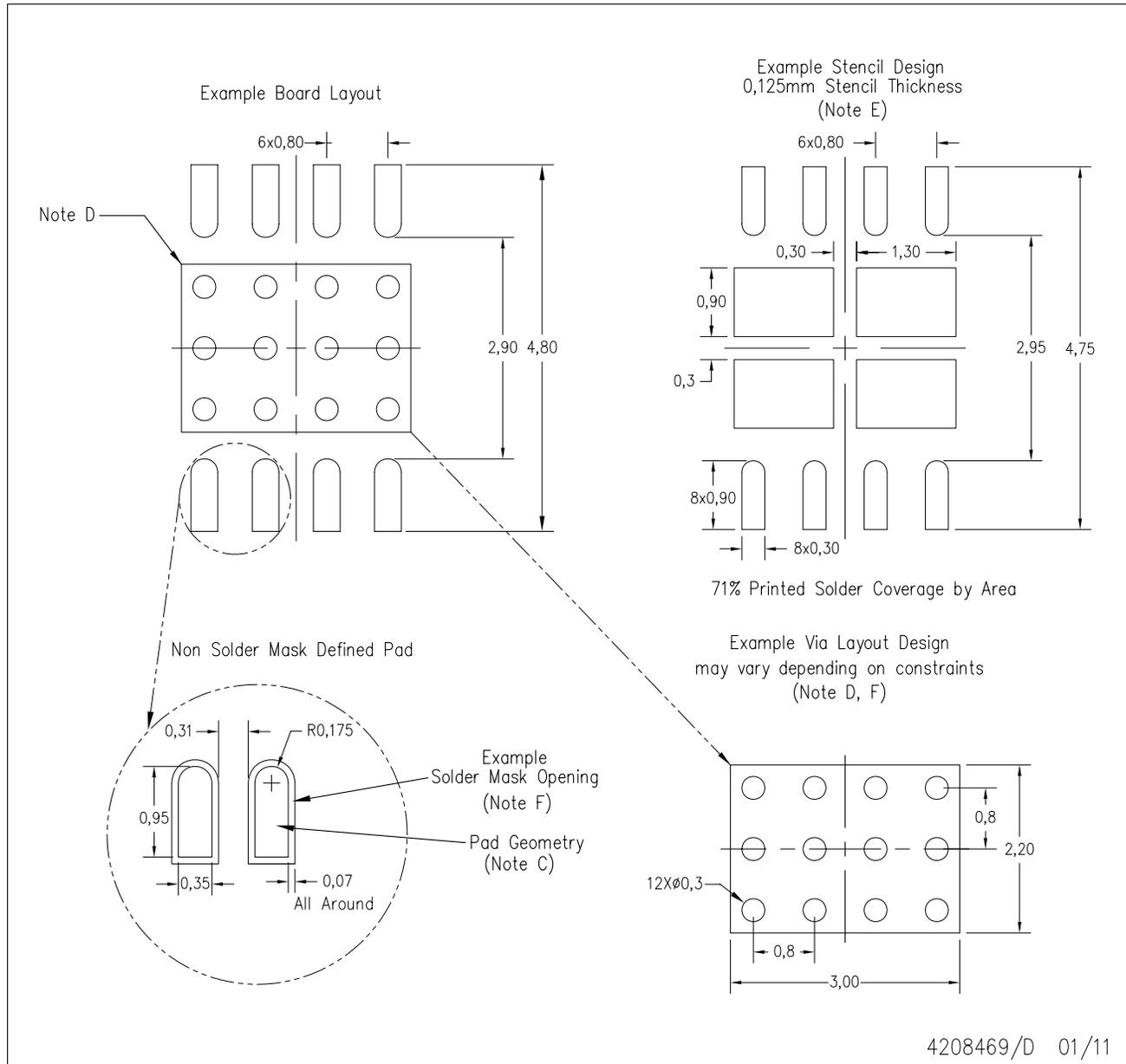Exposed Thermal Pad Dimensions

4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S−PWSON−N8)   SMALL PACKAGE OUTLINE NO−LEAD

Example Board Layout

6x0,80

Note D

2,90   4,80

Non Solder Mask Defined Pad

0,31   R0,175

0,95

0,35   0,07
        All Around

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

Example Stencil Design
0,125mm Stencil Thickness
(Note E)

6x0,80

0,30   1,30

0,90

0,3

2,95   4,75

8x0,90

8x0,30

71% Printed Solder Coverage by Area

Example Via Layout Design
may vary depending on constraints
(Note D, F)

0,8

2,20

12X∅0,3

0,8

3,00

4208469/D   01/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout. These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for solder mask tolerances and vias tenting
              recommendations for vias placed in the thermal pad.

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.228-.244   TYP
[5.80-6.19]

A

PIN 1 ID AREA

1

.189-.197
[4.81-5.00]
NOTE 3

4

B

.150-.157
[3.81-3.98]
NOTE 4

6X .050
[1.27]

8

2X

.150
[3.81]

5

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

C

SEATING PLANE

△ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
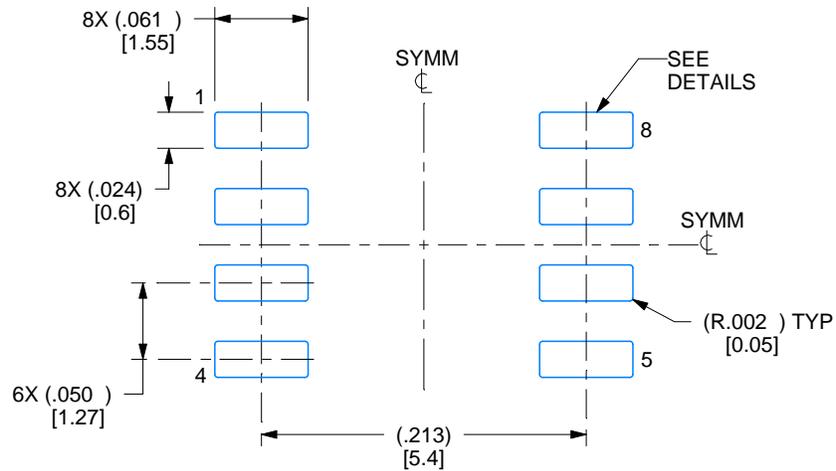TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
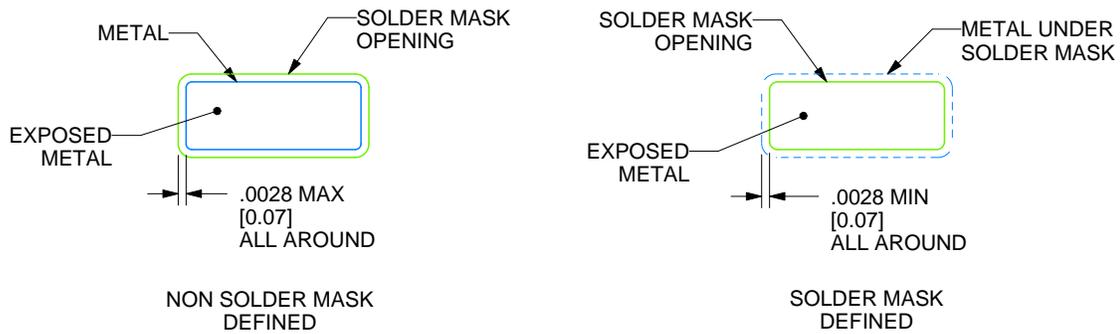₵

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
₵

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
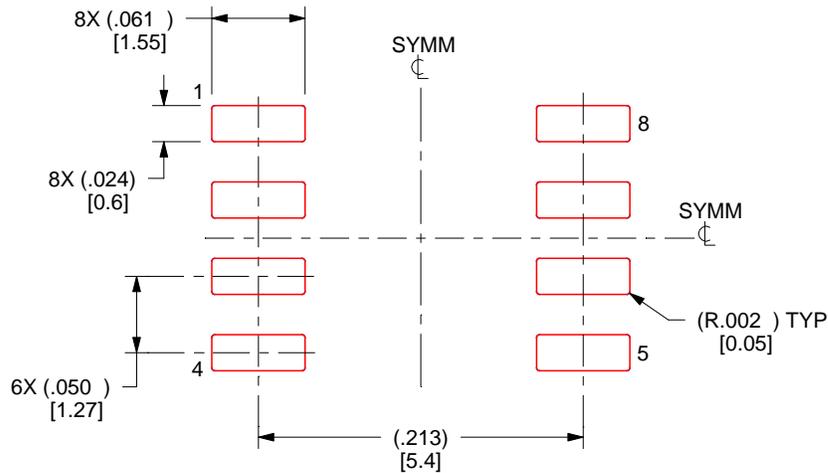7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

SYMM
₵

8

SYMM
₵

6X (.050)
[1.27]

4

5

(R.002) TYP
[0.05]

(.213)
[5.4]

SOLDER PASTE EXAMPLE
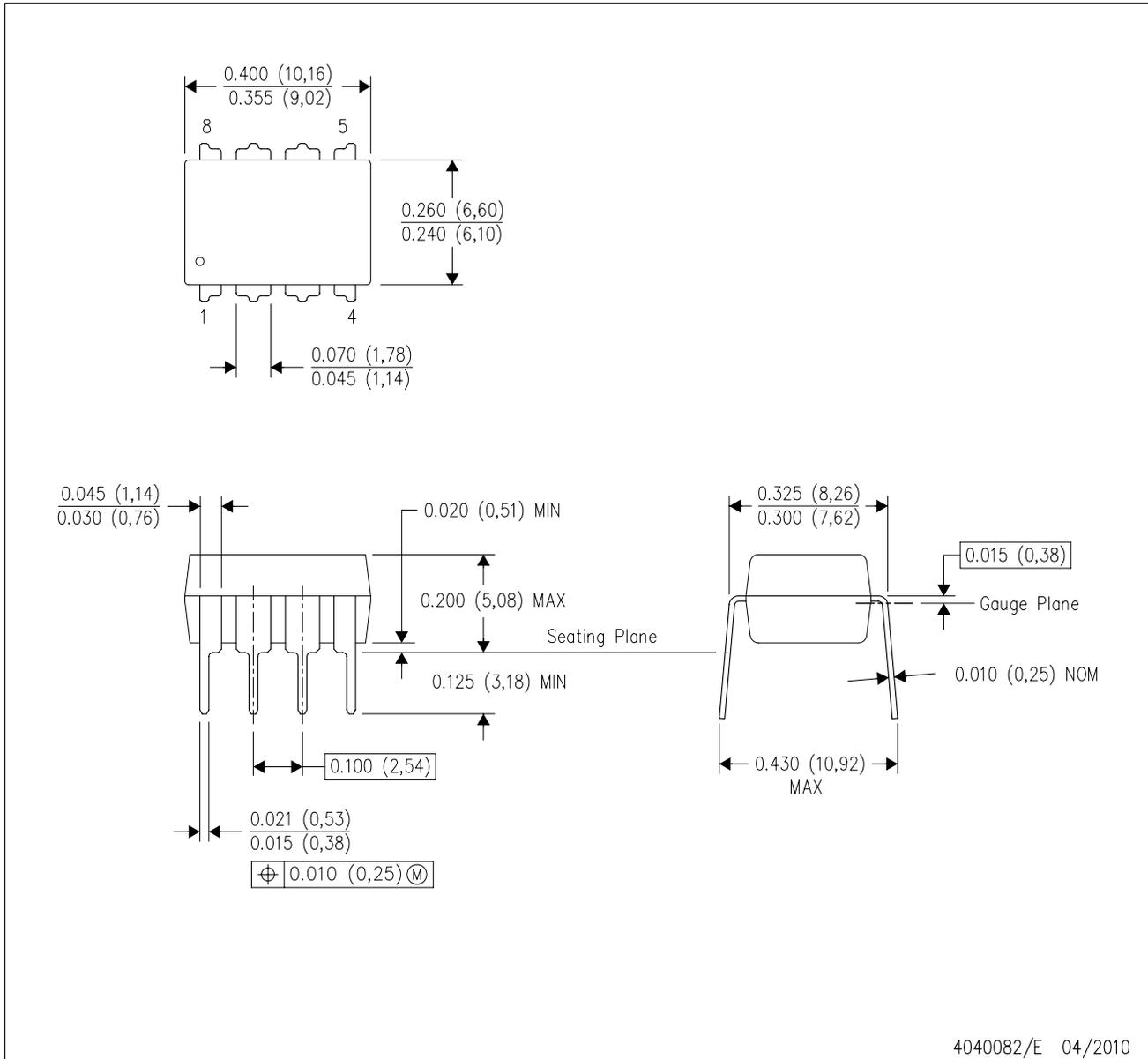BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE

$\dfrac{0.400\ (10,16)}{0.355\ (9,02)}$

8   5

$\dfrac{0.260\ (6,60)}{0.240\ (6,10)}$

1   4

$\dfrac{0.070\ (1,78)}{0.045\ (1,14)}$

$\dfrac{0.045\ (1,14)}{0.030\ (0,76)}$

0.020 (0,51) MIN

0.200 (5,08) MAX

0.125 (3,18) MIN

Seating Plane

0.100 (2,54)

$\dfrac{0.021\ (0,53)}{0.015\ (0,38)}$

⊕ 0.010 (0,25) Ⓜ

$\dfrac{0.325\ (8,26)}{0.300\ (7,62)}$

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX

4040082/E   04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Falls within JEDEC MS−001 variation BA.

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