MSP430FR596x、MSP430FR594x ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 組み込みマイクロコントローラ
  - 16ビットのRISCアーキテクチャ、最大16MHzのクロック
  - 3.6V～1.8Vの広い電源電圧範囲(最小電源電圧はSVSレベルにより制限されます。「SVS仕様」を参照)
- 最適化された超低消費電力モード
  - アクティブ・モード: 約100µA/MHz
  - スタンバイ(VLOありのLPM3): 0.4µA (標準値)
  - リアルタイム・クロック(LPM3.5): 0.25µA (標準値)(1)
  - シャットダウン(LPM4.5): 0.02µA (標準値)
- 超低消費電力の強誘電体RAM (FRAM)
  - 最大64KBの不揮発性メモリ
  - 超低消費電力の書き込み
  - ワードあたり125nsの高速書き込み(4msで64KB)
  - ユニファイド・メモリによりプログラム、データ、ストレージを1か所に保存
  - 10^{15}回の書き込み耐久性
  - 放射耐性および非磁性
- インテリジェントなデジタル・ペリフェラル
  - 32ビットのハードウェア・マルチプライヤ(MPY)
  - 3チャネルの内蔵DMA
  - カレンダーおよびアラーム機能を搭載したリアルタイム・クロック(RTC)
  - 5つの16ビット・タイマ、それぞれに最大7つのキャプチャ/比較レジスタを搭載
  - 16ビットの巡回冗長性チェッカ(CRC)
- 高性能アナログ
  - 16チャネルのアナログ・コンパレータ
  - 12ビットのアナログ/デジタル・コンバータ(ADC)、基準電圧とサンプル・アンド・ホールド機能を内蔵し、最大16の外部入力チャネル
- マルチファンクションの入力/出力ポート
  - すべてのピンが外付け部品なしで静電容量式タッチ機能をサポート
  - ビット、バイト、ワード単位でアクセス可能(ペアで)
  - すべてのポートでLPMからのウェークアップをエッジ選択可能
  - すべてのポートでプルアップおよびプルダウンをプログラム可能
- コードのセキュリティと暗号化
  - 128ビットまたは256ビットのAESセキュリティ暗号化および復号化コプロセッサ
  - 乱数シードによる乱数生成アルゴリズム
- シリアル通信の拡張機能
  - eUSCI_A0およびeUSCI_A1でのサポート
    - 自動ボーレート検出機能付きのUART
    - IrDAのエンコードおよびデコード
    - SPI
  - eUSCI_B0でのサポート
    - 複数のスレーブ・アドレシングを持つI^2C
    - SPI
  - ハードウェアUARTまたはI^2Cブートローダー(BSL)
- 柔軟なクロック・システム
  - 固定周波数DCO、出荷時にトリムされた10の周波数を選択可能
  - 低電力、低周波数の内部クロック・ソース(VLO)
  - 32kHzの水晶振動子(LFXT)
  - 高周波数の水晶振動子(HFXT)
- 開発ツールとソフトウェア
  - 無償のプロフェッショナル開発環境: EnergyTrace++™ テクノロジを使用
  - 開発キット(MSP-TS430RGZ48C)
- ファミリ製品
  - 利用可能なデバイスのバリエーションおよびパッケージ・タイプについては、「デバイスの比較」の概要を参照してください。
- モジュールの完全な説明については、*『MSP430FR58xx、MSP430FR59xx、MSP430FR6xxファミリ・ユーザー・ガイド』*を参照してください。

(1) RTCは3.7pFの水晶振動子によりクロック供給を受けます。

1.2 アプリケーション

- 計量
- 環境発電のセンサ・ノード
- ウェアラブル・エレクトロニクス
- センサ管理
- データ・ロギング

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1.3 概要

MSP430™超低消費電力(ULP) FRAMプラットフォームは、独自の組み込みFRAMと包括的な超低消費電力システム・アーキテクチャとを組み合わせ、より低いエネルギー・バジェットで性能向上を可能にした、イノベータ向けの製品です。FRAMテクノロジにより、SRAMの速度、柔軟性、耐久性と、フラッシュの安定性および信頼性の両方が、はるかに低い消費電力で得られます。

MSP430 ULP FRAMポートフォリオは、FRAM、ULP 16ビットMSP430 CPU、およびインテリジェントなペリフェラルを搭載し、各種のアプリケーションを対象とした、多様なデバイスのセットで構成されます。ULPアーキテクチャには7つの低消費電力モードがあり、エネルギーの制約が厳しいアプリケーションでバッテリ駆動時間を延長できるよう最適化されています。

製品情報(1)

型番	パッケージ	本体サイズ(2)
MSP430FR5969IRGZ	VQFN (48)	7mm×7mm
MSP430FR5959IRHA	VQFN (40)	6mm×6mm
MSP430FR5959IDA	TSSOP (38)	12.5mm×6.2mm

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については 9の「*付録:パッケージ・オプション*」またはwww.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9の「*メカニカル・データ*」を参照してください。

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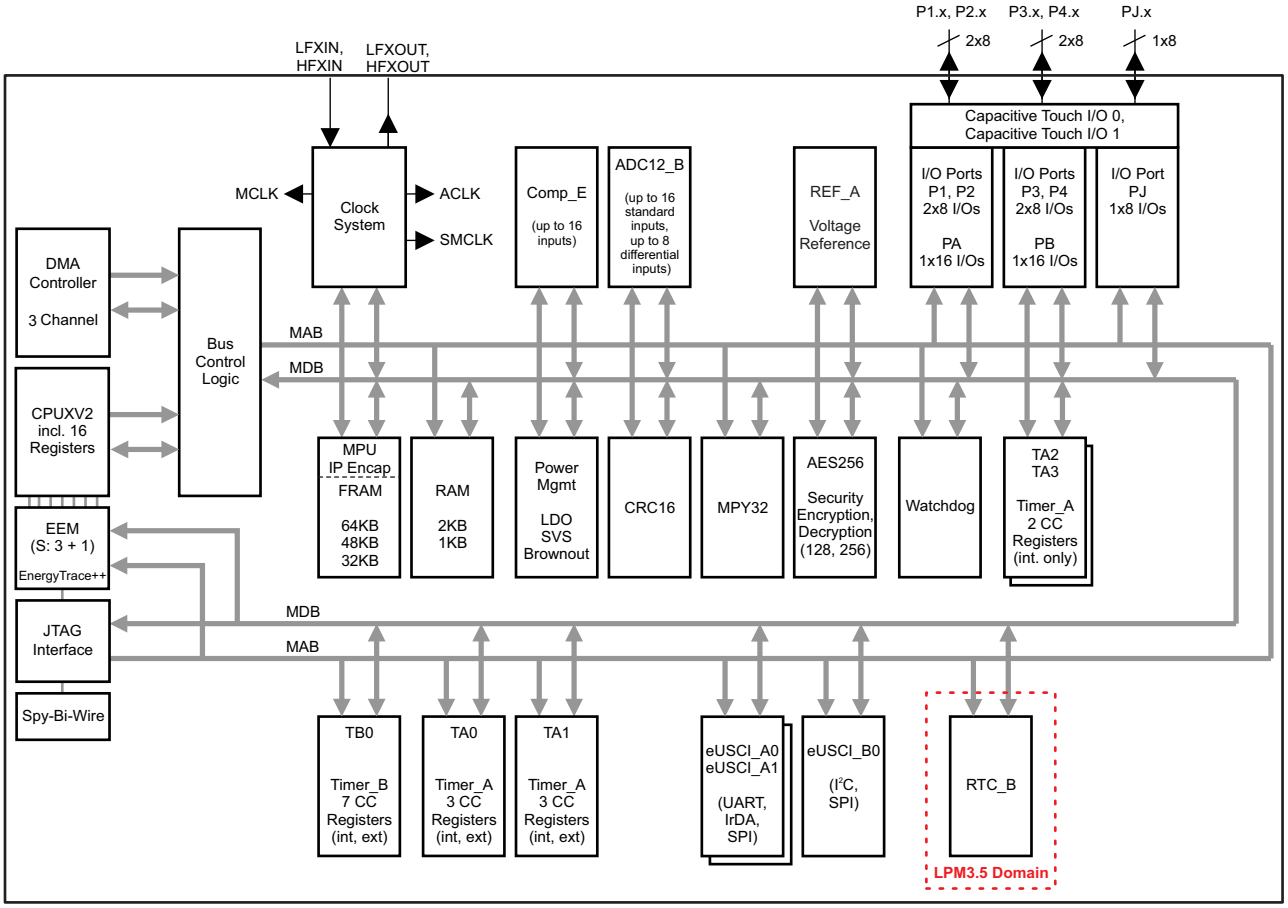
1.4 機能ブロック図

デバイスの機能ブロック図を図 1-1に示します。



A. 低周波数(LF)水晶発振器と、対応するLFXINおよびLFXOUTピンは、MSP430FR5x6xおよびMSP430FR5x4xデバイスでのみ利用可能です。

RTC_Bは、MSP430FR5x6xおよびMSP430FR5x4xデバイスのLF水晶発振器との組み合わせでのみ利用可能です。

B. 高周波数(HF)水晶発振器と、対応するHFXINおよびHFXOUTピンは、MSP430FR5x6xおよびMSP430FR5x5xデバイスでのみ利用可能です。

HF水晶発振器のみを搭載したMSP430FR5x5xデバイスには、RTC_Bモジュールは含まれません。

図 1-1. 機能ブロック図

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2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年3月10日発行分から2018年08月29日発行分への変更 **Page**

- Updated Section 3.1, *Related Products* 7
- Added note (1) to 表 5-2, *SVS*..... 26
- Changed capacitor value from 4.7 µF to 470 nF in 図 7-5, *ADC12_B Grounding and Noise Considerations* 120
- Changed capacitor value from 4.7 µF to 470 nF in the last paragraph of 7.2.1.2, *Design Requirements* 121
- 8.2「*デバイスの項目表記*」のテキストおよび図を更新..... 122

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)(2)

DEVICE	FRAM (KB)	SRAM (KB)	CLOCK SYSTEM	ADC12_B	Comp_E	Timer_A(3)	Timer_B(4)	eUSCI		AES	BSL	I/O	PACKAGE
								A(5)	B(6)				
MSP430FR5969	64	2	DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	40	48 RGZ
MSP430FR59691	64	2	DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	I^2C	40	48 RGZ
MSP430FR5968	48	2	DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	40	48 RGZ
MSP430FR5967	32	1	DCO **HFXT** **LFXT**	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	40	48 RGZ
MSP430FR5949	64	2	DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	33	40 RHA
				12 ext, 2 int ch.								31	38 DA
MSP430FR5948	48	2	DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	33	40 RHA
				12 ext, 2 int ch.								31	38 DA
MSP430FR5947	32	1	DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	33	40 RHA
				12 ext, 2 int ch.								31	38 DA
MSP430FR59471	32	1	DCO **LFXT**	14 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	I^2C	33	40 RHA
MSP430FR5959	64	2	DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	33	40 RHA
				12 ext, 2 int ch.								31	38 DA
MSP430FR5958	48	2	DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	33	40 RHA
				12 ext, 2 int ch.								31	38 DA
MSP430FR5957	32	1	DCO **HFXT**	14 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2(8)	7	2	1	yes	UART	33	40 RHA
				12 ext, 2 int ch.								31	38 DA

(1) For the most current device, package, and ordering information for all available devices, see the *Package Option Addendum* in 9, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(5) eUSCI_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
(6) eUSCI_B supports I^2C with multiple slave addresses, and SPI.
(7) Timers TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
(8) Timers TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any).

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3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing and measurement microcontrollers One platform. One ecosystem. Endless possibilities.

Products for MSP430 ultrasonic and performance sensing microcontrollers Ultra-low-power single-chip MCUs with integrated sensing peripherals

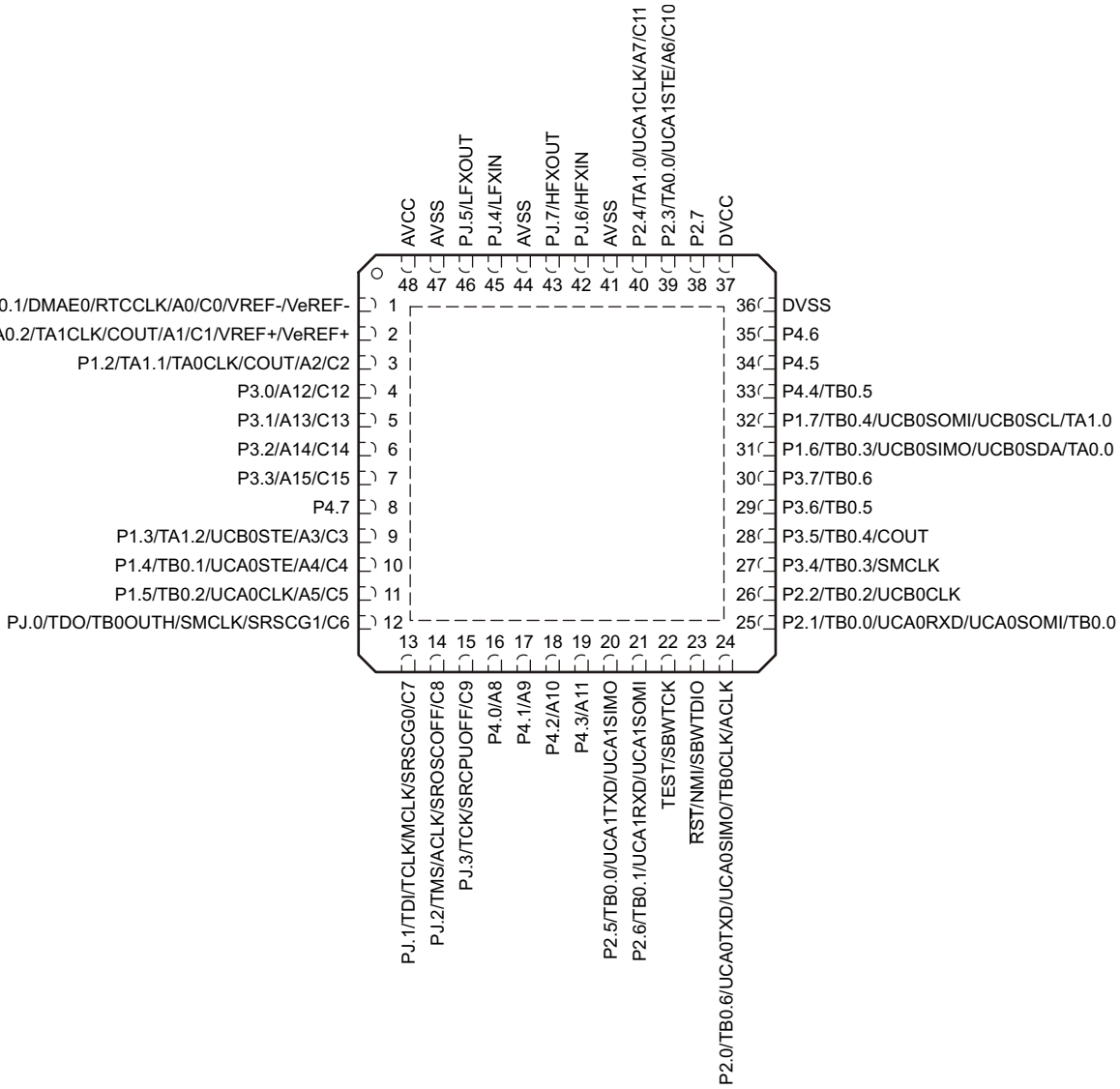
Companion Products for MSP430FR5969 Review products that are frequently purchased or used with this product.

Reference Designs for MSP430FR5969 The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the 48-pin RGZ package for the MSP430FR596x and MSP430FR596x1 MCUs.



NOTE: TI recommends connecting the QFN package pad to V_{SS}.
NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX
NOTE: On devices with I^2C BSL: P1.6: BSLSDA; P1.7: BSLSCL

Figure 4-1. 48-Pin RGZ Package (Top View) – MSP430FR596x and MSP430FR596x1

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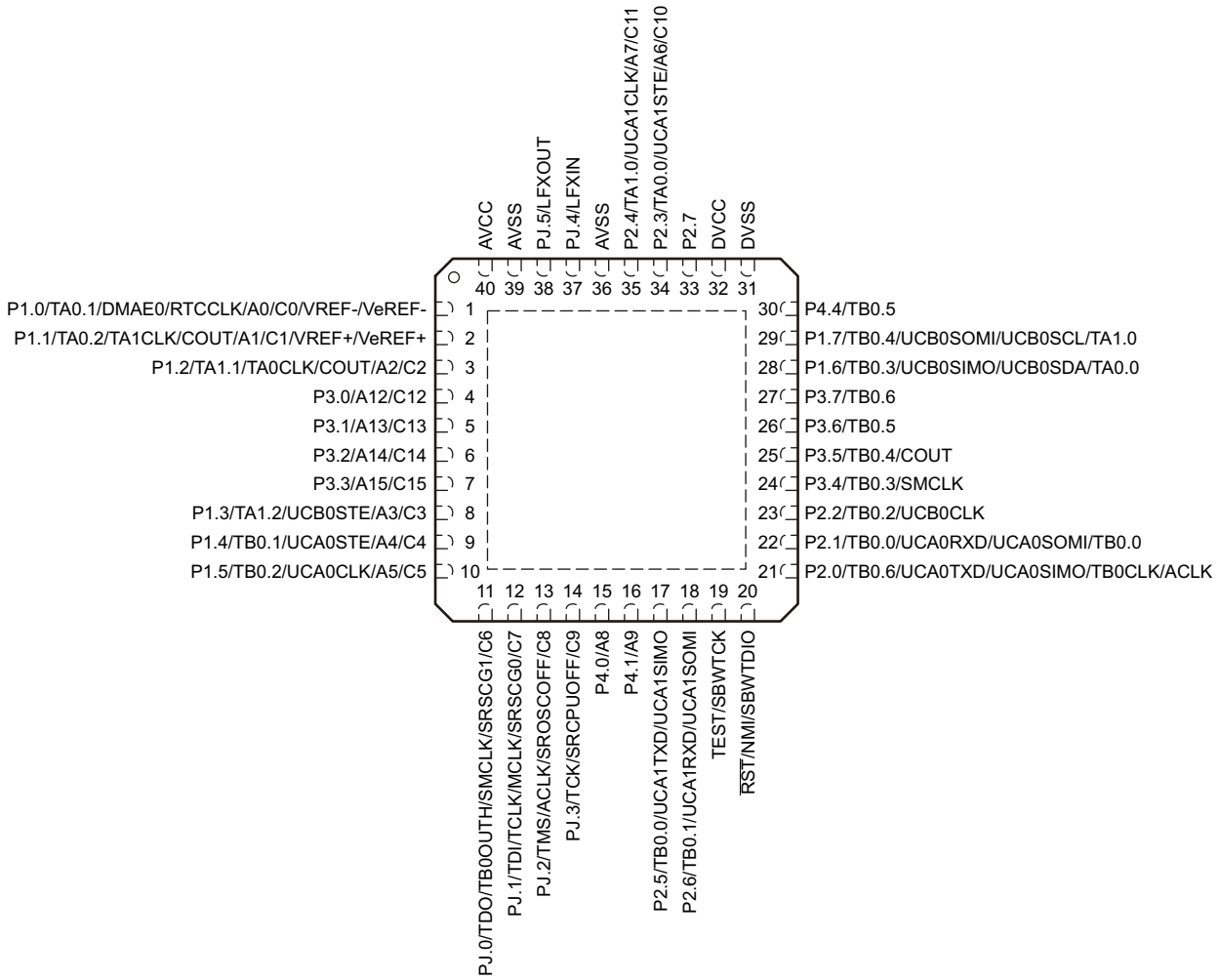
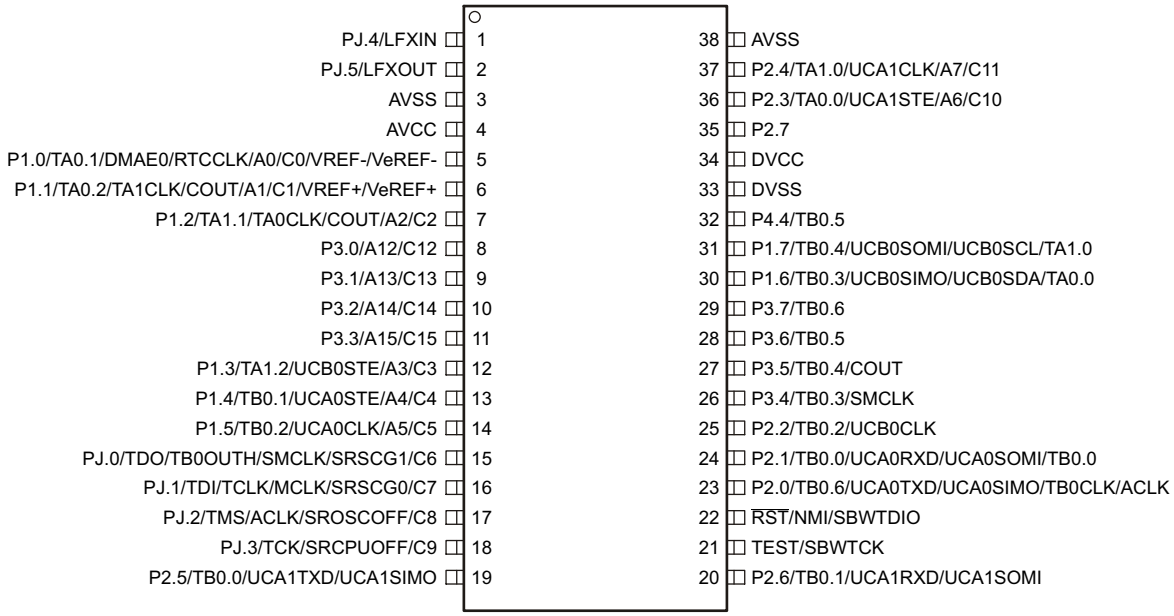
Figure 4-2 shows the 40-pin RHA package for the MSP430FR594x and MSP430FR594x1 MCUs (LFXT only).



NOTE: TI recommends connecting the QFN package pad to V_{SS}.
NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX
NOTE: On devices with I^2C BSL: P1.6: BSLSDA; P1.7: BSLSCL

Figure 4-2. 40-Pin RHA Package (Top View) – MSP430FR594x and MSP430FR594x1

Figure 4-3 shows the 38-pin DA package for the MSP430FR594x MCUs (LFXT only).



NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX

Figure 4-3. 38-Pin DA Package (Top View) – MSP430FR594x

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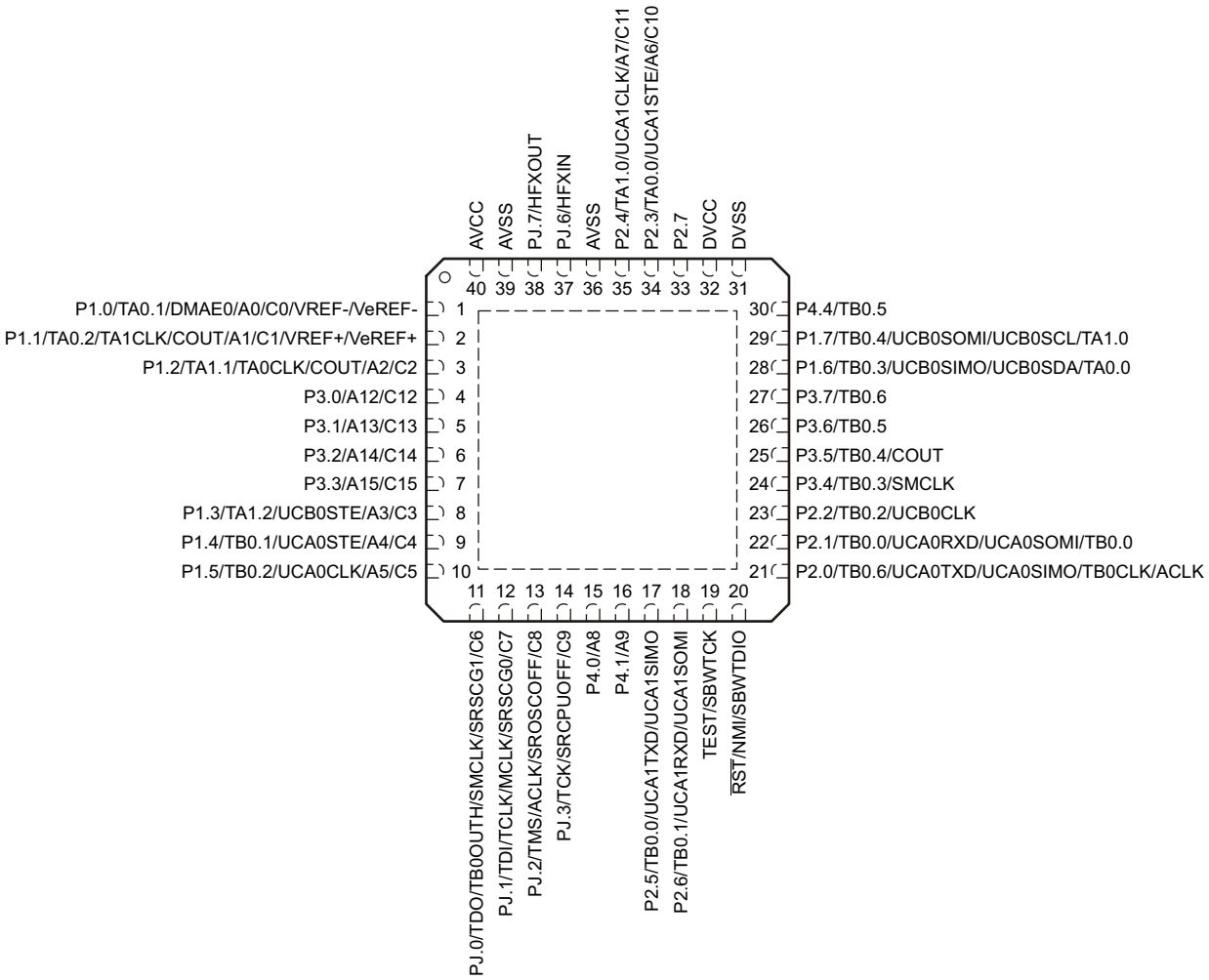
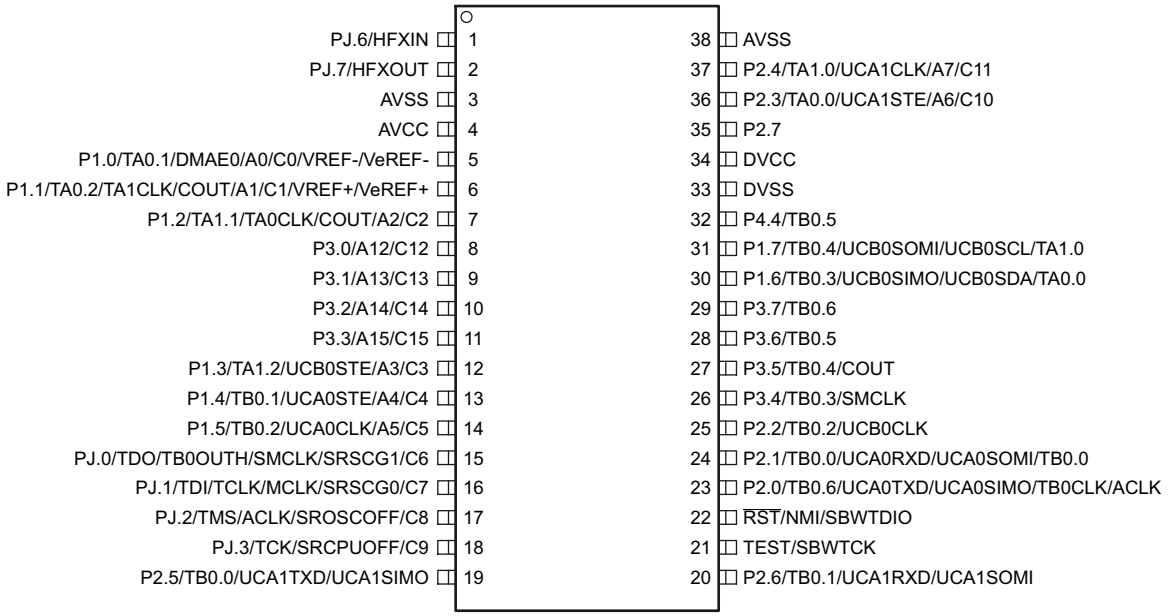
Figure 4-4 shows the 40-pin RHA package for the MSP430FR595x MCUs (HFXT only).



NOTE: TI recommends connecting the QFN package pad to V_{SS}.
NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX

Figure 4-4. 40-Pin RHA Package (Top View) – MSP430FR595x

Figure 4-5 shows the 38-pin DA package for the MSP430FR595x MCUs (HFXT only).



NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX

Figure 4-5. 38-Pin DA Package (Top View) – MSP430FR595x

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4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

TERMINAL				I/O (1)	DESCRIPTION
NAME	NO. (2)				
	RGZ	RHA	DA		
P1.0/TA0.1/DMAE0/ RTCCLK/A0/C0/VREF-/ VeREF-	1	1	5	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA0 CCR1 capture: CCI1A input, compare: Out1 External DMA trigger RTC clock calibration output (not available on MSP430FR5x5x devices) Analog input A0 for ADC Comparator input C0 Output of negative reference voltage Input for an external negative reference voltage to the ADC
P1.1/TA0.2/TA1CLK/ COUT/A1/C1/VREF+/ VeREF+	2	2	6	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA0 CCR2 capture: CCI2A input, compare: Out2 TA1 input clock Comparator output Analog input A1 for ADC Comparator input C1 Output of positive reference voltage Input for an external positive reference voltage to the ADC
P1.2/TA1.1/TA0CLK/ COUT/A2/C2	3	3	7	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA1 CCR1 capture: CCI1A input, compare: Out1 TA0 input clock Comparator output Analog input A2 for ADC Comparator input C2
P3.0/A12/C12	4	4	8	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A12 for ADC Comparator input C12
P3.1/A13/C13	5	5	9	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A13 for ADC Comparator input C13
P3.2/A14/C14	6	6	10	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A14 for ADC Comparator input C14
P3.3/A15/C15	7	7	11	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A15 for ADC Comparator input C15
P4.7	8	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
P1.3/TA1.2/UCB0STE/ A3/C3	9	8	12	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA1 CCR2 capture: CCI2A input, compare: Out2 Slave transmit enable – eUSCI_B0 SPI mode Analog input A3 for ADC Comparator input C3

(1) I = input, O = output
(2) N/A = not available

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O (1)	DESCRIPTION
NAME	NO. (2)				
	RGZ	RHA	DA		
P1.4/TB0.1/UCA0STE/ A4/C4	10	9	13	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR1 capture: CCI1A input, compare: Out1 Slave transmit enable – eUSCI_A0 SPI mode Analog input A4 for ADC Comparator input C4
P1.5/TB0.2/UCA0CLK/ A5/C5	11	10	14	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR2 capture: CCI2A input, compare: Out2 Clock signal input – eUSCI_A0 SPI slave mode, Clock signal output – eUSCI_A0 SPI master mode Analog input A5 for ADC Comparator input C5
PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1/C6	12	11	15	I/O	General-purpose digital I/O Test data output port Switch all PWM outputs high impedance input – TB0 SMCLK output Low-Power Debug: CPU Status Register Bit SCG1 Comparator input C6
PJ.1/TDI/TCLK/MCLK/ SRSCG0/C7	13	12	16	I/O	General-purpose digital I/O Test data input or test clock input MCLK output Low-Power Debug: CPU Status Register Bit SCG0 Comparator input C7
PJ.2/TMS/ACLK/ SROSCOFF/C8	14	13	17	I/O	General-purpose digital I/O Test mode select ACLK output Low-Power Debug: CPU Status Register Bit OSCOFF Comparator input C8
PJ.3/TCK/ SRCPUOFF/C9	15	14	18	I/O	General-purpose digital I/O Test clock Low-Power Debug: CPU Status Register Bit CPUOFF Comparator input C9
P4.0/A8	16	15	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A8 for ADC
P4.1/A9	17	16	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A9 for ADC
P4.2/A10	18	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A10 for ADC
P4.3/A11	19	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 Analog input A11 for ADC
P2.5/TB0.0/UCA1TXD/ UCA1SIMO	20	17	19	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR0 capture: CCI0B input, compare: Out0 Transmit data – eUSCI_A1 UART mode Slave in, master out – eUSCI_A1 SPI mode

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O (1)	DESCRIPTION
NAME	NO. (2)				
	RGZ	RHA	DA		
P2.6/TB0.1/UCA1RXD/ UCA1SOMI	21	18	20	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR1 compare: Out1 Receive data – eUSCI_A1 UART mode Slave out, master in – eUSCI_A1 SPI mode
TEST/SBWTCK	22	19	21	I	Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock
$\overline{\text{RST}}$/NMI/SBWTDIO	23	20	22	I/O	Reset input active low Nonmaskable interrupt input Spy-Bi-Wire data input/output
P2.0/TB0.6/UCA0TXD/ UCA0SIMO/TB0CLK/ ACLK	24	21	23	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR6 capture: CCI6B input, compare: Out6 Transmit data – eUSCI_A0 UART mode BSL Transmit (UART BSL) Slave in, master out – eUSCI_A0 SPI mode TB0 clock input ACLK output
P2.1/TB0.0/UCA0RXD/ UCA0SOMI/TB0.0	25	22	24	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR0 capture: CCI0A input, compare: Out0 Receive data – eUSCI_A0 UART mode BSL receive (UART BSL) Slave out, master in – eUSCI_A0 SPI mode TB0 CCR0 capture: CCI0A input, compare: Out0
P2.2/TB0.2/UCB0CLK	26	23	25	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR2 compare: Out2 Clock signal input – eUSCI_B0 SPI slave mode Clock signal output – eUSCI_B0 SPI master mode
P3.4/TB0.3/SMCLK	27	24	26	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR3 capture: CCI3A input, compare: Out3 SMCLK output
P3.5/TB0.4/COUT	28	25	27	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR4 capture: CCI4A input, compare: Out4 Comparator output
P3.6/TB0.5	29	26	28	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR5 capture: CCI5A input, compare: Out5
P3.7/TB0.6	30	27	29	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR6 capture: CCI6A input, compare: Out6
P1.6/TB0.3/UCB0SIMO/ UCB0SDA/TA0.0	31	28	30	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR3 capture: CCI3B input, compare: Out3 Slave in, master out – eUSCI_B0 SPI mode I^2C data – eUSCI_B0 I^2C mode BSL Data (I^2C BSL) TA0 CCR0 capture: CCI0A input, compare: Out0

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O (1)	DESCRIPTION
NAME	NO. (2)				
	RGZ	RHA	DA		
P1.7/TB0.4/UCB0SOMI/ UCB0SCL/TA1.0	32	29	31	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0 CCR4 capture: CCI4B input, compare: Out4 Slave out, master in – eUSCI_B0 SPI mode I^2C clock – eUSCI_B0 I^2C mode BSL clock (I^2C BSL) TA1 CCR0 capture: CCI0A input, compare: Out0
P4.4/TB0.5	33	30	32	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TB0CCR5 capture: CCI5B input, compare: Out5
P4.5	34	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
P4.6	35	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
DVSS	36	31	33		Digital ground supply
DVCC	37	32	34		Digital power supply
P2.7	38	33	35	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
P2.3/TA0.0/UCA1STE/ A6/C10	39	34	36	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA0 CCR0 capture: CCI0B input, compare: Out0 Slave transmit enable – eUSCI_A1 SPI mode Analog input A6 for ADC Comparator input C10
P2.4/TA1.0/UCA1CLK/ A7/C11	40	35	37	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5 TA1 CCR0 capture: CCI0B input, compare: Out0 Clock signal input – eUSCI_A1 SPI slave mode Clock signal output – eUSCI_A1 SPI master mode Analog input A7 for ADC Comparator input C11
AVSS	41	36	38		Analog ground supply
PJ.6/HFXIN	42	37	1	I/O	General-purpose digital I/O Input for high-frequency crystal oscillator HFXT (in RHA and DA packages: MSP430FR595x devices only)
PJ.7/HFXOUT	43	38	2	I/O	General-purpose digital I/O Output for high-frequency crystal oscillator HFXT (in RHA and DA packages: MSP430FR595x devices only)
AVSS	44	N/A	N/A		Analog ground supply
PJ.4/LFXIN	45	37	1	I/O	General-purpose digital I/O Input for low-frequency crystal oscillator LFXT (in RHA and DA packages: MSP430FR594x devices only)
PJ.5/LFXOUT	46	38	2	I/O	General-purpose digital I/O Output of low-frequency crystal oscillator LFXT (in RHA and DA packages: MSP430FR594x devices only)
AVSS	47	39	3		Analog ground supply
AVCC	48	40	4		Analog power supply
QFN Pad	Pad	Pad	N/A		QFN package exposed thermal pad. TI recommends connection to V_{SS}.

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4.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see 6.11.

4.4 Connection of Unused Pins

Table 4-2 lists the correct termination of all unused pins.

Table 4-2. Connection of Unused Pins(1)

PIN	POTENTIAL	COMMENT
AVCC	DV_{CC}	
AVSS	DV_{SS}	
Px.0 to Px.7	Open	Set to port function, output direction (PxDIR.n = 1)
$\overline{RST}$/NMI	DV_{CC} or V_{CC}	47-kΩ pullup or internal pullup selected with 2.2-nF (10-nF(2)) pulldown
PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK	Open	The JTAG pins are shared with general-purpose I/O function (PJ.x). If not used as JTAG pins, these pins should be switched to port function, output direction. When used as JTAG pins, these pins should remain open.
TEST	Open	This pin always has an internal pulldown enabled.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 2.2 nF when using devices in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers. If JTAG or Spy-Bi-Wire access is not needed, up to a 10-nF pulldown capacitor may be used.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3	4.1	V
Voltage difference between DVCC and AVCC pins(2)		±0.3	V
Voltage applied to any pin (3)	–0.3	V_{CC} + 0.3 V (4.1 Max)	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg}(4)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
(3) All voltages referenced to V_{SS}.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical data are based on V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins(1) (2) (3)		1.8(4)		3.6	V
V_{SS}	Supply voltage applied at all DVSS and AVSS pins			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{DVCC}	Capacitor value at DVCC(5)		$1_{-20\%}$			µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(6)	No FRAM wait states (NWAITSx = 0)	0		8(7)	MHz
		With FRAM wait states (NWAITSx = 1)(8)	0		16(9)	
f_{ACLK}	Maximum ACLK frequency				50	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(9)	MHz

(1) TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in Absolute Maximum Ratings. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
(2) See 表 5-1 for additional important information.
(3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(4) The minimum supply voltage is defined by the supervisor SVS levels. See 表 5-2 for the values.
(5) Connect a low-ESR capacitor with at least the value specified and a maximum tolerance of 20% as close as possible to the DVCC pin.
(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) DCO settings and HF crystals with a typical value less or equal the specified MAX value are permitted.
(8) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
(9) DCO settings and HF crystals with a typical value less or equal the specified MAX value are permitted. If a clock sources with a larger typical value is used, the clock must be divided in the clock system.

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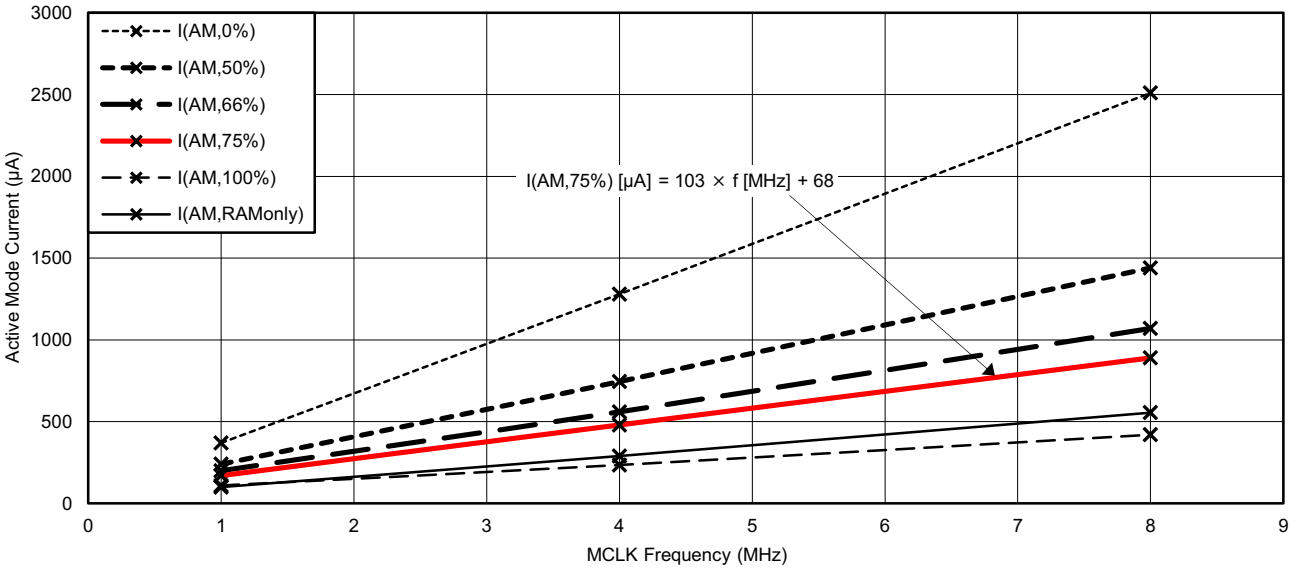
5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	EXECUTION MEMORY	V_{CC}	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)										UNIT
			1 MHz 0 wait states (NWAITSx = 0)		4 MHz 0 wait states (NWAITSx = 0)		8 MHz 0 wait states (NWAITSx = 0)		12 MHz 1 wait states (NWAITSx = 1)		16 MHz 1 wait states (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM_UNI}$ (Unified memory)(3)	FRAM	3.0 V	210		640		1220		1475		1845		µA
$I_{AM, FRAM (0\%)}$(4) (5)	FRAM 0% cache hit ratio	3.0 V	370		1280		2510		2080		2650		µA
$I_{AM, FRAM (50\%)}$(4) (5)	FRAM 50% cache hit ratio	3.0 V	240		745		1440		1575		1990		µA
$I_{AM, FRAM (66\%)}$(4) (5)	FRAM 66% cache hit ratio	3.0 V	200		560		1070		1300		1620		µA
$I_{AM, FRAM (75\%)}$(4) (5)	FRAM 75% cache hit ratio	3.0 V	170	255	480		890	1085	1155	1310	1420	1620	µA
$I_{AM, FRAM (100\%)}$(4) (5)	FRAM 100% cache hit ratio	3.0 V	110		235		420		640		730		µA
$I_{AM, RAM}$ (6)	RAM	3.0 V	130		320		585		890		1070		µA
$I_{AM, RAM only}$ (7) (5)	RAM	3.0 V	100	180	290		555		860		1040	1300	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, f_{DCO}= 24 MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO}/2$.
At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ($f_{MCLK,eff}$) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.
The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff} = f_{MCLK}$ / [wait states × (1 – cache hit ratio) + 1]
For example, with 1 wait state and 75% cache hit ratio, $f_{MCKL,eff} = f_{MCLK}$ / [1 × (1 – 0.75) + 1] = f_{MCLK} / 1.25.
(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.
(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.
(5) See Figure 5-1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data from Section 5.4.
(6) Program and data reside entirely in RAM. All execution is from RAM.
(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

5.5 Typical Characteristics – Active Mode Supply Currents



NOTE: I(AM, cache hit ratio): Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

NOTE: I(AM, RAMonly): Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

Figure 5-1. Typical Active Mode Supply Currents vs MCLK frequency, No Wait States

5.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	FREQUENCY (f_{SMCLK})										UNIT
		1 MHz		4 MHz		8 MHz		12 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	2.2 V	70		95		150		250		215		µA
	3.0 V	80	115	105		160		260		225	260	
I_{LPM1}	2.2 V	35		60		115		215		180		µA
	3.0 V	35	60	60		115		215		180	205	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} at specified frequency, except for 12 MHz. For 12 MHz, f_{DCO} = 24 MHz and f_{SMCLK} = f_{DCO} / 2.

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5.7 Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM2,XT12}$	Low-power mode 2, 12-pF crystal (2) (3) (4)	2.2 V	0.5		0.9		2.2		6.1		µA
		3.0 V	0.5		0.9	1.8	2.2		6.1	17	
$I_{LPM2,XT3.7}$	Low-power mode 2, 3.7-pF cyrstal (2) (5) (4)	2.2 V	0.5		0.9		2.2		6.0		µA
		3.0 V	0.5		0.9		2.2		6.0		
$I_{LPM2,VLO}$	Low-power mode 2, VLO, includes SVS (6)	2.2 V	0.3		0.7		1.9		5.8		µA
		3.0 V	0.3		0.7	1.6	1.9		5.8	16.7	
$I_{LPM3,XT12}$	Low-power mode 3, 12-pF crystal, excludes SVS (2) (3) (7)	2.2 V	0.5		0.6		0.9		1.85		µA
		3.0 V	0.5		0.6	0.9	0.9		1.85	4.9	
$I_{LPM3,XT3.7}$	Low-power mode 3, 3.7-pF cyrstal, excludes SVS (2) (5) (8) (also see Figure 5-2)	2.2 V	0.4		0.5		0.8		1.7		µA
		3.0 V	0.4		0.5		0.8		1.7		
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS (9)	2.2 V	0.3		0.4		0.7		1.6		µA
		3.0 V	0.3		0.4	0.7	0.7		1.6	4.7	
$I_{LPM4,SVS}$	Low-power mode 4, includes SVS (10) (also see Figure 5-3)	2.2 V	0.4		0.5		0.8		1.7		µA
		3.0 V	0.4		0.5	0.8	0.8		1.7	4.8	
I_{LPM4}	Low-power mode 4, excludes SVS (11)	2.2 V	0.2		0.3		0.6		1.5		µA
		3.0 V	0.2		0.3	0.6	0.6		1.5	4.6	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(4) Low-power mode 2, crystal oscillator test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 are included. Current for brownout and SVS are included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Characterized with a SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(6) Low-power mode 2, VLO test conditions:
Current for watchdog timer clocked by ACLK is included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS are included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(7) Low-power mode 3, 12-pF crystal, excludes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 are included. Current for brownout is included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(8) Low-power mode 3, 3.7-pF crystal, excludes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 are included. Current for brownout is included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(9) Low-power mode 3, VLO, excludes SVS test conditions:
Current for watchdog timer clocked by ACLK is included. RTC disabled (RTCHOLD = 1). Current for brownout is included. SVS is disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(10) Low-power mode 4, includes SVS test conditions:
Current for brownout and SVS are included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(11) Low-power mode 4, excludes SVS test conditions:
Current for brownout is included. SVS is disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz

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Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) [1]

PARAMETER		V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{IDLE,GroupA}$	Additional idle current if one or more modules from Group A (see 表 6-3) are activated in LPM3 or LPM4.	3.0V			0.02				0.33	1.3	µA
$I_{IDLE,GroupB}$	Additional idle current if one or more modules from Group B (see 表 6-3) are activated in LPM3 or LPM4	3.0V			0.015				0.25	1.0	µA

5.8 Low-Power Mode (LPM3.5, LPM4.5) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) [1]

PARAMETER		V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5,XT12}$	Low-power mode 3.5, 12-pF crystal, includes SVS [2][3][4]	2.2 V	0.4		0.45		0.5		0.7		µA
		3.0 V	0.4		0.45	0.7	0.5		0.7	1.2	
$I_{LPM3.5,XT3.7}$	Low-power mode 3.5, 3.7-pF cyrstal, excludes SVS [2][5][6] (also see Figure 5-4)	2.2 V	0.2		0.25		0.3		0.45		µA
		3.0 V	0.2		0.25		0.3		0.5		
$I_{LPM4.5,SVS}$	Low-power mode 4.5, includes SVS [7] (also see Figure 5-5)	2.2 V	0.2		0.2		0.2		0.3		µA
		3.0 V	0.2		0.2	0.4	0.2		0.3	0.55	
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS [8] (also see Figure 5-5)	2.2 V	0.02		0.02		0.02		0.08		µA
		3.0 V	0.02		0.02		0.02		0.08	0.35	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(4) Low-power mode 3.5, 12-pF crystal, includes SVS test conditions:
Current for RTC clocked by XT1 is included. Current for brownout and SVS are included (SVSHE = 1). Core regulator is disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Characterized with a SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(6) Low-power mode 3.5, 3.7-pF crystal, excludes SVS test conditions:
Current for RTC clocked by XT1 is included. Current for brownout is included. SVS is disabled (SVSHE = 0). Core regulator isdisabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(7) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS are included (SVSHE = 1). Core regulator is disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(8) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout is included. SVS is disabled (SVSHE = 0). Core regulator is disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz

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5.9 Typical Characteristics, Low-Power Mode Supply Currents

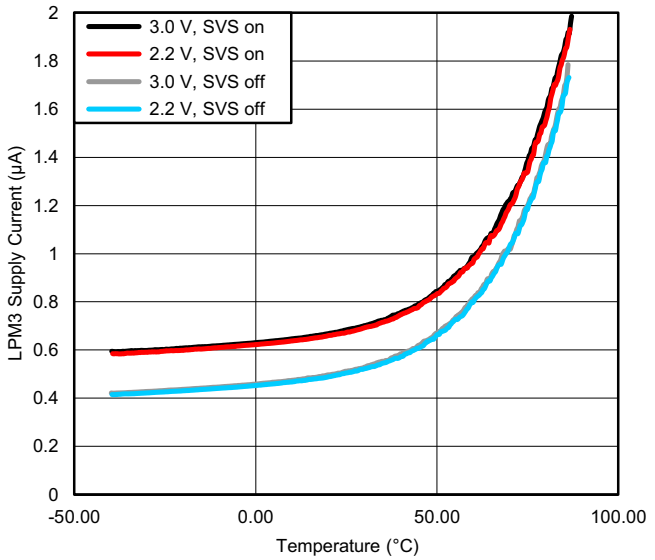

Figure 5-2. LPM3,XT3.7 Supply Current vs Temperature

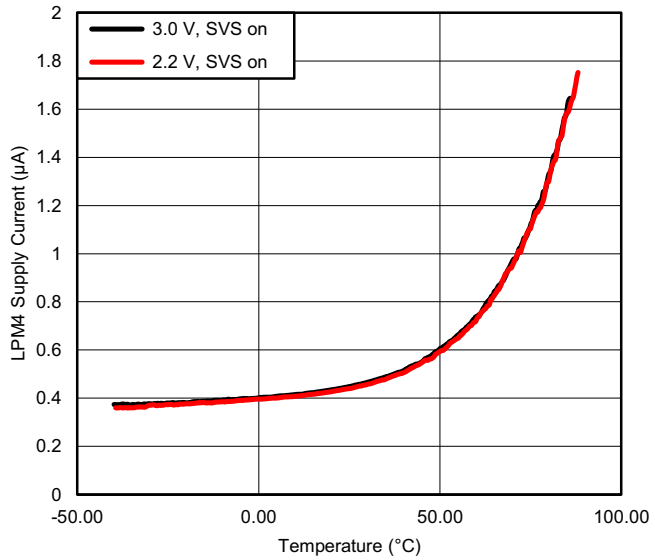

Figure 5-3. LPM4,SVS Supply Current vs Temperature

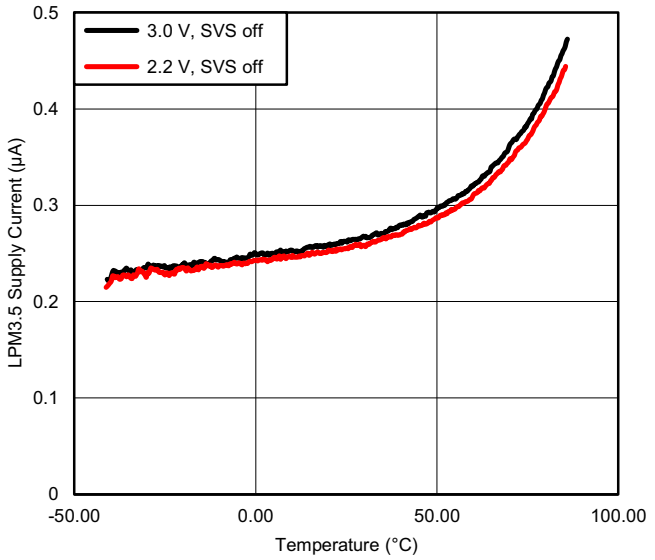

Figure 5-4. LPM3.5,XT3.7 Supply Current vs Temperature

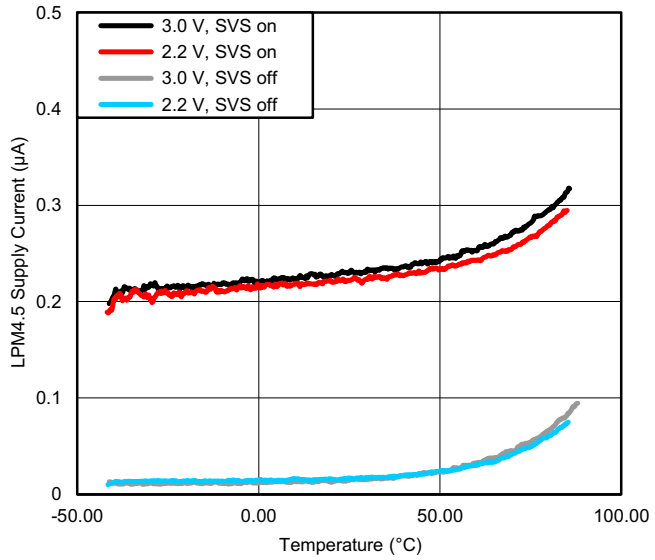

Figure 5-5. LPM4.5 Supply Current vs Temperature

5.10 Typical Characteristics, Current Consumption per Module(1)

MODULE	TEST CONDITIONS	REFERENCE CLOCK	MIN	TYP	MAX	UNIT
Timer_A		Module input clock		3		µA/MHz
Timer_B		Module input clock		5		µA/MHz
eUSCI_A	UART mode	Module input clock		5.5		µA/MHz
eUSCI_A	SPI mode	Module input clock		3.5		µA/MHz
eUSCI_B	SPI mode	Module input clock		3.5		µA/MHz
eUSCI_B	I^2C mode, 100 kbaud	Module input clock		3.5		µA/MHz
RTC_B		32 kHz		100		nA
MPY	Only from start to end of operation	MCLK		25		µA/MHz
AES	Only from start to end of operation	MCLK		21		µA/MHz
CRC	Only from start to end of operation	MCLK		2.5		µA/MHz

(1) For other module currents not listed here, see the module specific parameter sections.

5.11 Thermal Resistance Characteristics

THERMAL METRIC		PACKAGE	VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	QFN-48 (RGZ)	30.6	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)		17.2	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		7.2	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		7.2	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.2	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(4)		1.2	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	QFN-40 (RHA)	30.1	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)		18.7	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		6.4	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		6.3	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.3	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(4)		1.5	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	TSSOP-38 (DA)	65.5	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)		12.5	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		32.3	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		31.8	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.3	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(4)		N/A	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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5.12 Timing and Switching Characteristics

5.12.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in Absolute Maximum Ratings. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

At power up, the device does not start executing code before the supply voltage reaches V_{SVSH+} if the supply rises monotonically to this level.

表 5-1 lists the reset power ramp requirements.

表 5-1. Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCC_BOR-}	Brownout power-down level(1)(2)	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s(3)	0.7		1.66	V
		$\lvert dDV_{CC}/d_t \rvert > 300$ V/s(3)	0			V
V_{VCC_BOR+}	Brownout power-up level(2)	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s(4)	0.79		1.68	V

(1) In case of a supply voltage brownout, the device supply voltages need to ramp down to the specified brownout power-down level V_{VCC_BOR-} before the voltage is ramped up again to ensure a reliable device start-up and performance according to the data sheet including the correct operation of the on-chip SVS module.
(2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/µs). Following the data sheet recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
(3) The brownout levels are measured with a slowly changing supply. With faster slopes the MIN level required to reset the device properly can decrease to 0 V. Use the graph in 図 5-6 to estimate the V_{VCC_BOR-} level based on the down slope of the supply voltage. After removing VCC the down slope can be estimated based on the current consumption and the capacitance on DVCC: dV/dt = I/C with dV/dt: slope, I: current, C: capacitance.
(4) The brownout levels are measured with a slowly changing supply.

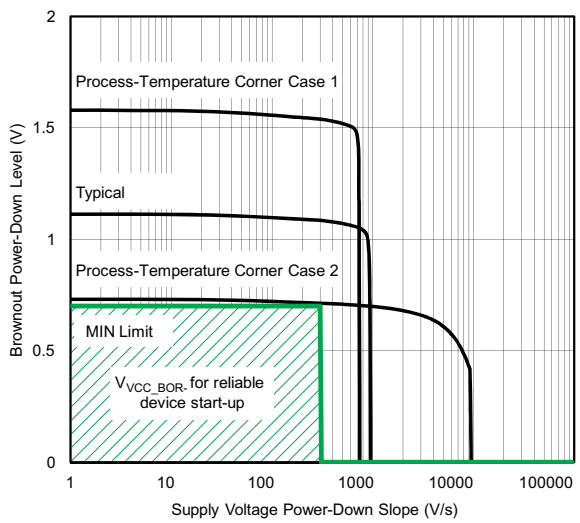

図 5-6. Brownout Power-Down Level vs Supply Voltage Down Slope

表 5-2 lists the characteristics of the SVS.

表 5-2. SVS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SVSH,LPM}$	SVS_H current consumption, low power modes			170	300	nA
V_{SVSH-}	SVS_H power-down level(1)		1.75	1.80	1.85	V
V_{SVSH+}	SVS_H power-up level(1)		1.77	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis		40		120	mV
$t_{PD,SVSH,\ AM}$	SVS_H propagation delay, active mode	dV_{Vcc}/dt = –10 mV/µs			10	µs

(1) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

5.12.2 Reset Timing

Table 5-11 lists the required reset input timing.

表 5-3. Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC}	MIN	MAX	UNIT
$t_{(RST)}$	External reset pulse duration on $\overline{RST}$(1)	2.2 V, 3.0 V	2		µs

(1) Not applicable if $\overline{RST}$/NMI pin configured as NMI.

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5.12.3 Clock Specifications

Table 5-4 lists the characteristics of the LFXT.

Table 5-4. Low-Frequency Crystal Oscillator, LFXT(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC.LFXT}$	Current consumption	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 3.7 pF, ESR ≈ 44 kΩ	3.0 V		180		nA
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {1}, T_A = 25°C, $C_{L,eff}$ = 6 pF, ESR ≈ 40 kΩ			185		
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {2}, T_A = 25°C, $C_{L,eff}$ = 9 pF, ESR ≈ 40 kΩ			225		
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF, ESR ≈ 40 kΩ			330		
f_{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0			32768		Hz
DC_{LFXT}	LFXT oscillator duty cycle	Measured at ACLK, f_{LFXT} = 32768 Hz		30%		70%	
$f_{LFXT,SW}$	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1(2) (3)		10.5	32.768	50	kHz
$DC_{LFXT, SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%		70%	
OA_{LFXT}	Oscillation allowance for LF crystals(4)	LFXTBYPASS = 0, LFXTDRIVE = {1}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF			300		
C_{LFXIN}	Integrated load capacitance at LFXIN terminal(5) (6)				2		pF
C_{LFXOUT}	Integrated load capacitance at LFXOUT terminal(5) (6)				2		pF

(1) To improve EMI on the LFXT oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
- Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF.
- For LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {3}, 9 pF ≤ $C_{L,eff}$ ≤ 12.5 pF

(5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} are the total capacitance at the LFXIN and LFXOUT terminals, respectively.

(6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

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Table 5-4. Low-Frequency Crystal Oscillator, LFXT(1) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{START,LFXT}$	Start-up time(7)	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 3.7 pF	3.0 V		800		ms
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF	3.0 V		1000		
$f_{Fault,LFXT}$	Oscillator fault frequency(8) (9)			0		3500	Hz

(7) Includes start-up counter of 1024 clock cycles.
(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the characteristics of the HFXT.

Table 5-5. High-Frequency Crystal Oscillator, HFXT(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.HFXT}$	HFXT oscillator crystal current HF mode at typical ESR	f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1(2) T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}	3.0 V		75		µA
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}			120		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}			190		
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T_A = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, C_{shunt}			250		
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 1(2)(3)		4		8	MHz
		HFXTBYPASS = 0, HFFREQ = 2(3)		8.01		16	
		HFXTBYPASS = 0, HFFREQ = 3(3)		16.01		24	
DC_{HFXT}	HFXT oscillator duty cycle	Measured at SMCLK, f_{HFXT} = 16 MHz		40%	50%	60%	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1, HFFREQ = 0(4)(3)		0.9		4	MHz
		HFXTBYPASS = 1, HFFREQ = 1(4)(3)		4.01		8	
		HFXTBYPASS = 1, HFFREQ = 2(4)(3)		8.01		16	
		HFXTBYPASS = 1, HFFREQ = 3(4)(3)		16.01		24	
$DC_{HFXT,\ SW}$	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1		40%		60%	

(1) To improve EMI on the HFXT oscillator, observe the following guidelines.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
- Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator HFXIN and HFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{HFXT,\ SW}$.

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Table 5-5. High-Frequency Crystal Oscillator, HFXT[1] (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{START,HFXT}$	Start-up time[5]	f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1, T_A = 25°C, $C_{L,eff}$ = 16 pF	3.0 V		1.6		ms
		f_{OSC} = 24 MHz , HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T_A = 25°C, $C_{L,eff}$ = 16 pF	3.0 V		0.6		
C_{HFXIN}	Integrated load capacitance at HFXIN terminal[6] [7]				2		pF
C_{HFXOUT}	Integrated load capacitance at HFXOUT terminal[6] [7]				2		pF
$f_{Fault,HFXT}$	Oscillator fault frequency[8] [9]			0		800	kHz

(5) Includes start-up counter of 1024 clock cycles.
(6) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} are the total capacitance at the HFXIN and HFXOUT terminals, respectively.
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX might set the flag. A static condition or stuck at fault condition set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-6 lists the characteristics of the DCO.

Table 5-6. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{DCO1}	DCO frequency range 1 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 0, DCORSEL = 1, DCOFSEL = 0			1	±3.5%	MHz
$f_{DCO2.7}$	DCO frequency range 2.7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 1			2.667	±3.5%	MHz
$f_{DCO3.5}$	DCO frequency range 3.5 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 2			3.5	±3.5%	MHz
f_{DCO4}	DCO frequency range 4 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 3			4	±3.5%	MHz
$f_{DCO5.3}$	DCO frequency range 5.3 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 4, DCORSEL = 1, DCOFSEL = 1			5.333	±3.5%	MHz
f_{DCO7}	DCO frequency range 7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 5, DCORSEL = 1, DCOFSEL = 2			7	±3.5%	MHz
f_{DCO8}	DCO frequency range 8 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 6, DCORSEL = 1, DCOFSEL = 3			8	±3.5%	MHz
f_{DCO16}	DCO frequency range 16 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 1, DCOFSEL = 4			16	±3.5%(1)	MHz
f_{DCO21}	DCO frequency range 21 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 5			21	±3.5%(1)	MHz
f_{DCO24}	DCO frequency range 24 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 6			24	±3.5%(1)	MHz
$f_{DCO,DC}$	Duty cycle	Measured at SMCLK, divide by 1, no external divide, all DCORSEL/DCOFSEL settings except DCORSEL = 1, DCOFSEL = 5 and DCORSEL = 1, DCOFSEL = 6		48%	50%	52%	
$t_{DCO,\ JITTER}$	DCO jitter	Based on f_{signal} = 10 kHz and DCO used for 12-bit SAR ADC sampling source. This achieves >74 dB SNR due to jitter (that is, it is limited by ADC performance).			2	3	ns
df_{DCO}/dT	DCO temperature drift(2)		3.0 V		0.01		%/ºC

(1) After a wakeup from LPM1, LPM2, LPM3, or LPM4, the DCO frequency f_{DCO} might exceed the specified frequency range for a few clock cycles by up to 5% before settling into the specified steady-state frequency range.
(2) Calculated using the box method: (MAX(–40ºC to 85ºC) – MIN(–40ºC to 85ºC)) / MIN(–40ºC to 85ºC) / (85ºC – (–40ºC))

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Table 5-7 lists the characteristics of the VLO.

Table 5-7. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VLO}	Current consumption			100		nA
f_{VLO}	VLO frequency	Measured at ACLK	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK (1)		0.2		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK (2)		0.7		%/V
$f_{VLO,DC}$	Duty cycle	Measured at ACLK	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40ºC to 85°C) – MIN(–40ºC to 85°C)) / MIN(–40ºC to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8 lists the characteristics of the MODOSC.

Table 5-8. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption	Enabled		25		µA
f_{MODOSC}	MODOSC frequency		4.0	4.8	5.4	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift (1)			0.08		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift (2)			1.4		%/V
DC_{MODOSC}	Duty cycle	Measured at SMCLK, divide by 1	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40ºC to 85°C) – MIN(–40ºC to 85°C)) / MIN(–40ºC to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.12.4 Wake-up Characteristics

Table 5-9 list the device wake-up times.

Table 5-9. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	(Additional) wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected for wakeup				6	10	µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		2.2 V, 3.0 V			400 + 1.5 / f_{DCO}	ns
$t_{WAKE-UP\ LPM1}$	Wake-up time from LPM1 to active mode (1)		2.2 V, 3.0 V		6		µs
$t_{WAKE-UP\ LPM2}$	Wake-up time from LPM2 to active mode (1)		2.2 V, 3.0 V		6		µs
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (1)		2.2 V, 3.0 V		7	10	µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode (1)		2.2 V, 3.0 V		7	10	µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		2.2 V, 3.0 V		250	350	µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	2.2 V, 3.0 V		250	350	µs
		SVSHE = 0	2.2 V, 3.0 V		1	1.5	ms
$t_{WAKE-UP-RST}$	Wake-up time from a $\overline{RST}$ pin triggered reset to active mode (2)		2.2 V, 3.0 V		250	350	µs
$t_{WAKE-UP-BOR}$	Wake-up time from power-up to active mode (2)		2.2 V, 3.0 V		1	1.5	ms

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge. MCLK is sourced by the DCO and the MCLK divider is set to divide-by-1 (DIVMx = 000b, $f_{MCLK} = f_{DCO}$). This time includes the activation of the FRAM during wakeup.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

Table 5-10 list the typical wake-up charges.

Table 5-10. Typical Wake-up Charge (1)

also see Figure 5-7 and Figure 5-8

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Q_{WAKE-UP\ FRAM}$	Charge used for activating the FRAM in AM or during wakeup from LPM0 if previously disabled by the FRAM controller.			15.1		nAs
$Q_{WAKE-UP\ LPM0}$	Charge used for wakeup from LPM0 to active mode (with FRAM active)			4.4		nAs
$Q_{WAKE-UP\ LPM1}$	Charge used for wakeup from LPM1 to active mode (with FRAM active)			15.1		nAs
$Q_{WAKE-UP\ LPM2}$	Charge used for wakeup from LPM2 to active mode (with FRAM active)			15.3		nAs
$Q_{WAKE-UP\ LPM3}$	Charge used for wakeup from LPM3 to active mode (with FRAM active)			16.5		nAs
$Q_{WAKE-UP\ LPM4}$	Charge used for wakeup from LPM4 to active mode (with FRAM active)			16.5		nAs
$Q_{WAKE-UP\ LPM3.5}$	Charge used for wakeup from LPM3.5 to active mode (2)			76		nAs
$Q_{WAKE-UP\ LPM4.5}$	Charge used for wakeup from LPM4.5 to active mode (2)	SVSHE = 1		77		nAs
		SVSHE = 0		77.5		nAs
$Q_{WAKE-UP-RESET}$	Charge used for reset from $\overline{RST}$ or BOR event to active mode (2)			75		nAs

(1) Charge used during the wake-up time from a given low-power mode to active mode. This does not include the energy required in active mode (for example, for an interrupt service routine).
(2) Charge required until start of user code. This does not include the energy required to reconfigure the device.

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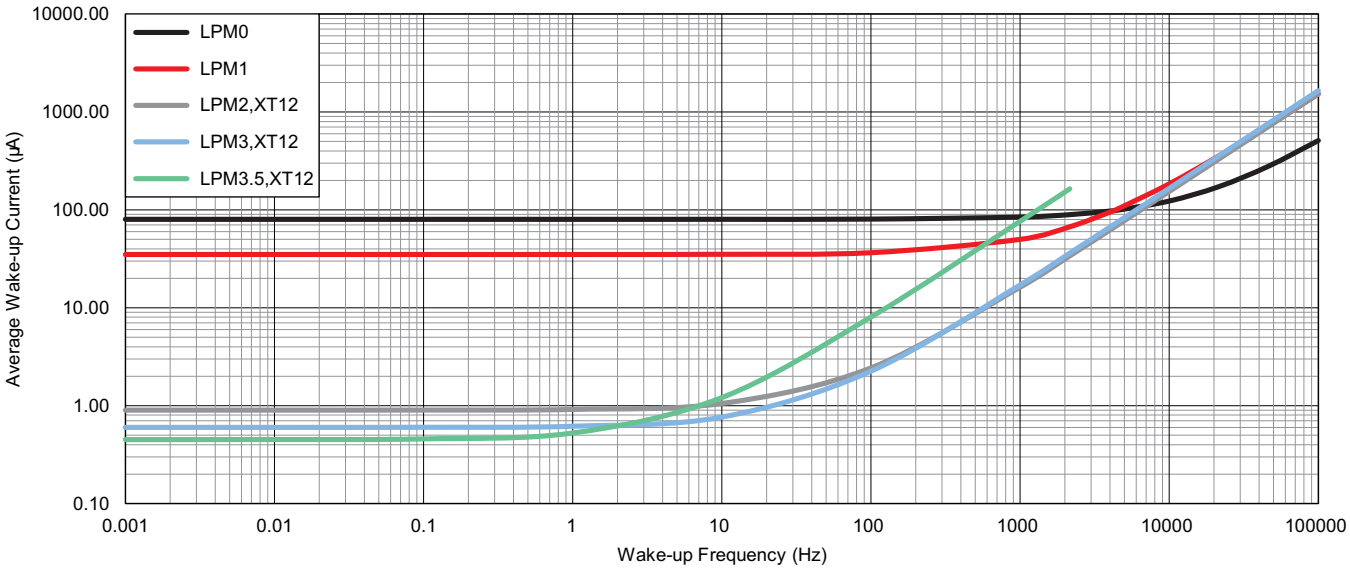
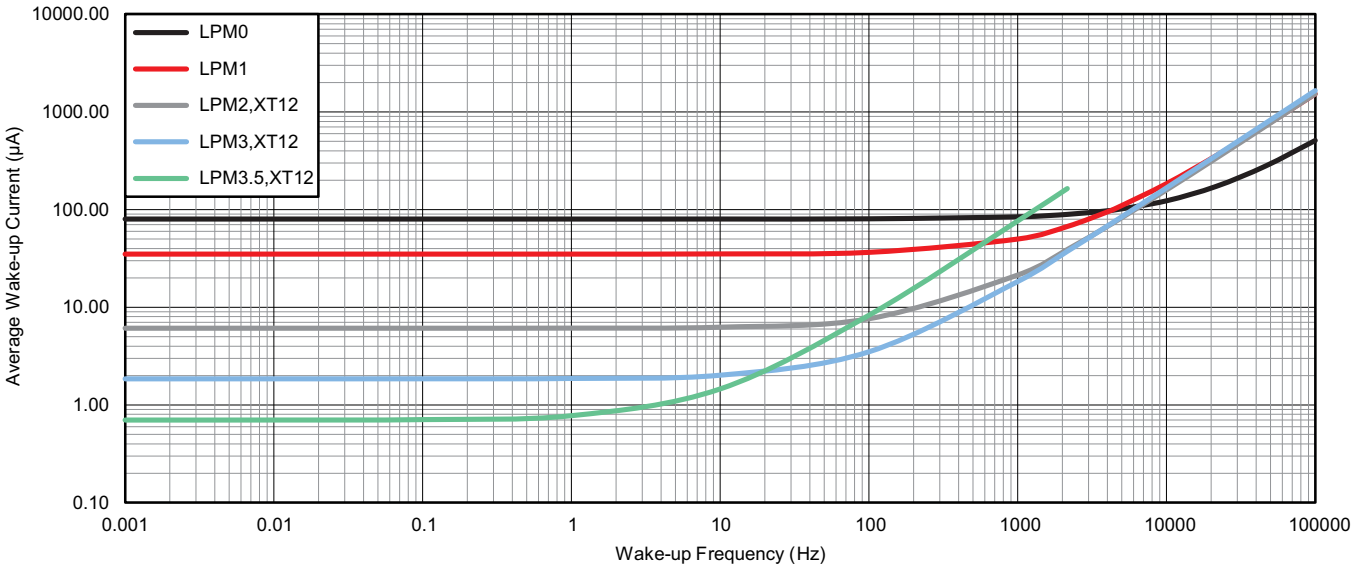
5.12.4.1 Typical Characteristics, Average LPM Currents vs Wake-up Frequency



NOTE: The average wakeup current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-7. Average LPM Currents vs Wake-up Frequency at 25°C



NOTE: The average wakeup current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-8. Average LPM Currents vs Wake-up Frequency at 85°C

5.12.5 Digital I/Os

Table 5-11 lists the characteristics of the digital inputs.

Table 5-11. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2.2 V	1.2		1.65	V
			3.0 V	1.65		2.25	
V_{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.00	V
			3.0 V	0.75		1.35	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2.2 V	0.44		0.98	V
			3.0 V	0.60		1.30	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions (1)	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance input leakage current	See (2)(3)	2.2 V, 3.0 V	–20		+20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag) (4)	Ports with interrupt capability (see 1.4 and Section 4.2)	2.2 V, 3.0 V	20			ns
$t_{(RST)}$	External reset pulse duration on $\overline{RST}$ (5)		2.2 V, 3.0 V	2			µs

(1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN and/or PJ.5/LFXOUT.
(2) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(3) The input leakage of the digital port pins is measured individually. The port pin is selected for input, and the pullup or pulldown resistor is disabled.
(4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.
(5) Not applicable if $\overline{RST}$/NMI pin configured as NMI.

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Table 5-12 lists the characteristics of the digital outputs.

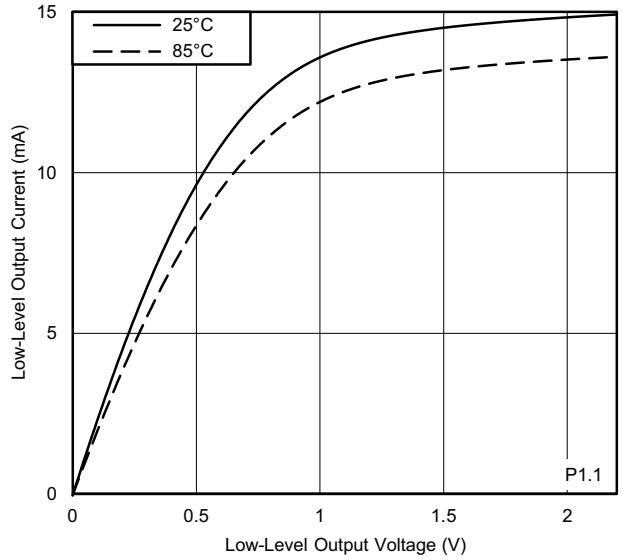
Table 5-12. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (also see Figure 5-9, Figure 5-10, Figure 5-11, and Figure 5-12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(1)	2.2 V	V_{CC} – 0.25		V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.60		V_{CC}	
		$I_{(OHmax)}$ = –2 mA(1)	3.0 V	V_{CC} – 0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.60		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	2.2 V	V_{SS}		V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}		V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(1)	3.0 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}		V_{SS} + 0.60	
$f_{Px.y}$	Port output frequency (with load)(3)	C_L = 20 pF, R_L (4) (5)	2.2 V	16			MHz
			3.0 V	16			
f_{Port_CLK}	Clock output frequency(3)	ACLK, MCLK, or SMCLK at configured output port, C_L = 20 pF(5)	2.2 V	16			MHz
			3.0 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2.2 V		4	15	ns
			3.0 V		3	15	
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2.2 V		4	15	ns
			3.0 V		3	15	
$t_{rise,ana}$	Port output rise time, port pins with shared analog functions	C_L = 20 pF	2.2 V		6	15	ns
			3.0 V		4	15	
$t_{fall,ana}$	Port output fall time, port pins with shared analog functions	C_L = 20 pF	2.2 V		6	15	ns
			3.0 V		4	15	

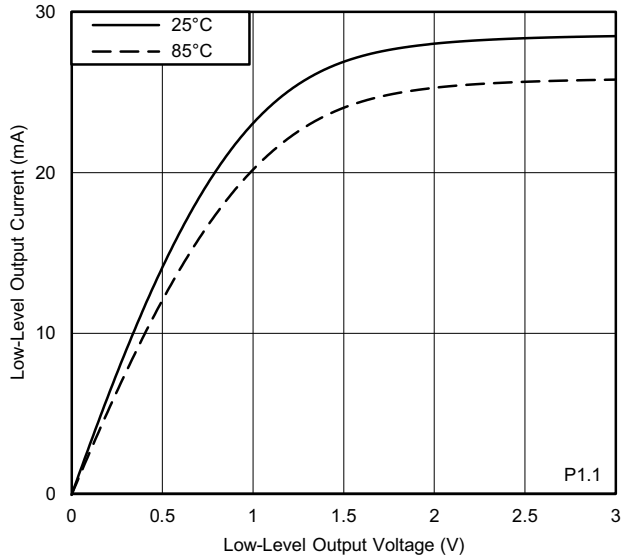
(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit, and the port might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
(5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.12.5.1 Typical Characteristics, Digital Outputs at 3.0 V and 2.2 V



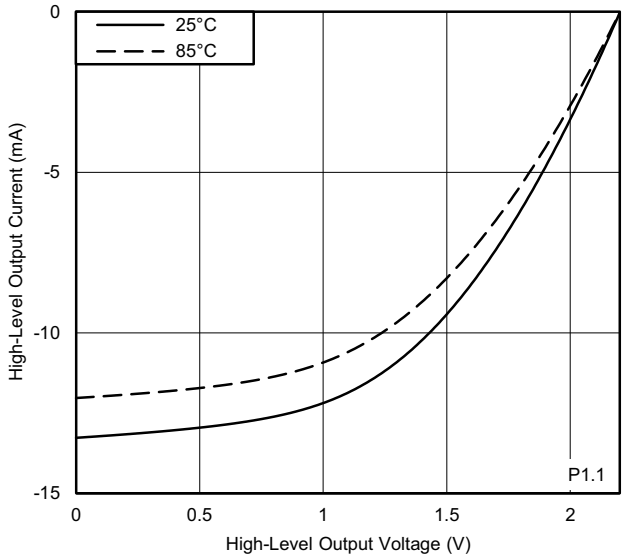
V_{CC} = 2.2 V

Figure 5-9. Typical Low-Level Output Current vs Low-Level Output Voltage



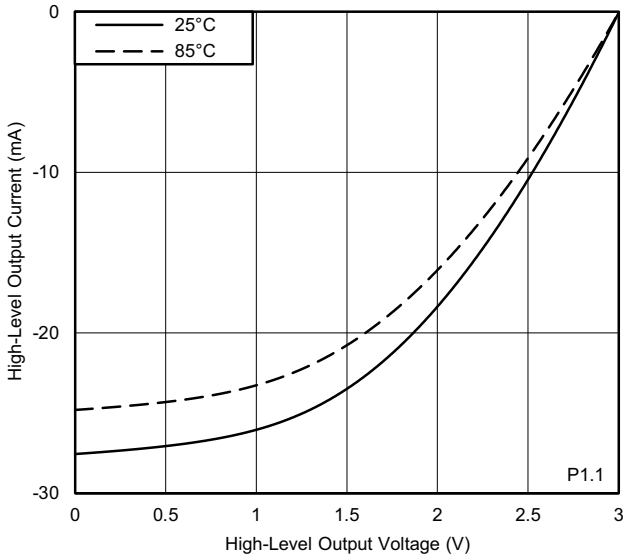
V_{CC} = 3.0 V

Figure 5-10. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 2.2 V

Figure 5-11. Typical High-Level Output Current vs High-Level Output Voltage



V_{CC} = 3.0 V

Figure 5-12. Typical High-Level Output Current vs High-Level Output Voltage

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Table 5-13 lists the frequencies of the pin oscillator.

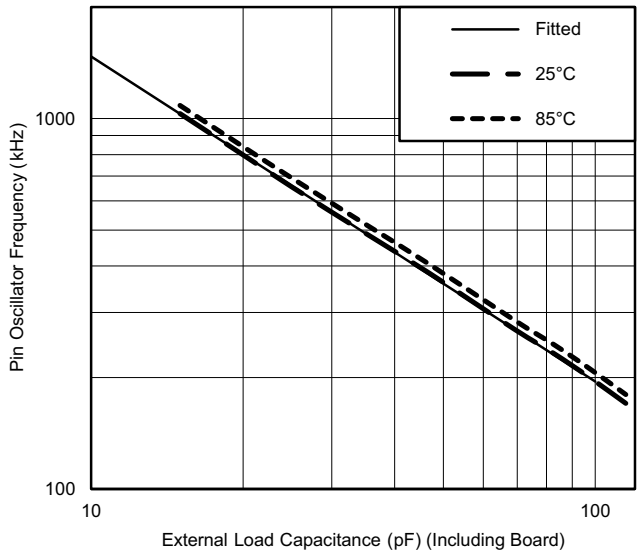
Table 5-13. Pin-Oscillator Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-13 and Figure 5-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{Px.y}$	Pin-oscillator frequency	Px.y, C_L = 10 pF(1)	3.0 V		1640		kHz
		Px.y, C_L = 20 pF(1)			870		

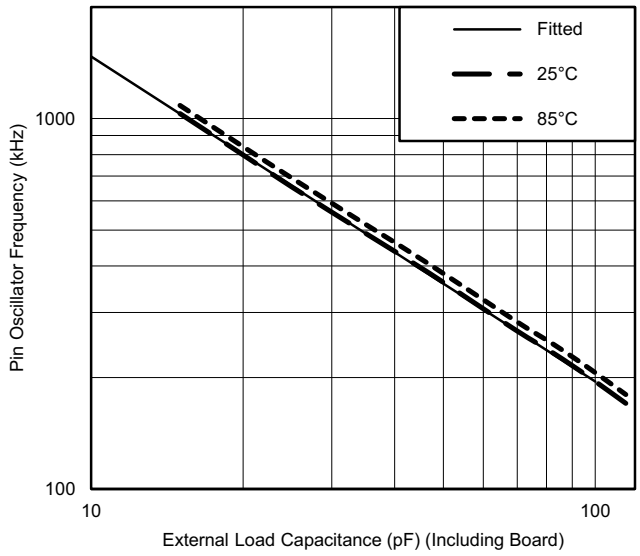
(1) C_L is the external load capacitance connected from the output to V_{SS} and includes all parasitic effects such as PCB traces.

5.12.5.2 Typical Characteristics, Pin-Oscillator Frequency



V_{CC} = 2.2 V One output active at a time.

Figure 5-13. Typical Oscillation Frequency vs Load Capacitance



V_{CC} = 3.0 V One output active at a time.

Figure 5-14. Typical Oscillation Frequency vs Load Capacitance

5.12.6 Timer_A and Timer_B

Table 5-14 lists the characteristics of the Timer_A.

Table 5-14. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

Table 5-15 lists the characteristics of the Timer_B.

Table 5-15. Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

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5.12.7 eUSCI

Table 5-16 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-16. eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			4	MHz

Table 5-17 lists the deglitch times of the eUSCI in UART mode.

Table 5-17. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0	2.2 V, 3.0 V	5		30	ns
		UCGLITx = 1		20		90	
		UCGLITx = 2		35		160	
		UCGLITx = 3		50		220	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum usable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-18 lists the supported clock frequencies of the eUSCI in SPI master mode.

Table 5-18. eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		16	MHz

Table 5-19 lists the characteristics of the eUSCI in SPI master mode.

Table 5-19. eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see note (1))

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10		1		UCxCLK cycles
$t_{STE,LAG}$	STE lag time, last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10		1		
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V		60	ns
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V		60	ns
$t_{SU,MI}$	SOMI input data setup time		2.2 V	35		ns
			3.0 V	35		
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0		ns
			3.0 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		10	ns
			3.0 V		10	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.2 V	0		ns
			3.0 V	0		

(1) $f_{UCxCLK} = 1 / 2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-15 and Figure 5-16.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-15 and Figure 5-16.

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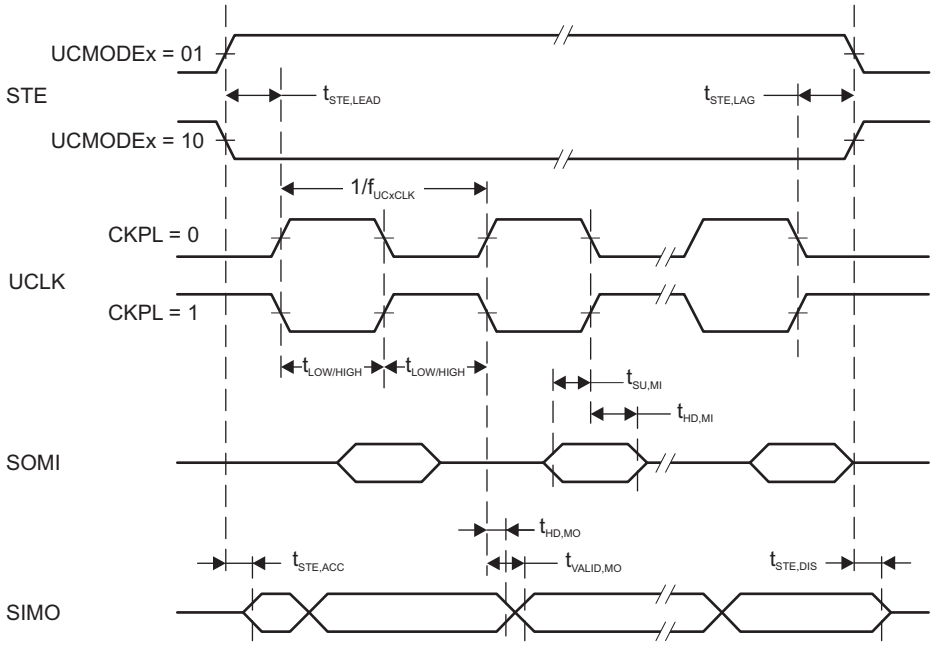

Figure 5-15. SPI Master Mode, CKPH = 0

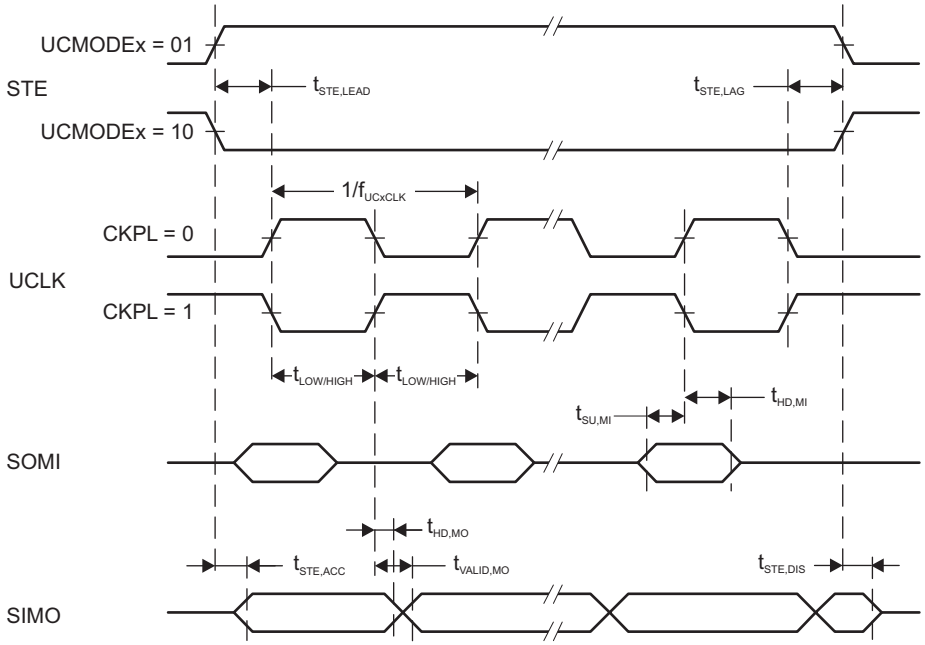

Figure 5-16. SPI Master Mode, CKPH = 1

Table 5-20 lists the characteristics of the eUSCI in SPI slave mode.

Table 5-20. eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note (1))

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.2 V	45		ns
			3.0 V	40		
$t_{STE,LAG}$	STE lag time, last clock to STE inactive		2.2 V	0		ns
			3.0 V	0		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.2 V		45	ns
			3.0 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.2 V		40	ns
			3.0 V		35	
$t_{SU,SI}$	SIMO input data setup time		2.2 V	4		ns
			3.0 V	4		
$t_{HD,SI}$	SIMO input data hold time		2.2 V	7		ns
			3.0 V	7		
$t_{VALID,SO}$	SOMI output data valid time (2)	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		35	ns
			3.0 V		35	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	2.2 V	0		ns
			3.0 V	0		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-17 and Figure 5-18.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-17 and Figure 5-18.

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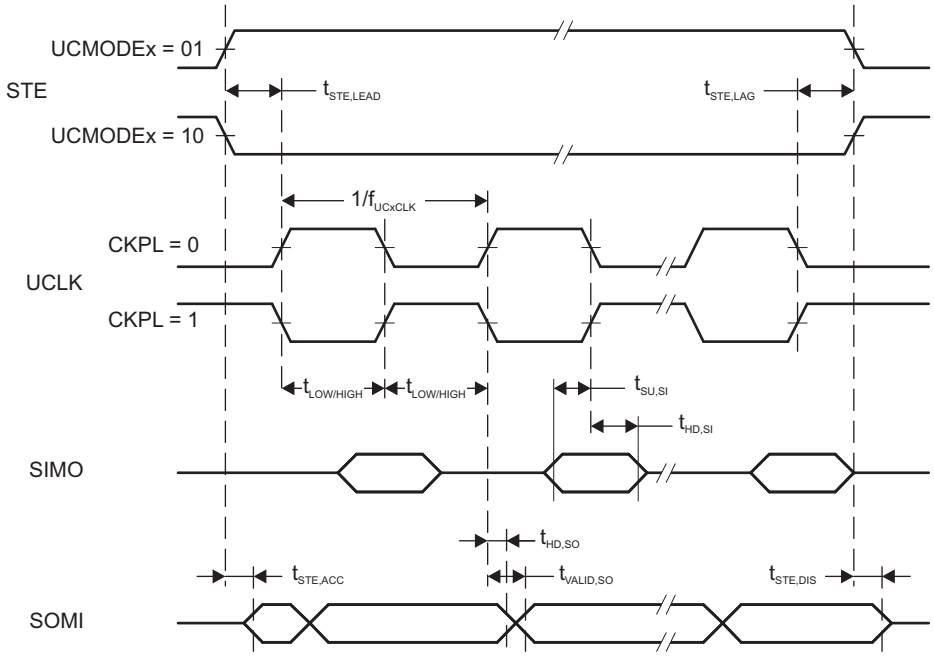

Figure 5-17. SPI Slave Mode, CKPH = 0

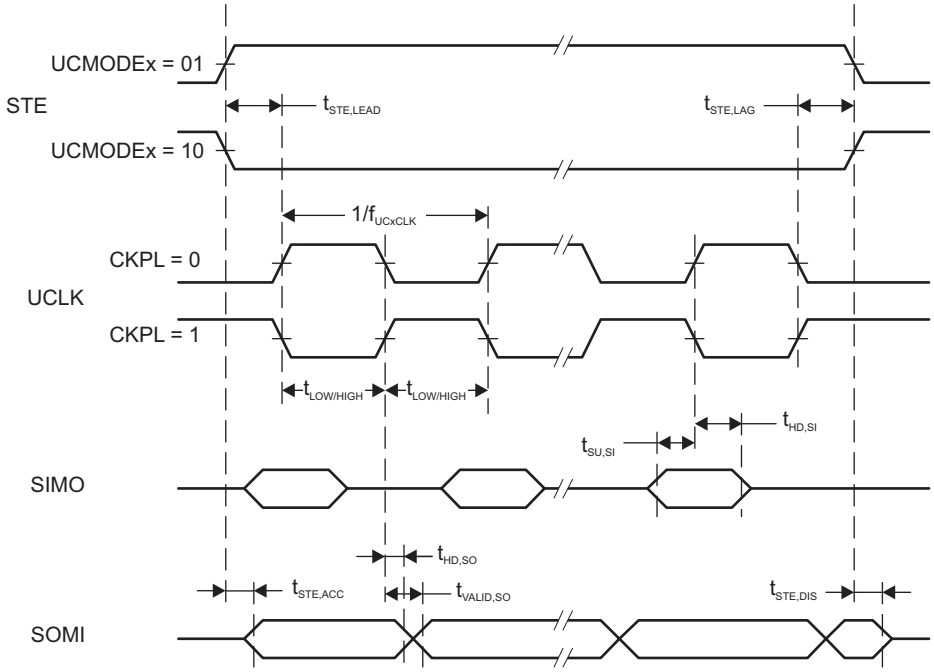

Figure 5-18. SPI Slave Mode, CKPH = 1

Table 5-21 lists the characteristics of the eUSCI in I²C mode.

Table 5-21. eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				16	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3.0 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3.0 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3.0 V	100			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{BUF}	Bus free time between a STOP and START condition	f_{SCL} = 100 kHz		4.7			µs
		f_{SCL} > 100 kHz		1.3			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2.2 V, 3.0 V	50		250	ns
		UCGLITx = 1		25		125	
		UCGLITx = 2		12.5		62.5	
		UCGLITx = 3		6.3		31.5	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2.2 V, 3.0 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

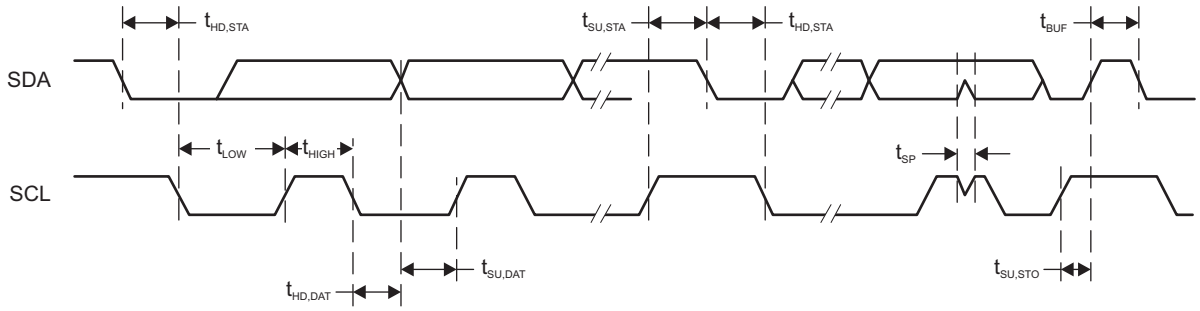

Figure 5-19. I²C Mode Timing

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5.12.8 ADC

表 5-22 lists the input requirements of the ADC.

表 5-22. 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
V(Ax)	Analog input voltage range(1)	All ADC12 analog input pins Ax		0		AVCC	V
I(ADC12_B) single-ended mode	Operating supply current into AVCC plus DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		145	185	µA
			2.2 V		140	180	
I(ADC12_B) differential mode	Operating supply current into AVCC plus DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 1, REFON = 0, ADC12SHTx= 0, ADC12DIV = 0	3.0 V		175	225	µA
			2.2 V		170	220	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		10	15	pF
R_I	Input MUX ON resistance	0 V ≤ V(Ax) ≤ AVCC	>2 V		0.5	4	kΩ
			<2 V		1	10	kΩ

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference supply current is not included in current consumption parameter $I_{(ADC12_B)}$.
(3) Approximately 60% (typical) of the total current into the AVCC and DVCC terminals is from AVCC.

Table 5-23 lists the timing parameters of the ADC.

Table 5-23. 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	Frequency for specified performance	For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0. If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here.		0.45		5.4	MHz
$f_{ADC12CLK}$	Frequency for reduced performance	Linearity parameters have reduced performance			32.768		kHz
$f_{ADC12OSC}$	Internal oscillator(1)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK		4	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK, ADC12WINC = 0		2.6		3.5	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			See (2)		
$t_{ADC12ON}$	Turnon settling time of the ADC	See (3)				100	ns
$t_{ADC12OFF}$	Time ADC must be off before it can be turned on again	$t_{ADC12OFF}$ must be met to make sure that $t_{ADC12ON}$ time holds.		100			ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 4 kΩ, C_I = 15 pF, C_{pext}= 8 pF(4)	All pulse sample mode (ADC12SHP = 1) and extended sample mode (ADC12SHP = 0) with buffered reference (ADC12VRSEL = 0x1, 0x3, 0x5, 0x7, 0x9, 0xB, 0xD, 0xF)	1			µs
			Extended sample mode (ADC12SHP = 0) with unbuffered reference (ADC12VRSEL= 0x0, 0x2, 0x4, 0x6, 0xC, 0xE)	See (5)			µs

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(2) 14 × 1 / $f_{ADC12CLK}$. If ADC12WINC = 1, then 15 × 1 / $f_{ADC12CLK}$
(3) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(4) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB: $t_{sample} = \ln(2^{n+2}) \times (R_S + R_I) \times (C_I + C_{pext})$, $R_S < 10$ kΩ, where n = ADC resolution = 12, R_S= external source resistance, C_{pext} = external parasitic capacitance.
(5) 6 × 1 / $f_{ADC12CLK}$

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Table 5-24 lists the linearity parameters of the ADC when using an external reference.

Table 5-24. 12-Bit ADC, Linearity Parameters With External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Number of no missing code output-code bits		12			bits
E_I	Integral linearity error (INL) for differential input	$1.2\ V \le V_{R+} - V_{R-} \le AV_{CC}$			±1.8	LSB
E_I	Integral linearity error (INL) for single ended inputs	$1.2\ V \le V_{R+} - V_{R-} \le AV_{CC}$			±2.2	LSB
E_D	Differential linearity error (DNL)		–0.99		+1.0	LSB
E_O	Offset error(2) (3)	ADC12VRSEL = 0x2 or 0x4 without TLV calibration, TLV calibration data can be used to improve the parameter(4)		±0.5	±1.5	mV
$E_{G,ext}$	Gain error	With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter(4), V_{R+} = 2.5 V, V_{R-} = AVSS		±0.8	±2.5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V_{R+} = 2.5 V, V_{R-} = AVSS		±1	±20	
$E_{T,ext}$	Total unadjusted error	With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter(4), V_{R+} = 2.5 V, V_{R-} = AVSS		±1.4	±3.5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V_{R+} = 2.5 V, V_{R-} = AVSS		±1.4	±21.0	

(1) See Table 5-26 and Table 5-32 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.
(3) Offset increases as I_R drop increases when V_{R-} is AVSS.
(4) For details, see the device descriptor in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

Table 5-25 lists the dynamic performance characteristics of the ADC with differential inputs and an external reference.

Table 5-25. 12-Bit ADC, Dynamic Performance for Differential Inputs With External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise	V_{R+} = 2.5 V, V_{R-} = AVSS	68	71		dB
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	10.7	11.2		bits

(1) See Table 5-26 and Table 5-32 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-26 lists the dynamic performance characteristics of the ADC with differential inputs and an internal reference.

Table 5-26. 12-Bit ADC, Dynamic Performance for Differential Inputs With Internal Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	10.3	10.7		Bits

(1) See Table 5-32 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-27 lists the dynamic performance characteristics of the ADC with single-ended inputs and an external reference.

Table 5-27. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise	V_{R+} = 2.5 V, V_{R-} = AVSS	64	68		dB
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	10.2	10.7		bits

(1) See Table 5-28 and Table 5-32 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-28 lists the dynamic performance characteristics of the ADC with single-ended inputs and an internal reference.

Table 5-28. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With Internal Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits(2)	V_{R+} = 2.5 V, V_{R-} = AVSS	9.4	10.4		bits

(1) See Table 5-32 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-29 lists the dynamic performance characteristics of the ADC using a 32.678-kHz clock.

Table 5-29. 12-Bit ADC, Dynamic Performance With 32.768-kHz Clock

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
ENOB	Effective number of bits(1)	Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, V_{R+} = 2.5 V, V_{R-} = AVSS	10	bits

(1) ENOB = (SINAD – 1.76) / 6.02

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Table 5-30 lists the characteristics of the temperature sensor and built-in $V_{1/2}$ of the ADC.

Table 5-30. 12-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (1) (2) (also see Figure 5-20)	ADC12ON = 1, ADC12TCMAP = 1, T_A = 0°C		700		mV
TC_{SENSOR}	See (2)	ADC12ON = 1, ADC12TCMAP = 1		2.5		mV/°C
$t_{SENSOR(sample)}$	Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected(3)	ADC12ON = 1, ADC12TCMAP = 1, Error of conversion result ≤ 1 LSB	30			µs
$V_{1/2}$	AVCC voltage divider for ADC12BATMAP = 1 on MAX input channel	ADC12ON = 1, ADC12BATMAP = 1	47.5%	50%	52.5%	
$I_{V\ 1/2}$	Current for battery monitor during sample time	ADC12ON = 1, ADC12BATMAP = 1		38	63	µA
$t_{V\ 1/2\ (sample)}$	Sample time required if ADC12BATMAP = 1 and channel MAX is selected(4)	ADC12ON = 1, ADC12BATMAP = 1	1.7			µs

(1) The temperature sensor offset can be as much as ±30°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each available reference voltage level. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times$ (Temperature, °C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 250 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V1/2(sample)}$; no additional on time is needed.

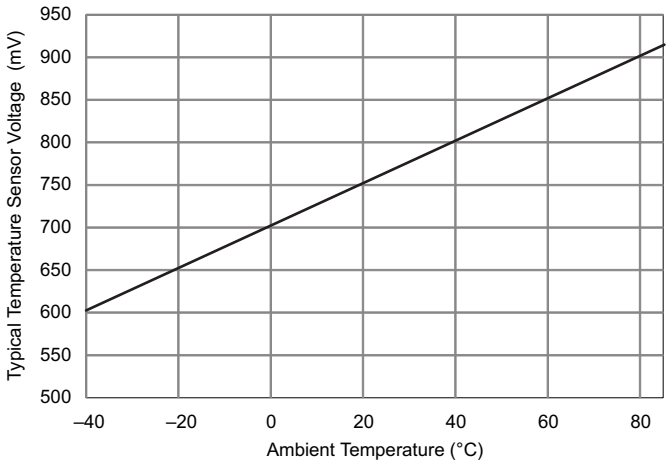

Figure 5-20. Typical Temperature Sensor Voltage

Table 5-31 lists the external reference requirements for the ADC.

Table 5-31. 12-Bit ADC, External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{R+}	Positive external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
V_{R-}	Negative external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	0		1.2	V
$V_{R+} - V_{R-}$	Differential external reference voltage input	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
I_{VeREF+}, I_{VeREF-}	Static input current, singled-ended input mode	1.2 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 0, ADC12PWRMD = 0			±10	µA
		1.2 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 0, ADC12PWRMD = 01			±2.5	
I_{VeREF+}, I_{VeREF-}	Static input current, differential input mode	1.2 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 1, ADC12PWRMD = 0			±20	µA
		1.2 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 1, ADC12PWRMD = 1			±5	
I_{VeREF+}	Peak input current with single-ended input	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC12DIF = 0			1.5	mA
I_{VeREF+}	Peak input current with differential input	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC12DIF = 1			3	mA
$C_{VeREF+/-}$	Capacitance at VeREF+ or VeREF- terminal	See (2)	10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.

(2) Connect two decoupling capacitors, 10 µF and 470 nF, to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_B. Also see the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

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5.12.9 Reference

Table 5-32 lists the characteristics of the built-in voltage reference.

Table 5-32. REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1	2.7 V		2.5	±1.5%	V
		REFVSEL = {1} for 2.0 V, REFON = 1	2.2 V		2.0	±1.5%	
		REFVSEL = {0} for 1.2 V, REFON = 1	1.8 V		1.2	±1.8%	
Noise	RMS noise at VREF(1)	From 0.1 Hz to 10 Hz, REFVSEL = {0}			110	600	µV
$V_{OS_BUF_INT}$	VREF ADC BUF_INT buffer offset(2)	T_A = 25°C , ADC ON, REFVSEL = {0}, REFON = 1, REFOUT = 0		–12		+12	mV
$V_{OS_BUF_EXT}$	VREF ADC BUF_EXT buffer offset(2)	T_A = 25°C, REFVSEL = {0} , REFOUT = 1, REFON = 1 or ADC ON		–12		+12	mV
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into AVCC terminal(3)	REFON = 1	3 V		8	15	µA
$I_{REF+_ADC_BUF}$	Operating supply current into AVCC terminal(3)	ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0,	3 V		225	355	µA
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0			1030	1660	
		ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1			120	185	
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1			545	895	
		ADC OFF, REFON = 1, REFOUT = 1, REFVSEL = {0, 1, 2}			1085	1780	
$I_{O(VREF+)}$	VREF maximum load current, VREF+ terminal	REFVSEL = {0, 1, 2}, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1		–1000		+10	µA
ΔVout/ΔIo (VREF+)	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2}, $I_{O(VREF+)}$ = +10 µA or –1000 µA, AV_{CC} = $AV_{CC(min)}$ for each reference level, REFON = REFOUT = 1				2500	µV/mA
$C_{VREF+/-}$	Capacitance at VREF+ and VREF- terminals	REFON = REFOUT = 1		0		100	pF
TC_{REF+}	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, T_A = –40°C to 85°C(4)			18	50	ppm/K
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = $AV_{CC(min)}$ to $AV_{CC(max)}$, T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1			120	400	µV/V
PSRR_AC	Power supply rejection ratio (AC)	dAV_{CC}= 0.1 V at 1 kHz			3.0		mV/V
t_{SETTLE}	Settling time of reference voltage(5)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0 → 1			75	80	µs

(1) Internal reference noise affects ADC performance when ADC uses internal reference. See *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal versus external reference.
(2) Buffer offset affects ADC gain error and thus total unadjusted error.
(3) The internal reference current is supplied through the AVCC terminal.
(4) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(5) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.12.10 Comparator

Table 5-33 lists the characteristics of the comparator.

Table 5-33. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{AVCC_COMP}	Comparator operating supply current into AVCC, excludes reference resistor ladder	CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)	2.2 V, 3.0 V		11	20	µA
		CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)			9	17	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 30°C				0.5	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 85°C				1.3	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, including REF module current	CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 0	2.2 V, 3.0 V		12	15	µA
		CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 1			5	7	
V_{REF}	Reference voltage level	CERSx = 11, CEREFLx = 01, CEREFACC = 0	1.8 V	1.17	1.2	1.23	V
		CERSx = 11, CEREFLx = 10, CEREFACC = 0	2.2 V	1.92	2.0	2.08	
		CERSx = 11, CEREFLx = 11, CEREFACC = 0	2.7 V	2.40	2.5	2.60	
		CERSx = 11, CEREFLx = 01, CEREFACC = 1	1.8 V	1.10	1.2	1.245	
		CERSx = 11, CEREFLx = 10, CEREFACC = 1	2.2 V	1.90	2.0	2.08	
		CERSx = 11, CEREFLx = 11, CEREFACC = 1	2.7 V	2.35	2.5	2.60	
V_{IC}	Common-mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CEPWRMD = 00		–32		32	mV
		CEPWRMD = 01		–32		32	
		CEPWRMD = 10		–30		30	
C_{IN}	Input capacitance	CEPWRMD = 00 or CEPWRMD = 01			9		pF
		CEPWRMD = 10			9		
R_{SIN}	Series input resistance	On (switch closed)			1	3	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV			260	330	ns
		CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV			350	460	
		CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV				15	µs
$t_{PD,filter}$	Propagation delay with filter active	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00			700	1000	ns
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01			1.0	1.8	µs
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10			2.0	3.5	
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11			4.0	7.0	
t_{EN_CMP}	Comparator enable time	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 00			0.9	1.5	µs
		CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 01			0.9	1.5	
		CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 10			15	100	
$t_{EN_CMP_VREF}$	Comparator and reference ladder and reference voltage enable time	CEON = 0 → 1, CEREFLX = 10, CERSx = 10 or 11, CEREF0 = CEREF1 = 0x0F, Overdrive ≥ 20 mV			350	1500	µs
V_{CE_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

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5.12.11 FRAM

Table 5-34 lists the characteristics of the FRAM.

Table 5-34. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Read and write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
		T_J = 70°C	40			
		T_J = 85°C	10			
I_{WRITE}	Current to write into FRAM		I_{READ} (1)			nA
I_{ERASE}	Erase current		n/a (2)			nA
t_{WRITE}	Write time		t_{READ} (3)			ns
t_{READ}	Read time	NWAITSx = 0	1 / f_{SYSTEM} (4)			ns
		NWAITSx = 1	2 / f_{SYSTEM} (4)			

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption numbers $I_{AM,FRAM}$.
(2) FRAM does not require a special erase sequence.
(3) Writing into FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

5.13 Emulation and Debug

Table 5-35 lists the characteristics of the JTAG and Spy-Bi-Wire interface.

Table 5-35. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{JTAG}	Supply current adder when JTAG active (but not clocked)	2.2 V, 3.0 V		40	100	µA
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3.0 V	0		10	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3.0 V	0.04		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V, 3.0 V			110	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG (2)	2.2 V	0		16	MHz
		3.0 V	0		16	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3.0 V	20	35	50	kΩ
f_{TCLK}	TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f_{SYSTEM})				16	MHz
$t_{TCLK,Low/High}$	TCLK low or high clock pulse duration, no FRAM access				25	ns
$f_{TCLK,FRAM}$	TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f_{SYSTEM} with no FRAM wait states)				4	MHz
$t_{TCLK,FRAM,Low/High}$	TCLK low or high clock pulse duration, including FRAM accesses				100	ns

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the $t_{SBW,En}$ time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Overview

The Texas Instruments MSP430FR59xx family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes is optimized to achieve extended battery life for example in portable measurement applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The MSP430FR59xx devices are microcontroller configurations with up to five 16-bit timers, Comparator, universal serial communication interfaces (eUSCI) supporting UART, SPI, and I^2C, hardware multiplier, AES accelerator, DMA, real-time clock module with alarm capabilities, up to 40 I/O pins, and an high-performance 12-bit analog-to-digital converter (ADC).

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

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6.3 Operating Modes

The MSP430FR59xx MCUs have one active mode and seven software-selectable low-power modes of operation (see 表 6-1). An interrupt event can wake up the device from a low-power mode (LPM0 to LPM4), service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

表 6-1. Operating Modes

MODE	AM		LPM0	LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	ACTIVE	ACTIVE, FRAM OFF(1)	CPU Off(2)	CPU OFF	STANDBY	STANDBY	OFF	RTC ONLY	SHUTDOWN WITH SVS	SHUTDOWN WITHOUT SVS
Maximum system clock	16 MHz		16 MHz	16 MHz	50 kHz	50 kHz	0(3)	50 kHz	0(3)	
Typical current consumption, T_A = 25°C	103 µA/MHz	65 µA/MHz	70 µA at 1 MHz	35 µA at 1 MHz	0.7 µA	0.4 µA	0.3 µA	0.25 µA	0.2 µA	0.02 µA
Typical wake-up time	N/A		instant	6 µs	6 µs	7 µs	7 µs	250 µs	250 µs	1000 µs
Wake-up events	N/A		all	all	LF I/O Comp	LF I/O Comp	I/O Comp	RTC I/O	I/O	
CPU	**on**		off	off	off	off	off	reset	reset	
FRAM	**on**	off(1)	standby (or off(1))	off	off	off	off	off	off	
Peripherals in high-frequency state(4)	**yes**		**yes**	**yes**	no	no	no	reset	reset	
Peripherals in low-frequency state(4)	**yes**		**yes**	**yes**	**yes**	**yes**(5)	no	RTC	reset	
Peripherals in unclocked state(4)	**yes**		**yes**	**yes**	**yes**	**yes**(5)	**yes**(5)	reset	reset	
MCLK	**on** (16 MHz_{MAX})		off	off	off	off	off	off	off	
SMCLK	optional(6) (16 MHz_{MAX})		optional(6) (16 MHz_{MAX})	optional(6) (16 MHz_{MAX})	off	off	off	off	off	
ACLK	**on** (50 kHz_{MAX})		**on** (50 kHz_{MAX})	**on** (50 kHz_{MAX})	**on** (50 kHz_{MAX})	**on** (50 kHz_{MAX})	off	off	off	
External clock	optional (16 MHz_{MAX})		optional (16 MHz_{MAX})	optional (16 MHz_{MAX})	optional (50 kHz_{MAX})	optional (50 kHz_{MAX})	optional (50 kHz_{MAX})	off	off	
Full retention	**yes**		**yes**	**yes**	**yes**	**yes**	**yes**	no	no	

(1) FRAM disabled in FRAM controller
(2) Disabling the FRAM through the FRAM controller allows the application to lower the LPM current consumption but the wake-up time increases as soon as FRAM is accessed (for example, to fetch an interrupt vector). For a wakeup that does not involve the FRAM (for example, DMA transfer to RAM), the wakeup is not delayed.
(3) All clocks disabled
(4) See 表 6-2 for a detailed description of peripherals in high-frequency, low-frequency, or unclocked state.
(5) See 6.3.1, which describes the use of peripherals in LPM3 and LPM4.
(6) Controlled by SMCLKOFF.

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表 6-1. Operating Modes (continued)

MODE	AM		LPM0	LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	ACTIVE	ACTIVE, FRAM OFF(1)	CPU Off(2)	CPU OFF	STANDBY	STANDBY	OFF	RTC ONLY	SHUTDOWN WITH SVS	SHUTDOWN WITHOUT SVS
SVS	always		always	always	optional(7)	optional(7)	optional(7)	optional(7)	on(8)	off(9)
Brownout	**always**		**always**	**always**	**always**	**always**	**always**	**always**	**always**	

(7) Activated SVS (SVSHE = 1) results in higher current consumption. SVS is not included in typical current consumption.
(8) SVSHE = 1
(9) SVSHE = 0

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6.3.1 Peripherals in Low-Power Modes

Peripherals can be in different states that impact the achievable power modes of the device. The states depend on the operational modes of the peripherals. The states are:

- A peripheral is in a "high frequency state" if it requires or uses a clock with a "high" frequency of more than 50 kHz.
- A peripheral is in a "low frequency state" if it requires or uses a clock with a "low" frequency of 50 kHz or less.
- A peripheral is in an "unclocked state" if it does not require nor use an internal clock.

If the CPU requests a power mode that does not support the current state of all active peripherals, the device cannot enter the requested power mode but does enter a power mode that still supports the current state of the peripherals, unless an external clock is used. If an external clock is used, the application must ensure the correct frequency range for the requested power mode.

表 6-2. Peripheral States

PERIPHERAL	IN HIGH-FREQUENCY STATE(1)	IN LOW-FREQUENCY STATE(2)	IN UNCLOCKED STATE(3)
WDT	Clocked by SMCLK	Clocked by ACLK	Not applicable
DMA(4)	Not applicable	Not applicable	Waiting for a trigger
RTC_B	Not applicable	Clocked by LFXT	Not applicable
Timer_A, TAx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
Timer_B, TBx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Ax in UART mode	Clocked by SMCLK	Clocked by ACLK	Waiting for first edge of START bit
eUSCI_Ax in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Ax in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Bx in I^2C master mode	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Not applicable
eUSCI_Bx in I^2C slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Waiting for START condition or clocked by external clock ≤50 kHz
eUSCI_Bx in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Bx in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
ADC12_B	Clocked by SMCLK or by MODOSC	Clocked by ACLK	Waiting for a trigger
REF_A	Not applicable	Not applicable	Always
COMP_E	Not applicable	Not applicable	Always
CRC(5)	Not applicable	Not applicable	Not applicable
MPY(5)	Not applicable	Not applicable	Not applicable
AES(5)	Not applicable	Not applicable	Not applicable

(1) Peripherals are in a state that requires or uses a clock with a "high" frequency of more than 50 kHz.
(2) Peripherals are in a state that requires or uses a clock with a "low" frequency of 50 kHz or less.
(3) Peripherals are in a state that does not require or does not use an internal clock.
(4) The DMA always transfers data in active mode but can wait for a trigger in any low power mode. A DMA trigger during a low power mode will cause a temporary transition into active mode for the time of the transfer.
(5) Operates only during active mode and will eventually delay the transition into a low power mode until its operation is completed.

6.3.1.1 Idle Currents of Peripherals in LPM3 and LPM4

Most peripherals can be activated to be operational in LPM3 if clocked by ACLK. Some modules are operational in LPM4, because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To limit the idle current adder, certain peripherals are grouped together. To achieve optimal current consumption, use modules within one group and limit the number of groups with active modules. 表 6-3 lists the grouping of the peripherals. Modules not listed in this table are either already included in the standard LPM3 current consumption or cannot be used in LPM3 or LPM4.

The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C), See the I_{IDLE} current parameters in Section 5.7 for details.

表 6-3. Peripheral Groups

Group A	Group B
Timer TA1	Timer TA0
Timer TA2	Timer TA3
Timer TB0	Comparator
eUSCI_A0	ADC12_B
eUSCI_A1	REF_A
eUSCI_B0	

6.4 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address and signatures are in the address range 0FFFFh to 0FF80h. 図 6-1 summarizes the content of this address range.

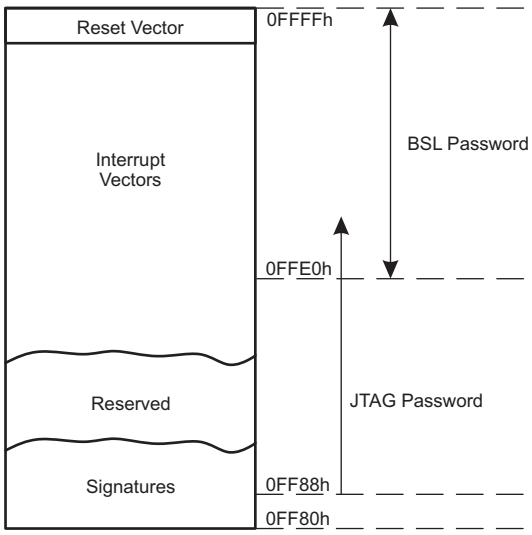

図 6-1. Interrupt Vectors, Signatures and Passwords

The power-up start address or reset vector is at 0FFFFh to 0FFFEh. It contains a 16-bit address that points to the start address of the application program.

The interrupt vectors start at 0FFFDh and extend to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. 表 6-4 lists the device specific interrupt vector locations.

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The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as BSL password (if enabled by the corresponding signature).

The signatures are located at 0FF80h extending to higher addresses. Signatures are evaluated during device start-up. 表 6-5 lists the device specific signature locations.

A JTAG password can be programmed starting from address 0FF88h and extending to higher addresses. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password. The length of the JTAG password depends on the JTAG signature.

See the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide* for details.

表 6-4. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, Brownout, Supply Supervisor External Reset RST Watchdog Time-out (Watchdog mode) WDT, FRCTL MPU, CS, PMM Password Violation FRAM uncorrectable bit error detection MPU segment violation FRAM access time error Software POR, BOR	SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW UBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG ACCTEIFG PMMPORIFG, PMMBORIFG (SYSRSTIV)(1) (2)	Reset	0FFFEh	highest
System NMI Vacant Memory Access JTAG Mailbox FRAM bit error detection MPU segment violation	VMAIFG JMBNIFG, JMBOUTIFG CBDIFG, UBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG (SYSSNIV)(1) (3)	(Non)maskable	0FFFCh	
User NMI External NMI Oscillator Fault	NMIIFG, OFIFG (SYSUNIV)(1) (3)	(Non)maskable	0FFFAh	
Comparator_E	CEIFG, CEIIFG (CEIV)(1)	Maskable	0FFF8h	
TB0	TB0CCR0.CCIFG	Maskable	0FFF6h	
TB0	TB0CCR1.CCIFG ... TB0CCR6.CCIFG, TB0CTL.TBIFG (TB0IV)(1)	Maskable	0FFF4h	
Watchdog Timer (Interval Timer Mode)	WDTIFG	Maskable	0FFF2h	
eUSCI_A0 Receive or Transmit	UCA0IFG: UCRXIFG, UCTXIFG (SPI mode) UCA0IFG: UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA0IV)(1)	Maskable	0FFF0h	
eUSCI_B0 Receive or Transmit	UCB0IFG: UCRXIFG, UCTXIFG (SPI mode) UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB0IV)(1)	Maskable	0FFEEh	
ADC12_B	ADC12IFG0 to ADC12IFG31 ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC21OVIFG, ADC12TOVIFG (ADC12IV)(1)	Maskable	0FFECh	
TA0	TA0CCR0.CCIFG	Maskable	0FFEAh	
TA0	TA0CCR1.CCIFG, TA0CCR2.CCIFG, TA0CTL.TAIFG (TA0IV)(1)	Maskable	0FFE8h	

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space
(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot disable it.

表 6-4. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_A1 Receive or Transmit	UCA1IFG: UCRXIFG, UCTXIFG (SPI mode) UCA1IFG: UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA1IV)(1)	Maskable	0FFE6h	
DMA	DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG (DMAIV)(1)	Maskable	0FFE4h	
TA1	TA1CCR0.CCIFG	Maskable	0FFE2h	
TA1	TA1CCR1.CCIFG, TA1CCR2.CCIFG, TA1CTL.TAIFG (TA1IV)(1)	Maskable	0FFE0h	
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)	Maskable	0FFDEh	
TA2	TA2CCR0.CCIFG	Maskable	0FFDCh	
TA2	TA2CCR1.CCIFG TA2CTL.TAIFG (TA2IV)(1)	Maskable	0FFDAh	
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)	Maskable	0FFD8h	
TA3	TA3CCR0.CCIFG	Maskable	0FFD6h	
TA3	TA3CCR1.CCIFG TA3CTL.TAIFG (TA3IV)(1)	Maskable	0FFD4h	
I/O Port P3	P3IFG.0 to P3IFG.7 (P3IV)(1)	Maskable	0FFD2h	
I/O Port P4	P4IFG.0 to P4IFG.2 (P4IV)(1)	Maskable	0FFD0h	
RTC_B	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV)(1)	Maskable	0FFCEh	
AES	AESRDYIFG	Maskable	0FFCCh	lowest

表 6-5. Signatures

SIGNATURE	WORD ADDRESS
IP Encapsulation Signature 2	0FF8Ah
IP Encapsulation Signature 1(1)	0FF88h
BSL Signature 2	0FF86h
BSL Signature 1	0FF84h
JTAG Signature 2	0FF82h
JTAG Signature 1	0FF80h

(1) Must not contain 0AAAAh if used as JTAG password and IP encapsulation functionality is not desired.

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6.5 Memory Organization

表 6-6 summarizes the memory map for all device variants.

表 6-6. Memory Organization(1)

		MSP430FR59x9	MSP430FR59x8	MSP430FR59x7
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Total Size	63KB 00FFFFh to 00FF80h 013FFFh to 004400h	47KB 00FFFFh to 00FF80h 00FF7Fh to 004400h	32KB 00FFFFh to 00FF80h 00FF7Fh to 008000h
RAM		2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h	1KB 001FFFh to 001C00h
Device Descriptor Info (TLV) (FRAM)		256 B 001AFFh to 001A00h	256 B 001AFFh to 001A00h	256 B 001AFFh to 001A00h
Information memory (FRAM)	Info A	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h
	Info B	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h
	Info C	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h
Bootloader (BSL) memory (ROM)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 0h	4KB 000FFFh to 0h	4KB 000FFFh to 0h

(1) All address space not listed is considered vacant memory.

6.6 Bootloader (BSL)

The BSL enables users to program the FRAM or RAM using a UART serial interface (FRxxxx devices) or an I^2C interface (FRxxxx1 devices). Access to the device memory through the BSL is protected by an user-defined password. 表 6-7 list the BSL pins requirements. BSL entry requires a specific entry sequence on the $\overline{RST}$/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 FRAM Device Bootloader (BSL) User's Guide*.

表 6-7. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{RST}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P2.0	Devices with UART BSL (FRxxxx): Data transmit
P2.1	Devices with UART BSL (FRxxxx): Data receive
P1.6	Devices with I^2C BSL (FRxxxx1): Data
P1.7	Devices with I^2C BSL (FRxxxx1): Clock
VCC	Power supply
VSS	Ground supply

6.7 JTAG Operation

6.7.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. 表 6-8 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

表 6-8. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

6.7.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-9 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

表 6-9. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
VCC		Power supply
VSS		Ground supply

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6.8 FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

注

Wait States

For MCLK frequencies > 8 MHz, wait states must be configured following the flow described in the *Wait State Control* section of the *FRAM Controller (FRCTRL)* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see *MSP430™ FRAM Technology – How To and Best Practices*.

6.9 Memory Protection Unit Including IP Encapsulation

The FRAM can be protected from inadvertent CPU execution, read access, or write access by the MPU. Features of the MPU include:

- IP encapsulation with programmable boundaries in steps of 1KB (prevents reads from "outside"; for example, JTAG or non-IP software).
- Main memory partitioning is programmable up to three segments in steps of 1KB.
- Each segment's access rights can be individually selected (main and information memory).
- Access violation flags with interrupt capability for easy servicing of access violations.

6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, see the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

6.10.1 Digital I/O

Up to four 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all ports.
- Read and write access to port control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- All pins of ports P1, P2, P3, P4, and PJ support Capacitive Touch I/O functionality.
- No cross-currents during start-up.

注

Configuration of Digital I/Os After BOR Reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers, and their module functions disabled. To enable the I/O functionality after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section of the *Digital I/O* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

6.10.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch-crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK). ACLK can be sourced from a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external low-frequency (<50 kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal digitally controlled oscillator DCO, a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

6.10.3 Power-Management Module (PMM)

The primary functions of the PMM are:

- Supply regulated voltages to the core logic
- Supervise voltages that are connected to the device (at DVCC pins)
- Give reset signals to the device during power on and power off

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6.10.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

6.10.5 Real-Time Clock (RTC_B) (Only MSP430FR596x and MSP430FR594x)

The RTC_B module contains an integrated real-time clock (RTC). The RTC integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

6.10.6 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. 表 6-10 lists the clock sources for the WDT_A module.

表 6-10. WDT_A Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	LFMODCLK

6.10.7 System Module (SYS)

The SYS module manages many of the system functions within the device. These system functions include power on reset (POR) and power up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader (BSL) entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. 表 6-11 lists the SYS module interrupt vector registers.

表 6-11. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		MPUPW MPU password violation (PUC)	22h	
		CSPW CS password violation (PUC)	24h	
		MPUSEGPIFG encapsulated IP memory segment violation (PUC)	26h	
		MPUSEGIIFG information memory segment violation (PUC)	28h	
		MPUSEG1IFG segment 1 memory violation (PUC)	2Ah	
		MPUSEG2IFG segment 2 memory violation (PUC)	2Ch	
		MPUSEG3IFG segment 3 memory violation (PUC)	2Eh	
		ACCTEIFG access time error (PUC) (1)	30h	
		Reserved	32h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		Reserved	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		MPUSEGPIFG encapsulated IP memory segment violation	08h	
		MPUSEGIIFG information memory segment violation	0Ah	
		MPUSEG1IFG segment 1 memory violation	0Ch	
		MPUSEG2IFG segment 2 memory violation	0Eh	
		MPUSEG3IFG segment 3 memory violation	10h	
		VMAIFG vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest

(1) Indicates incorrect wait state settings.

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表 6-11. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG NMI pin	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

6.10.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to wake to move data to or from a peripheral. 表 6-12 lists the available triggers for the DMA.

表 6-12. DMA Trigger Assignments(1)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	AES Trigger 0	AES Trigger 0	AES Trigger 0
12	AES Trigger 1	AES Trigger 1	AES Trigger 1
13	AES Trigger 2	AES Trigger 2	AES Trigger 2
14	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
15	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
16	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
17	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
18	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)
19	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)
20	UCB0RXIFG1 (I^2C)	UCB0RXIFG1 (I^2C)	UCB0RXIFG1 (I^2C)
21	UCB0TXIFG1 (I^2C)	UCB0TXIFG1 (I^2C)	UCB0TXIFG1 (I^2C)
22	UCB0RXIFG2 (I^2C)	UCB0RXIFG2 (I^2C)	UCB0RXIFG2 (I^2C)
23	UCB0TXIFG2 (I^2C)	UCB0TXIFG2 (I^2C)	UCB0TXIFG2 (I^2C)
24	UCB0RXIFG3 (I^2C)	UCB0RXIFG3 (I^2C)	UCB0RXIFG3 (I^2C)
25	UCB0TXIFG3 (I^2C)	UCB0TXIFG3 (I^2C)	UCB0TXIFG3 (I^2C)
26	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion
27	Reserved	Reserved	Reserved

(1) If a reserved trigger source is selected, no trigger is generated.

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表 6-12. DMA Trigger Assignments[(1)] (continued)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

6.10.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3 or 4 pin) and I^2C.

Two eUSCI_A modules and one eUSCI_B module are implemented.

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6.10.10 TA0, TA1

TA0 and TA1 are 16-bit timers and counters (Timer_A type) with three capture/compare registers each. TA0 and TA can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-13 and 表 6-14). TA0 and TA have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-13. TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.2	TA0CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.2	$\overline{\text{TA0CLK}}$	INCLK				
P1.6	TA0.0	CCI0A	CCR0	TA0	TA0.0	P1.6
P2.3	TA0.0	CCI0B				P2.3
	DVSS	GND				
	DVCC	V_{CC}				
P1.0	TA0.1	CCI1A	CCR1	TA1	TA0.1	P1.0
	COUT (internal)	CCI1B				ADC12(internal) ADC12SHSx = {1}
	DVSS	GND				
	DVCC	V_{CC}				
P1.1	TA0.2	CCI2A	CCR2	TA2	TA0.2	P1.1
	ACLK (internal)	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				

表 6-14. TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.1	TA1CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.1	$\overline{\text{TA1CLK}}$	INCLK				
P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	P1.7
P2.4	TA1.0	CCI0B				P2.4
	DVSS	GND				
	DVCC	V_{CC}				
P1.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	P1.2
	COUT (internal)	CCI1B				ADC12(internal) ADC12SHSx = {4}
	DVSS	GND				
	DVCC	V_{CC}				
P1.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	P1.3
	ACLK (internal)	CCI2B				
	DVSS	GND				
	DVCC	V_{CC}				

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6.10.11 TA2, TA3

TA2 and TA3 are 16-bit timers and counters (Timer_A type) with two capture/compare registers each and with internal connections only. TA2 and TA3 can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-15 and 表 6-16). TA2 and TA3 have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-15. TA2 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 0 (internal)	INCLK			
TA3 CCR0 output (internal)	CCI0A	CCR0	TA0	TA3 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V_{CC}			
From Capacitive Touch I/O 0 (internal)	CCI1A	CCR1	TA1	ADC12(internal) ADC12SHSx = {5}
COUT (internal)	CCI1B			
DVSS	GND			
DVCC	V_{CC}			

表 6-16. TA3 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 1 (internal)	INCLK			
TA2 CCR0 output (internal)	CCI0A	CCR0	TA0	TA2 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V_{CC}			
From Capacitive Touch I/O 1 (internal)	CCI1A	CCR1	TA1	ADC12(internal) ADC12SHSx = {6}
COUT (internal)	CCI1B			
DVSS	GND			
DVCC	V_{CC}			

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6.10.12 TB0

TB0 is a 16-bit timer and counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-17). TB0 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-17. TB0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.0	TB0CLK	TBCLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.0	$\overline{\text{TB0CLK}}$	INCLK				
P2.1	TB0.0	CCI0A	CCR0	TB0	TB0.0	P2.1
P2.5	TB0.0	CCI0B				P2.5
	DVSS	GND				ADC12 (internal) ADC12SHSx = {2}
	DVCC	V_{CC}				
P1.4	TB0.1	CCI1A	CCR1	TB1	TB0.1	P1.4
	COUT (internal)	CCI1B				P2.6
	DVSS	GND				ADC12 (internal) ADC12SHSx = {3}
	DVCC	V_{CC}				
P1.5	TB0.2	CCI2A	CCR2	TB2	TB0.2	P1.5
	ACLK (internal)	CCI2B				P2.2
	DVSS	GND				
	DVCC	V_{CC}				
P3.4	TB0.3	CCI3A	CCR3	TB3	TB0.3	P3.4
P1.6	TB0.3	CCI3B				P1.6
	DVSS	GND				
	DVCC	V_{CC}				
P3.5	TB0.4	CCI4A	CCR4	TB4	TB0.4	P3.5
P1.7	TB0.4	CCI4B				P1.7
	DVSS	GND				
	DVCC	V_{CC}				
P3.6	TB0.5	CCI5A	CCR5	TB5	TB0.5	P3.6
P4.4	TB0.5	CCI5B				P4.4
	DVSS	GND				
	DVCC	V_{CC}				
P3.7	TB0.6	CCI6A	CCR6	TB6	TB0.6	P3.7
P2.0	TB0.6	CCI6B				P2.0
	DVSS	GND				
	DVCC	V_{CC}				

6.10.13 ADC12_B

The ADC12_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

表 6-18 lists the external trigger sources.

表 6-18. ADC12_B Trigger Signal Connections

ADC12SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC12SC)
001	1	TA0 CCR1 output
010	2	TB0 CCR0 output
011	3	TB0 CCR1 output
100	4	TA1 CCR1 output
101	5	TA2 CCR1 output
110	6	TA3 CCR1 output
111	7	Reserved (DVSS)

表 6-19 lists the available multiplexing between internal and external analog inputs.

表 6-19. ADC12_B External and Internal Signal Mapping

CONTROL BIT IN ADC12CTL3 REGISTER	EXTERNAL ADC INPUT (CONTROL BIT = 0)	INTERNAL ADC INPUT (CONTROL BIT = 1)
ADC12BATMAP	A31	Battery monitor
ADC12TCMAP	A30	Temperature sensor
ADC12CH0MAP	A29	N/A (1)
ADC12CH1MAP	A28	N/A (1)
ADC12CH2MAP	A27	N/A (1)
ADC12CH3MAP	A26	N/A (1)

(1) N/A = No internal signal is available on this device.

6.10.14 Comparator_E

The primary function of the Comparator_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.10.15 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking. The CRC16 module signature is based on the CRC-CCITT standard.

6.10.16 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

6.10.17 True Random Seed

The Device Descriptor (TLV) (see 6.12) contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

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6.10.18 Shared Reference (REF)

The REF module generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

6.10.19 Embedded Emulation

6.10.19.1 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.10.19.2 EnergyTrace++ Technology

The devices implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology allows you to observe information about the internal states of the microcontroller. These states include the CPU Program Counter (PC), the ON or OFF status of the peripherals and the system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

The activity of the following modules can be observed:

- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REFBG or REFGEN active and BG in static mode.
- COMP is on.
- AES is encrypting or decrypting.
- eUSCI_A0 is transferring (receiving or transmitting) data.
- eUSCI_A1 is transferring (receiving or transmitting) data.
- eUSCI_B0 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.

6.10.20 Peripheral File Map

表 6-20 lists the base address for each peripheral. For complete module register descriptions, see the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

表 6-20. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see 表 6-21)	0100h	000h to 01Fh
PMM (see 表 6-22)	0120h	000h to 01Fh
FRAM Control (see 表 6-23)	0140h	000h to 00Fh
CRC16 (see 表 6-24)	0150h	000h to 007h
Watchdog (see 表 6-25)	015Ch	000h to 001h
CS (see 表 6-26)	0160h	000h to 00Fh
SYS (see 表 6-27)	0180h	000h to 01Fh
Shared Reference (see 表 6-28)	01B0h	000h to 001h
Port P1, P2 (see 表 6-29)	0200h	000h to 01Fh
Port P3, P4 (see 表 6-30)	0220h	000h to 01Fh
Port PJ (see 表 6-31)	0320h	000h to 01Fh
TA0 (see 表 6-32)	0340h	000h to 02Fh
TA1 (see 表 6-33)	0380h	000h to 02Fh
TB0 (see 表 6-34)	03C0h	000h to 02Fh
TA2 (see 表 6-35)	0400h	000h to 02Fh
Capacitive Touch I/O 0 (see 表 6-36)	0430h	000h to 00Fh
TA3 (see 表 6-37)	0440h	000h to 02Fh
Capacitive Touch I/O 1 (see 表 6-38)	0470h	000h to 00Fh
Real-Time Clock (RTC_B) (see 表 6-39)	04A0h	000h to 01Fh
32-Bit Hardware Multiplier (see 表 6-40)	04C0h	000h to 02Fh
DMA General Control (see 表 6-41)	0500h	000h to 00Fh
DMA Channel 0 (see 表 6-41)	0510h	000h to 00Fh
DMA Channel 1 (see 表 6-41)	0520h	000h to 00Fh
DMA Channel 2 (see 表 6-41)	0530h	000h to 00Fh
MPU Control (see 表 6-42)	05A0h	000h to 00Fh
eUSCI_A0 (see 表 6-43)	05C0h	000h to 01Fh
eUSCI_A1 (see 表 6-44)	05E0h	000h to 01Fh
eUSCI_B0 (see 表 6-45)	0640h	000h to 02Fh
ADC12_B (see 表 6-46)	0800h	000h to 09Fh
Comparator_E (see 表 6-47)	08C0h	000h to 00Fh
AES (see 表 6-48)	09C0h	000h to 00Fh

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表 6-21. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

表 6-22. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

表 6-23. FRAM Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

表 6-24. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

表 6-25. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

表 6-26. CS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch

表 6-27. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh

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表 6-27. SYS Registers (Base Address: 0180h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

表 6-28. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

表 6-29. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

表 6-30. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 selection 0	P3SEL0	0Ah
Port P3 selection 1	P3SEL1	0Ch
Port P3 interrupt vector word	P3IV	0Eh
Port P3 complement selection	P3SELC	16h
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch

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表 6-30. Port P3, P4 Registers (Base Address: 0220h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh
Port P4 selection 1	P4SEL1	0Dh
Port P4 complement selection	P4SELC	17h
Port P4 interrupt vector word	P4IV	1Eh
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

表 6-31. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ selection 0	PJSEL0	0Ah
Port PJ selection 1	PJSEL1	0Ch
Port PJ complement selection	PJSELC	16h

表 6-32. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
Capture/compare 3	TA0CCR3	18h
Capture/compare 4	TA0CCR4	1Ah
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

表 6-33. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h

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表 6-33. TA1 Registers (Base Address: 0380h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

表 6-34. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

表 6-35. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

表 6-36. Capacitive Touch I/O 0 Registers (Base Address: 0430h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch I/O 0 control	CAPTIO0CTL	0Eh

表 6-37. TA3 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA3 control	TA3CTL	00h
Capture/compare control 0	TA3CCTL0	02h

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表 6-37. TA3 Registers (Base Address: 0440h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capture/compare control 1	TA3CCTL1	04h
TA3 counter	TA3R	10h
Capture/compare 0	TA3CCR0	12h
Capture/compare 1	TA3CCR1	14h
TA3 expansion 0	TA3EX0	20h
TA3 interrupt vector	TA3IV	2Eh

表 6-38. Capacitive Touch I/O 1 Registers (Base Address: 0470h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive touch I/O 1 control	CAPTIO1CTL	0Eh

表 6-39. RTC_B Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds	RTCSEC/RTCNT1	10h
RTC minutes	RTCMIN/RTCNT2	11h
RTC hours	RTCHOUR/RTCNT3	12h
RTC day of week	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion	BIN2BCD	1Ch
BCD-to-binary conversion	BCD2BIN	1Eh

表 6-40. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch

表 6-40. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

表 6-41. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

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表 6-42. MPU Control Registers (Base Address: 05A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
MPU control 0	MPUCTL0	00h
MPU control 1	MPUCTL1	02h
MPU segmentation border 2	MPUSEGB2	04h
MPU segmentation border 1	MPUSEGB1	06h
MPU access management	MPUSAM	08h
MPU IP control 0	MPUIPC0	0Ah
MPU IP encapsulation segment border 2	MPUIPSEGB2	0Ch
MPU IP encapsulation segment border 1	MPUIPSEGB1	0Eh

表 6-43. eUSCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI _A control word 1	UCA0CTLW1	02h
eUSCI_A baud rate 0	UCA0BR0	06h
eUSCI_A baud rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status word	UCA0STATW	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	UCA0IRTCTL	12h
eUSCI_A IrDA receive control	UCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

表 6-44. eUSCI_A1 Registers (Base Address:05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI _A control word 1	UCA1CTLW1	02h
eUSCI_A baud rate 0	UCA1BR0	06h
eUSCI_A baud rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status word	UCA1STATW	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	UCA1IRTCTL	12h
eUSCI_A IrDA receive control	UCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

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表 6-45. eUSCI_B0 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B received address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI I2C slave address	UCB0I2CSA	20h
eUSCI interrupt enable	UCB0IE	2Ah
eUSCI interrupt flags	UCB0IFG	2Ch
eUSCI interrupt vector word	UCB0IV	2Eh

表 6-46. ADC12_B Registers (Base Address: 0800h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B control 0	ADC12CTL0	00h
ADC12_B control 1	ADC12CTL1	02h
ADC12_B control 2	ADC12CTL2	04h
ADC12_B control 3	ADC12CTL3	06h
ADC12_B window comparator low threshold	ADC12LO	08h
ADC12_B window comparator high threshold	ADC12HI	0Ah
ADC12_B interrupt flag 0	ADC12IFGR0	0Ch
ADC12_B interrupt flag 1	ADC12IFGR1	0Eh
ADC12_B interrupt flag 2	ADC12IFGR2	10h
ADC12_B interrupt enable 0	ADC12IER0	12h
ADC12_B interrupt enable 1	ADC12IER1	14h
ADC12_B interrupt enable 2	ADC12IER2	16h
ADC12_B interrupt vector	ADC12IV	18h
ADC12_B memory control 0	ADC12MCTL0	20h
ADC12_B memory control 1	ADC12MCTL1	22h
ADC12_B memory control 2	ADC12MCTL2	24h
ADC12_B memory control 3	ADC12MCTL3	26h
ADC12_B memory control 4	ADC12MCTL4	28h
ADC12_B memory control 5	ADC12MCTL5	2Ah
ADC12_B memory control 6	ADC12MCTL6	2Ch
ADC12_B memory control 7	ADC12MCTL7	2Eh
ADC12_B memory control 8	ADC12MCTL8	30h
ADC12_B memory control 9	ADC12MCTL9	32h
ADC12_B memory control 10	ADC12MCTL10	34h
ADC12_B memory control 11	ADC12MCTL11	36h
ADC12_B memory control 12	ADC12MCTL12	38h

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表 6-46. ADC12_B Registers (Base Address: 0800h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B memory control 13	ADC12MCTL13	3Ah
ADC12_B memory control 14	ADC12MCTL14	3Ch
ADC12_B memory control 15	ADC12MCTL15	3Eh
ADC12_B memory control 16	ADC12MCTL16	40h
ADC12_B memory control 17	ADC12MCTL17	42h
ADC12_B memory control 18	ADC12MCTL18	44h
ADC12_B memory control 19	ADC12MCTL19	46h
ADC12_B memory control 20	ADC12MCTL20	48h
ADC12_B memory control 21	ADC12MCTL21	4Ah
ADC12_B memory control 22	ADC12MCTL22	4Ch
ADC12_B memory control 23	ADC12MCTL23	4Eh
ADC12_B memory control 24	ADC12MCTL24	50h
ADC12_B memory control 25	ADC12MCTL25	52h
ADC12_B memory control 26	ADC12MCTL26	54h
ADC12_B memory control 27	ADC12MCTL27	56h
ADC12_B memory control 28	ADC12MCTL28	58h
ADC12_B memory control 29	ADC12MCTL29	5Ah
ADC12_B memory control 30	ADC12MCTL30	5Ch
ADC12_B memory control 31	ADC12MCTL31	5Eh
ADC12_B memory 0	ADC12MEM0	60h
ADC12_B memory 1	ADC12MEM1	62h
ADC12_B memory 2	ADC12MEM2	64h
ADC12_B memory 3	ADC12MEM3	66h
ADC12_B memory 4	ADC12MEM4	68h
ADC12_B memory 5	ADC12MEM5	6Ah
ADC12_B memory 6	ADC12MEM6	6Ch
ADC12_B memory 7	ADC12MEM7	6Eh
ADC12_B memory 8	ADC12MEM8	70h
ADC12_B memory 9	ADC12MEM9	72h
ADC12_B memory 10	ADC12MEM10	74h
ADC12_B memory 11	ADC12MEM11	76h
ADC12_B memory 12	ADC12MEM12	78h
ADC12_B memory 13	ADC12MEM13	7Ah
ADC12_B memory 14	ADC12MEM14	7Ch
ADC12_B memory 15	ADC12MEM15	7Eh
ADC12_B memory 16	ADC12MEM16	80h
ADC12_B memory 17	ADC12MEM17	82h
ADC12_B memory 18	ADC12MEM18	84h
ADC12_B memory 19	ADC12MEM19	86h
ADC12_B memory 20	ADC12MEM20	88h
ADC12_B memory 21	ADC12MEM21	8Ah
ADC12_B memory 22	ADC12MEM22	8Ch
ADC12_B memory 23	ADC12MEM23	8Eh
ADC12_B memory 24	ADC12MEM24	90h
ADC12_B memory 25	ADC12MEM25	92h
ADC12_B memory 26	ADC12MEM26	94h
ADC12_B memory 27	ADC12MEM27	96h

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表 6-46. ADC12_B Registers (Base Address: 0800h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B memory 28	ADC12MEM28	98h
ADC12_B memory 29	ADC12MEM29	9Ah
ADC12_B memory 30	ADC12MEM30	9Ch
ADC12_B memory 31	ADC12MEM31	9Eh

表 6-47. Comparator_E Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator_E control 0	CECTL0	00h
Comparator_E control 1	CECTL1	02h
Comparator_E control 2	CECTL2	04h
Comparator_E control 3	CECTL3	06h
Comparator_E interrupt	CEINT	0Ch
Comparator_E interrupt vector word	CEIV	0Eh

表 6-48. AES Accelerator Registers (Base Address: 09C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
AES accelerator control 0	AESACTL0	00h
AES accelerator control 1	AESACTL1	02h
AES accelerator status	AESASTAT	04h
AES accelerator key	AESAKEY	06h
AES accelerator data in	AESADIN	008h
AES accelerator data out	AESADOUT	00Ah
AES accelerator XORed data in	AESAXDIN	00Ch
AES accelerator XORed data in (no trigger)	AESAXIN	00Eh

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6.11 Input/Output Diagrams

6.11.1 Capacitive Touch Functionality Ports P1, P2, P3, P4, and PJ

All port pins provide the Capacitive Touch I/O functionality as shown in 図 6-2. The Capacitive Touch I/O functionality is controlled using the Capacitive Touch I/O control registers CAPTIO0CTL and CAPTIO1CTL as described in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*. The Capacitive Touch I/O functionality is not shown in the individual pin diagrams in the following sections.

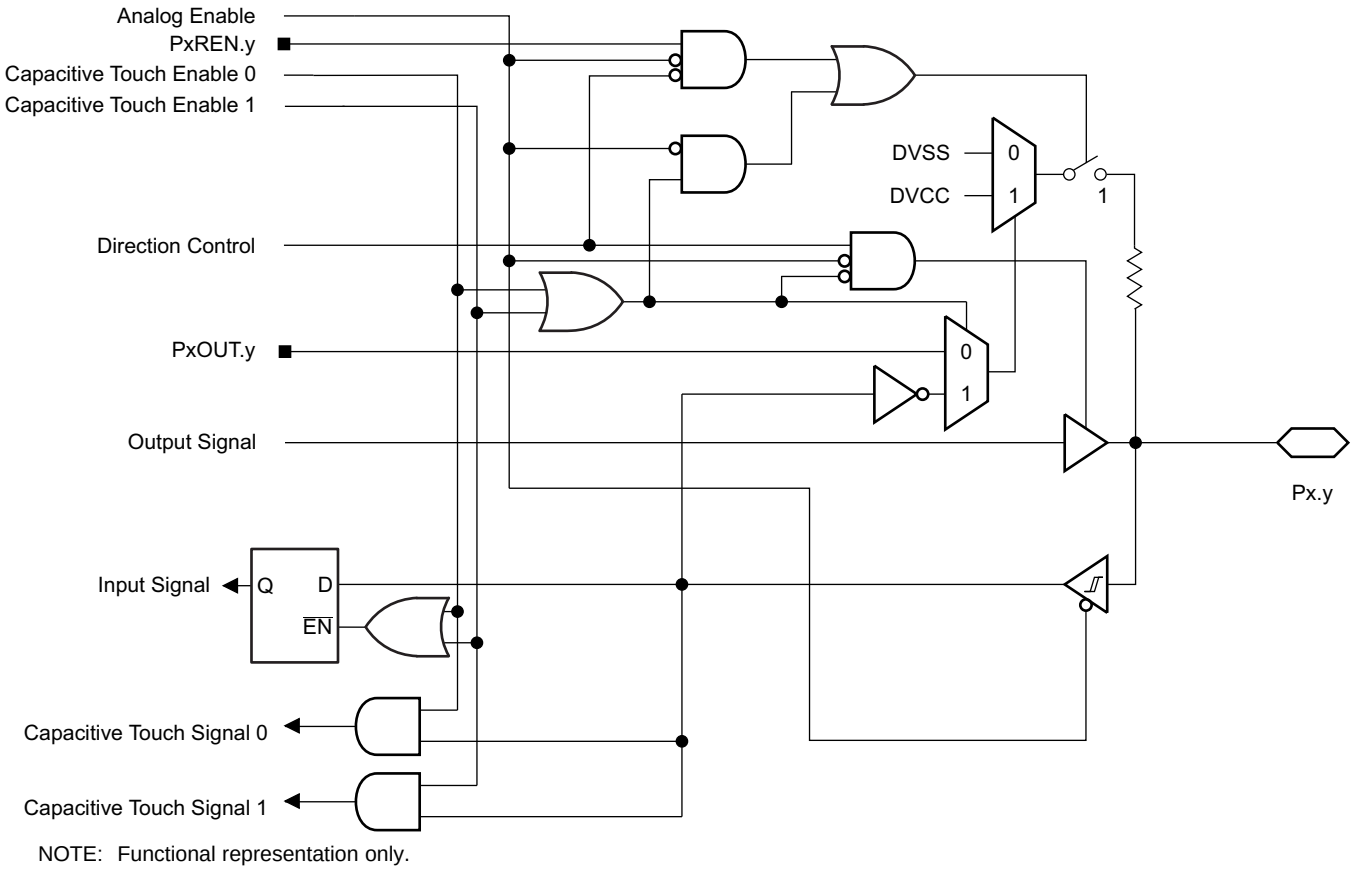
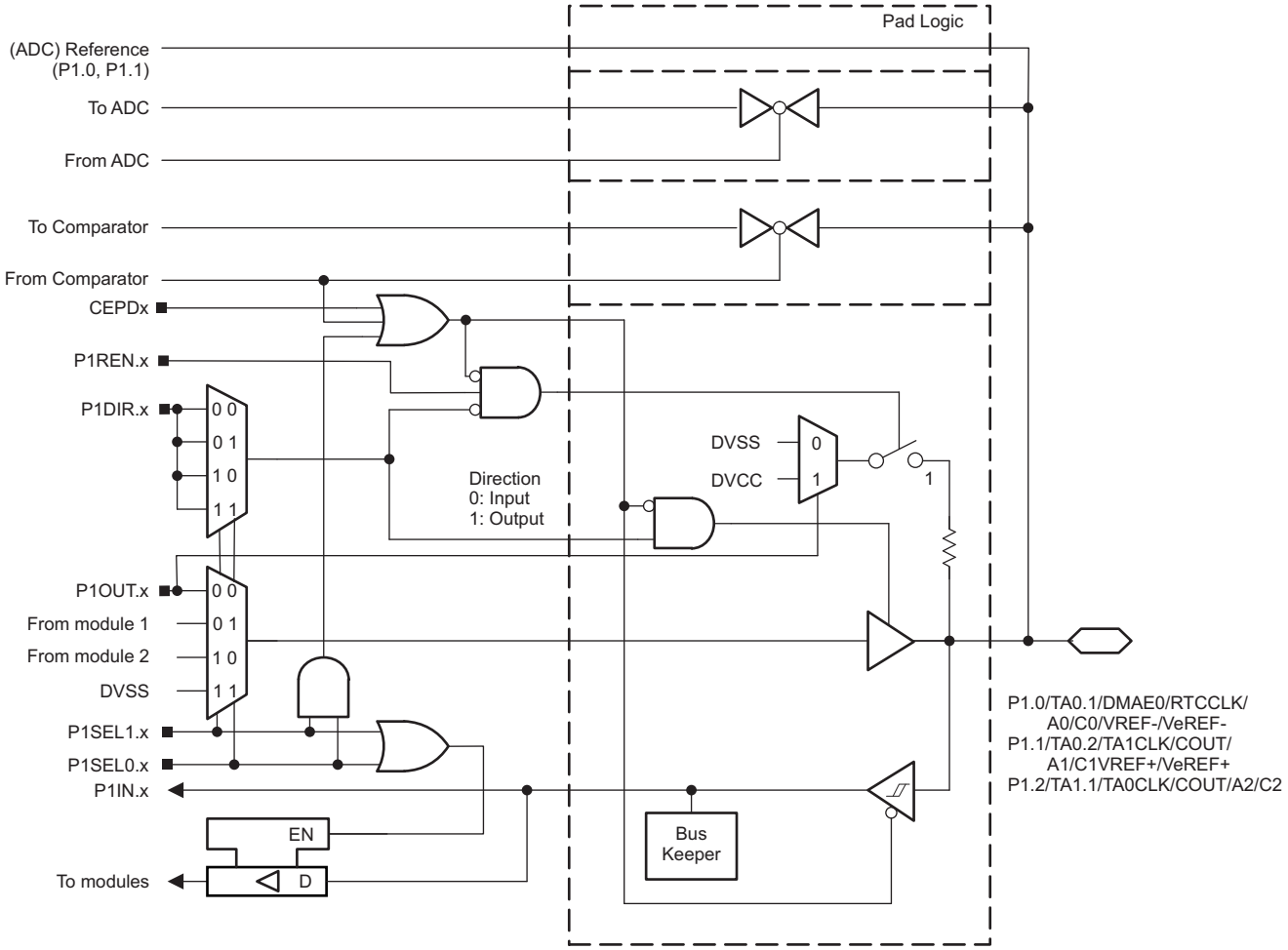


図 6-2. Capacitive Touch Diagram

6.11.2 Port P1 (P1.0 to P1.2) Input/Output With Schmitt Trigger

図 6-3 shows the port diagram. 表 6-49 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-3. Port P1 (P1.0 to P1.2) Diagram

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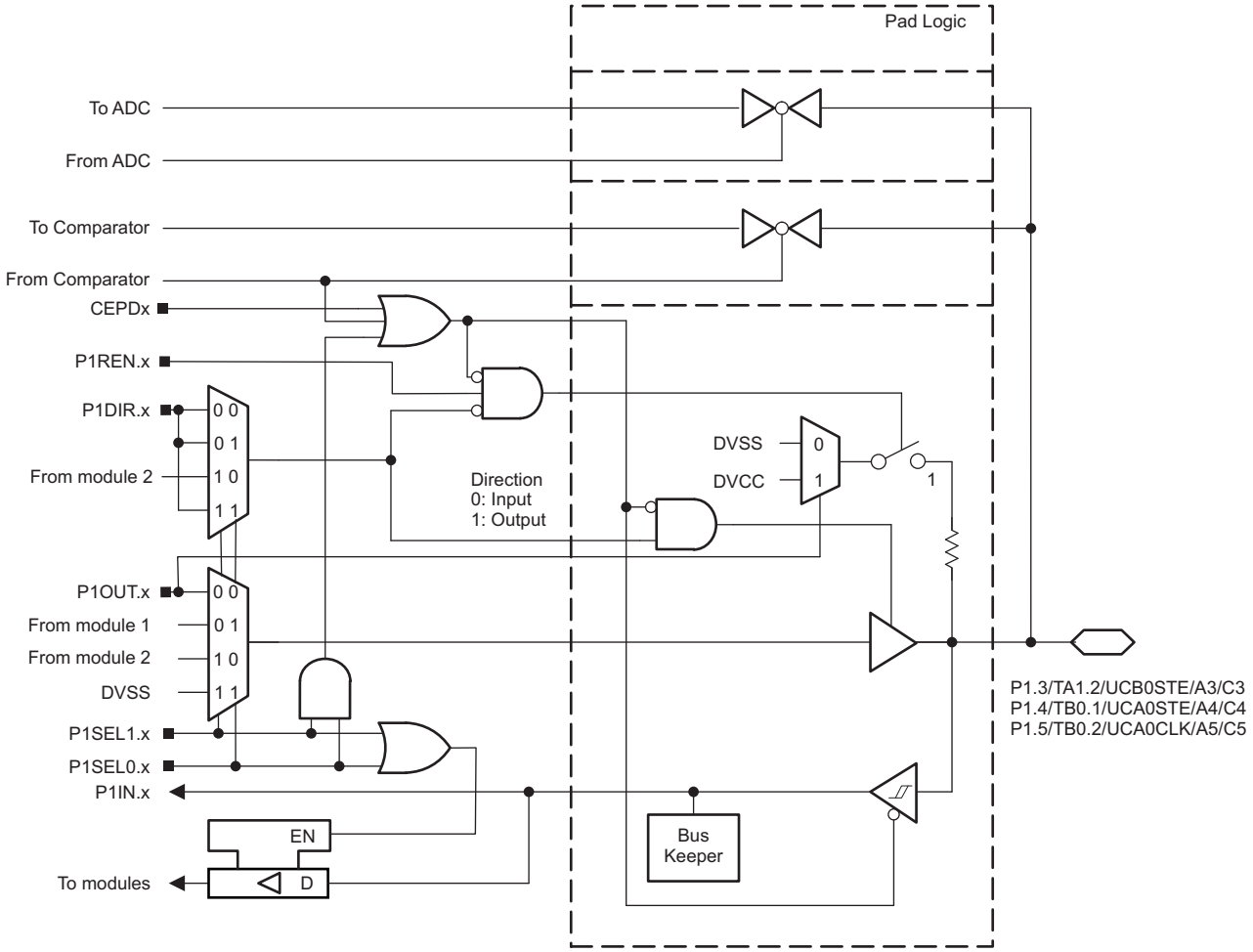
表 6-49. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/ VREF-/VeREF-	0	P1.0 (I/O)	I: 0; O: 1	0	0
		TA0.CCI1A	0	0	1
		TA0.1	1		
		DMAE0	0	1	0
		RTCCLK[2][3]	1		
		A0, C0, VREF-, VeREF-[4][5]	X	1	1
P1.1/TA0.2/TA1CLK/COUT/A1/C1/ VREF+/VeREF+	1	P1.1 (I/O)	I: 0; O: 1	0	0
		TA0.CCI2A	0	0	1
		TA0.2	1		
		TA1CLK	0	1	0
		COUT[6]	1		
		A1, C1, VREF+, VeREF+[4][5]	X	1	1
P1.2/TA1.1/TA0CLK/COUT/A2/C2	2	P1.2 (I/O)	I: 0; O: 1	0	0
		TA1.CCI1A	0	0	1
		TA1.1	1		
		TA0CLK	0	1	0
		COUT[7]	1		
		A2, C2[4][5]	X	1	1

(1) X = Don't care
(2) Not available on MSP430FR5x5x devices
(3) Do not use this pin as RTCCLK output if the DMAE0 functionality is used on any other pin. Select an alternative RTCCLK output pin.
(4) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.
(6) Do not use this pin as COUT output if the TA1CLK functionality is used on any other pin. Select an alternative COUT output pin.
(7) Do not use this pin as COUT output if the TA0CLK functionality is used on any other pin. Select an alternative COUT output pin.

6.11.3 Port P1 (P1.3 to P1.5) Input/Output With Schmitt Trigger

図 6-4 shows the port diagram. 表 6-50 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-4. Port P1 (P1.3 to P1.5) Diagram

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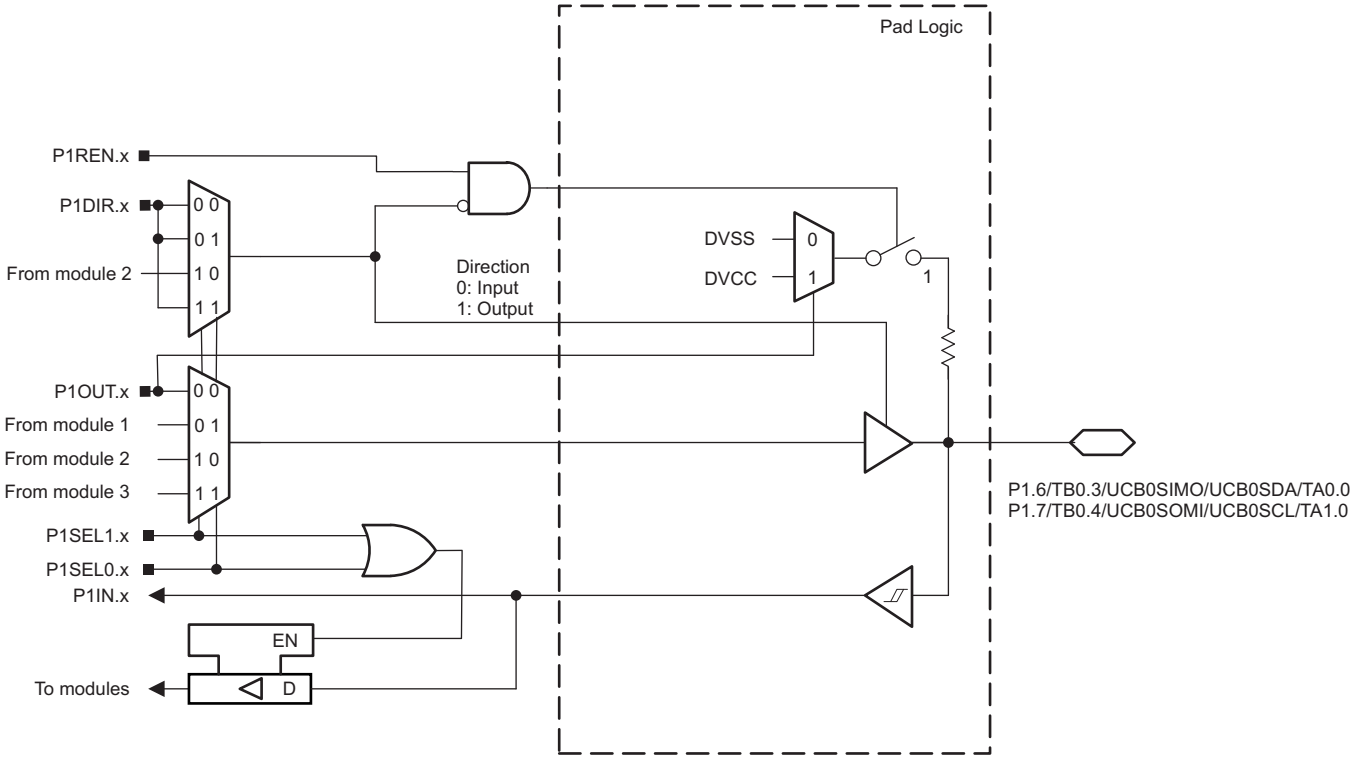
表 6-50. Port P1 (P1.3 to P1.5) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.3/TA1.2/UCB0STE/A3/C3	3	P1.3 (I/O)	I: 0; O: 1	0	0
		TA1.CCI2A	0	0	1
		TA1.2	1		
		UCB0STE	X[2]	1	0
		A3, C3[3][4]	X	1	1
P1.4/TB0.1/UCA0STE/A4/C4	4	P1.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI1A	0	0	1
		TB0.1	1		
		UCA0STE	X[5]	1	0
		A4, C4[3][4]	X	1	1
P1.5/TB0.2/UCA0CLK/A5/C5	5	P1.5(I/O)	I: 0; O: 1	0	0
		TB0.CCI2A	0	0	1
		TB0.2	1		
		UCA0CLK	X[5]	1	0
		A5, C5[3][4]	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B0 module.
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.
(5) Direction controlled by eUSCI_A0 module.

6.11.4 Port P1 (P1.6 and P1.7) Input/Output With Schmitt Trigger

図 6-5 shows the port diagram. 表 6-51 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-5. Port P1 (P1.6 and P1.7) Diagram

表 6-51. Port P1 (P1.6 and P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[(1)]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.6/TB0.3/UCB0SIMO/UCB0SDA/ TA0.0	6	P1.6 (I/O)	I: 0; O: 1	0	0
		TB0.CCI3B	0	0	1
		TB0.3	1		
		UCB0SIMO/UCB0SDA	X[(2)]	1	0
		TA0.CCI0A	0	1	1
		TA0.0	1		
P1.7/TB0.4/UCB0SOMI/UCB0SCL/ TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0	0
		TB0.CCI4B	0	0	1
		TB0.4	1		
		UCB0SOMI/UCB0SCL	X[(3)]	1	0
		TA1.CCI0A	0	1	1
		TA1.0	1		

(1) X = Don't care
(2) Direction controlled by eUSCI_B0 module.
(3) Direction controlled by eUSCI_A0 module.

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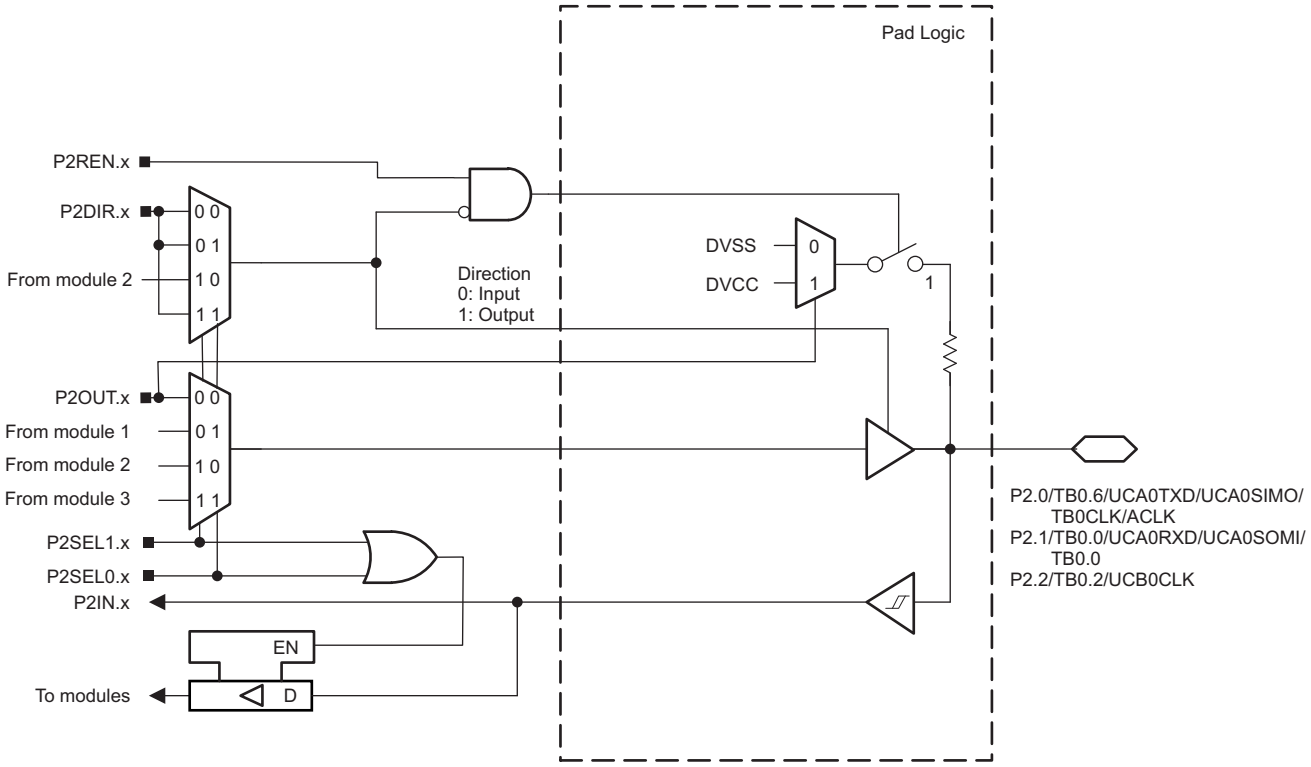
6.11.5 Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger

図 6-6 shows the port diagram. 表 6-52 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-6. Port P2 (P2.0 to P2.2) Diagram

表 6-52. Port P2 (P2.0 to P2.2) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.0/TB0.6/UCA0TXD/UCA0SIMO/ TB0CLK/ACLK	0	P2.0 (I/O)	I: 0; O: 1	0	0
		TB0.CCI6B	0	0	1
		TB0.6	1		
		UCA0TXD/UCA0SIMO	X[2]	1	0
		TB0CLK	0	1	1
		ACLK[3]	1		
P2.1/TB0.0/UCA0RXD/UCA0SOMI/ TB0.0	1	P2.1 (I/O)	I: 0; O: 1	0	0
		TB0.CCI0A	0	X	1
		TB0.0	1		
		UCA0RXD/UCA0SOMI	X[2]	1	0

(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) Do not use this pin as ACLK output if the TB0CLK functionality is used on any other pin. Select an alternative ACLK output pin.

表 6-52. Port P2 (P2.0 to P2.2) Pin Functions (continued)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.2/TB0.2/UCB0CLK	2	P2.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TB0.2	1		
		UCB0CLK	X [4]	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		

(4) Direction controlled by eUSCI_B0 module.

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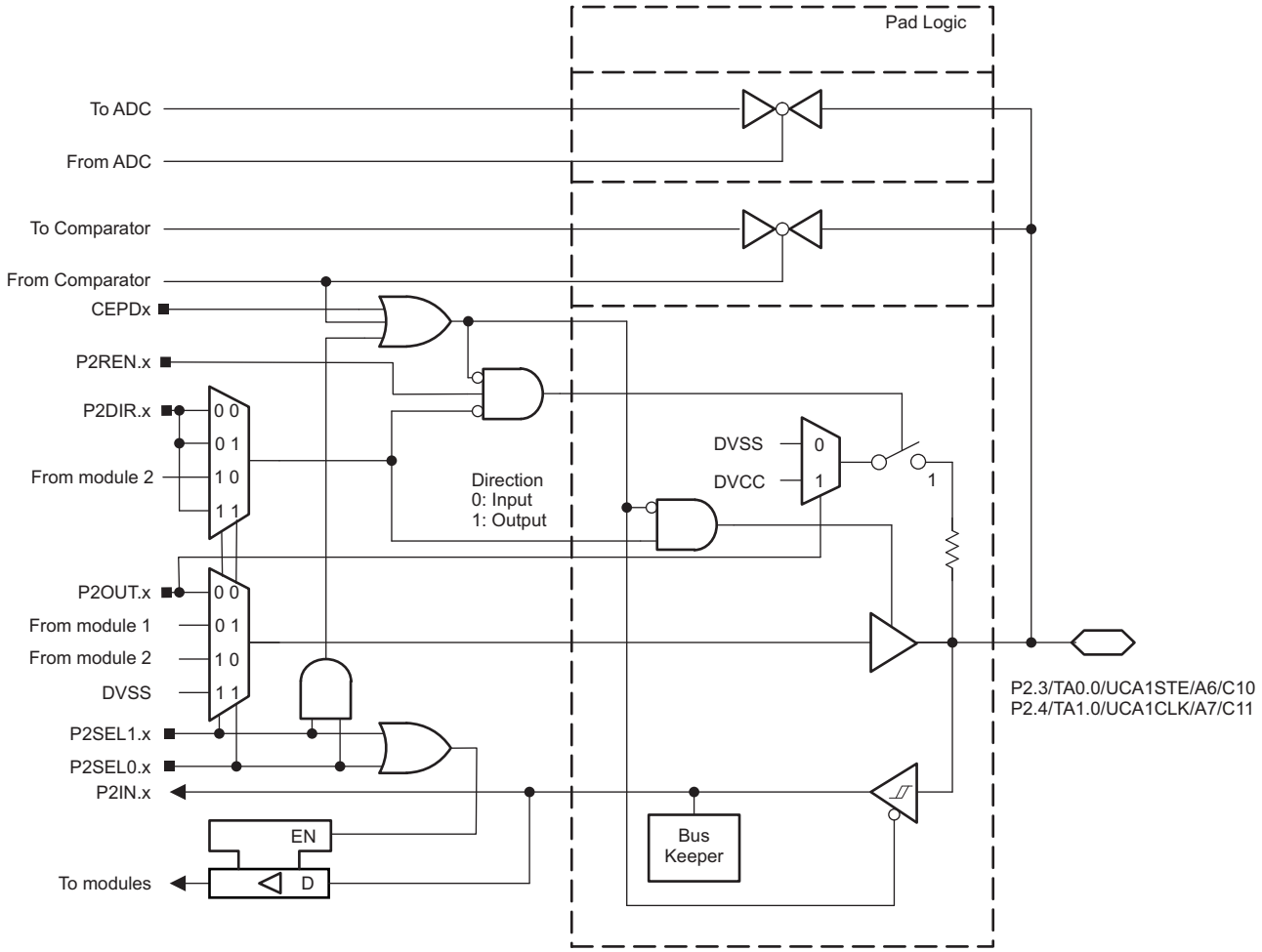
6.11.6 Port P2 (P2.3 and P2.4) Input/Output With Schmitt Trigger



NOTE: Functional representation only.

図 6-7. Port P2 (P2.3 and P2.4) Diagram

表 6-53. Port P2 (P2.3 and P2.4) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.3/TA0.0/UCA1STE/A6/C10	3	P2.3 (I/O)	I: 0; O: 1	0	0
		TA0.CCI0B	0	0	1
		TA0.0	1		
		UCA1STE	X [2]	1	0
		A6, C10[3][4]	X	1	1
P2.4/TA1.0/UCA1CLK/A7/C11	4	P2.4 (I/O)	I: 0; O: 1	0	0
		TA1.CCI0B	0	0	1
		TA1.0	1		
		UCA1CLK	X [2]	1	0
		A7, C11[3][4]	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

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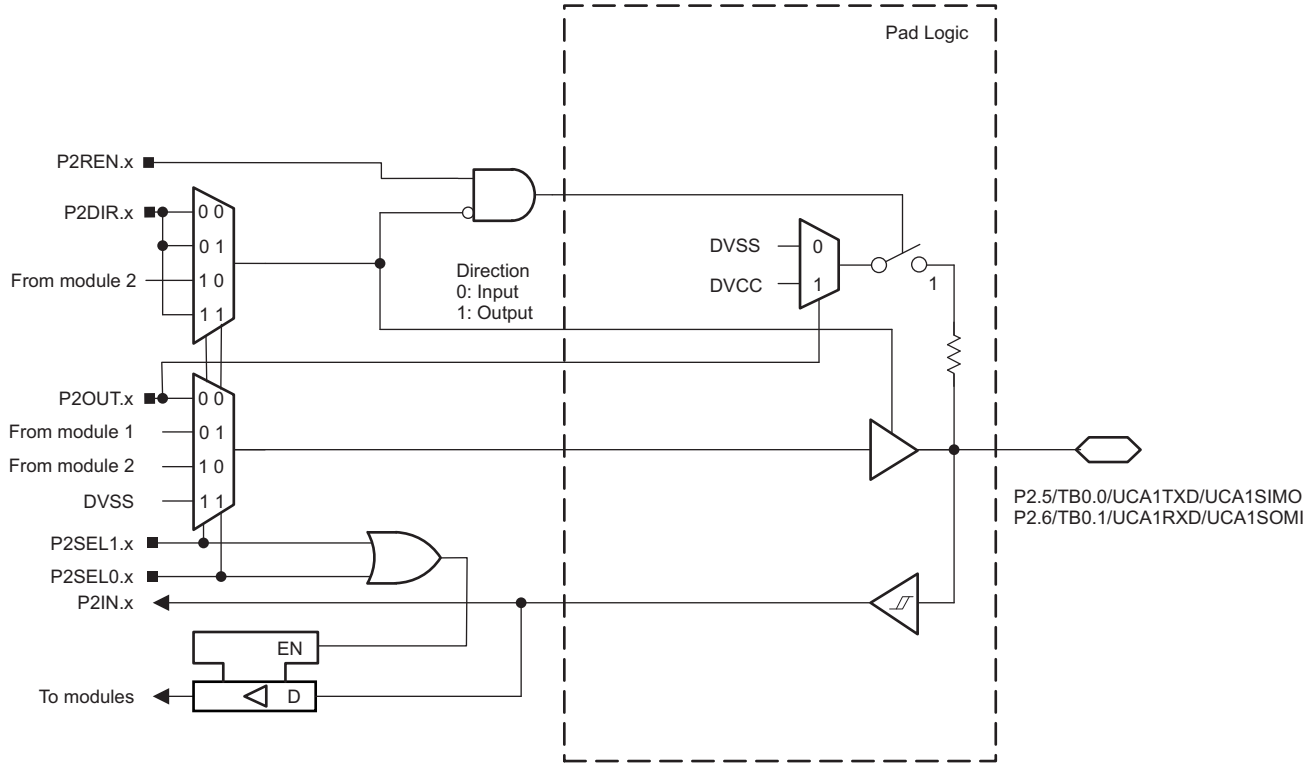
6.11.7 Port P2 (P2.5 and P2.6) Input/Output With Schmitt Trigger

図 6-8 shows the port diagram. 表 6-54 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-8. Port P2 (P2.5 and P2.6) Diagram

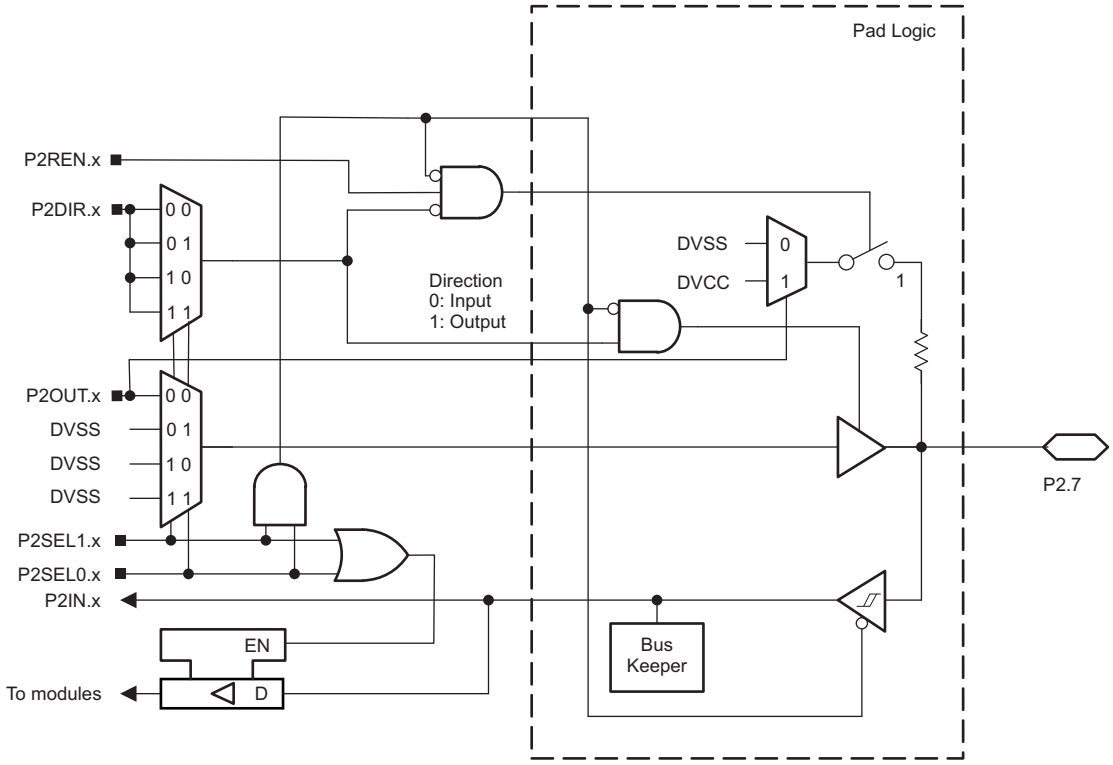
表 6-54. Port P2 (P2.5 and P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.5/TB0.0/UCA1TXD/UCA1SIMO	5	P2.5(I/O)	I: 0; O: 1	0	0
		TB0.CCI0B	0	0	1
		TB0.0	1		
		UCA1TXD/UCA1SIMO	X[2]	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		
P2.6/TB0.1/UCA1RXD/UCA1SOMI	6	P2.6(I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		TB0.1	1		
		UCA1RXD/UCA1SOMI	X[2]	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.

6.11.8 Port P2 (P2.7) Input/Output With Schmitt Trigger

図 6-9 shows the port diagram. 表 6-55 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-9. Port P2 (P2.7) Diagram

表 6-55. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[(1)]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.7	7	P2.7(I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		

(1) X = Don't care

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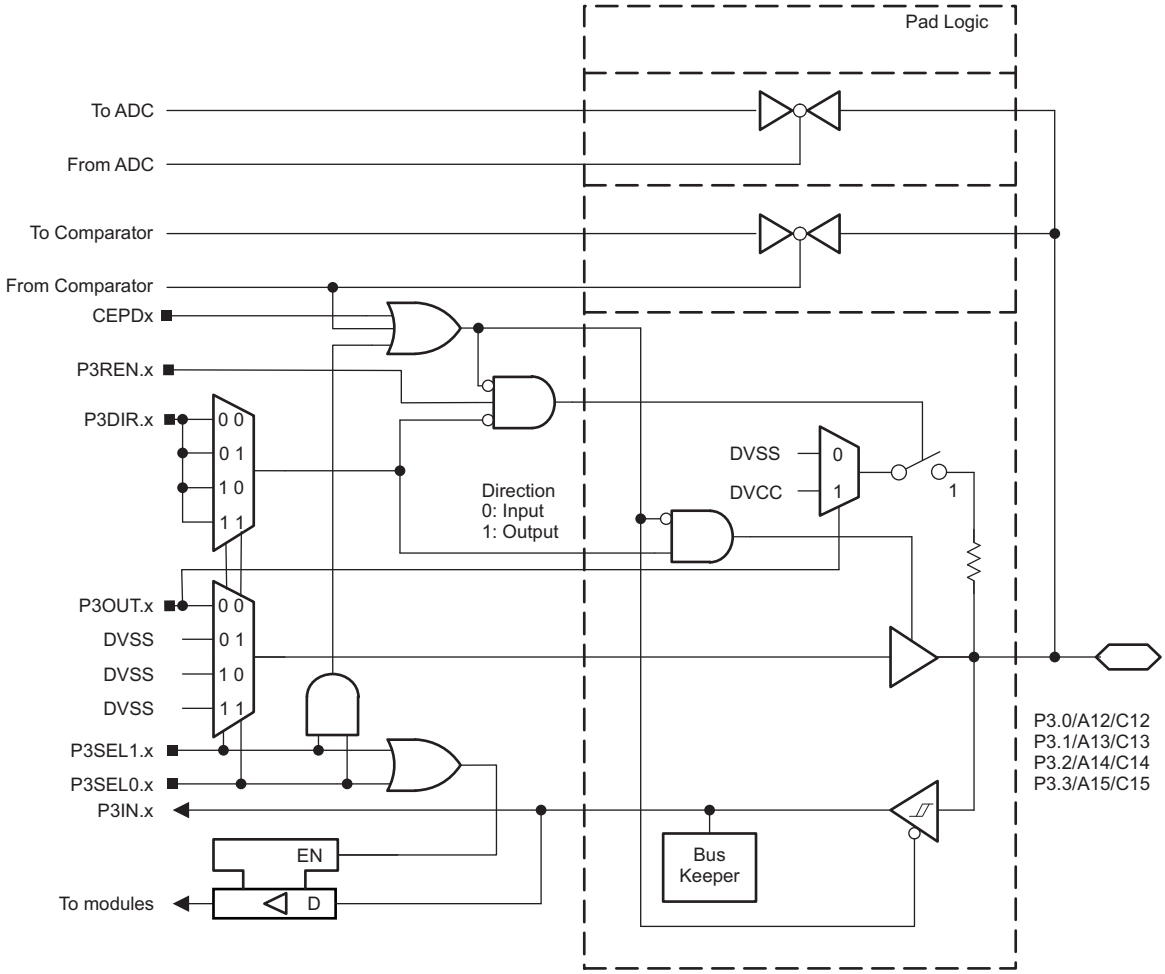
6.11.9 Port P3 (P3.0 to P3.3) Input/Output With Schmitt Trigger

図 6-10 shows the port diagram. 表 6-56 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-10. Port P3 (P3.0 to P3.3) Diagram

表 6-56. Port P3 (P3.0 to P3.3) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.0/A12/C12	0	P3.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A12/C12[2][3]	X	1	1
P3.1/A13/C13	1	P3.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A13/C13[2][3]	X	1	1
P3.2/A14/C14	2	P3.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A14/C14[2][3]	X	1	1
P3.3/A15/C15	3	P3.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A15/C15[2][3]	X	1	1

(1) X = Don't care
(2) Setting P3SEL1.x and P3SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

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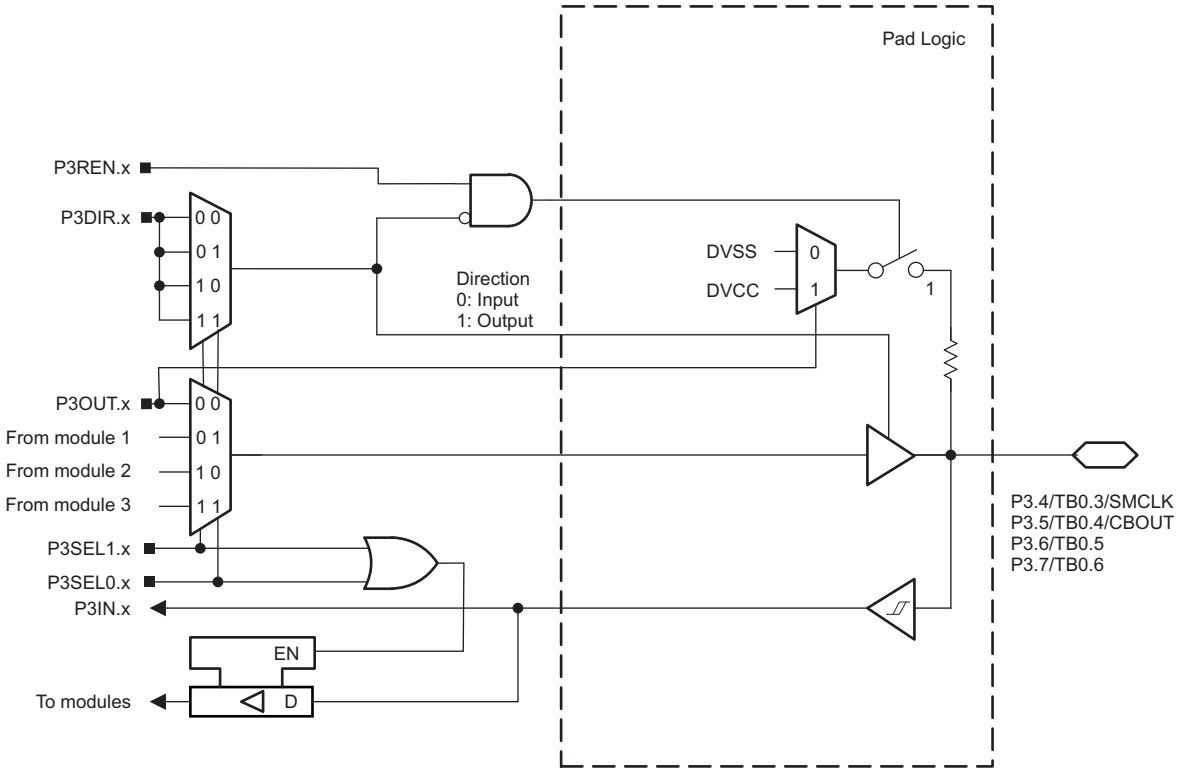
6.11.10 Port P3 (P3.4 to P3.7) Input/Output With Schmitt Trigger

図 6-11 shows the port diagram. 表 6-57 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-11. Port P3 (P3.4 to P3.7) Diagram

表 6-57. Port P3 (P3.4 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS (1)		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.4/TB0.3/SMCLK	4	P3.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI3A	0	0	1
		TB0.3	1		
		N/A	0	1	X
		SMCLK	1		
P3.5/TB0.4/COUT	5	P3.5 (I/O)	I: 0; O: 1	0	0
		TB0.CCI4A	0	0	1
		TB0.4	1		
		N/A	0	1	X
		COUT	1		
P3.6/TB0.5	6	P3.6 (I/O)	I: 0; O: 1	0	0
		TB0.CCI5A	0	0	1
		TB0.5	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P3.7/TB0.6	7	P3.7 (I/O)	I: 0; O: 1	0	0
		TB0.CCI6A	0	0	1
		TB0.6	1		
		N/A	0	1	X
		Internally tied to DVSS	1		

(1) X = Don't care

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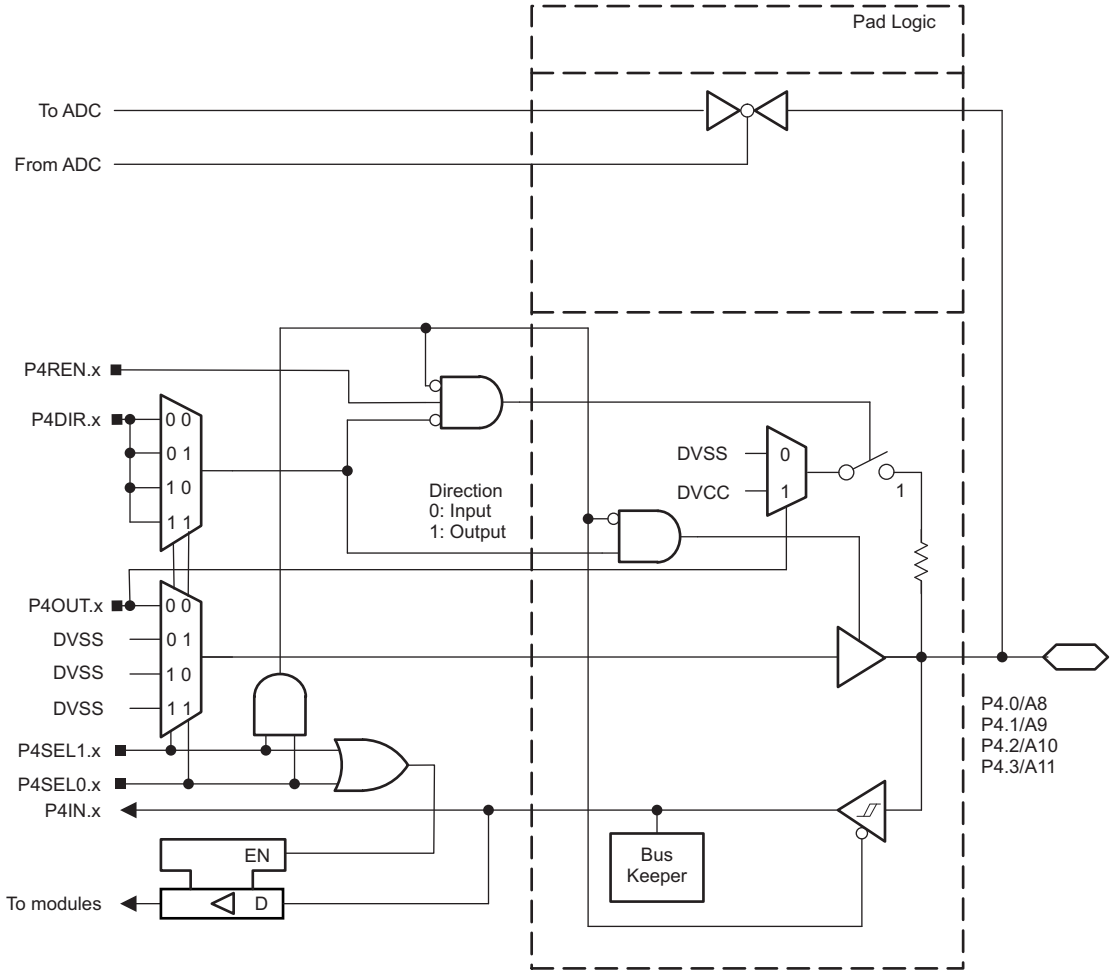
6.11.11 Port P4 (P4.0 to P4.3) Input/Output With Schmitt Trigger

図 6-12 shows the port diagram. 表 6-58 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-12. Port P4 (P4.0 to P4.3) Diagram

表 6-58. Port P4 (P4.0 to P4.3) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.0/A8	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A8[2]	X	1	1
P4.1/A9	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A9[2]	X	1	1
P4.2/A10	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A10[2]	X	1	1
P4.3/A11	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A11[2]	X	1	1

(1) X = Don't care
(2) Setting P4SEL1.x and P4SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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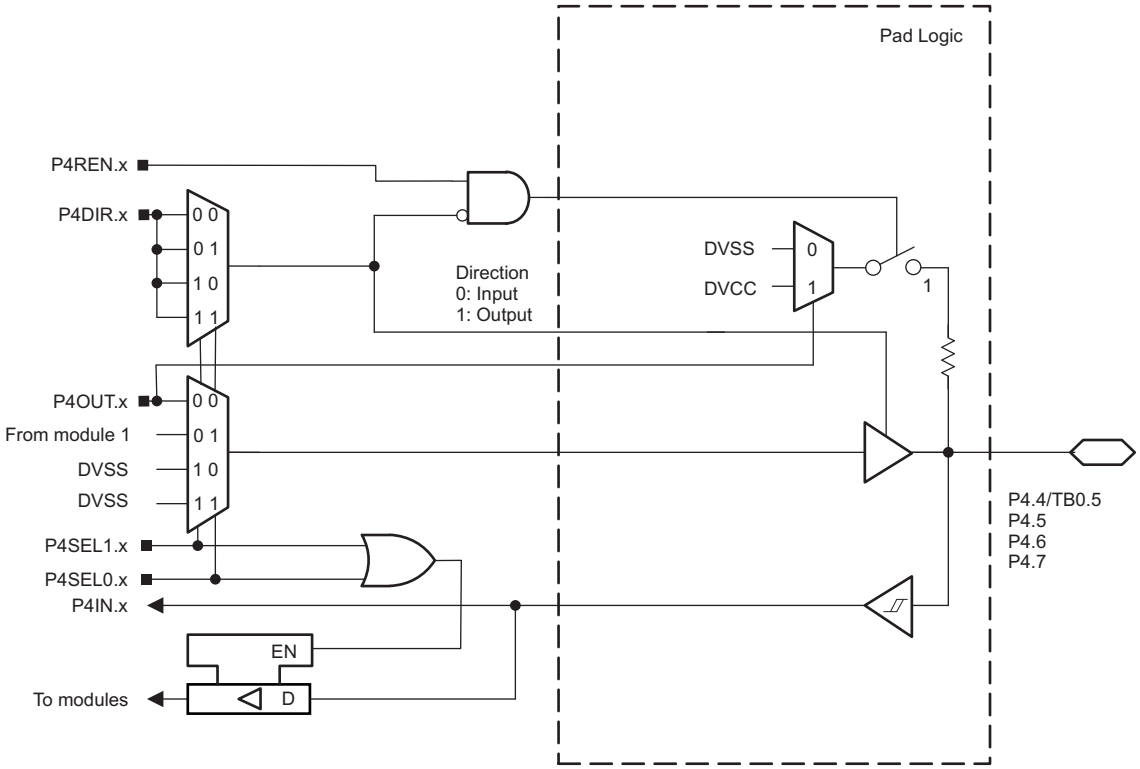
6.11.12 Port P4 (P4.4 to P4.7) Input/Output With Schmitt Trigger

図 6-13 shows the port diagram. 表 6-59 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-13. Port P4 (P4.4 to P4.7) Diagram

表 6-59. Port P4 (P4.4 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[(1)]		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.4/TB0.5	4	P4.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI5B	0	0	1
		TB0.5	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P4.5	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P4.6	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		
P4.7	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	X
		Internally tied to DVSS	1		

(1) X = Don't care

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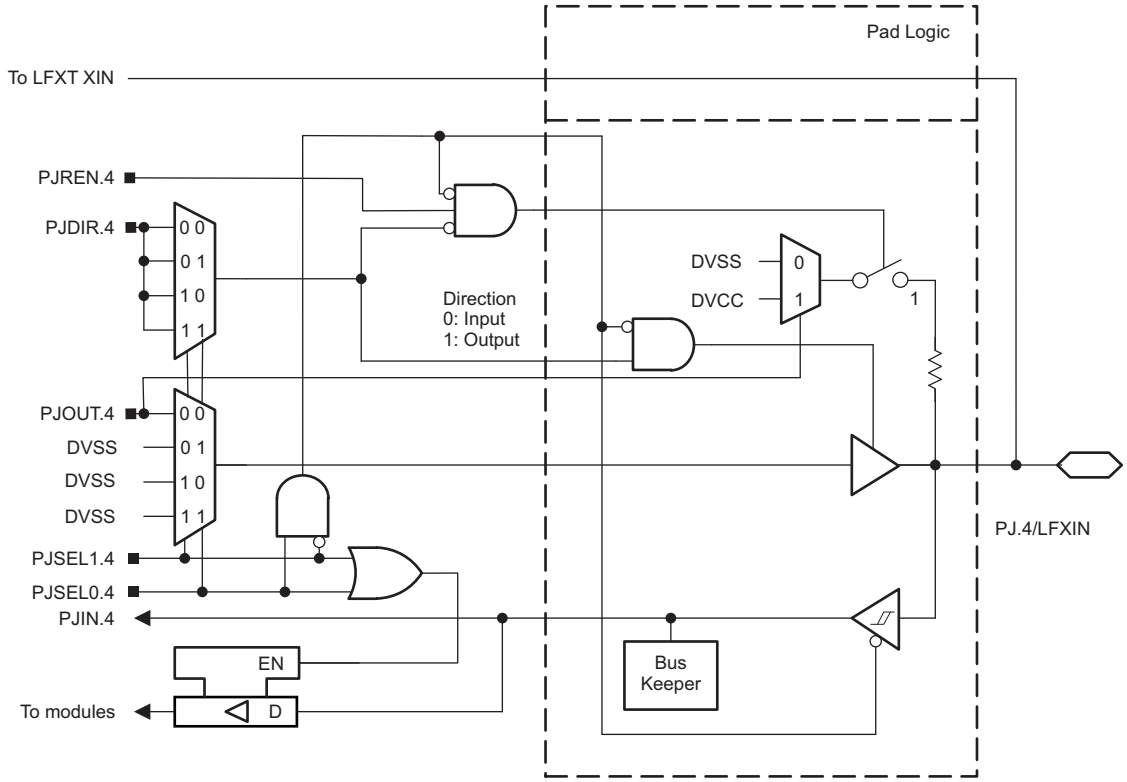
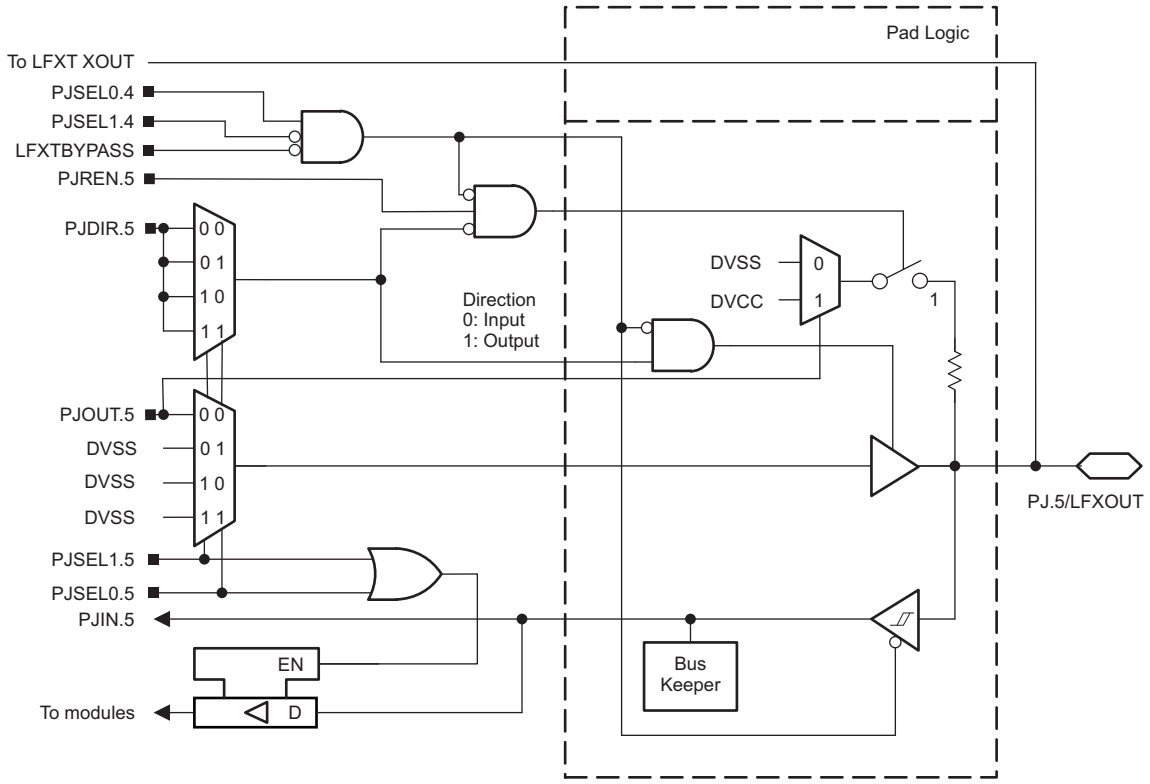
6.11.13 Port PJ, PJ.4 and PJ.5 Input/Output With Schmitt Trigger

図 6-14 and 図 6-15 show the port diagrams. 表 6-60 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-14. Port PJ (PJ.4) Diagram



NOTE: Functional representation only.

図 6-15. Port PJ (PJ.5) Diagram

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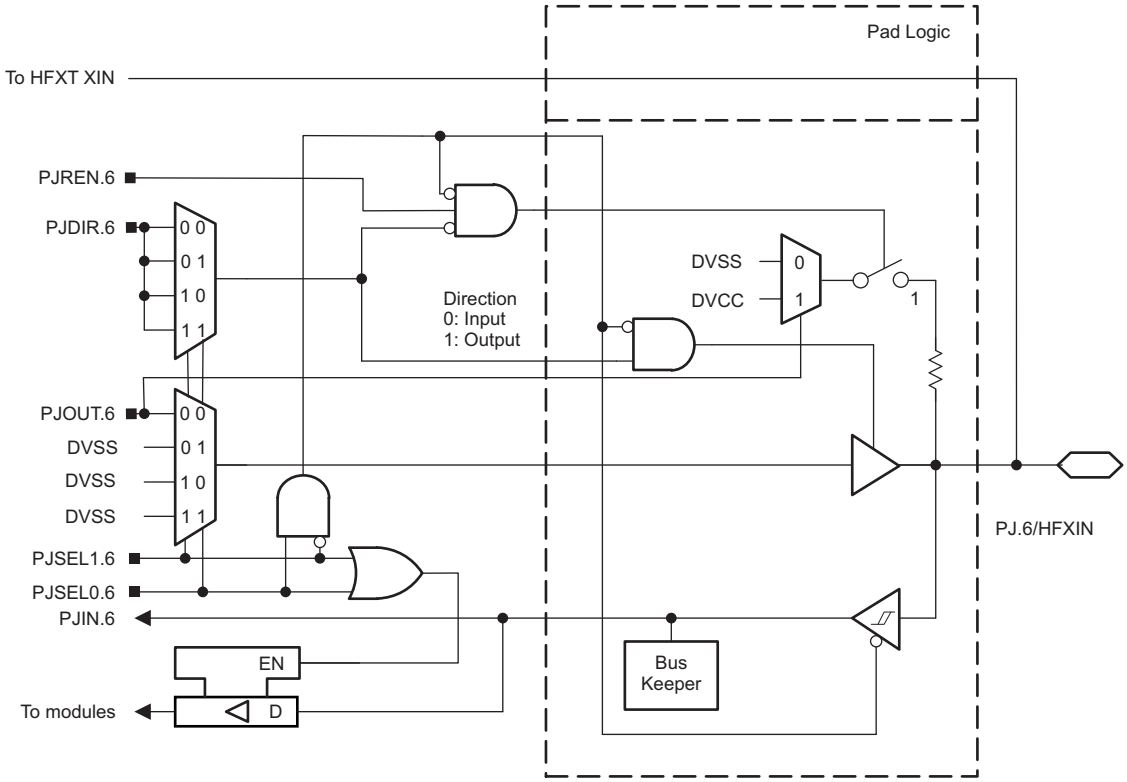
表 6-60. Port PJ (PJ.4 and PJ.5) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)					
			PJDIR.x	PJSEL1.5	PJSEL0.5	PJSEL1.4	PJSEL0.4	LFXT BYPASS
PJ.4/LFXIN	4	PJ.4 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		LFXIN crystal mode(2)	X	X	X	0	1	0
		LFXIN bypass mode(2)	X	X	X	0	1	1
PJ.5/LFXOUT	5	PJ.5 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1(3)
		N/A	0	see(4)	see(4)	0	0	0
						1	X	
						X	X	1(3)
		Internally tied to DVSS	1	see(4)	see(4)	0	0	0
						1	X	
						X	X	1(3)
		LFXOUT crystal mode(2)	X	X	X	0	1	0

(1) X = Don't care
(2) If PJSEL1.4 = 0 and PJSEL0.4 = 1, the general-purpose I/O is disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.
(4) If PJSEL0.5 = 1 or PJSEL1.5 = 1, the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

6.11.14 Port PJ (PJ.6 and PJ.7) Input/Output With Schmitt Trigger

図 6-16 and 図 6-17 show the port diagrams. 表 6-61 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-16. Port PJ (PJ.6) Diagram

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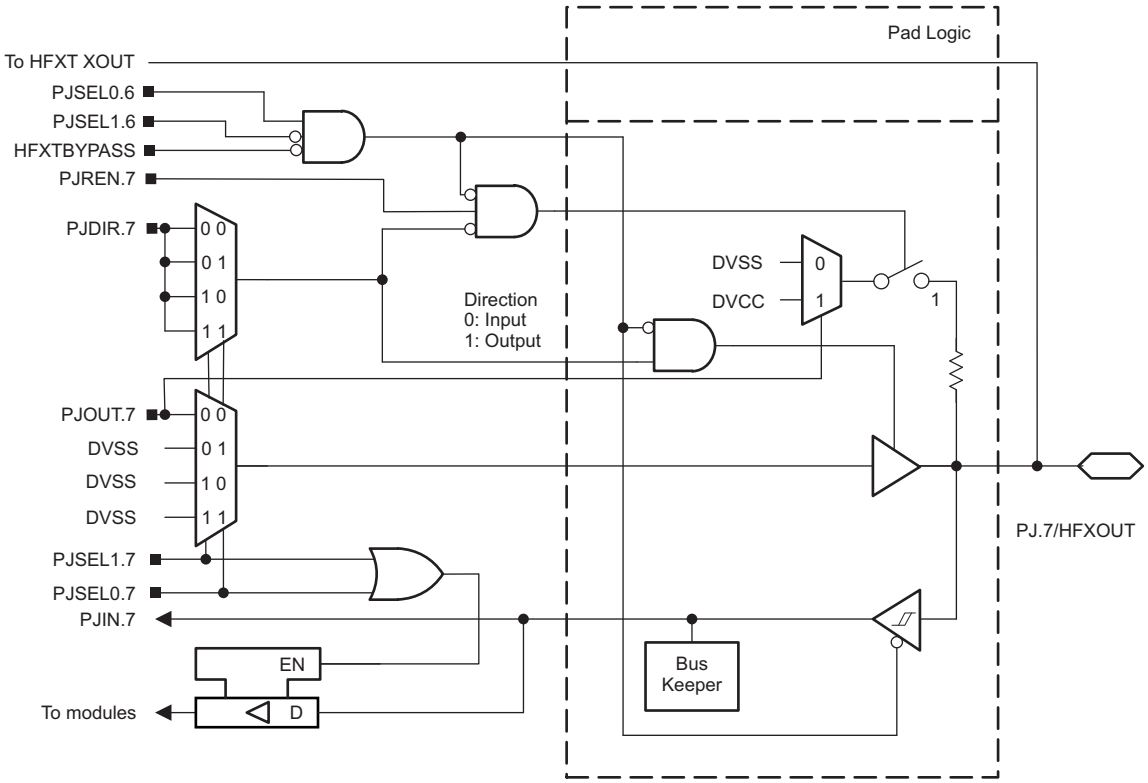

NOTE: Functional representation only.

図 6-17. Port PJ (PJ.7) Diagram

表 6-61. Port PJ (PJ.6 and PJ.7) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)					
			PJDIR.x	PJSEL1.7	PJSEL0.7	PJSEL1.6	PJSEL0.6	HFXT BYPASS
PJ.6/HFXIN	6	PJ.6 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		HFXIN crystal mode(2)	X	X	X	0	1	0
		HFXIN bypass mode(2)	X	X	X	0	1	1
PJ.7/HFXOUT	7	PJ.7 (I/O)(3)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1(4)
		N/A	0	see (3)	see (3)	0	0	0
						1	X	
						X	X	1(4)
		Internally tied to DVSS	1	see (3)	see (3)	0	0	0
						1	X	
						X	X	1(4)
		HFXOUT crystal mode(2)	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are do not care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation, and PJ.7 is configured as general-purpose I/O.
(3) With PJSEL0.7 = 1 or PJSEL1.7 = 1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.
(4) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.

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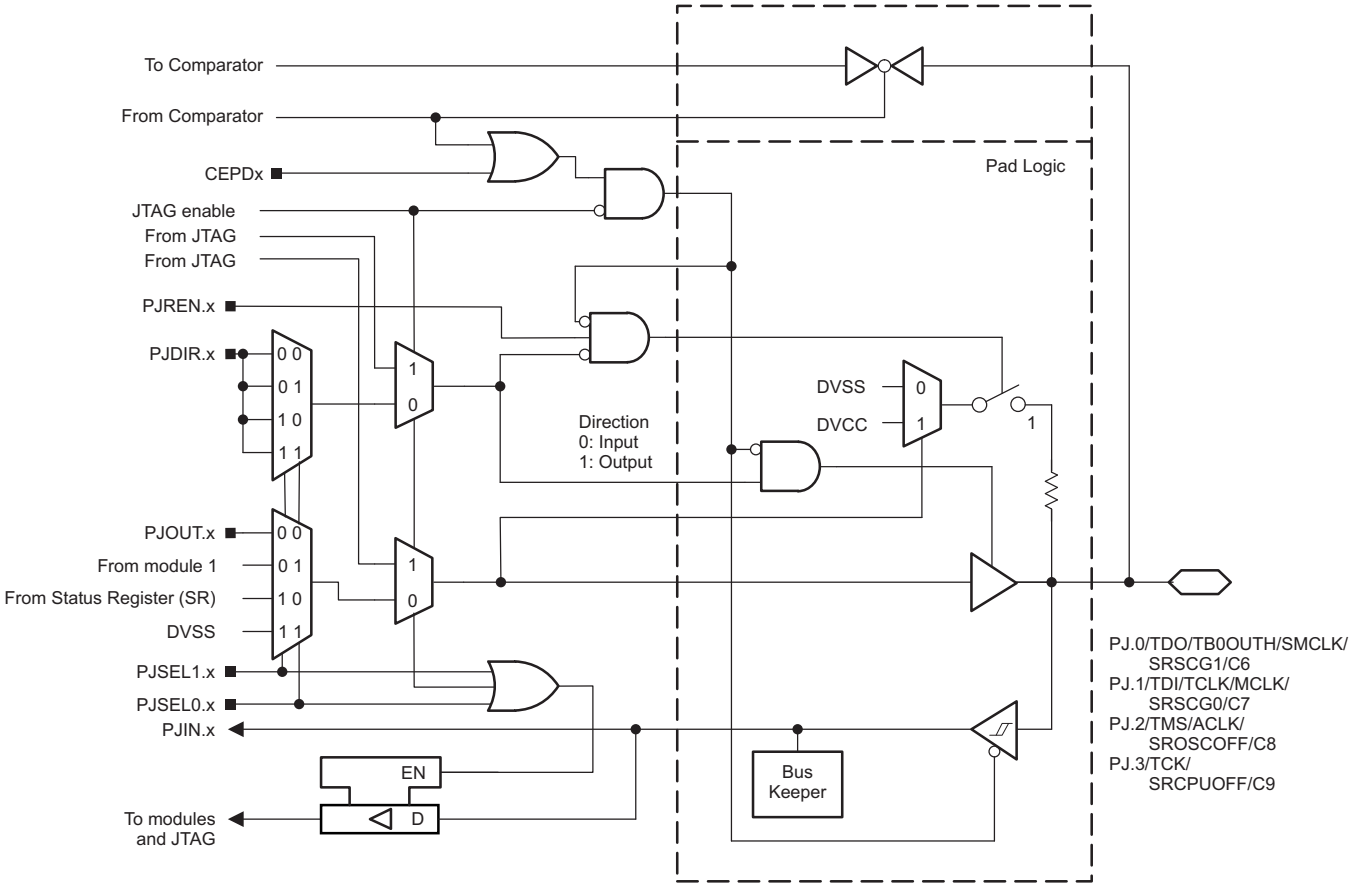
6.11.15 Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

図 6-18 shows the port diagram. 表 6-62 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-18. Port PJ (PJ.0 to PJ.3) Diagram

表 6-62. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[1]			
			PJDIR.x	PJSEL1.x	PJSEL0.x	CEPDx (Cx)
PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1/C6	0	PJ.0 (I/O)[2]	I: 0; O: 1	0	0	0
		TDO[3]	X	X	X	0
		TB0OUTH	0	0	1	0
		SMCLK[4]	1			
		N/A	0	1	0	0
		CPU Status Register Bit SCG1	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C6[5]	X	X	X	1
PJ.1/TDI/TCLK/MCLK/ SRSCG0/C7	1	PJ.1 (I/O)[2]	I: 0; O: 1	0	0	0
		TDI/TCLK[3] [6]	X	X	X	0
		N/A	0	0	1	0
		MCLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit SCG0	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C7[5]	X	X	X	1
PJ.2/TMS/ACLK/ SROSCOFF/C8	2	PJ.2 (I/O)[2]	I: 0; O: 1	0	0	0
		TMS[3] [6]	X	X	X	0
		N/A	0	0	1	0
		ACLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit OSCOFF	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C8[5]	X	X	X	1
PJ.3/TCK/SRCPUOFF/C9	3	PJ.3 (I/O)[2]	I: 0; O: 1	0	0	0
		TCK[3] [6]	X	X	X	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		CPU Status Register Bit CPUOFF	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		C9[5]	X	X	X	1

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made via the SYS module or by the Spy-Bi-Wire four-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPDx bits have an effect in these cases.
(4) Do not use this pin as SMCLK output if the TB0OUTH functionality is used on any other pin. Select an alternative SMCLK output pin.
(5) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.
(6) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

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6.12 Device Descriptor (TLV)

表 6-63 lists the Device IDs of the MSP430FR59xx(1) devices. 表 6-64 lists the contents of the device descriptor tag-length-value (TLV) structure for MSP430FR59xx(1) devices including AES.

表 6-63. Device IDs

DEVICE	DEVICE ID	
	01A05h	01A04h
MSP430FR5969(1)	081h	069h
MSP430FR5968	081h	068h
MSP430FR5967	081h	067h
MSP430FR5949	081h	061h
MSP430FR5948	081h	060h
MSP430FR5947(1)	081h	05Fh
MSP430FR5959	081h	065h
MSP430FR5958	081h	064h
MSP430FR5957	081h	063h

表 6-64. Device Descriptor(1)

DESCRIPTION		MSP430FR59xx (UART BSL)		MSP430FR59xx1 (I2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
Info Block	Info length	01A00h	06h	01A00h	06h
	CRC length	01A01h	06h	01A01h	06h
	CRC value	01A02h	Per unit	01A02h	Per unit
		01A03h	Per unit	01A03h	Per unit
	Device ID	01A04h	See 表 6-63.	01A04h	See 表 6-63.
		01A05h			
	Hardware revision	01A06h	Per unit	01A06h	Per unit
	Firmware revision	01A07h	Per unit	01A07h	Per unit
Die Record	Die record tag	01A08h	08h	01A08h	08h
	Die record length	01A09h	0Ah	01A09h	0Ah
	Lot/Wafer ID	01A0Ah	Per unit	01A0Ah	Per unit
		01A0Bh	Per unit	01A0Bh	Per unit
		01A0Ch	Per unit	01A0Ch	Per unit
		01A0Dh	Per unit	01A0Dh	Per unit
	Die X position	01A0Eh	Per unit	01A0Eh	Per unit
		01A0Fh	Per unit	01A0Fh	Per unit
	Die Y position	01A10h	Per unit	01A10h	Per unit
		01A11h	Per unit	01A11h	Per unit
	Test results	01A12h	Per unit	01A12h	Per unit
		01A13h	Per unit	01A13h	Per unit

(1) NA = Not applicable, Per unit = content can differ from device to device

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表 6-64. Device Descriptor[1] (continued)

DESCRIPTION		MSP430FR59xx (UART BSL)		MSP430FR59xx1 (I2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
ADC12 Calibration	ADC12 calibration tag	01A14h	11h	01A14h	11h
	ADC12 calibration length	01A15h	10h	01A15h	10h
	ADC gain factor[2]	01A16h	Per unit	01A16h	Per unit
		01A17h	Per unit	01A17h	Per unit
	ADC offset[3]	01A18h	Per unit	01A18h	Per unit
		01A19h	Per unit	01A19h	Per unit
	ADC 1.2-V reference Temperature sensor 30°C	01A1Ah	Per unit	01A1Ah	Per unit
		01A1Bh	Per unit	01A1Bh	Per unit
	ADC 1.2-V reference Temperature sensor 85°C	01A1Ch	Per unit	01A1Ch	Per unit
		01A1Dh	Per unit	01A1Dh	Per unit
	ADC 2.0-V reference Temperature sensor 30°C	01A1Eh	Per unit	01A1Eh	Per unit
		01A1Fh	Per unit	01A1Fh	Per unit
	ADC 2.0-V reference Temperature sensor 85°C	01A20h	Per unit	01A20h	Per unit
		01A21h	Per unit	01A21h	Per unit
	ADC 2.5-V reference Temperature sensor 30°C	01A22h	Per unit	01A22h	Per unit
		01A23h	Per unit	01A23h	Per unit
	ADC 2.5-V reference Temperature sensor 85°C	01A24h	Per unit	01A24h	Per unit
		01A25h	Per unit	01A25h	Per unit
REF Calibration	REF calibration tag	01A26h	12h	01A26h	12h
	REF calibration length	01A27h	06h	01A27h	06h
	REF 1.2-V reference	01A28h	Per unit	01A28h	Per unit
		01A29h	Per unit	01A29h	Per unit
	REF 2.0-V reference	01A2Ah	Per unit	01A2Ah	Per unit
		01A2Bh	Per unit	01A2Bh	Per unit
	REF 2.5-V reference	01A2Ch	Per unit	01A2Ch	Per unit
		01A2Dh	Per unit	01A2Dh	Per unit

(2) ADC gain: the gain correction factor is measured at room temperature using a 2.5-V external voltage reference without internal buffer (ADC12VRSEL=0x2, 0x4, or 0xE). Other settings (for example, using internal reference) can result in different correction factors.
(3) ADC offset: the offset correction factor is measured at room temperature using ADC12VRSEL= 0x2 or 0x4, an external reference, VR+ = external 2.5 V, VR- = AVSS.

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表 6-64. Device Descriptor[(1)] (continued)

DESCRIPTION		MSP430FR59xx (UART BSL)		MSP430FR59xx1 (I2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
Random Number	128-bit random number tag	01A2Eh	15h	01A2Eh	15h
	Random number length	01A2Fh	10h	01A2Fh	10h
	128-bit random number[(4)]	01A30h	Per unit	01A30h	Per unit
		01A31h	Per unit	01A31h	Per unit
		01A32h	Per unit	01A32h	Per unit
		01A33h	Per unit	01A33h	Per unit
		01A34h	Per unit	01A34h	Per unit
		01A35h	Per unit	01A35h	Per unit
		01A36h	Per unit	01A36h	Per unit
		01A37h	Per unit	01A37h	Per unit
		01A38h	Per unit	01A38h	Per unit
		01A39h	Per unit	01A39h	Per unit
		01A3Ah	Per unit	01A3Ah	Per unit
		01A3Bh	Per unit	01A3Bh	Per unit
		01A3Ch	Per unit	01A3Ch	Per unit
		01A3Dh	Per unit	01A3Dh	Per unit
		01A3Eh	Per unit	01A3Eh	Per unit
		01A3Fh	Per unit	01A3Fh	Per unit
BSL Configuration	BSL tag	01A40h	1Ch	01A40h	1Ch
	BSL length	01A41h	02h	01A41h	02h
	BSL Interface	01A42h	00h	01A42h	01h
	BSL interface configuration	01A43h	00h	01A43h	48h

(4) 128-bit random number: The random number is generated during production test using the CryptGenRandom() function from Microsoft®.

6.13 Identification

6.13.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in 6.12.

6.13.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in 6.12.

6.13.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming With the JTAG Interface*.

7 Applications, Implementation, and Layout

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section describes the recommended guidelines when designing with the MSP430. These guidelines ensure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1-µF capacitor and a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can affect supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital to analog circuits on the board and to achieve high analog accuracy.

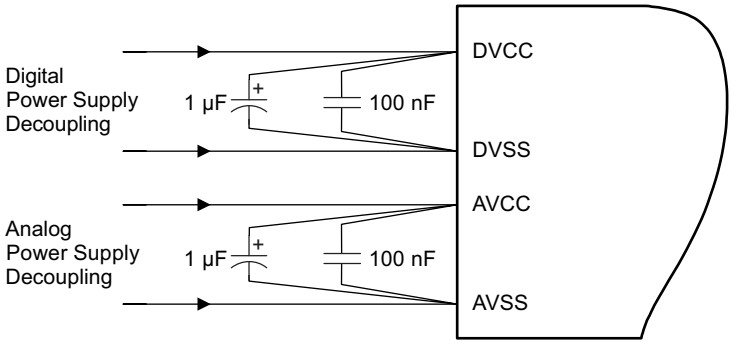

図 7-1. Power Supply Decoupling

7.1.2 External Oscillator

Depending on the device variant (see Section 3), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If the LFXIN and HFXIN are left unused, they must be terminated according to Section 4.4.

図 7-2 shows a typical connection diagram.

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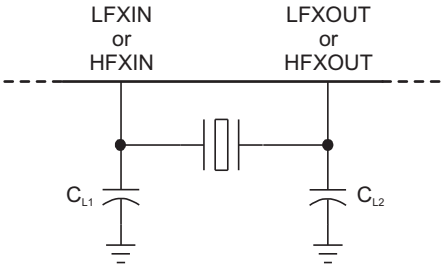


図 7-2. Typical Crystal Connection

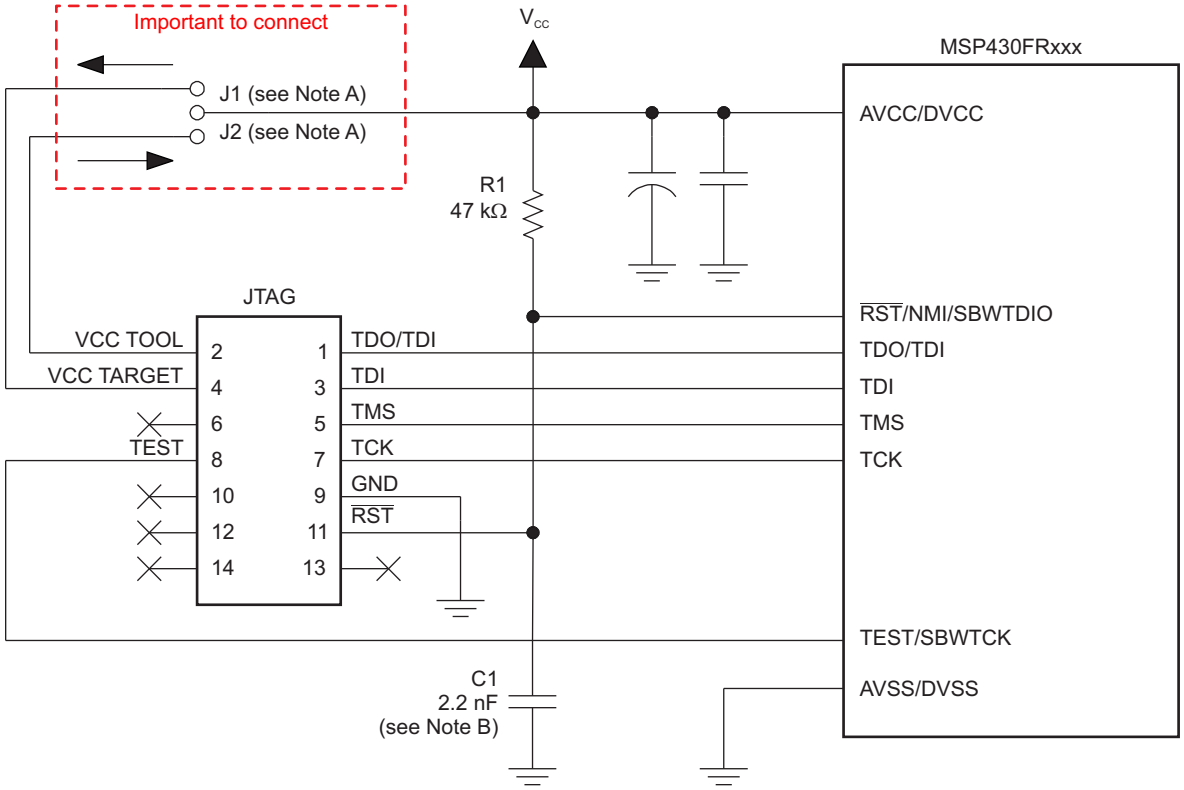
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 図 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 図 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 図 7-3 and 図 7-4 show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.



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A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 2.2 nF when using current TI tools.

図 7-3. Signal Connections for 4-Wire JTAG Communication

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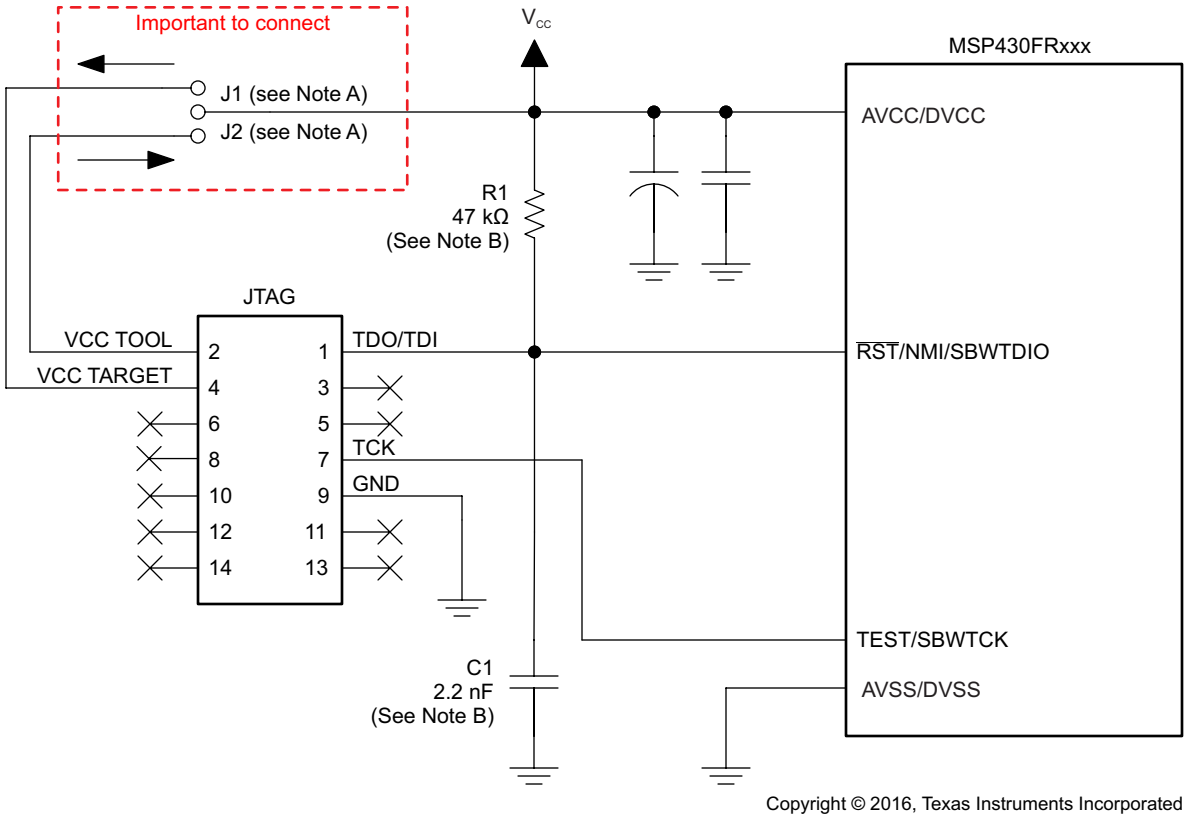

A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

図 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers. If JTAG or Spy-Bi-Wire access is not needed, up to a 10-nF pulldown capacitor may be used.

See the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide* for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see Section 4.4.

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.7 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in Section 5.1. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC12_B Peripheral

7.2.1.1 Partial Schematic

図 7-5 shows the recommended decoupling circuit when an external voltage reference is used.

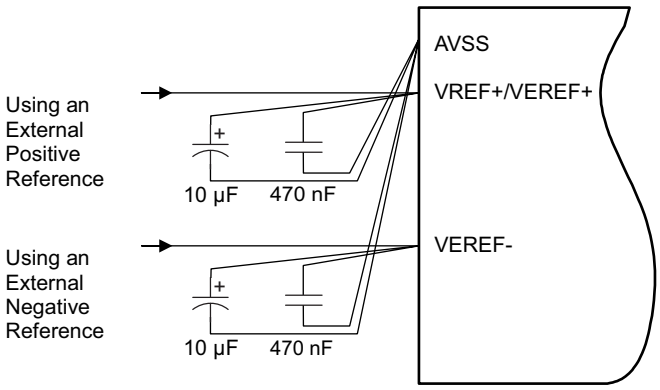

図 7-5. ADC12_B Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in 7.1.1 combined with the connections in 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

図 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the Reference module's $I_{O(VREF+)}$ specification.

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The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor is used to buffer the reference pin and filter low-frequency ripple. A 470-nF bypass capacitor is used to filter high-frequency noise.

7.2.1.3 Detailed Design Procedure

For additional design information, see Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC.

7.2.1.4 Layout Guidelines

Component that are shown in the partial schematic (see 図 7-5) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

8 デバイスおよびドキュメントのサポート

8.1 使い始めと次の手順

MSP430ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「Getting Started」ページを参照してください。

8.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP　MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

XMS - 実験段階のデバイスで、最終的なデバイスの電気的仕様を表しているとは限りません。

MSP - 完全に認定済みの量産版デバイスです。

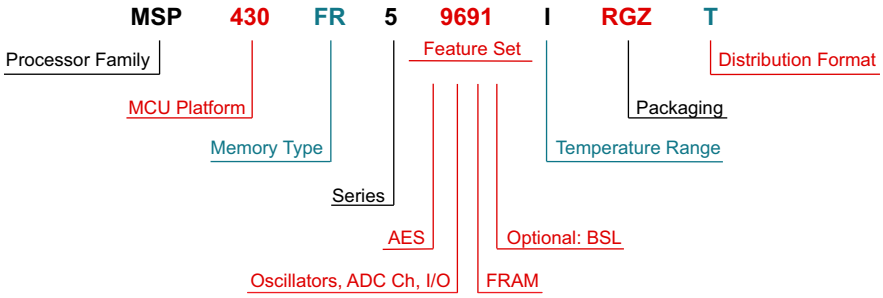
XMSデバイスは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方を図 8-1に示します。



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon			
MCU Platform	430 = TI's 16-bit MSP430 Low-Power Microcontroller Platform			
Memory Type	FR = FRAM			
Series	5 = FRAM 5 series up to 16 MHz without LCD			
Feature Set	**First Digit: AES** 9 = AES 8 = No AES	**Second Digit: Oscillators, ADC Channels, I/O** 6 = DCO/HFXT/LFXT, 16, 40 5 = DCO/HFXT, 14/12, 33/31 4 = DCO/LFXT, 14/12, 33/31	**Third Digit: FRAM (KB)** 9 = 64 8 = 48 7 = 32	**Optional Fourth Digit: BSL** 1 = I^2C No value = UART
Temperature Range	I = –40°C to 85°C			
Packaging	www.ti.com/packaging			
Distribution Format	T = Small reel R = Large reel No markings = Tube or tray			

NOTE: この図は、利用可能な機能とオプションの完全なリストではなく、与えられたデバイスまたはファミリについて、これらの機能とオプションのすべてが利用できることを示すものでもありません。

図 8-1. デバイスの項目表記 - 型番の読み方

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8.3 ツールとソフトウェア

表 8-1 は、MSP430FR59xx マイクロコントローラでサポートされるデバッグ機能の一覧です。利用可能な機能の詳細については、『*MSP430用Code Composer Studio ユーザー・ガイド*』を参照してください。

表 8-1. ハードウェアの特長

MSP430のアーキテクチャ	4線式 JTAG	2線式 JTAG	ブレーク・ポイント (N)	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMx.5デバッグ・サポート	EnergyTrace++テクノロジ
MSP430Xv2	○	○	3	○	○	×	×	○	○

EnergyTrace™ テクノロジは、Code Composer Studioのバージョン6.0およびそれ以降でサポートされています。EnergyTraceテクノロジには特化したデバッガ回路が必要で、第2世代のオンボードeZ-FETフラッシュ・エミュレーション・ツールおよび第2世代のスタンドアロンMSP-FET JTAGエミュレータでサポートされています。詳細情報については、以下を参照してください。

『拡張エミュレーション・モジュール(EEM)とCode Composer Studioによる高度なデバッグ』

『MSP430™の高度な電力最適化: ULP Advisor™およびEnergyTrace™テクノロジ』

設計キットと評価モジュール

MSP430FR5969 LaunchPad™開発キット MSP-EXP430FR5969 LaunchPad開発キットは、MSP430FR5969 MCU用の使いやすいマイクロコントローラ開発ボードです。プログラミング、デバッグ、電力測定を行うためのオンボード・エミュレーションなど、MSP430FRxx FRAMプラットフォームの迅速な開発に必要なすべての機能を備えています。

MSP430FRxx FRAM MCU用の、48ピンのターゲット開発ボードとMSP-FETプログラマ・バンドル MSP-FET430U48Cは、MSP MCU上でアプリケーションを迅速に開発するための、強力な設計キットです。この基板には、JTAG インターフェイスまたはピン数を低減した Spy Bi-Wire (2 線式 JTAG) プロトコルを経由して、システム内の MSP MCU のプログラムとデバッグに使用する USB デバッグ・インターフェイスが付属しています。FRAMは、数回のキー操作により、数秒で消去およびプログラムできます。また、MSP FRAMの消費電力は非常に低いため、外部電源は不要です。

MSP-TS430RGZ48C - MSP430FRxx FRAM MCU用の48ピン・ターゲット開発ボード MSP-TS430RGZ48C はスタンドアロンの 48 ピン ZIF ソケット・ターゲット・ボードで、JTAG インターフェイスまたは Spy Bi-Wire (2 線式の JTAG) プロトコルによりシステム内の MSP430 をプログラムおよびデバッグするために使用できます。

ソフトウェア

MSP430Ware™ソフトウェア MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存の MSP430 MCU 設計リソースの完全なコレクションに加えて、MSP430Ware ソフトウェアには、MSP ドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430WareソフトウェアはCCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

MSP430FR59xx、MSP430FR58xxのサンプル・コード すべてのMSPデバイス用に、内蔵の各ペリフェラルをさまざまなアプリケーションの要求に応じて構成するためのCコード・サンプルが用意されています。

MSP超低消費電力マイクロコントローラ用FRAM組み込みソフトウェア・ユーティリティ TI FRAMユーティリティ・ソフトウェアは、組み込みソフトウェア・ユーティリティのコレクションとして成長するように設計されており、超低消費電力と、ほぼ無限のFRAM書き込み耐性を活用できます。このユーティリティは MSP430FRxx FRAMマイクロコントローラで利用でき、アプリケーション開発を始めるために役立つコード例が用意されています。

静電容量式タッチ・ソフトウェア・ライブラリ MSP430 MCU で静電容量式タッチ機能を有効にするための、無償のCライブラリです。MSP430 MCU バージョンのライブラリには、ROおよびRC方式を含む、いくつかの静電容量式タッチ機能の実装が含まれています。

MSPドライバ・ライブラリ MSPドライバ・ライブラリの抽象化されたAPIには、使いやすい関数呼び出しが含まれているため、MSP430ハードウェアのビットやバイトを直接操作する煩雑さから解放されます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTrace™テクノロジ MSP430マイクロコントローラ用のEnergyTraceテクノロジは、エネルギーを基準としたコード解析ツールで、アプリケーションのエネルギー・プロファイルを測定して表示し、消費電力が極めて低くなるよう最適化するため役立ちます。

ULP (超低消費電力) Advisor ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラの超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorはマイクロコントローラに熟練した開発者と、新しい開発者の両方を対象としており、包括的なULPチェックリストを使用してコードをチェックし、アプリケーションのエネルギー消費を最小化するため役立ちます。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

IEC60730ソフトウェア・パッケージ IEC60730 MSP430ソフトウェア・パッケージは、クラスBまでの製品について、お客様がIEC 60730-1:2010 (家庭および同様な用途に使用される自動電気制御 – 第1部: 一般的な要件)に準拠するため役立つよう開発されています。この分類には家電機器、アーク検出器、電力コンバータ、電動工具、電動アシスト自転車、その他多くの製品が含まれます。IEC60730 MSP430ソフトウェア・パッケージは、MSP430で実行するお客様のアプリケーションに組み込むことができるため、消費者向けデバイスがIEC 60730-1:2010クラスBの機能安全性に準拠していることの認定作業を簡素化できます。

MSP用の固定小数点算術ライブラリ MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

MSP430用の浮動小数点算術ライブラリ 低消費電力で低コストのマイクロコントローラ分野にさらなる革新を引き起こすため、TIはMSPMATHLIBを提供します。この浮動小数点算術ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、標準のMSP430算術関数よりも最高で26倍も高速なスカラー関数です。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio IDEとIAR Embedded Workbench IDEの両方に組み込まれています。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境 Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。CCSには、最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。

コマンドライン・プログラマ MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

MSP MCUプログラマおよびデバッガ MSP-FETは強力なエミュレーション開発ツールで、多くの場合にデバッグ・プローブと呼ばれます。ユーザーはこのツールを使用して、MSP低消費電力MCUのアプリケーション開発をすぐに始めることができます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。

MSP-GANG量産プログラマ MSP Gang プログラマは MSP430 または MSP432 用のデバイス・プログラマで、8 つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang プログラマは、標準の RS-232 または USB 接続を使用してホスト PC と接続し、柔軟なプログラミング・オプションが用意されているため、ユーザーはプロセスを完全にカスタマイズ可能です。

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8.4 ドキュメントのサポート

以下のドキュメントには、MSP430FR59xx MCU について記述されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでご利用の製品のフォルダへ移動します(製品フォルダへのリンクについては、8.5を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430FR5969正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR59691正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5968正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5967正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5959正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5958正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5957正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5949正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5948正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR5947正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR59471正誤表』 には、機能仕様に対する既知の例外が記載されています。

ユーザー・ガイド

『MSP430FR58xx、MSP430FR59xx、MSP430FR6xxファミリ・ユーザー・ガイド』 このデバイス・ファミリで利用可能なすべてのモジュールとペリフェラルについての詳細情報です。

『MSP430 FRAMデバイス・ブートローダ(BSL)ユーザー・ガイド』 ブートローダー(BSL、従来はブートストラップ・ローダーと呼ばれていました)は、MSP430 MCUプロジェクトの開発および更新時にメモリをプログラムするための手段を提供します。シリアル・プロトコルを使用してコマンドを送信するユーティリティにより、この機能をアクティブにできます。BSLにより、ユーザーはMSP430の動作を制御し、パーソナル・コンピュータや他のデバイスを使用してデータを交換できます。

『JTAGインターフェイスによるMSP430のプログラミング』 このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』 このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

アプリケーション・レポート

『MSP430 FRAMテクノロジ - ハウツーとベスト・プラクティス』 FRAMは不揮発性メモリ・テクノロジで、SRAMと同様に動作し、多くの新しいアプリケーションを可能にすると同時に、ファームウェアの設計方法に変革をもたらすものです。このアプリケーション・レポートでは、組み込みソフトウェア開発の観点から、MSP430のFRAMテクノロジを使用する方法と、そのベスト・プラクティスについて概説しています。特定用途向けのコード、定数、データ容量の制限、FRAMの使用に従って、アプリケーションのエネルギー消費を最適化するようメモリ・レイアウトを実装する方法について解説します。

『MSP430 32kHz水晶発振器』 適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430 システム・レベルESDの考慮事項』 シリコン・テクノロジがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まっていくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。

8.5 関連リンク

表 8-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430FR5969	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR59691	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5968	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5967	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5959	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5958	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5957	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5949	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5948	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR5947	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR59471	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 商標

EnergyTrace++, MSP430, EnergyTrace, LaunchPad, MSP430Ware, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.
Microsoft is a registered trademark of Microsoft Corporation.
All other trademarks are the property of their respective owners.

8.8 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR59471IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59471	Samples
MSP430FR59471IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59471	Samples
MSP430FR5947IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5947	Samples
MSP430FR5947IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5947	Samples
MSP430FR5947IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5947	Samples
MSP430FR5947IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5947	Samples
MSP430FR5948IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5948	Samples
MSP430FR5948IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5948	Samples
MSP430FR5948IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5948	Samples
MSP430FR5948IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5948	Samples
MSP430FR5949IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5949	Samples
MSP430FR5949IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5949	Samples
MSP430FR5949IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5949	Samples
MSP430FR5949IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5949	Samples
MSP430FR5957IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5957	Samples
MSP430FR5957IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5957	Samples
MSP430FR5957IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5957	Samples
MSP430FR5957IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5957	Samples
MSP430FR5958IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5958	Samples
MSP430FR5958IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5958	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR5958IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5958	Samples
MSP430FR5958IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5958	Samples
MSP430FR5959IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5959	Samples
MSP430FR5959IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5959	Samples
MSP430FR5959IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5959	Samples
MSP430FR5959IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5959	Samples
MSP430FR5967IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5967	Samples
MSP430FR5967IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5967	Samples
MSP430FR5968IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5968	Samples
MSP430FR5968IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5968	Samples
MSP430FR59691IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59691	Samples
MSP430FR59691IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59691	Samples
MSP430FR5969IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5969	Samples
MSP430FR5969IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5969	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

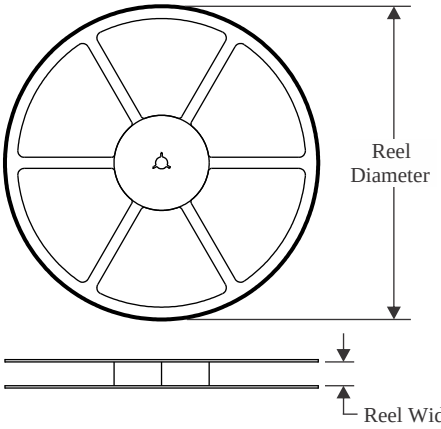
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

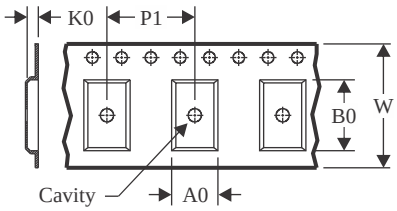
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

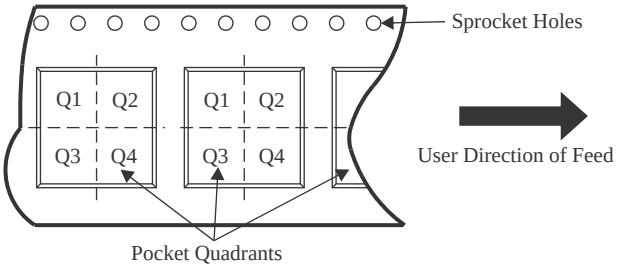


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

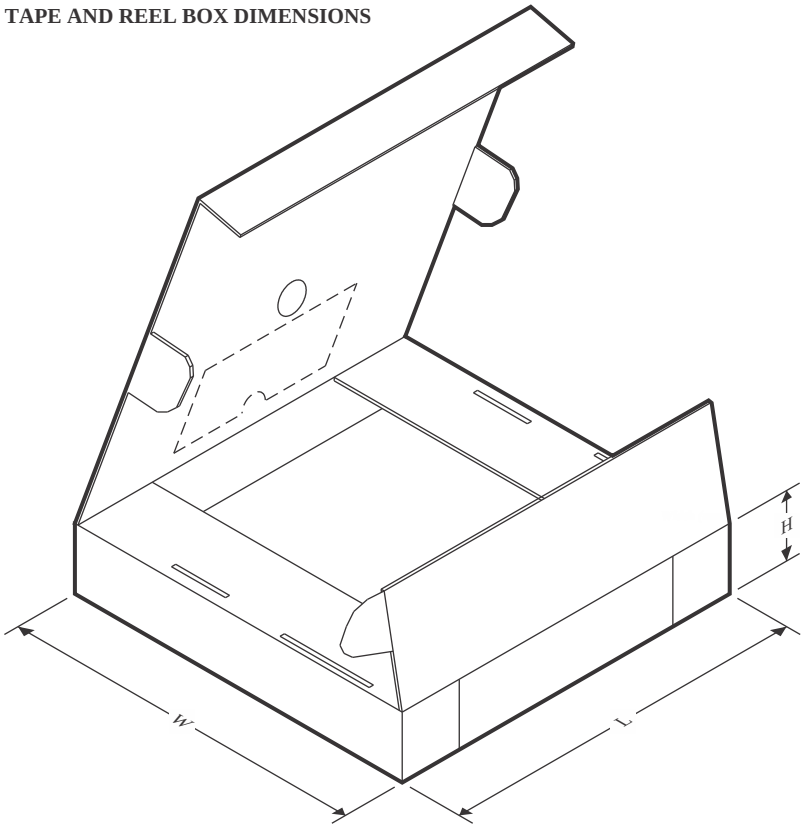


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR59471IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR59471IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5947IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5947IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5947IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5948IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5948IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5948IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5949IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5949IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5949IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5957IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5957IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5957IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5958IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5958IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR5958IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5959IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5959IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5959IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5967IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5967IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5967IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5968IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5968IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5968IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5968IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR59691IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR59691IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR59691IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR59691IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5969IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5969IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5969IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430FR5969IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

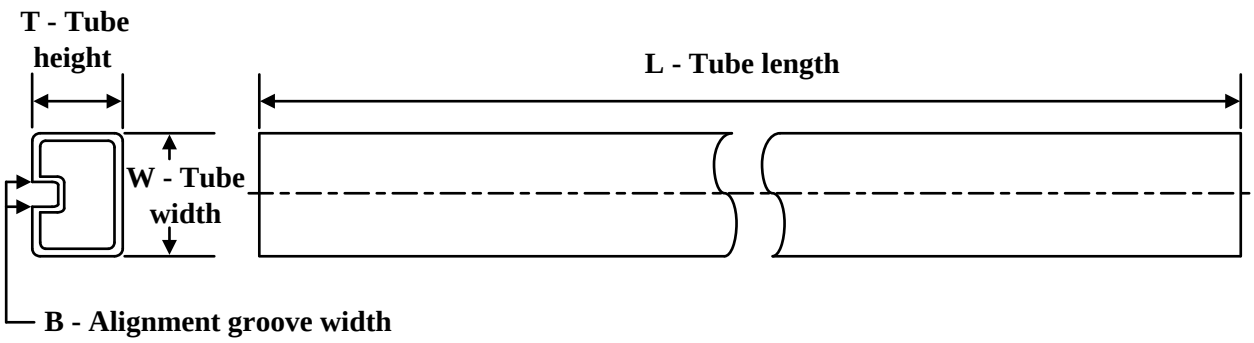


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR59471IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR59471IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5947IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430FR5947IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5947IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5948IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430FR5948IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5948IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5949IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430FR5949IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5949IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5957IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430FR5957IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5957IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5958IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430FR5958IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5958IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5959IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR5959IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5959IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5967IRGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
MSP430FR5967IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430FR5967IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430FR5968IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430FR5968IRGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
MSP430FR5968IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430FR5968IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430FR59691IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430FR59691IRGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
MSP430FR59691IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430FR59691IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430FR5969IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430FR5969IRGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
MSP430FR5969IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430FR5969IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

TUBE

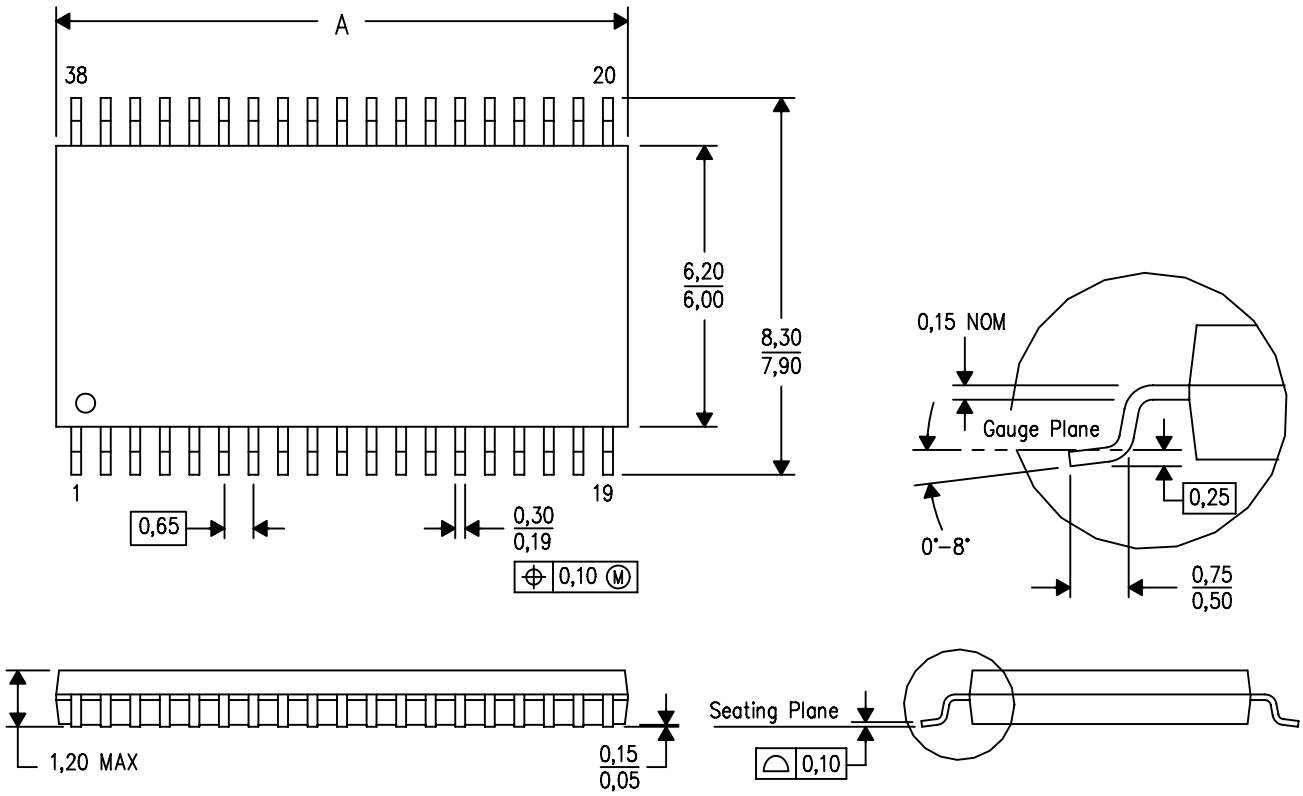


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430FR5947IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5948IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5949IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5957IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5958IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5959IDA	DA	TSSOP	38	40	530	11.89	3600	4.9

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN

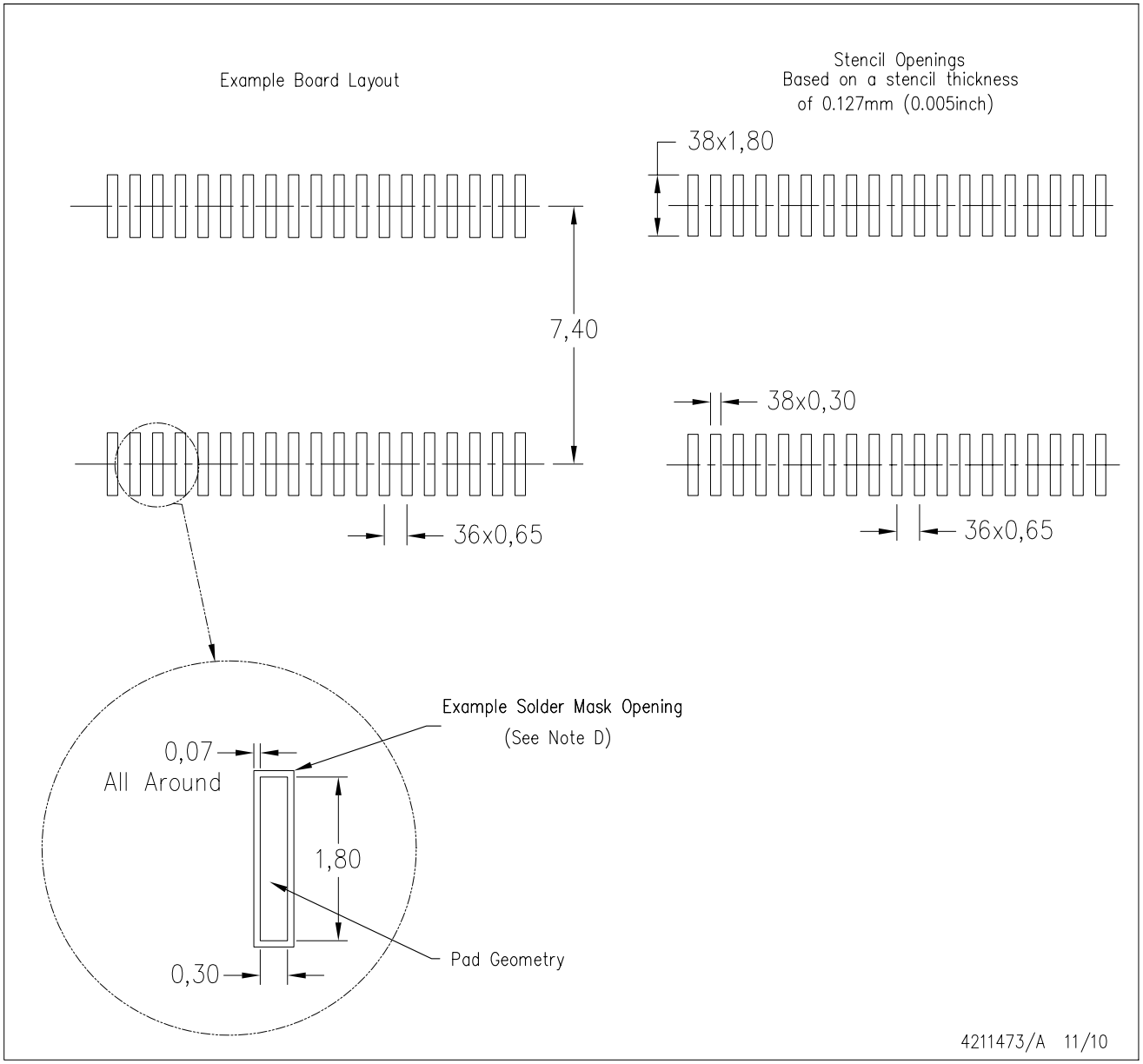


DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–153, except 30 pin body length.

DA (R-PDSO-G38) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
D. Contact the board fabrication site for recommended soldermask tolerances.

GENERIC PACKAGE VIEW

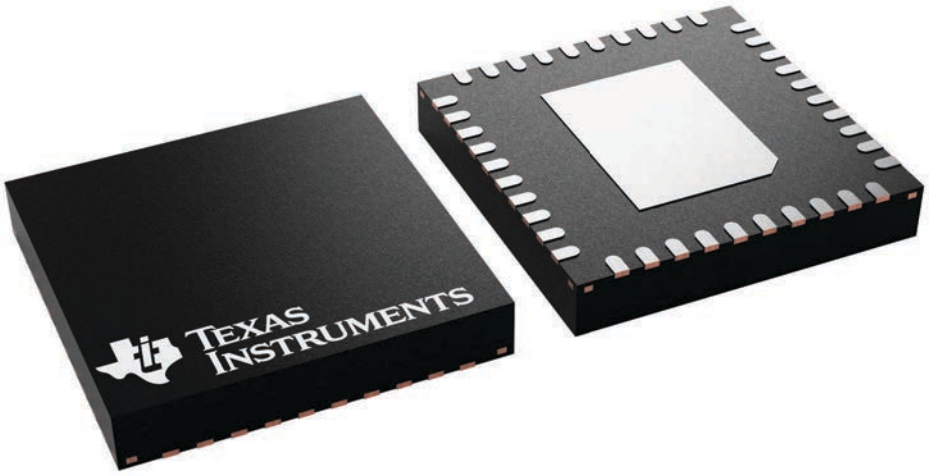
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



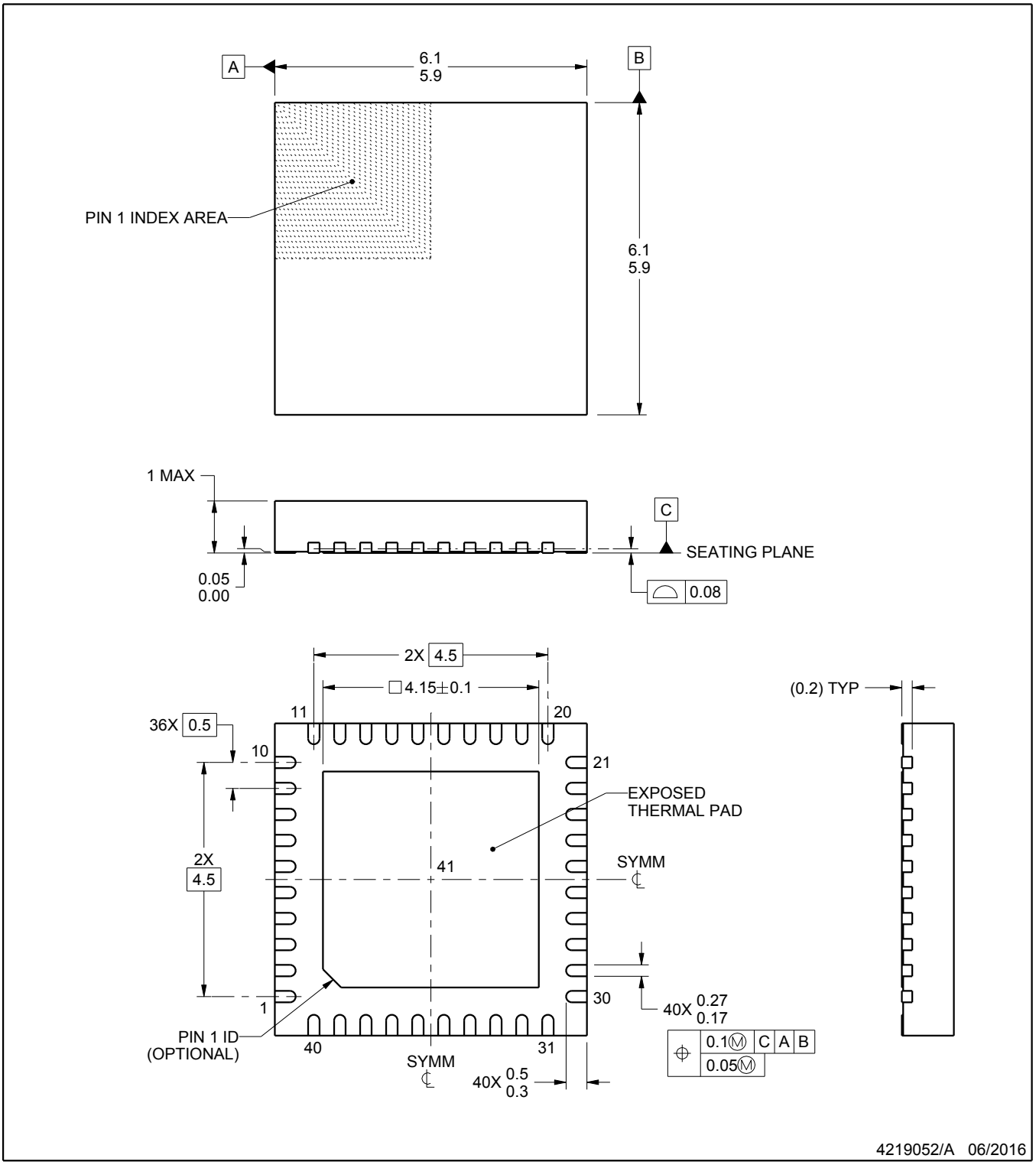
4225870/A

PACKAGE OUTLINE

RHA0040B

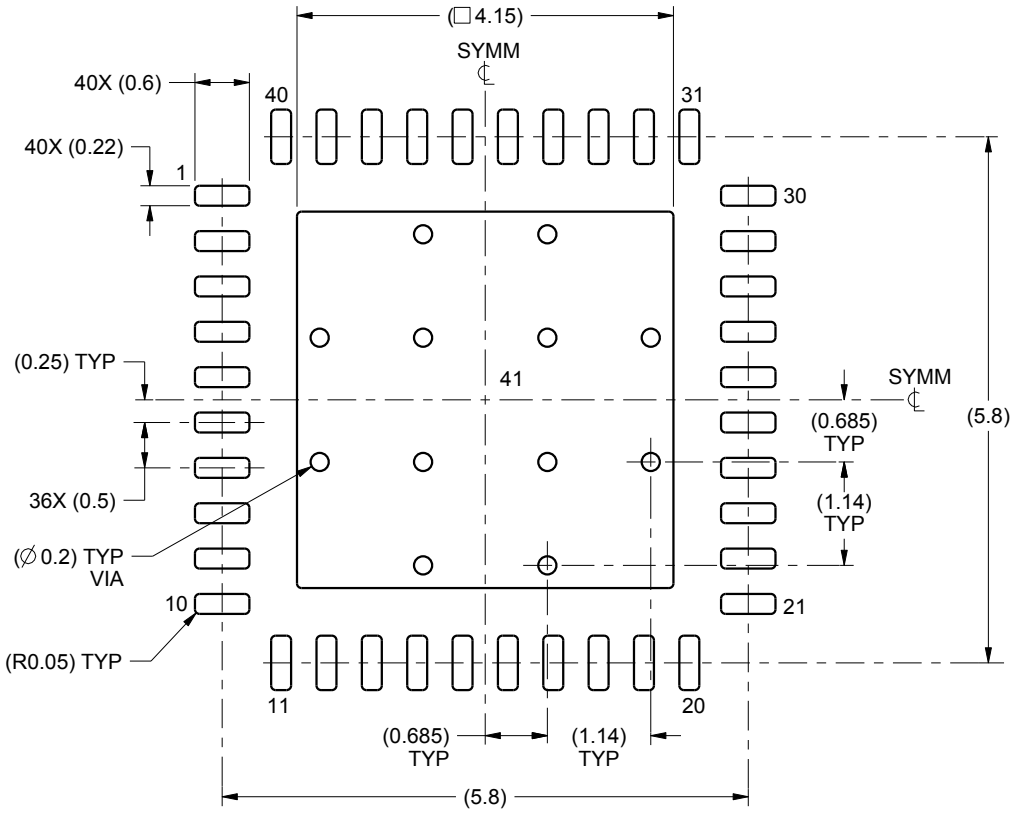
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

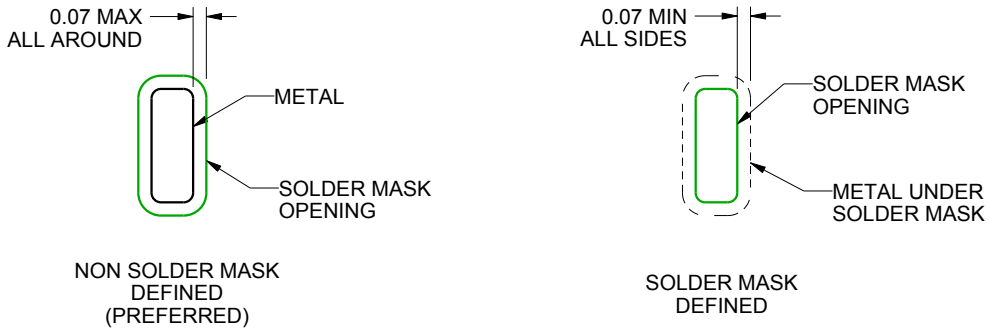


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

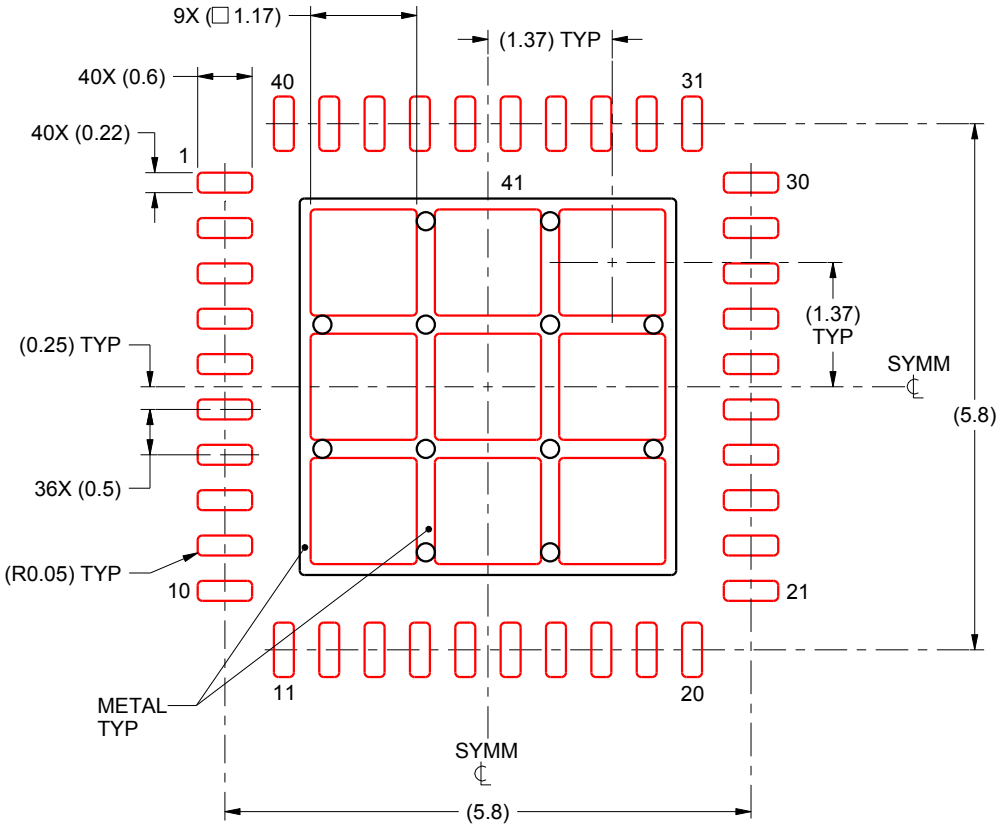


SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

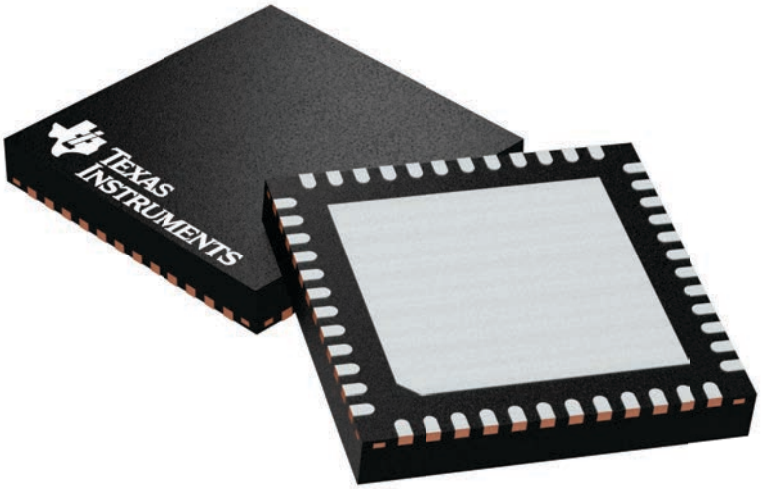
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

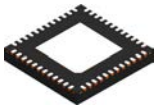
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

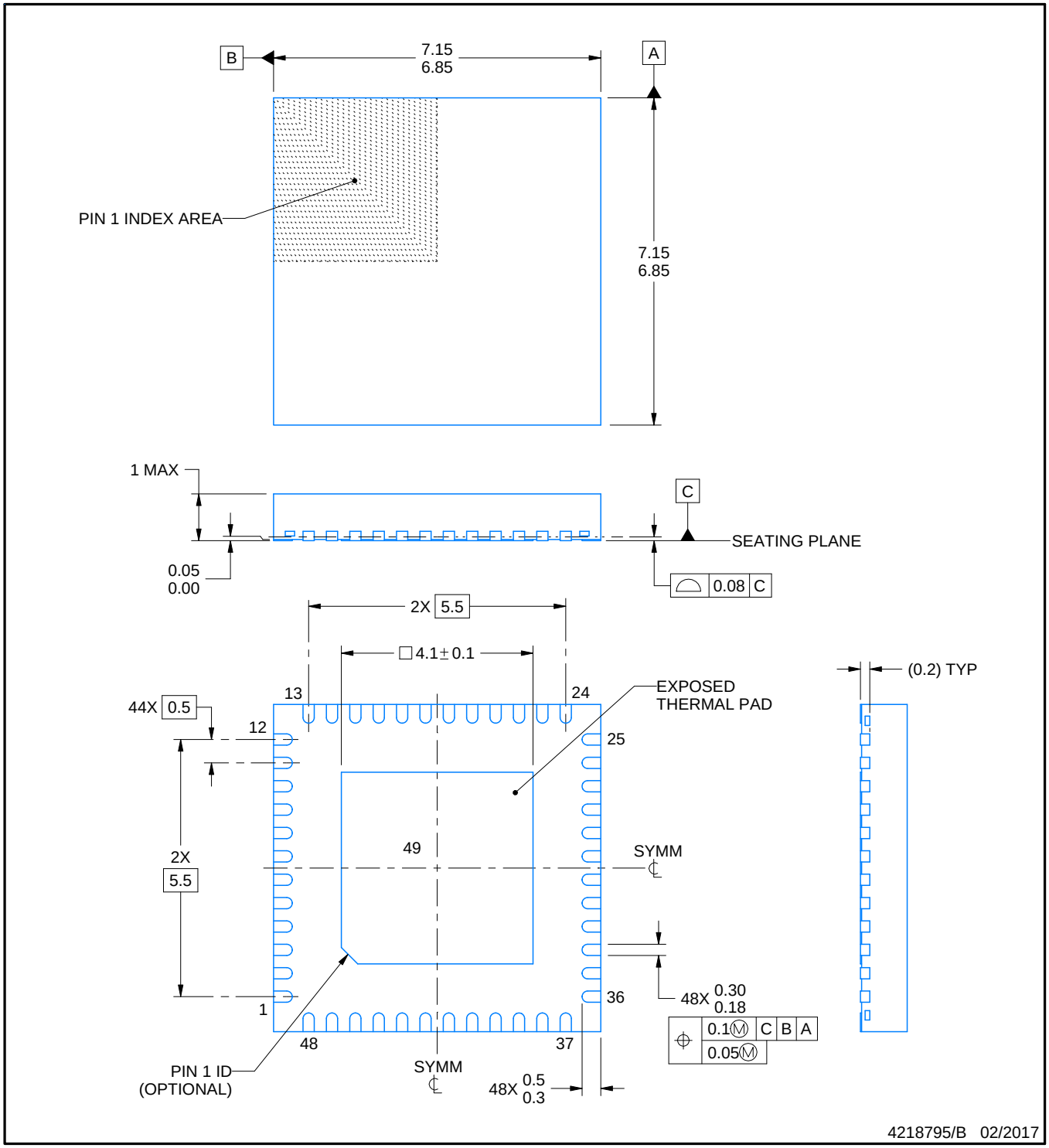
RGZ0048B



PACKAGE OUTLINE

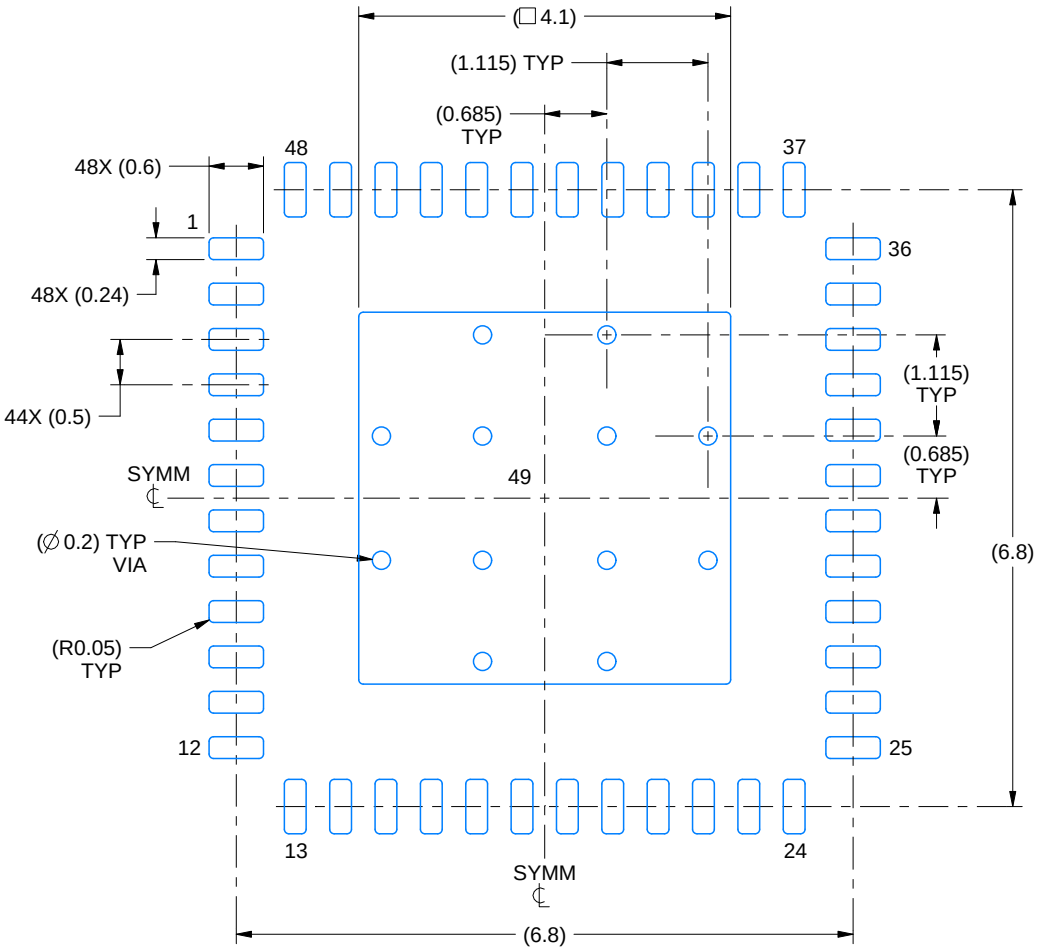
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

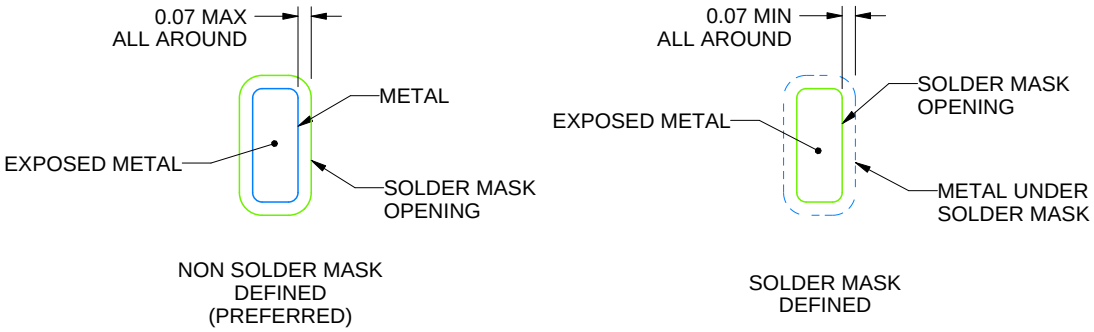


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

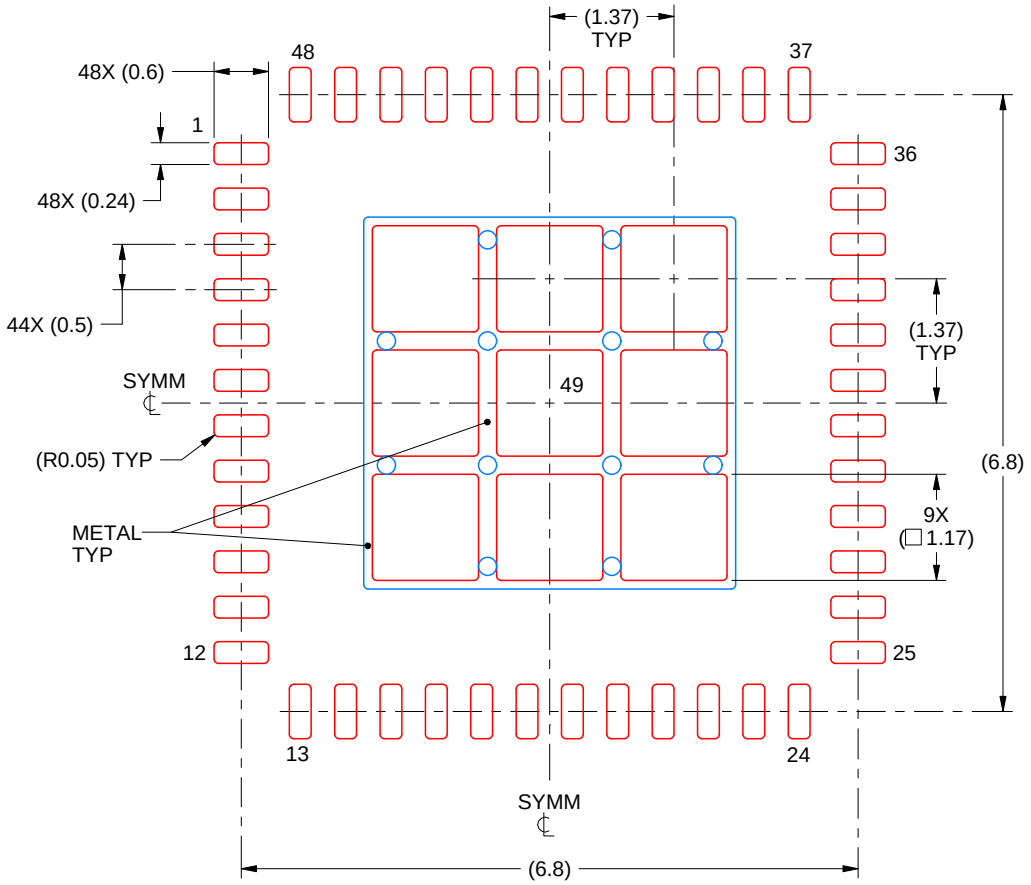


SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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