MSP430FR604x(1)、MSP430FR603x(1) 水量計アプリケーション用の超音波センシングMSP430™マイクロコントローラ

1 デバイスの概要

1.1 特長

- クラス最高の超音波水流測定を超低消費電力で実現
  - 25ps未満の差分タイム・オブ・フライト(dTOF)精度
  - 高精度の時間測定: 分解能5ps未満
  - 低い流量率の検出能力(毎時1リットル未満)
  - 毎秒1回の測定で、合計消費電流約3µA
- ISO 4064、OIML R49、EN 1434精度規格に準拠または上回る精度
- 標準の超音波センサと直接接続可能(最高2.5MHz)
- アナログ・フロント・エンド内蔵 - 次の機能を含む超音波センシング・ソリューション(USS)
  - プログラマブル・パルス生成(PPG)による各種周波数のパルス生成
  - 統合物理インターフェイス(PHY)と低インピーダンス(4Ω)の出力ドライバにより、入力および出力チャネルを制御
  - 高性能、高速の12ビットシグマ-デルタADC (SDHS)、最高8MSPSの出力データ・レート
  - -6.5dB～30.8dBのプログラマブル・ゲイン・アンプ(PGA)
  - 高性能の位相ロック・ループ(PLL)、出力範囲68MHz～80MHz
- 計量テスト・インターフェイス(MTIF)
  - パルス・ジェネレータとパルス・カウンタ
  - 毎秒最高1016パルスのパルス・レート(p/s)
  - 最高65535までのカウント能力(16ビット)
  - LPM3.5において200nAで動作(標準値)
- 低消費電力アクセラレータ(LEA)
  - CPUと独立に動作
  - 4KBのRAMをCPUと共有
  - 効率的な256ポイントの複素FFT: Arm® Cortex®-M0+コアよりも最大で40倍高速
- 組み込みマイクロコントローラ
  - 16ビットのRISCアーキテクチャ、最大16MHzのクロック
  - 3.6V～1.8Vの広い電源電圧範囲(最小電源電圧はSVSレベルにより制限されます。「SVS仕様」を参照)
- 最適化された超低消費電力モード
  - アクティブ・モード: 約120µA/MHz
  - リアルタイム・クロック(RTC)使用のスタンバイ・モード(LPM3.5): 450nA (1)
  - シャットダウン(LPM4.5): 30nA
- 強誘電体ランダム・アクセス・メモリ(FRAM)
  - 最大256KBの不揮発性メモリ
  - 超低消費電力の書き込み
  - ワードあたり125nsの高速書き込み(4msで64KB)
  - ユニファイド・メモリによりプログラム、データ、ストレージを1か所に保存
  - 10^{15}回の書き込み耐久性
  - 放射耐性および非磁性
- インテリジェントなデジタル・ペリフェラル
  - 32ビットのハードウェア乗算器(MPY)
  - 6チャネルの内蔵DMA
  - カレンダーおよびアラーム機能を持つRTC
  - 6つの16ビット・タイマ、それぞれに7つのキャプチャ/比較レジスタを搭載
  - 32ビットおよび16ビットの巡回冗長性検査(CRC)
- 高性能アナログ
  - 16チャネルのアナログ・コンパレータ
  - ウィンドウ・コンパレータ、内部基準電圧、サンプル・アンド・ホールド機能を持つ12ビットのSAR ADC、最大16の外部入力チャネル
  - 最大264セグメントのコントラスト制御を搭載した内蔵LCDドライバ
- マルチファンクションの入力/出力ポート
  - ビット、バイト、ワード単位でアクセス可能(ペアで)
  - すべてのポートでLPMからのウェークアップをエッジ選択可能
  - すべてのポートでプルアップおよびプルダウンをプログラム可能
- コードのセキュリティと暗号化
  - 128または256ビットAESセキュリティ暗号化/復号化コプロセッサ
  - 乱数シードによる乱数生成アルゴリズム
  - IPカプセル化により外部アクセスからメモリを保護
  - FRAM固有のセキュリティ上の利点

(1) RTCは3.7pFの水晶振動子によりクロック供給を受けます。

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

- シリアル通信の拡張機能
  - 最大4つのeUSCI_Aシリアル通信ポート
    - 自動ボーレート検出機能付きのUART
    - IrDAのエンコードおよびデコード
  - 最大2つのeUSCI_Bシリアル通信ポート
    - 複数スレーブ・アドレッシングに対応したI^2C
  - ハードウェアUARTまたはI^2Cブートローダー(BSL)
- 柔軟なクロック・システム
  - 固定周波数DCO、出荷時にトリムされた10の周波数を選択可能
  - 低電力、低周波数の内部クロック・ソース(VLO)
  - 32kHzの水晶振動子(LFXT)
  - 高周波数の水晶振動子(HFXT)
- 開発ツールとソフトウェア(「ツールとソフトウェア」も参照)
  - 超音波センシング設計センター・グラフィカル・ユーザー・インターフェイス
  - 超音波センシング・ソフトウェア・ライブラリ
  - EVM430-FR6047 水量計評価モジュール基板
  - MSP-TS430PZ100E 100ピン・パッケージ用のターゲット・ソケット基板
  - EnergyTrace++テクノロジを含む無償のプロフェッショナル開発環境
  - MSP430™マイクロコントローラ用のMSP430Ware™
- 利用可能なデバイスのバリエーションおよびパッケージ・オプションについては、「デバイスの比較」の概要を参照してください。
- モジュールの完全な説明については、*『MSP430FR58xx、MSP430FR59xx、MSP430FR6xxファミリ・ユーザー・ガイド』*を参照してください。

1.2 アプリケーション

- 超音波スマート水量計
- 超音波スマート熱量計
- 液面検出
- 水漏れ検出

1.3 概要

テキサス・インスツルメンツのMSP430FR604xおよびMSP430FR603xファミリの超音波センシングおよび測定SoCは、強力で高度に統合されたマイクロコントローラ(MCU)で、水および熱量計に最適化されています。MSP430FR604x MCUは統合された超音波センシング・ソリューション(USS)モジュールとなり、広範囲の流量率について高い精度を実現します。USSモジュールは最大限に統合されており、ごく少数の外付け部品しか必要としないため、超低消費電力の計量と、システム・コストの低減を達成できます。MSP430FR604xおよびMSP430FR603x MCUには、高速なADCベースの信号収集と、それに続く内蔵の低消費電力アクセラレータ(LEA)を使用する、最適化された信号デジタル処理が組み込まれているため、非常に消費電力が低い高精度の計量ソリューションとなり、バッテリ駆動の計量アプリケーションに最適です。

USSモジュールには、プログラマブル・パルス・ジェネレータ(PPG)と、低インピーダンスの出力ドライバを持つ物理インターフェイス(PHY)が含まれており、最適なセンサ励起と正確なインピーダンス整合を行い、ゼロ流量ドリフト(ZFD)について最良の結果が得られます。モジュールには、プログラマブル・ゲイン・アンプ(PGA)と高速な12ビット、8MSPSシグマ-デルタADC (SDHS)も含まれており、業界標準の超音波トランスデューサから正確な信号を収集できます。

さらに、MSP430FR604xおよびMSP430FR603x MCUには、計量をシステムへより的確に組み込むため役立つ、他のペリフェラルも内蔵されています。デバイスには計量テスト・インターフェイス(MTIF)モジュールがあり、メータにより測定された流量を示すパルス生成が実装されています。また、MSP430FR604xおよびMSP430FR603x MCUには、オンチップの8-mux LCDドライバ、RTC、12ビットSAR ADC、アナログ・コンパレータ、高度暗号化アクセラレータ(AES256)、巡回冗長性検査(CRC)モジュールも内蔵されています。

MSP430FR604xおよびMSP430FR603x MCUは、大規模なハードウェアおよびソフトウェアのエコシステムによってサポートされており、リファレンス・デザインやコード・サンプルによって設計を迅速に開始できます。開発キットには、MSP-TS430PZ100E 100ピン・ターゲット開発基板およびEVM430-FR6047 超音波水流量計EVMが含まれています。TIは、超音波センシング設計センター、超音波センシング・ソフトウェア・ライブラリ、およびMSP430Ware™ソフトウェアを含む無償のソフトウェアも提供しています。

MSP430超低消費電力(ULP) FRAMマイクロコントローラ・プラットフォームは、独自の組み込みFRAMと包括的な超低消費電力のシステム・アーキテクチャを組み合わせたもので、システム設計者は性能向上とエネルギー消費量削減を同時に実現できます。FRAMテクノロジは、RAMの低エネルギーでの高速書き込み、柔軟性、耐久性と、フラッシュの不揮発性を併せ持つものです。

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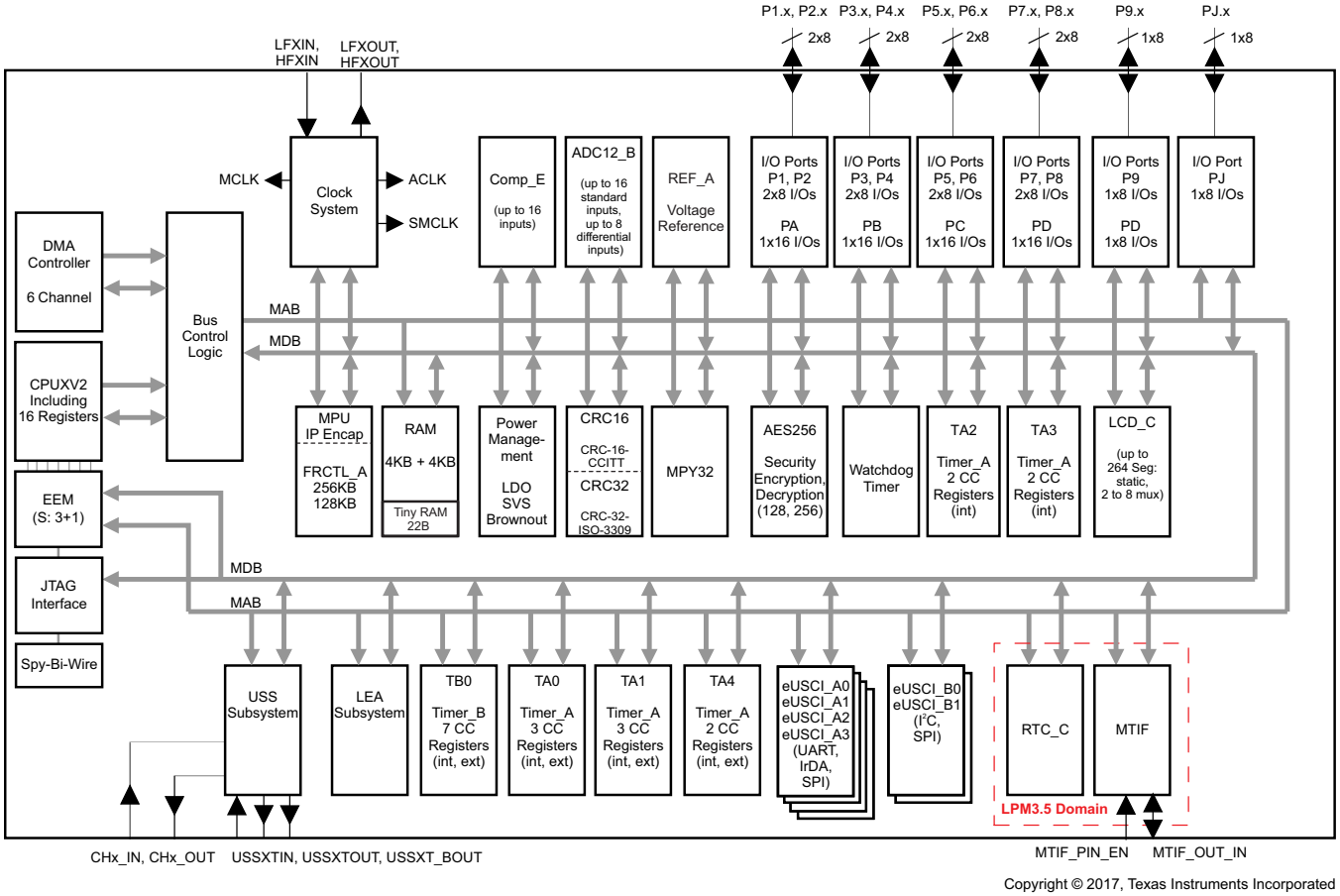
製品情報(1)(2)

型番	パッケージ	本体サイズ(3)
MSP430FR6047IPZ MSP430FR60471IPZ MSP430FR6045IPZ MSP430FR6037IPZ MSP430FR60371IPZ MSP430FR6035IPZ	LQFP (100)	14mm×14mm

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については 9の「付録:パッケージ・オプション」またはwww.ti.comのTI Webサイトを参照してください。
(2) 利用可能なデバイスのバリエーションすべての比較については、3を参照してください。
(3) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、9の「メカニカル・データ」を参照してください。

1.4 機能ブロック図

デバイスの機能ブロック図を、図 1-1および図 1-2に示します。



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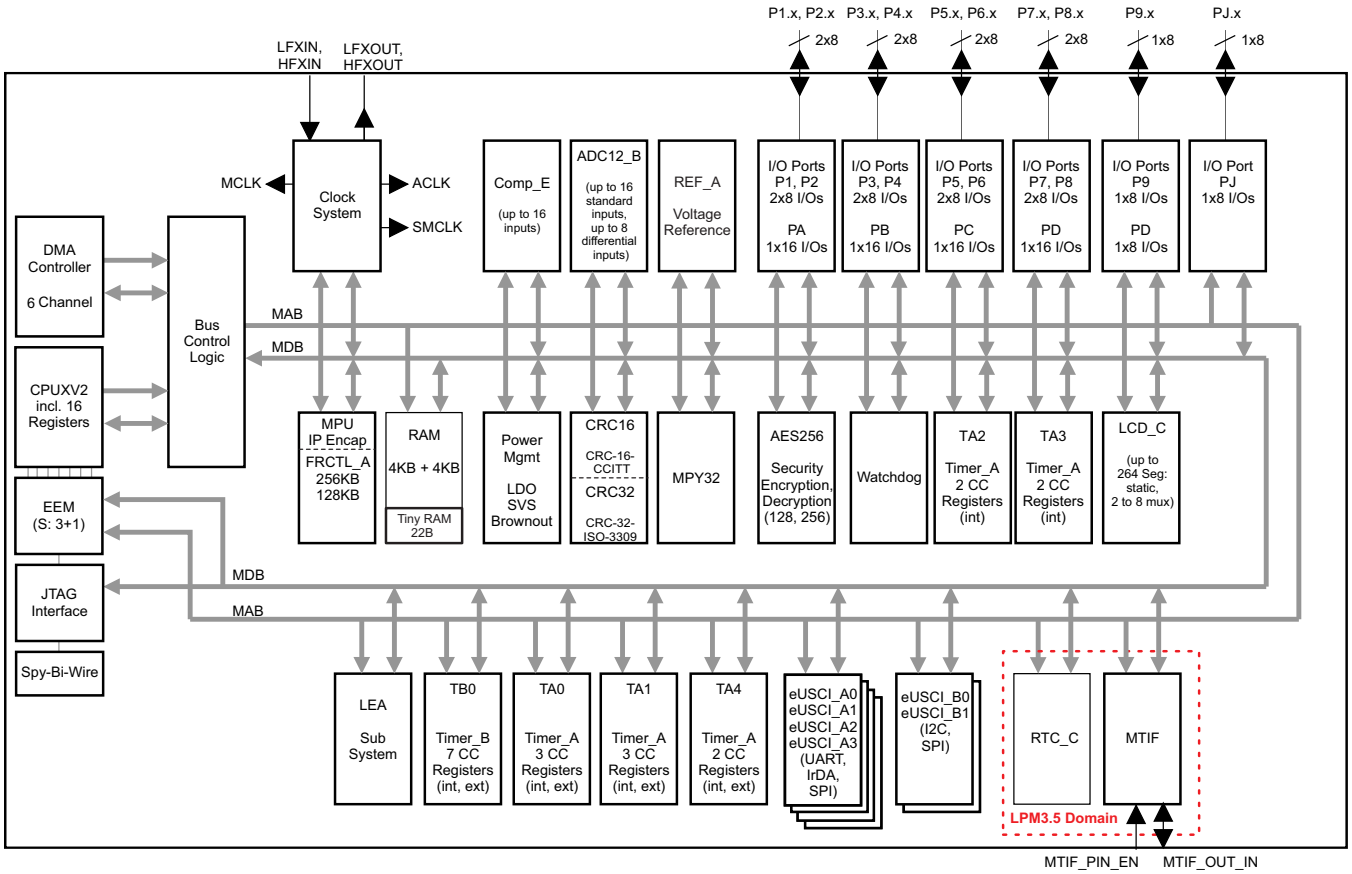
NOTE: このデバイスには8KBのRAMがあり、そのうち4KBはLEAサブシステムと共有されています。

図 1-1. MSP430FR604xの機能ブロック図



NOTE: このデバイスには8KBのRAMがあり、そのうち4KBはLEAサブシステムと共有されています。

図 1-2. MSP430FR603xの機能ブロック図

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2 改訂履歴

2017年12月16日発行分から2018年09月25日発行分への変更 **Page**

- Updated 3.1, *Related Products* 8
- Added note (1) to 表 5-2, *SVS* 39
- Changed capacitor value from 4.7 µF to 470 nF in 図 7-10, *ADC12_B Grounding and Noise Considerations* 173
- Changed capacitor value from 4.7 µF to 470 nF in the last paragraph of 7.2.1.2, *Design Requirements* 174
- 8.2「*デバイスの項目表記*」のテキストおよび図を更新 176

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3 Device Comparison

表 3-1 summarizes the available family members.

表 3-1. Device Comparison(1)(2)

DEVICE	FRAM (KB)	SRAM (KB)	CLOCK SYSTEM	LEA	USS USSXT	MTIF	ADC12_B	Comp_E	Timer_A(3)	Timer_B(4)	eUSCI		AES	BSL	I/Os	PACKAGE
											A(5)	B(6)				
MSP430FR6047	256	8	DCO **HFXT** **LFXT**	Yes	Yes	Yes	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2,2(8)	7	4	2	Yes	UART	76	100 PZ (LQFP)
MSP430FR60471	256	8	DCO **HFXT** **LFXT**	Yes	Yes	Yes	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2,2(8)	7	4	2	Yes	I^2C	76	100 PZ (LQFP)
MSP430FR6037	256	8	DCO **HFXT** **LFXT**	Yes	No	Yes	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2,2(8)	7	4	2	Yes	UART	76	100 PZ (LQFP)
MSP430FR60371	256	8	DCO **HFXT** **LFXT**	Yes	No	Yes	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2,2(8)	7	4	2	Yes	I^2C	76	100 PZ (LQFP)
MSP430FR6045	128	8	DCO **HFXT** **LFXT**	Yes	Yes	Yes	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2,2(8)	7	4	2	Yes	UART	76	100 PZ (LQFP)
MSP430FR6035	128	8	DCO **HFXT** **LFXT**	Yes	No	Yes	16 ext, 2 int ch.	16 ch.	3, 3(7) 2, 2,2(8)	7	4	2	Yes	UART	76	100 PZ (LQFP)

(1) For the most current package and ordering information, see the *Package Option Addendum* in 9, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having three capture/compare registers and PWM output generators and the second instantiation having five capture/compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having three capture/compare registers and PWM output generators and the second instantiation having five capture/compare registers and PWM output generators, respectively.
(5) eUSCI_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
(6) eUSCI_B supports I^2C with multiple slave addresses and SPI.
(7) Timers TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
(8) Timers TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any) whereas Timer TA4 provides internal, external capture/compare inputs and internal, external PWM outputs.

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3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing and measurement microcontrollers One platform. One ecosystem. Endless possibilities.

Products for MSP430 ultrasonic and performance sensing microcontrollers Ultra-low-power single-chip MCUs with integrated sensing peripherals

Companion products for MSP430FR6047 Review products that are frequently purchased or used with this product.

Reference designs for MSP430FR6047 The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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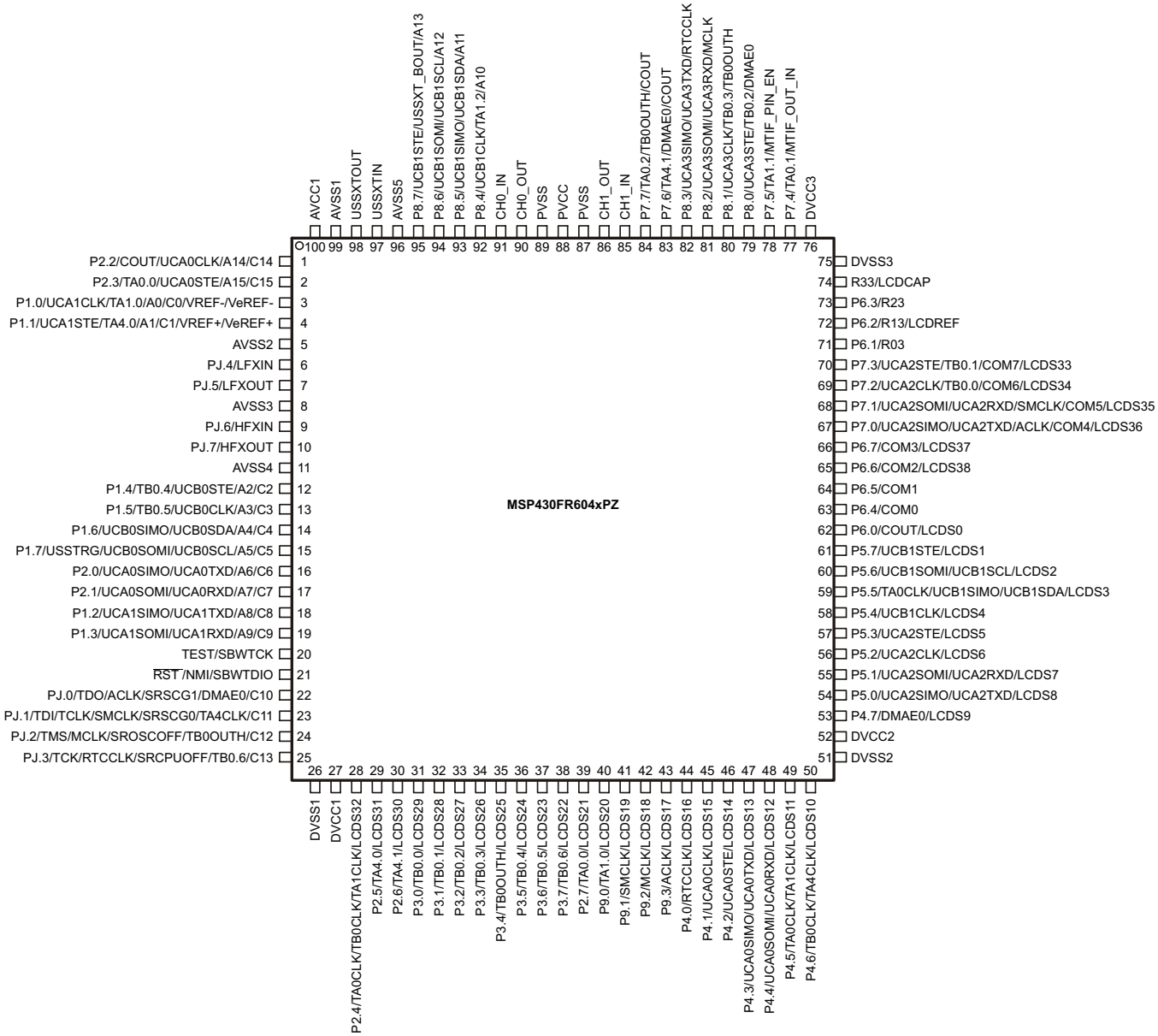
4 Terminal Configuration and Functions

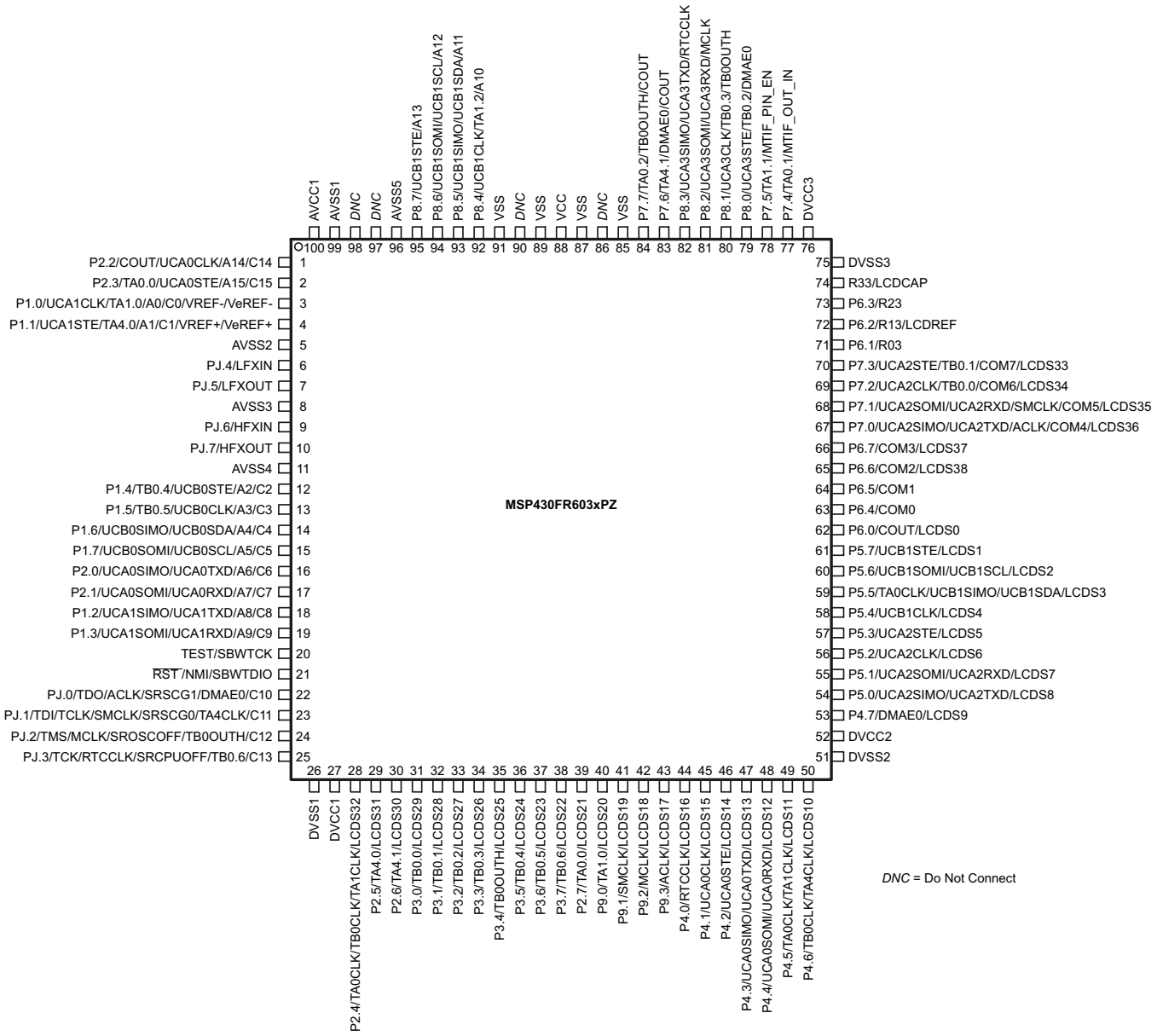
4.1 Pin Diagram

図 4-1 and 図 4-2 show the pinouts of the 100-pin PZ packages.



On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX
On devices with I^{2}C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

図 4-1. MSP430FR604x 100-Pin PZ Package (Top View)



On devices with UART BSL: P2.0 is BSLTX, P2.1 is BSLRX
On devices with I^{2}C BSL: P1.6 is BSLSDA, P1.7 is BSLSCL

図 4-2. MSP430FR603x 100-Pin PZ Package (Top View)

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4.2 Pin Attributes

表 4-1 lists the attributes of each pin.

表 4-1. Pin Attributes

PIN NUMBER	SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE (5)	RESET STATE AFTER BOR (6)
1	P2.2	I/O	LVCMOS	DVCC	OFF
	COUT	O	LVCMOS	DVCC	–
	UCA0CLK	I/O	LVCMOS	DVCC	–
	A14	I	Analog	DVCC	–
	C14	I	Analog	DVCC	–
2	P2.3	I/O	LVCMOS	DVCC	OFF
	TA0.0	I/O	LVCMOS	DVCC	–
	UCA0STE	I/O	LVCMOS	DVCC	–
	A15	I	Analog	DVCC	–
	C15	I	Analog	DVCC	–
3	P1.0	I/O	LVCMOS	DVCC	OFF
	UCA1CLK	I/O	LVCMOS	DVCC	–
	TA1.0	I/O	LVCMOS	DVCC	–
	A0	I	Analog	DVCC	–
	C0	I	Analog	DVCC	–
	VREF-	O	Analog	DVCC	–
	VeREF-	I	Analog	DVCC	–
4	P1.1	I/O	LVCMOS	DVCC	OFF
	UCA1STE	I/O	LVCMOS	DVCC	–
	TA4.0	I/O	LVCMOS	DVCC	–
	A1	I	Analog	DVCC	–
	C1	I	Analog	DVCC	–
	VREF+	O	Analog	DVCC	–
	VeREF+	I	Analog	DVCC	–
5	AVSS2	P	Power	–	N/A
6	PJ.4	I/O	LVCMOS	DVCC	OFF
	LFXIN	I	Analog	DVCC	–
7	PJ.5	I/O	LVCMOS	DVCC	OFF
	LFXOUT	O	Analog	DVCC	–
8	AVSS3	P	Power	–	N/A
9	PJ.6	I/O	LVCMOS	DVCC	–
	HFXIN	I	Analog	DVCC	–
10	PJ.7	I/O	LVCMOS	DVCC	OFF
	HFXOUT	O	Analog	DVCC	–
11	AVSS4	P	Power	–	N/A

(1) The signal that is listed first for each pin is the reset default pin name.
(2) To determine the pin mux encodings for each pin, see 6.14.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output.
(4) Buffer Types: LVCMOS, Analog, or Power (see 表 4-3 for details)
(5) The power source shown in this table is the I/O power source, which may differ from the module power source.
(6) Reset States:

OFF = High impedance with Schmitt-trigger input and pullup or pulldown (if available) disabled

PU = Pullup is enabled

PD = Pulldown is enabled

N/A = Not applicable

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表 4-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME[(1) (2)]	SIGNAL TYPE[(3)]	BUFFER TYPE[(4)]	POWER SOURCE[(5)]	RESET STATE AFTER BOR[(6)]
12	P1.4	I/O	LVCMOS	DVCC	OFF
	TB0.4	I/O	LVCMOS	DVCC	–
	UCB0STE	I/O	LVCMOS	DVCC	–
	A2	I	Analog	DVCC	–
	C2	I	Analog	DVCC	–
13	P1.5	I/O	LVCMOS	DVCC	OFF
	TB0.5	I/O	LVCMOS	DVCC	–
	UCB0CLK	I/O	LVCMOS	DVCC	–
	A3	I	Analog	DVCC	–
	C3	I	Analog	DVCC	–
14	P1.6	I/O	LVCMOS	DVCC	OFF
	UCB0SIMO	I/O	LVCMOS	DVCC	–
	UCB0SDA	I/O	LVCMOS	DVCC	–
	A4	I	Analog	DVCC	–
	C4	I	Analog	DVCC	–
15	P1.7	I/O	LVCMOS	DVCC	OFF
	USSTRG	I	LVCMOS	DVCC	–
	UCB0SOMI	I/O	LVCMOS	DVCC	–
	UCB0SCL	I/O	LVCMOS	DVCC	–
	A5	I	Analog	DVCC	–
	C5	I	Analog	DVCC	–
16	P2.0	I/O	LVCMOS	DVCC	OFF
	UCA0TXD	O	LVCMOS	DVCC	–
	UCA0SIMO	I/O	LVCMOS	DVCC	–
	A6	I	Analog	DVCC	–
	C6	I	Analog	DVCC	–
17	P2.1	I/O	LVCMOS	DVCC	OFF
	UCA0RXD	I	LVCMOS	DVCC	–
	UCA0SOMI	I/O	LVCMOS	DVCC	–
	A7	I	Analog	DVCC	–
	C7	I	Analog	DVCC	–
18	P1.2	I/O	LVCMOS	DVCC	OFF
	UCA1TXD	O	LVCMOS	DVCC	–
	UCA1SIMO	I/O	LVCMOS	DVCC	–
	A8	I	Analog	DVCC	–
	C8	I	Analog	DVCC	–
19	P1.3	I/O	LVCMOS	DVCC	OFF
	UCA1RXD	I	LVCMOS	DVCC	–
	UCA1SOMI	I/O	LVCMOS	DVCC	–
	A9	I	Analog	DVCC	–
	C9	I	Analog	DVCC	–
20	TEST	I	LVCMOS	DVCC	PD
	SBWTCK	I	LVCMOS	DVCC	–
21	$\overline{\text{RST}}$	I/O	LVCMOS	DVCC	PU
	NMI	I	LVCMOS	DVCC	–
	SBWTDIO	I/O	LVCMOS	DVCC	–

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表 4-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE (5)	RESET STATE AFTER BOR (6)
22	PJ.0	I/O	LVCMOS	DVCC	OFF
	TDO	O	LVCMOS	DVCC	–
	ACLK	O	LVCMOS	DVCC	–
	SRSCG1	O	LVCMOS	DVCC	–
	DMAE0	I	LVCMOS	DVCC	–
	C10	I	Analog	DVCC	–
23	PJ.1	I/O	LVCMOS	DVCC	OFF
	TDI	I	LVCMOS	DVCC	–
	TCLK	I	LVCMOS	DVCC	–
	SMCLK	O	LVCMOS	DVCC	–
	SRSCG0	O	LVCMOS	DVCC	–
	TA4CLK	I	LVCMOS	DVCC	–
	C11	I	Analog	DVCC	–
24	PJ.2	I/O	LVCMOS	DVCC	OFF
	TMS	I	LVCMOS	DVCC	–
	MCLK	O	LVCMOS	DVCC	–
	SROSCOFF	O	LVCMOS	DVCC	–
	TB0OUTH	I	LVCMOS	DVCC	–
	C12	I	Analog	DVCC	–
25	PJ.3	I/O	LVCMOS	DVCC	OFF
	TCK	I	LVCMOS	DVCC	–
	RTCCLK	O	LVCMOS	DVCC	–
	SRCPUOFF	O	LVCMOS	DVCC	–
	TB0.6	I/O	LVCMOS	DVCC	–
	C13	I	Analog	DVCC	–
26	DVSS1	P	Power	–	N/A
27	DVCC1	P	Power	–	N/A
28	P2.4	I/O	LVCMOS	DVCC	OFF
	TA0CLK	I	LVCMOS	DVCC	–
	TB0CLK	I	LVCMOS	DVCC	–
	TA1CLK	I	LVCMOS	DVCC	–
	S32	O	Analog	DVCC	–
29	P2.5	I/O	LVCMOS	DVCC	OFF
	TA4.0	I/O	LVCMOS	DVCC	–
	S31	O	Analog	DVCC	–
30	P2.6	I/O	LVCMOS	DVCC	OFF
	TA4.1	I/O	LVCMOS	DVCC	–
	S30	O	Analog	DVCC	–
31	P3.0	I/O	LVCMOS	DVCC	OFF
	TB0.0	I/O	LVCMOS	DVCC	–
	S29	O	Analog	DVCC	–
32	P3.1	I/O	LVCMOS	DVCC	OFF
	TB0.1	O	LVCMOS	DVCC	–
	S28	O	Analog	DVCC	–
33	P3.2	I/O	LVCMOS	DVCC	OFF
	TB0.2	O	LVCMOS	DVCC	–
	S27	O	Analog	DVCC	–

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表 4-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER BOR(6)
34	P3.3	I/O	LVCMOS	DVCC	OFF
	TB0.3	I/O	LVCMOS	DVCC	–
	S26	O	Analog	DVCC	–
35	P3.4	I/O	LVCMOS	DVCC	OFF
	TB0OUTH	I	LVCMOS	DVCC	–
	S25	O	Analog	DVCC	–
36	P3.5	I/O	LVCMOS	DVCC	OFF
	TB0.4	I/O	LVCMOS	DVCC	–
	S24	O	Analog	DVCC	–
37	P3.6	I/O	LVCMOS	DVCC	OFF
	TB0.5	I/O	LVCMOS	DVCC	–
	S23	O	Analog	DVCC	–
38	P3.7	I/O	LVCMOS	DVCC	OFF
	TB0.6	I/O	LVCMOS	DVCC	–
	S22	O	Analog	DVCC	–
39	P2.7	I/O	LVCMOS	DVCC	OFF
	TA0.0	I/O	LVCMOS	DVCC	–
	S21	O	Analog	DVCC	–
40	P9.0	I/O	LVCMOS	DVCC	OFF
	TA1.0	I/O	LVCMOS	DVCC	–
	S20	O	Analog	DVCC	–
41	P9.1	I/O	LVCMOS	DVCC	OFF
	SMCLK	O	LVCMOS	DVCC	–
	S19	O	Analog	DVCC	–
42	P9.2	I/O	LVCMOS	DVCC	OFF
	MCLK	O	LVCMOS	DVCC	–
	S18	O	Analog	DVCC	–
43	P9.3	I/O	LVCMOS	DVCC	OFF
	ACLK	O	LVCMOS	DVCC	–
	S17	O	Analog	DVCC	–
44	P4.0	I/O	LVCMOS	DVCC	OFF
	RTCCLK	O	LVCMOS	DVCC	–
	S16	O	Analog	DVCC	–
45	P4.1	I/O	LVCMOS	DVCC	OFF
	UCA0CLK	I/O	LVCMOS	DVCC	–
	S15	O	Analog	DVCC	–
46	P4.2	I/O	LVCMOS	DVCC	OFF
	UCA0STE	I/O	LVCMOS	DVCC	–
	S14	O	Analog	DVCC	–
47	P4.3	I/O	LVCMOS	DVCC	OFF
	UCA0TXD	O	LVCMOS	DVCC	–
	UCA0SIMO	I/O	LVCMOS	DVCC	–
	S13	O	Analog	DVCC	–
48	P4.4	I/O	LVCMOS	DVCC	OFF
	UCA0RXD	I	LVCMOS	DVCC	–
	UCA0SOMI	I/O	LVCMOS	DVCC	–
	S12	O	Analog	DVCC	–

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表 4-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE (5)	RESET STATE AFTER BOR (6)
49	P4.5	I/O	LVCMOS	DVCC	OFF
	TA0CLK	I	LVCMOS	DVCC	–
	TA1CLK	I	LVCMOS	DVCC	–
	S11	O	Analog	DVCC	–
50	P4.6	I/O	LVCMOS	DVCC	OFF
	TB0CLK	I	LVCMOS	DVCC	–
	TA4CLK	I	LVCMOS	DVCC	–
	S10	O	Analog	DVCC	–
51	DVSS2	P	Power	–	N/A
52	DVCC2	P	Power	–	N/A
53	P4.7	I/O	LVCMOS	DVCC	OFF
	DMAE0	I	LVCMOS	DVCC	–
	S9	O	Analog	DVCC	–
54	P5.0	I/O	LVCMOS	DVCC	OFF
	UCA2TXD	O	LVCMOS	DVCC	–
	UCA2SIMO	I/O	LVCMOS	DVCC	–
	S8	O	Analog	DVCC	–
55	P5.1	I/O	LVCMOS	DVCC	OFF
	UCA2RXD	I	LVCMOS	DVCC	–
	UCA2SOMI	I/O	LVCMOS	DVCC	–
	S7	O	Analog	DVCC	–
56	P5.2	I/O	LVCMOS	DVCC	OFF
	UCA2CLK	I/O	LVCMOS	DVCC	–
	S6	O	Analog	DVCC	–
57	P5.3	I/O	LVCMOS	DVCC	OFF
	UCA2STE	I/O	LVCMOS	DVCC	–
	S5	O	Analog	DVCC	–
58	P5.4	I/O	LVCMOS	DVCC	OFF
	UCB1CLK	I/O	LVCMOS	DVCC	–
	S4	O	Analog	DVCC	–
59	P5.5	I/O	LVCMOS	DVCC	OFF
	TA0CLK	I	LVCMOS	DVCC	–
	UCB1SIMO	I/O	LVCMOS	DVCC	–
	UCB1SDA	I/O	LVCMOS	DVCC	–
	S3	O	Analog	DVCC	–
60	P5.6	I/O	LVCMOS	DVCC	OFF
	UCB1SOMI	I/O	LVCMOS	DVCC	–
	UCB1SCL	I/O	LVCMOS	DVCC	–
	S2	O	Analog	DVCC	–
61	P5.7	I/O	LVCMOS	DVCC	OFF
	UCB1STE	I/O	LVCMOS	DVCC	–
	S1	O	Analog	DVCC	–
62	P6.0	I/O	LVCMOS	DVCC	OFF
	COUT	I	LVCMOS	DVCC	–
	S0	O	Analog	DVCC	–
63	P6.4	I/O	LVCMOS	DVCC	OFF
	COM0	O	Analog	DVCC	–

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表 4-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER BOR(6)
64	P6.5	I/O	LVCMOS	DVCC	OFF
	COM1	O	Analog	DVCC	–
65	P6.6	I/O	LVCMOS	DVCC	OFF
	COM2	O	Analog	DVCC	–
	S38	O	Analog	DVCC	–
66	P6.7	I/O	LVCMOS	DVCC	OFF
	COM3	O	Analog	DVCC	–
	S37	O	Analog	DVCC	–
67	P7.0	I/O	LVCMOS	DVCC	OFF
	UCA2TXD	O	LVCMOS	DVCC	–
	UCA2SIMO	I/O	LVCMOS	DVCC	–
	ACLK	O	LVCMOS	DVCC	–
	COM4	O	Analog	DVCC	–
	S36	O	Analog	DVCC	–
68	P7.1	I/O	LVCMOS	DVCC	OFF
	UCA2RXD	I	LVCMOS	DVCC	–
	UCA2SOMI	I/O	LVCMOS	DVCC	–
	SMCLK	O	LVCMOS	DVCC	–
	COM5	O	Analog	DVCC	–
	S35	O	Analog	DVCC	–
69	P7.2	I/O	LVCMOS	DVCC	OFF
	UCA2CLK	I/O	LVCMOS	DVCC	–
	TB0.0	I/O	LVCMOS	DVCC	–
	COM6	O	Analog	DVCC	–
	S34	O	Analog	DVCC	–
70	P7.3	I/O	LVCMOS	DVCC	OFF
	UCA2STE	I/O	LVCMOS	DVCC	–
	TB0.1	I/O	LVCMOS	DVCC	–
	COM7	O	Analog	DVCC	–
	S33	O	Analog	DVCC	–
71	P6.1	I/O	LVCMOS	DVCC	OFF
	R03	I/O	Analog	DVCC	–
72	P6.2	I/O	LVCMOS	DVCC	OFF
	R13	I/O	Analog	DVCC	–
	LCDREF	I	Analog	-	–
73	P6.3	I/O	LVCMOS	DVCC	OFF
	R23	I/O	Analog	DVCC	–
74	R33	I/O	Analog	DVCC	-
	LCDCAP	I/O	Analog	DVCC	–
75	DVSS3	P	Power	–	N/A
76	DVCC3	P	Power	–	N/A
77	P7.4	I/O	LVCMOS	DVCC	OFF
	TA0.1	I/O	LVCMOS	DVCC	–
	MTIF_OUT_IN	I/O	LVCMOS	DVCC	–
78	P7.5	I/O	LVCMOS	DVCC	OFF
	TA1.1	I/O	LVCMOS	DVCC	–
	MTIF_PIN_EN	I	LVCMOS	DVCC	–

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表 4-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER BOR(6)
79	P8.0	I/O	LVCMOS	DVCC	OFF
	UCA3STE	I/O	LVCMOS	DVCC	–
	TB0.2	I/O	LVCMOS	DVCC	–
	DMAE0	I	LVCMOS	DVCC	–
80	P8.1	I/O	LVCMOS	DVCC	OFF
	UCA3CLK	I/O	LVCMOS	DVCC	–
	TB0.3	I/O	LVCMOS	DVCC	–
	TB0OUTH	I	LVCMOS	DVCC	–
81	P8.2	I/O	LVCMOS	DVCC	OFF
	UCA3RXD	O	LVCMOS	DVCC	–
	UCA3SOMI	I/O	LVCMOS	DVCC	–
	MCLK	O	LVCMOS	DVCC	–
82	P8.3	I/O	LVCMOS	DVCC	OFF
	UCA3TXD	O	LVCMOS	DVCC	–
	UCA3SIMO	I/O	LVCMOS	DVCC	–
	RTCCLK	O	LVCMOS	DVCC	–
83	P7.6	I/O	LVCMOS	DVCC	OFF
	TA4.1	I/O	LVCMOS	DVCC	–
	DMAE0	I	LVCMOS	DVCC	–
	COUT	O	LVCMOS	DVCC	–
84	P7.7	I/O	LVCMOS	DVCC	OFF
	TA0.2	I/O	LVCMOS	DVCC	–
	TB0OUTH	I	LVCMOS	DVCC	–
	COUT	O	LVCMOS	DVCC	–
85	CH1_IN	I	Analog	PVCC	–
86	CH1_OUT	O	Analog	PVCC	–
87	PVSS	P	Power	–	N/A
88	PVCC	P	Power	–	N/A
89	PVSS	P	Power	–	N/A
90	CH0_OUT	O	Analog	PVCC	–
91	CH0_IN	I	Analog	PVCC	–
92	P8.4	I/O	LVCMOS	DVCC	OFF
	UCB1CLK	I/O	LVCMOS	DVCC	–
	TA1.2	I/O	LVCMOS	DVCC	–
	A10	I	Analog	DVCC	–
93	P8.5	I/O	LVCMOS	DVCC	OFF
	UCB1SIMO	I/O	LVCMOS	DVCC	–
	UCB1SDA	I/O	LVCMOS	DVCC	–
	A11	I	Analog	DVCC	–
94	P8.6	I/O	LVCMOS	DVCC	OFF
	UCB1SOMI	I/O	LVCMOS	DVCC	–
	UCB1SCL	I/O	LVCMOS	DVCC	–
	A12	I	Analog	DVCC	–
95	P8.7	I/O	LVCMOS	DVCC	OFF
	UCB1STE	I/O	LVCMOS	DVCC	–
	USSXT_BOUT	I/O	LVCMOS	DVCC	–
	A13	I	Analog	DVCC	–

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表 4-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME (1) (2)	SIGNAL TYPE (3)	BUFFER TYPE (4)	POWER SOURCE (5)	RESET STATE AFTER BOR (6)
96	AVSS5	P	Power	–	N/A
97	USSXTIN (7)	I	Analog	1.5V	–
98	USSXTOUT (7)	O	Analog	1.5V	–
99	AVSS1	P	Power	–	N/A
100	AVCC1	P	Power	–	N/A

(7) Do not connect USSXTIN and USSXTOUT pins to AVCC nor to DVCC. USSXTIN does not support bypass mode, so do not drive an external clock on the USSXTIN pin.

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4.3 Signal Descriptions

表 4-2 describes the signals.

表 4-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
ADC	A0	3	I	ADC analog input A0
	A1	4	I	ADC analog input A1
	A2	12	I	ADC analog input A2
	A3	13	I	ADC analog input A3
	A4	14	I	ADC analog input A4
	A5	15	I	ADC analog input A5
	A6	16	I	ADC analog input A6
	A7	17	I	ADC analog input A7
	A8	18	I	ADC analog input A8
	A9	19	I	ADC analog input A9
	A10	92	I	ADC analog input A10
	A11	93	I	ADC analog input A11
	A12	94	I	ADC analog input A12
	A13	95	I	ADC analog input A13
	A14	1	I	ADC analog input A14
	A15	2	I	ADC analog input A15
	VREF+	4	O	Output of positive reference voltage
	VREF-	3	O	Output of negative reference voltage
	VeREF+	4	I	Input for an external positive reference voltage to the ADC
	VeREF-	3	I	Input for an external negative reference voltage to the ADC
Clock	ACLK	22, 43, 67	O	ACLK output
	HFXIN	9	I	Input for high-frequency crystal oscillator HFXT
	HFXOUT	10	O	Output for high-frequency crystal oscillator HFXT
	LFXIN	6	I	Input for low-frequency crystal oscillator LFXT
	LFXOUT	7	O	Output of low-frequency crystal oscillator LFXT
	MCLK	24, 42, 81	O	MCLK output
	SMCLK	23, 41, 68	O	SMCLK output

(1) I = input, O = output, P = power

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
Comparator	C0	3	I	Comparator input C0
	C1	4	I	Comparator input C1
	C2	12	I	Comparator input C2
	C3	13	I	Comparator input C3
	C4	14	I	Comparator input C4
	C5	15	I	Comparator input C5
	C6	16	I	Comparator input C6
	C7	17	I	Comparator input C7
	C8	18	I	Comparator input C8
	C9	19	I	Comparator input C9
	C10	22	I	Comparator input C10
	C11	23	I	Comparator input C11
	C12	24	I	Comparator input C12
	C13	25	I	Comparator input C13
	C14	1	I	Comparator input C14
	C15	2	I	Comparator input C15
	COUT	1, 83, 84	O	Comparator output
DMA	DMAE0	22, 79, 83	I	External DMA trigger
Debug	SBWTCK	20	I	Spy-Bi-Wire input clock
	SBWTDIO	21	I/O	Spy-Bi-Wire data input/output
	SRCPUOFF	25	O	Low-power debug: CPU Status register bit CPUOFF
	SROSCOFF	24	O	Low-power debug: CPU Status register bit OSCOFF
	SRSCG0	23	O	Low-power debug: CPU Status register bit SCG0
	SRSCG1	22	O	Low-power debug: CPU Status register bit SCG1
	TCK	25	I	Test clock
	TCLK	23	I	Test clock input
	TDI	23	I	Test data input
	TDO	22	O	Test data output port
	TEST	20	I	Test mode pin, selects digital I/O on JTAG pins
	TMS	24	I	Test mode select
GPIO Port 1	P1.0	3	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.1	4	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.2	18	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.3	19	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.4	12	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.5	13	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.6	14	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P1.7	15	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5

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表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
GPIO Port 2	P2.0	16	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.1	17	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.2	1	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.3	2	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.4	28	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.5	29	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.6	30	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P2.7	39	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO Port 3	P3.0	31	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.1	32	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.2	33	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.3	34	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.4	35	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.5	36	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.6	37	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P3.7	38	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO Port 4	P4.0	44	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.1	45	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.2	46	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.3	47	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.4	48	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.5	49	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.6	50	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P4.7	53	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO Port 5	P5.0	54	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.1	55	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.2	56	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.3	57	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.4	58	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.5	59	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.6	60	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P5.7	61	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO Port 6	P6.0	62	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.1	71	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.2	72	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.3	73	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.4	63	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.5	64	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.6	65	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P6.7	66	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5

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表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
GPIO Port 7	P7.0	67	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P7.1	68	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P7.2	69	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P7.3	70	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P7.4	77	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P7.5	78	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P7.6	83	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P7.7	84	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO Port 8	P8.0	79	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P8.1	80	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P8.2	81	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P8.3	82	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P8.4	92	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P8.5	93	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P8.6	94	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P8.7	95	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO Port 9	P9.0	40	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P9.1	41	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P9.2	42	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
	P9.3	43	I/O	General-purpose digital I/O with port interrupt and wakeup from LPMx.5
GPIO Port J	PJ.0	22	I/O	General-purpose digital I/O
	PJ.1	23	I/O	General-purpose digital I/O
	PJ.2	24	I/O	General-purpose digital I/O
	PJ.3	25	I/O	General-purpose digital I/O
	PJ.4	6	I/O	General-purpose digital I/O
	PJ.5	7	I/O	General-purpose digital I/O
	PJ.6	9	I/O	General-purpose digital I/O
	PJ.7	10	I/O	General-purpose digital I/O
I^2C	UCB0SCL	15	I/O	I^2C clock for eUSCI_B0 I^2C mode
	UCB0SDA	14	I/O	I^2C data for eUSCI_B0 I^2C mode
	UCB1SCL	94, 60	I/O	I^2C clock for eUSCI_B1 I^2C mode
	UCB1SDA	93, 59	I/O	I^2C data for eUSCI_B1 I^2C mode

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表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
LCD	COM0	63	O	LCD common output COM0 for LCD backplane
	COM1	64	O	LCD common output COM1 for LCD backplane
	COM2	65	O	LCD common output COM2 for LCD backplane
	COM3	66	O	LCD common output COM3 for LCD backplane
	COM4	67	O	LCD common output COM4 for LCD backplane
	COM5	68	O	LCD common output COM5 for LCD backplane
	COM6	69	O	LCD common output COM6 for LCD backplane
	COM7	70	O	LCD common output COM7 for LCD backplane
	LCDCAP	74	I/O	LCD capacitor connection CAUTION: LCDCAP/R33 must be connected to DVSS if not used.
	LCDREF	72	I	External reference voltage input for regulated LCD voltage
	R03	71	I/O	Input/output port of lowest analog LCD voltage (V5)
	R13	72	I/O	Input/output port of third most positive analog LCD voltage (V3 or V4)
	R23	73	I/O	Input/output port of second most positive analog LCD voltage (V2)
	R33	74	I/O	Input/output port of most positive analog LCD voltage (V1) CAUTION: LCDCAP/R33 must be connected to DVSS if not used.
	S0	62	O	LCD segment output
	S1	61	O	LCD segment output
	S2	60	O	LCD segment output
	S3	59	O	LCD segment output
	S4	58	O	LCD segment output
	S5	57	O	LCD segment output
	S6	56	O	LCD segment output
	S7	55	O	LCD segment output
	S8	54	O	LCD segment output
	S9	53	O	LCD segment output
	S10	50	O	LCD segment output
	S11	49	O	LCD segment output
	S12	48	O	LCD segment output
	S13	47	O	LCD segment output
	S14	46	O	LCD segment output
	S15	45	O	LCD segment output
	S16	44	O	LCD segment output
	S17	43	O	LCD segment output
	S18	42	O	LCD segment output
	S19	41	O	LCD segment output
	S20	40	O	LCD segment output
	S21	39	O	LCD segment output
	S22	38	O	LCD segment output
	S23	37	O	LCD segment output
	S24	36	O	LCD segment output
	S25	35	O	LCD segment output
	S26	34	O	LCD segment output
	S27	33	O	LCD segment output
	S28	32	O	LCD segment output
	S29	31	O	LCD segment output

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表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
LCD (continued)	S30	30	O	LCD segment output
	S31	29	O	LCD segment output
	S32	28	O	LCD segment output
	S33	70	O	LCD segment output
	S34	69	O	LCD segment output
	S35	68	O	LCD segment output
	S36	67	O	LCD segment output
	S37	66	O	LCD segment output
	S38	65	O	LCD segment output
MTIF	MTIF_PIN_EN	78	I	Meter test interface pin enable
	MTIF_OUT_IN	77	I/O	Meter test interface input and output
Power	AVCC1	100	P	Analog power supply
	AVSS1	99	P	Analog ground supply
	AVSS2	5	P	Analog ground supply
	AVSS3	8	P	Analog ground supply
	AVSS4	11	P	Analog ground supply
	AVSS5	96	P	Analog ground supply
	DVCC1	27	P	Digital power supply
	DVCC2	52	P	Digital power supply
	DVCC3	76	P	Digital power supply
	DVSS1	26	P	Digital ground supply
	DVSS2	51	P	Digital ground supply
	DVSS3	75	P	Digital ground supply
	PVCC	88	P	USS power supply
	PVSS	87, 89	P	USS ground supply
RTC	RTCCLK	25, 44, 82	O	RTC clock calibration output

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表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
SPI	UCA0CLK	1, 45	I/O	Clock signal input for eUSCI_A0 SPI slave mode Clock signal output for eUSCI_A0 SPI master mode
	UCA0SIMO	16, 47	I/O	Slave in/master out for eUSCI_A0 SPI mode
	UCA0SOMI	17, 48	I/O	Slave out/master in for eUSCI_A0 SPI mode
	UCA0STE	2, 46	I/O	Slave transmit enable for eUSCI_A0 SPI mode
	UCA1CLK	3	I/O	Clock signal input for eUSCI_A1 SPI slave mode Clock signal output for eUSCI_A1 SPI master mode
	UCA1SIMO	18	I/O	Slave in/master out for eUSCI_A1 SPI mode
	UCA1SOMI	19	I/O	Slave out/master in for eUSCI_A1 SPI mode
	UCA1STE	4	I/O	Slave transmit enable for eUSCI_A1 SPI mode
	UCA2CLK	69, 56	I/O	Clock signal input for eUSCI_A2 SPI slave mode Clock signal output for eUSCI_A2 SPI master mode
	UCA2SIMO	67, 54	I/O	Slave in/master out for eUSCI_A2 SPI mode
	UCA2SOMI	68, 55	I/O	Slave out/master in for eUSCI_A2 SPI mode
	UCA2STE	70, 57	I/O	Slave transmit enable for eUSCI_A2 SPI mode
	UCA3CLK	80	I/O	Clock signal input for eUSCI_A3 SPI slave mode Clock signal output for eUSCI_A3 SPI master mode
	UCA3SIMO	82	I/O	Slave in/master out for eUSCI_A3 SPI mode
	UCA3SOMI	81	I/O	Slave out/master in for eUSCI_A3 SPI mode
	UCA3STE	79	I/O	Slave transmit enable for eUSCI_A3 SPI mode
	UCB0CLK	13	I/O	Clock signal input for eUSCI_B0 SPI slave mode Clock signal output for eUSCI_B0 SPI master mode
	UCB0SIMO	14	I/O	Slave in/master out for eUSCI_B0 SPI mode
	UCB0SOMI	15	I/O	Slave out/master in for eUSCI_B0 SPI mode
	UCB0STE	12	I/O	Slave transmit enable for eUSCI_B0 SPI mode
	UCB1CLK	92, 58	I/O	Clock signal input for eUSCI_B1 SPI slave mode Clock signal output for eUSCI_B1 SPI master mode
	UCB1SIMO	93, 59	I/O	Slave in/master out for eUSCI_B1 SPI mode
	UCB1SOMI	94, 60	I/O	Slave out/master in for eUSCI_B1 SPI mode
	UCB1STE	95, 61	I/O	Slave transmit enable for eUSCI_B1 SPI mode
System	NMI	21	I	Nonmaskable interrupt input
	$\overline{\text{RST}}$	21	I/O	Reset input active low

表 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
Timer	TA0.0	2	I/O	TA0 CCR0 capture: CCI0A input, compare: Out0
	TA0.0	39	I/O	TA0 CCR0 capture: CCI0B input, compare: Out0
	TA0.1	77	I/O	TA0 CCR1 capture: CCI1A input, compare: Out1
	TA0.2	84	I/O	TA0 CCR2 capture: CCI2A input, compare: Out2
	TA0CLK	28, 49, 59	I	TA0 input clock
	TA1.0	3	I/O	TA1 CCR0 capture: CCI0A input, compare: Out0
	TA1.0	40	I/O	TA1 CCR0 capture: CCI0B input, compare: Out0
	TA1.1	78	I/O	TA1 CCR1 capture: CCI1A input, compare: Out1
	TA1.2	92	I/O	TA1 CCR2 capture: CCI2A input, compare: Out2
	TA1CLK	28, 49	I	TA1 input clock
	TA4.0	4	I/O	TA4 CCR0 capture: CCI0A input, compare: Out0
	TA4.0	29	I/O	TA4 CCR0 capture: CCI0B input, compare: Out0
	TA4.1	30	I/O	TA4CCR1 capture: CCI1B input, compare: Out1
	TA4.1	83	I/O	TA4 CCR1 capture: CCI1A input, compare: Out1
	TA4CLK	23, 50	I	TA4 input clock
	TB0.0	31	I/O	TB0 CCR0 capture: CCI0B input, compare: Out0
	TB0.0	69	I/O	TB0 CCR0 capture: CCI0A input, compare: Out0
	TB0.1	32	I/O	TB0 CCR1 capture: CCI1A input, compare: Out1
	TB0.1	70	O	TB0 CCR1 compare: Out1
	TB0.2	33	I/O	TB0 CCR2 capture: CCI2A input, compare: Out2
	TB0.2	79	O	TB0 CCR2 compare: Out2
	TB0.3	34	I/O	TB0 CCR3 capture: CCI3A input, compare: Out3
	TB0.3	80	I/O	TB0 CCR3 capture: CCI3B input, compare: Out3
	TB0.4	12	I/O	TB0 CCR4 capture: CCI4A input, compare: Out4
	TB0.4	36	I/O	TB0 CCR4 capture: CCI4B input, compare: Out4
	TB0.5	13	I/O	TB0 CCR5 capture: CCI5A input, compare: Out5
	TB0.5	37	I/O	TB0CCR5 capture: CCI5B input, compare: Out5
	TB0.6	25	I/O	TB0 CCR6 capture: CCI6B input, compare: Out6
	TB0.6	38	I/O	TB0 CCR6 capture: CCI6A input, compare: Out6
	TB0CLK	28, 50	I	TB0 clock input
	TB0OUTH	24, 35, 80, 84	I	Switch all PWM outputs high impedance input – TB0
UART	UCA0RXD	17, 48	I	Receive data for eUSCI_A0 UART mode
	UCA0TXD	16, 47	O	Transmit data for eUSCI_A0 UART mode
	UCA1RXD	19	I	Receive data for eUSCI_A1 UART mode
	UCA1TXD	18	O	Transmit data for eUSCI_A1 UART mode
	UCA2RXD	68, 55	I	Receive data for eUSCI_A2 UART mode
	UCA2TXD	67, 54	O	Transmit data for eUSCI_A2 UART mode
	UCA3RXD	81	I	Receive data for eUSCI_A3 UART mode
	UCA3TXD	82	O	Transmit data for eUSCI_A3 UART mode

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表 **4-2. Signal Descriptions (continued)**

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE(1)	DESCRIPTION
		PZ		
USS	USSTRG	15	I	USS trigger
	USSXTIN	97	I	Input for crystal or resonator of oscillator USSXT
	USSXTOUT	98	O	Output for crystal or resonator of oscillator USSXT
	USSXT_BOUT	95	O	Buffered output clock of USSXT
	CH0_IN	91	I	USS channel 0 RX
	CH0_OUT	90	I/O	USS channel 0 TX
	CH1_IN	85	I	USS channel 1 RX
	CH1_OUT	86	I/O	USS channel 1 TX

4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see 6.14.

4.5 Buffer Type

表 4-3 describes the buffer types that are referenced in 表 4-1.

表 4-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PULLUP (PU) OR PULLDOWN (PD)	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
Analog (1)	3.0 V	N	N/A	N/A	N/A	See analog modules in 5 for details.
LVCMOS	3.0 V	Y (2)	Programmable	See 5.13.5.	See 5.13.5.	
Power (DVCC) (3)	3.0 V	N	N/A	N/A	N/A	SVS enables hysteresis on DVCC.
Power (AVCC) (3)	3.0 V	N	N/A	N/A	N/A	
Power (PVCC) (3)	3.0 V	N	N/A	N/A	N/A	
Power (DVSS and AVSS) (3)	0 V	N	N/A	N/A	N/A	

(1) This is a switch, not a buffer.
(2) Only for input pins
(3) This is supply input, not a buffer.

4.6 Connection of Unused Pins

表 4-4 lists the correct termination of unused pins.

表 4-4. Connection of Unused Pins (1)

PIN	POTENTIAL	COMMENT
AVCC	DV_{CC}	
PVCC	DV_{CC}	
AVSS	DV_{SS}	
PVSS	DV_{SS}	
CHx_IN, CHx_OUT	DV_{SS}	
USSXTIN	DV_{SS}	Do not connect to DVCC, AVCC, or PVCC
USSXTOUT	Open	
Px.0 to Px.7	Open	Switched to port function, output direction (PxDIR.n = 1)
$\overline{RST}$/NMI/SBWTDIO	DV_{CC} or V_{CC}	47-kΩ pullup or internal pullup selected with 10-nF (2.2-nF (2)) pulldown
PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK	Open	The JTAG pins are shared with general-purpose I/O function (PJ.x). If these pins are not used, set them to port function, output direction. If used as JTAG pins, leave them open.
TEST	Open	This pin always has an internal pulldown enabled.

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 pins.
(2) The pulldown capacitor must not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]	At DVCC and AVCC pins	–0.3	4.1	V
		At DVCC, AVCC, and PVCC pins	–0.3	4.1	
	Voltage difference between DVCC and AVCC pins[3]			±0.3	V
	Voltage difference among DVCC, AVCC, and PVCC pins[3]			±0.3	V
V_I	Input voltage[2]	Applied to CHx_IN	–0.3	1.65	V
		Applied to CHx_IN with a duty cycle of 10% over 1 ms	–0.3	1.8	
		Applied to USSXTIN (USSXTOUT)	–0.3	1.5	
		Applied to any other pin	–0.3	V_{CC} + 0.3 V (4.1 V Max)	
	Diode current at any device pin			±2	mA
T_{stg}	Storage temperature [4]		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to V_{SS}.
(3) Voltage differences between DVCC and AVCC that exceed the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (all except CHx_OUT terminals)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	
$V_{(ESD)}$	Electrostatic discharge (on CHx_OUT terminals)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

TYP data are based on V_{CC} = 3.0 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins(1) (2) (3) (4)		1.8(5)		3.6	V
V_{CC}	Supply voltage range applied at PVCC pin(1)		2.2		3.6	V
V_{SS}	Supply voltage applied at all DVSS, AVSS, and PVSS pins			0		V
T_A	Operating free-air temperature		–40		85	°C
C_{DVCC}	Capacitor value at DVCC(6)		1 – 20%			µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(7)	No FRAM wait states (NWAITSx = 0)	0		8(8)	MHz
		With FRAM wait states (NWAITSx = 1)(9)	0		16(10)	
f_{LEA}	LEA processor frequency		0		16(10)	
f_{ACLK}	Maximum ACLK frequency				50	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(10)	MHz

(1) TI recommends powering the AVCC, DVCC, PVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference among AVCC, DVCC, PVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/µs). Following the recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
(3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(4) The USS module must be disabled if AVCC and DVCC are lower than 2.2 V.
(5) The minimum supply voltage is defined by the supervisor SVS levels. See the PMM SVS threshold parameters for the exact values.
(6) As a decoupling capacitor for each supply pin pair (DVCC and DVSS or AVCC and AVSS), place a low-ESR 100-nF (minimum) ceramic capacitor as close as possible (within a few millimeters) to the respective pin pairs. For the PVCC and PVSS pair, place a low-ESR 22-µF (minimum) ceramic capacitor as close as possible (within a few millimeters) to the pin pair.
(7) Modules may have a different maximum input clock specification. See the specification of each module in this data sheet.
(8) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted.
(9) Wait states occur only on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always excecuted without wait states.
(10) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted. If a clock source with a higher typical value is used, the clock must be divided in the clock system.

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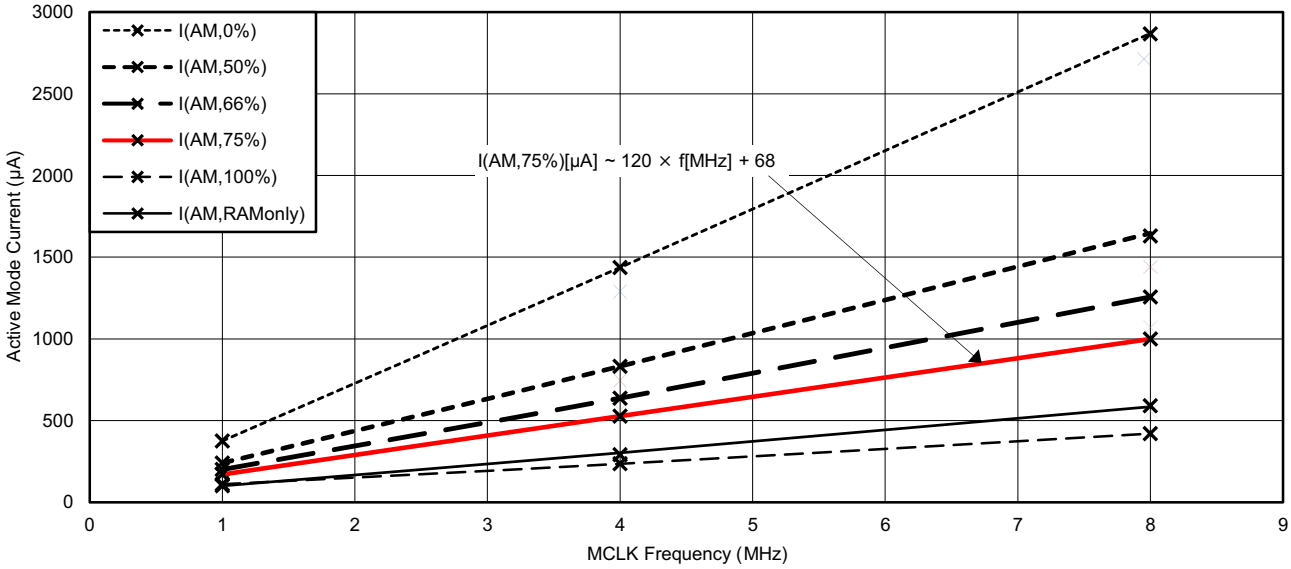
5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	EXECUTION MEMORY	V_{CC}	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)										UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		4 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		12 MHz 1 WAIT STATE (NWAITSx = 1)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM_UNI}$ (Unified memory)(3)	FRAM	3.0 V	225		665		1275		1550		1970		µA
$I_{AM, FRAM}$ (0%)(4) (5)	FRAM 0% cache hit ratio	3.0 V	420		1455		2850		2330		3000		µA
$I_{AM, FRAM}$ (50%)(4) (5)	FRAM 50% cache hit ratio	3.0 V	275		855	1022	1650	1888	1770	2041	2265	2606	µA
$I_{AM, FRAM}$ (66%)(4) (5)	FRAM 66% cache hit ratio	3.0 V	220		650		1240	1443	1490	1735	1880	2197	µA
$I_{AM, FRAM}$ (75%)(4) (5)	FRAM 75% cache hit ratio	3.0 V	192	261	535		1015	1170	1290	1490	1620	1870	µA
$I_{AM, FRAM}$ (100%)(4) (5)	FRAM 100% cache hit ratio	3.0 V	125		237		450		670		790		µA
$I_{AM, RAM}$ (6) (5)	RAM	3.0 V	140		323		590		880		1070		µA
$I_{AM, RAM\ only}$ (7) (5)	RAM	3.0 V	90	182	292		540		830		1020	1313	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, f_{DCO} = 24 MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO}/2$.
At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ($f_{MCLK,eff}$) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.
The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff} = f_{MCLK}$ / [wait states × (1 – cache hit ratio) + 1]
For example, with 1 wait state and 75% cache hit ratio, $f_{MCKL,eff} = f_{MCLK}$ / [1 × (1 – 0.75) + 1] = f_{MCLK} / 1.25.
(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.
(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesess divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.
(5) See for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Section 5.4.
(6) Program and data reside entirely in RAM. All execution is from RAM.
(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

5.5 Typical Characteristics, Active Mode Supply Currents



A. $I_{(AM,cache\ hit\ ratio)}$: Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

B. $I_{(AM,RAMonly)}$: Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

図 5-1. Typical Active Mode Supply Currents, No Wait States

5.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	FREQUENCY (f_{SMCLK})										UNIT
		1 MHz		4 MHz		8 MHz		12 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	2.2 V	80		115		180		276		250		µA
	3.0 V	95	148	125	178	190	245	286	340	265	316	
I_{LPM1}	2.2 V	40		70		136		230		205		µA
	3.0 V	40	70	70		136		235		210	250	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} at specified frequency, except for 12 MHz. For 12 MHz, f_{DCO} = 24 MHz and f_{MCLK} = f_{SMCLK} = f_{DCO} / 2.

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5.7 Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 5-2 and 図 5-3)

PARAMETER		V_{CC}	TEMPERATURE								UNIT
			–40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM2,XT12}$	Low-power mode 2, 12-pF crystal(1) (2) (3)	2.2 V	0.8		1.3		4.1		10.8		µA
		3 V	0.8		1.3		4.1		10.8		
$I_{LPM2,XT3.7}$	Low-power mode 2, 3.7-pF crystal(1) (4) (3)	2.2 V	0.6		1.2		4.0		10.7		µA
		3 V	0.6		1.2		4.0		10.7		
$I_{LPM2,VLO}$	Low-power mode 2, VLO, includes SVS(5)	2.2 V	0.5		1.0		3.8		10.5		µA
		3 V	0.5		1.0		3.8		10.5		
$I_{LPM3,XT12}$	Low-power mode 3, 12-pF crystal, includes SVS(1) (2) (6)	2.2 V	0.8	1.1	1.0		2.2		4.5	10.1	µA
		3 V	0.8		1.0		2.2		4.5		
$I_{LPM3,XT3.7}$	Low-power mode 3, 3.7-pF crystal, excludes SVS(1) (4) (7)	2.2 V	0.5		0.7		2.1		4.4	9.8	µA
		3 V	0.5		0.7		2.1		4.4	9.8	
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS(8)	2.2 V	0.4		0.5	1.2	1.9		4.2	9.6	µA
		3 V	0.4		0.5		1.9		4.2		
$I_{LPM3,VLO,RAMoff}$	Low-power mode 3, VLO, excludes SVS, RAM powered-down completely(8)	2.2 V	0.36		0.47	1.1	1.4	2.9	2.6	8.2	µA
		3 V	0.36		0.47		1.4		2.6		
$I_{LPM4,SVS}$	Low-power mode 4, includes SVS(9)	2.2 V	0.5		0.6	1.2	1.9		4.3	9.7	µA
		3 V	0.5	0.8	0.6		1.9		4.3		

(1) Not applicable for devices with HF crystal oscillator only.
(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(3) Low-power mode 2, crystal oscillator test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2), f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(5) Low-power mode 2, VLO test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2), f_{XT1} = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) Low-power mode 3, 12-pF crystal including SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
(7) Low-power mode 3, 3.7-pF crystal excluding SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
(8) Low-power mode 3, VLO excluding SVS test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). RAM disabled (RCCTL0 = 5A55h). Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), f_{XT1} = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
(9) Low-power mode 4 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

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Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 5-2 and 図 5-3)

PARAMETER		V_{CC}	TEMPERATURE								UNIT
			–40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM4}	Low-power mode 4, excludes SVS(10)	2.2 V	0.3		0.4	1.1	1.7		4.0	9.4	µA
		3 V	0.3		0.4		1.7		4.0		
$I_{LPM4,RAMoff}$	Low-power mode 4, excludes SVS, RAM powered-down completely(10)	2.2 V	0.3		0.37	1.0	1.2	2.8	2.5	8	µA
		3 V	0.3		0.37		1.2		2.5		
$I_{IDLE,GroupA}$	Additional idle current if one or more modules from Group A (see 表 6-3) are activated in LPM3 or LPM4	3 V			0.02				0.3		µA
$I_{IDLE,GroupB}$	Additional idle current if one or more modules from Group B (see 表 6-3) are activated in LPM3 or LPM4	3 V			0.02				0.35		µA
$I_{IDLE,GroupC}$	Additional idle current if one or more modules from Group C (see 表 6-3) are activated in LPM3 or LPM4	3 V			0.02				0.38		µA

(10) Low-power mode 4 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, f_{MCLK} = f_{SMCLK} = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

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5.8 Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	TEMPERATURE (T_A)								UNIT
			–40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT12}$ LCD, ext. bias	Low-power mode 3 (LPM3) current,12 pF crystal, LCD 4-mux mode, external biasing, excludes SVS (1) (2)	3.0 V	0.9		1.1		2.5		5.1		µA
$I_{LPM3,XT12}$ LCD, int. bias	Low-power mode 3 (LPM3) current,12 pF crystal, LCD 4-mux mode, internal biasing, charge pump disabled, excludes SVS (1) (3)	3.0 V	1.3		1.4	2.0	2.2	4.5	4.9	12.5	µA
$I_{LPM3,XT12}$ LCD,CP	Low-power mode 3 (LPM3) current,12 pF crystal, LCD 4-mux mode, internal biasing, charge pump enabled, 1/3 bias, excludes SVS (1) (4)	2.2 V	3.6		4		5.1		8.1		µA
		3.0 V	3.4		3.7		4.9		8.1		µA

(1) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current - idle current of Group containing LCD module already included. Refer to the idle currents specified for the respective peripheral groups.

(2) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Current through external resistors not included (voltage levels are supplied by test equipment).
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(3) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 (V_{LCD} = 3 V typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

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5.9 Low-Power Mode (LPMx.5) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 5-4 and 図 5-5)

PARAMETER		V_{CC}	TEMPERTURE (T_A)								UNIT
			–40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5,XT12}$	Low-power mode 3.5, 12-pF crystal including SVS(1) (2) (3)	2.2 V	0.45		0.5		0.55		0.75		µA
		3.0 V	0.45		0.5		0.55		0.75		
$I_{LPM3.5,XT3.7}$	Low-power mode 3.5, 3.7-pF crystal excluding SVS(1) (4) (5)	2.2 V	0.3		0.35		0.4		0.65		µA
		3.0 V	0.3		0.35		0.4		0.65		
$I_{LPM4.5,SVS}$	Low-power mode 4.5, including SVS(6)	2.2 V	0.23		0.2		0.28		0.4		µA
		3.0 V	0.23		0.2		0.28		0.4		
$I_{LPM4.5}$	Low-power mode 4.5, excluding SVS(7)	2.2 V	0.035		0.045		0.075		0.15		µA
		3.0 V	0.035		0.045		0.075		0.15		

(1) Not applicable for devices with HF crystal oscillator only.
(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
(3) Low-power mode 3.5, 1-pF crystal including SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(5) Low-power mode 3.5, 3.7-pF crystal excluding SVS test conditions:
Current for RTC clocked by XT1 included.Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) Low-power mode 4.5 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(7) Low-power mode 4.5 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, f_{ACLK} = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz

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5.10 Typical Characteristics, Low-Power Mode Supply Currents

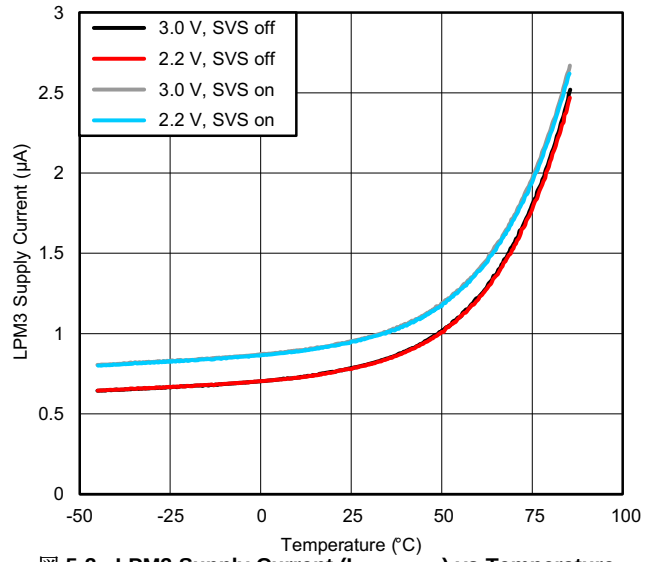

図 5-2. LPM3 Supply Current ($I_{LPM3,XT3.7}$) vs Temperature

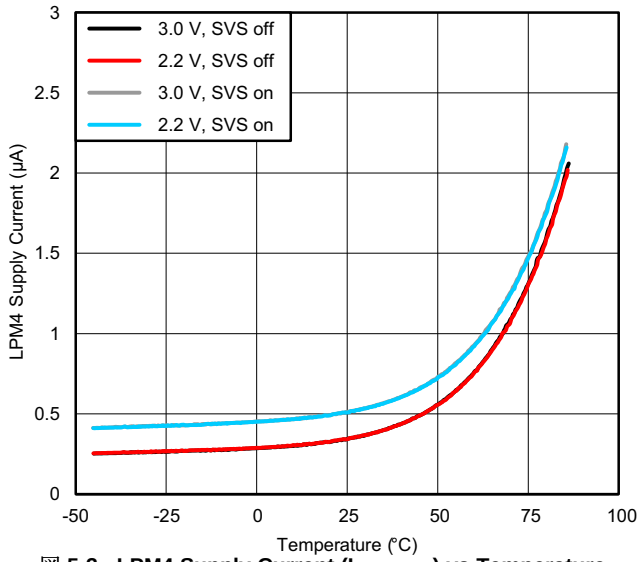

図 5-3. LPM4 Supply Current ($I_{LPM4,SVS}$) vs Temperature

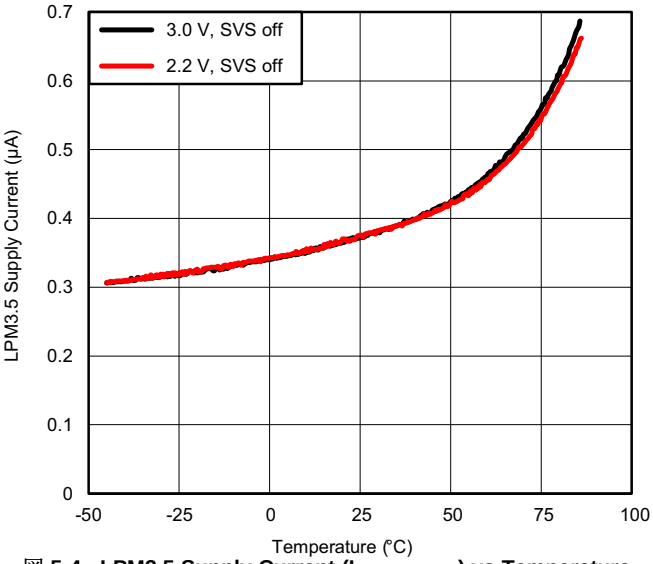

図 5-4. LPM3.5 Supply Current ($I_{LPM3.5,XT3.7}$) vs Temperature

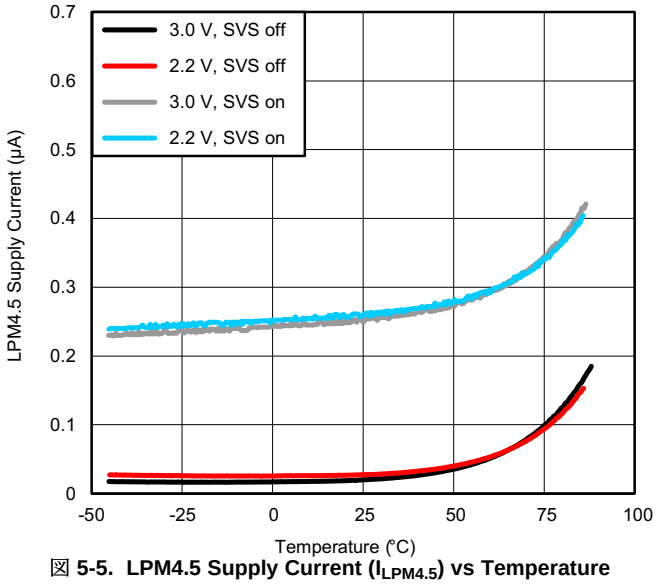

図 5-5. LPM4.5 Supply Current ($I_{LPM4.5}$) vs Temperature

5.11 Typical Characteristics, Current Consumption per Module(1)

MODULE	TEST CONDITIONS	REFERENCE CLOCK	MIN	TYP	MAX	UNIT
Timer_A		Module input clock		2.5		µA/MHz
Timer_B		Module input clock		3.8		µA/MHz
eUSCI_A	UART mode	Module input clock		6.3	7.0	µA/MHz
	SPI mode			4.4	4.8	
eUSCI_B	SPI mode	Module input clock		4.4		µA/MHz
	I^2C mode, 100 kbaud			4.4		
RTC_C		32 kHz		100		nA
MPY	Only from start to end of operation	MCLK		28		µA/MHz
CRC16	Only from start to end of operation	MCLK		3.3		µA/MHz
CRC32	Only from start to end of operation	MCLK		3.3		µA/MHz
LEA	256-point complex FFT, data = nonzero	MCLK	68	86		µA/MHz
	256-point complex FFT, data = zero			66		
MTIF	Generator and counter are enabled at 256 Hz, no terminal activity, pulse rate = 15 pulses	LFXT		0.20		µA

(1) For other module currents not listed here, see the module-specific parameter sections.

5.12 Thermal Resistance Characteristics for 100-Pin LQFP (PZ) Package(1)

THERMAL METRIC(2)		VALUE(3)	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	57.6	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance	14.9	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance	35.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter	35.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter	0.6	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) N/A = not applicable
(2) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

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5.13 Timing and Switching Characteristics

5.13.1 Power Supply Sequencing

TI recommends powering the AVCC, DVCC, and PVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference among AVCC, DVCC, and PVCC must not exceed the limits specified in Section 5.1. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.

表 5-1 lists the power ramp requirements for brownout and power up.

表 5-1. Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{VCC_BOR-}	Brownout power-down level(1)	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s	0.7	1.66	V
V_{VCC_BOR+}	Brownout power-up level(1)	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s(2)	0.79	1.68	V

(1) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/µs). Following the recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
(2) The brownout levels are measured with a slowly changing supply.

表 5-2 lists the characteristics of the SVS.

表 5-2. SVS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SVSH,LPM}$	SVS_H current consumption, low-power modes			170	300	nA
V_{SVSH-}	SVS_H power-down level(1)		1.75	1.80	1.85	V
V_{SVSH+}	SVS_H power-up level(1)		1.77	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis		40		120	mV
$t_{PD,SVSH,\ AM}$	SVS_H propagation delay, active mode	$dV_{Vcc}/dt = -10$ mV/µs			10	µs

(1) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

5.13.2 Reset Timing

表 5-3 lists the requirements for the reset input.

表 5-3. Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
$t_{(RST)}$	External reset pulse duration on $\overline{RST}$ (1)	2.2 V, 3.0 V	2			µs

(1) Not applicable if the $\overline{RST}$/NMI pin is configured as NMI.

5.13.3 Clock Specifications

Table 5-4 lists the characteristics of the low-frequency oscillator.

Table 5-4. Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC.LFXT}$	Current consumption	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 3.7 pF, ESR ≈ 44 kΩ	3.0 V		180		nA
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {1}, T_A = 25°C, $C_{L,eff}$ = 6 pF, ESR ≈ 40 kΩ			185		
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {2}, T_A = 25°C, $C_{L,eff}$ = 9 pF, ESR ≈ 40 kΩ			225		
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF, ESR ≈ 40 kΩ			330		
f_{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0			32768		Hz
DC_{LFXT}	LFXT oscillator duty cycle	Measured at ACLK, f_{LFXT} = 32768 Hz		30%		70%	
$f_{LFXT,SW}$	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 (2) (3)		10.5	32.768	50	kHz
$DC_{LFXT, SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%		70%	
OA_{LFXT}	Oscillation allowance for LF crystals (4)	LFXTBYPASS = 0, LFXTDRIVE = {1}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF			300		

(1) To improve EMI on the LFXT oscillator, observe the following guidelines:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
- Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF
- For LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {3}, 9 pF ≤ $C_{L,eff}$ ≤ 12.5 pF

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Table 5-4. Low-Frequency Crystal Oscillator, LFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{LFXIN}	Integrated load capacitance at LFXIN terminal[5] [6]				2		pF
C_{LFXOUT}	Integrated load capacitance at LFXOUT terminal[5] [6]				2		pF
$t_{START,LFXT}$	Start-up time[7]	f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 3.7 pF	3.0 V		800		ms
		f_{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF	3.0 V		1000		
$f_{Fault,LFXT}$	Oscillator fault frequency[8] [9]			0		3500	Hz

(5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} is the total capacitance at the LFXIN and LFXOUT terminals, respectively.
(6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(7) Includes start-up counter of 1024 clock cycles.
(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications may set the flag. A static condition or stuck at fault condition will set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the characteristics of the high-frequency oscillator.

Table 5-5. High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.HFXT}$	HFXT oscillator crystal current HF mode at typical ESR	f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1[2], T_A = 25°C, $C_{L,eff}$ = 18 pF, typical ESR, C_{shunt}	3.0 V		75		µA
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, T_A = 25°C, $C_{L,eff}$ = 18 pF, typical ESR, C_{shunt}			120		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, T_A = 25°C, $C_{L,eff}$ = 18 pF, typical ESR, C_{shunt}			190		
		f_{OSC} = 24 MHz HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T_A = 25°C, $C_{L,eff}$ = 18 pF, typical ESR, C_{shunt}			250		
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 1[2] [3]		4		8	MHz
		HFXTBYPASS = 0, HFFREQ = 2[3]		8.01		16	
		HFXTBYPASS = 0, HFFREQ = 3[3]		16.01		24	

(1) To improve EMI on the HFXT oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
- Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.
(3) Maximum frequency of operation of the entire device cannot be exceeded.

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Table 5-5. High-Frequency Crystal Oscillator, HFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
DC_{HFXT}	HFXT oscillator duty cycle	Measured at SMCLK, f_{HFXT} = 16 MHz		40%	50%	60%	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1, HFFREQ = 0[4] [3]		0.9		4	MHz
		HFXTBYPASS = 1, HFFREQ = 1[4] [3]		4.01		8	
		HFXTBYPASS = 1, HFFREQ = 2[4] [3]		8.01		16	
		HFXTBYPASS = 1, HFFREQ = 3[4] [3]		16.01		24	
$DC_{HFXT,SW}$	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1		40%		60%	
OA_{HFXT}	Oscillation allowance for HFXT crystals[5]	HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1[2], $f_{HFXT,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF			450		Ω
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $f_{HFXT,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF			320		
		HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, $f_{HFXT,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF			200		
		HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, $f_{HFXT,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF			200		
$t_{START,HFXT}$	Start-up time[6]	f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1, T_A = 25°C, $C_{L,eff}$ = 16 pF	3.0 V		1.6		ms
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T_A = 25°C, $C_{L,eff}$ = 16 pF	3.0 V		0.6		
C_{HFXIN}	Integrated load capacitance at HFXIN terminal[7] [8]				2		pF
C_{HFXOUT}	Integrated load capacitance at HFXOUT terminal[7] [8]				2		pF
$f_{Fault,HFXT}$	Oscillator fault frequency[9] [10]			0		800	kHz

(4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by $DC_{HFXT, SW}$.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes start-up counter of 1024 clock cycles.
(7) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} is the total capacitance at the HFXIN and HFXOUT terminals, respectively.
(8) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition will set the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-6 lists the characteristics of the DCO.

Table 5-6. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{DCO1}	DCO frequency range 1 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 0, DCORSEL = 1, DCOFSEL = 0			1	±3.5%	MHz
$f_{DCO2.7}$	DCO frequency range 2.7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 1			2.667	±3.5%	MHz
$f_{DCO3.5}$	DCO frequency range 3.5 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 2			3.5	±3.5%	MHz
f_{DCO4}	DCO frequency range 4 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 3			4	±3.5%	MHz
$f_{DCO5.3}$	DCO frequency range 5.3 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 4, DCORSEL = 1, DCOFSEL = 1			5.333	±3.5%	MHz
f_{DCO7}	DCO frequency range 7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 5, DCORSEL = 1, DCOFSEL = 2			7	±3.5%	MHz
f_{DCO8}	DCO frequency range 8 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 6, DCORSEL = 1, DCOFSEL = 3			8	±3.5%	MHz
f_{DCO16}	DCO frequency range 16 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 1, DCOFSEL = 4			16	±3.5% (1)	MHz
f_{DCO21}	DCO frequency range 21 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 5			21	±3.5% (1)	MHz
f_{DCO24}	DCO frequency range 24 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 6			24	±3.5% (1)	MHz
$f_{DCO,DC}$	Duty cycle	Measured at SMCLK, divide by 1, No external divide, all DCORSEL and DCOFSEL settings except DCORSEL = 1, DCOFSEL = 5 and DCORSEL = 1, DCOFSEL = 6		48%	50%	52%	
$t_{DCO,\ JITTER}$	DCO jitter	Based on f_{signal} = 10 kHz and DCO used for 12-bit SAR ADC sampling source. This achieves >74-dB SNR due to jitter; that is, limited by ADC performance.			2	3	ns
df_{DCO}/dT	DCO temperature drift (2)		3.0 V		0.01		%/ºC

(1) After a wakeup from LPM1, LPM2, LPM3, or LPM4, the DCO frequency f_{DCO} might exceed the specified frequency range for a few clock cycles by up to 5% before settling to the specified steady state frequency range.
(2) Calculated using the box method: (MAX(–40°C to 85ºC) – MIN(–40°C to 85ºC)) / MIN(–40°C to 85ºC) / (85ºC – (–40ºC))

Table 5-7 lists the characteristics of the VLO.

Table 5-7. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VLO}	Current consumption			100		nA
f_{VLO}	VLO frequency	Measured at ACLK	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK (1)		0.2		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK (2)		0.7		%/V
$f_{VLO,DC}$	Duty cycle	Measured at ACLK	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8 lists the characteristics of the MODOSC.

Table 5-8. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption	Enabled		25		µA
f_{MODOSC}	MODOSC frequency		4.0	4.8	5.4	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift (1)			0.08		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift (2)			1.4		%/V
DC_{MODOSC}	Duty cycle	Measured at SMCLK, divide by 1	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

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5.13.4 Wake-up Characteristics

Table 5-9 lists the times required to wake up from LPM or reset.

Table 5-9. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	(Additional) wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected for wakeup				6	10	µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		2.2 V, 3.0 V			400 + 1.5 / f_{DCO}	ns
$t_{WAKE-UP\ LPM1}$	Wake-up time from LPM1 to active mode (1)		2.2 V, 3.0 V		6		µs
$t_{WAKE-UP\ LPM2}$	Wake-up time from LPM2 to active mode (1)		2.2 V, 3.0 V		6		µs
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (1)		2.2 V, 3.0 V		6.6 + 2.0/f_{DCO}	9.6 + 2.5/f_{DCO}	µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode (1)		2.2 V, 3.0 V		6.6 + 2.0 / f_{DCO}	9.6 + 2.5 / f_{DCO}	µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		2.2 V, 3.0 V		350	450	µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	2.2 V, 3.0 V		350	450	µs
		SVSHE = 0	2.2 V, 3.0 V		0.4	0.8	ms
$t_{WAKE-UP-RST}$	Wake-up time from a $\overline{RST}$ pin triggered reset to active mode (2)		2.2 V, 3.0 V		480	596	µs
$t_{WAKE-UP-BOR}$	Wake-up time from power-up to active mode (2)		2.2 V, 3.0 V		0.5	1	ms

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge with MCLKREQEN = 1. This time includes the activation of the FRAM during wakeup. With MCLKREQEN = 0, the externally observable MCLK clock is gated one additional cycle.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

Table 5-10 lists the typical charges used during wakeup.

Table 5-10. Typical Wake-up Charges

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Q_{WAKE\text{-}UP\ FRAM}$	Charge used for activating the FRAM in AM or during wakeup from LPM0 if previously disabled by the FRAM controller.			16.5		nAs
$Q_{WAKE\text{-}UP\ LPM0}$	Charge used to wake up from LPM0 to active mode (with FRAM active)			3.8		nAs
$Q_{WAKE\text{-}UP\ LPM1}$	Charge used to wake up from LPM1 to active mode (with FRAM active)			21		nAs
$Q_{WAKE\text{-}UP\ LPM2}$	Charge used to wake up from LPM2 to active mode (with FRAM active)			22		nAs
$Q_{WAKE\text{-}UP\ LPM3}$	Charge used to wake up from LPM3 to active mode (with FRAM active)			28		nAs
$Q_{WAKE\text{-}UP\ LPM4}$	Charge used to wake up from LPM4 to active mode (with FRAM active)			28		nAs
$Q_{WAKE\text{-}UP\ LPM3.5}$	Charge used to wake up from LPM3.5 to active mode(2)			170		nAs
$Q_{WAKE\text{-}UP\ LPM4.5}$	Charge used to wake up from LPM4.5 to active mode(2)	SVSHE = 1		173		nAs
		SVSHE = 0		171		
$Q_{WAKE\text{-}UP\text{-}RESET}$	Charge used for reset from $\overline{RST}$ or BOR event to active mode(2)			148		nAs

(1) Charge used during the wake-up time from a given low-power mode to active mode. This does not include the energy required in active mode (for example, for an interrupt service routine).
(2) Charge required until start of user code. This does not include the energy required to reconfigure the device.

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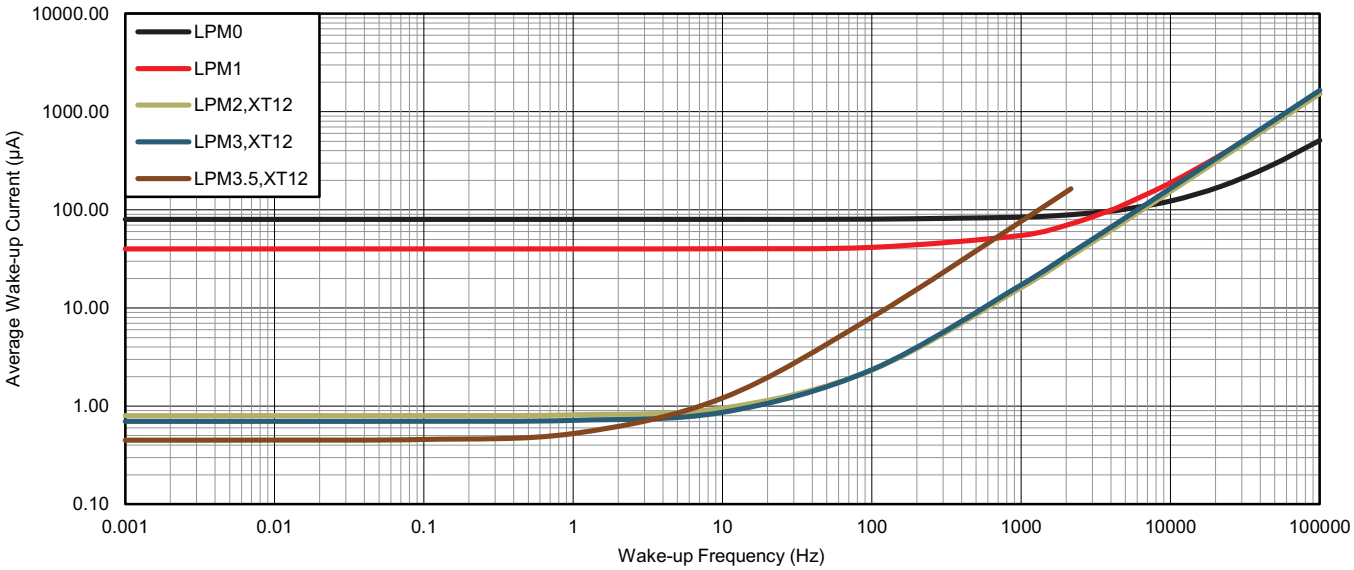
5.13.4.1 Typical Characteristics, Average LPM Currents vs Wake-up Frequency

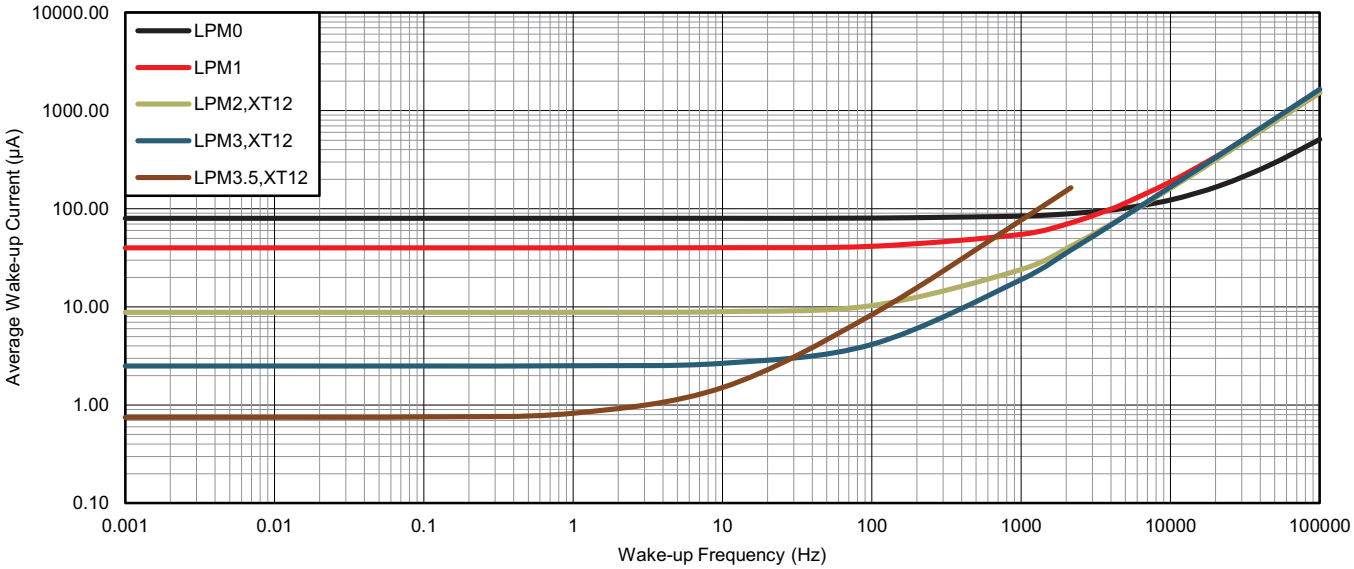
図 5-6 shows the average LPM currents vs wake-up frequency at 25°C.



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

図 5-6. Average LPM Currents vs Wake-up Frequency at 25°C

図 5-7 shows the average LPM currents vs wake-up frequency at 85°C.



NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

図 5-7. Average LPM Currents vs Wake-up Frequency at 85°C

5.13.5 Digital I/Os

Table 5-11 lists the characteristics of the digital inputs.

Table 5-11. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2.2 V	1.2		1.65	V
			3.0 V	1.65		2.25	
V_{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.00	V
			3.0 V	0.75		1.35	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		2.2 V	0.44		0.98	V
			3.0 V	0.60		1.30	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions (1)	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance input leakage current	See (2)(3)	2.2 V, 3.0 V	–20		+20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag) (4)	Ports with interrupt capability (see 1.4 and 4.3).	2.2 V, 3.0 V	20			ns
$t_{(RST)}$	External reset pulse duration on $\overline{RST}$ (5)		2.2 V, 3.0 V	2			µs

(1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN and/or PJ.5/LFXOUT.
(2) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(3) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It might be set by trigger signals shorter than $t_{(int)}$.
(5) Not applicable if $\overline{RST}$/NMI pin configured as NMI

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Table 5-12 lists the characteristics of the digital outputs.

Table 5-12. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (see 図 5-10 and 図 5-11)	$I_{(OHmax)}$ = –1 mA(1)	2.2 V	V_{CC} – 0.25		V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.60		V_{CC}	
		$I_{(OHmax)}$ = –2 mA(1)	3.0 V	V_{CC} – 0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.60		V_{CC}	
V_{OL}	Low-level output voltage (see 図 5-8 and 図 5-9)	$I_{(OLmax)}$ = 1 mA(1)	2.2 V	V_{SS}		V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}		V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(1)	3.0 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}		V_{SS} + 0.60	
$f_{Px.y}$	Port output frequency (with load)(3)	C_L = 20 pF, R_L (4) (5)	2.2 V	16			MHz
			3.0 V	16			
f_{Port_CLK}	Clock output frequency(3)	ACLK, MCLK, or SMCLK at configured output port, C_L = 20 pF(5)	2.2 V	16			MHz
			3.0 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2.2 V		4	15	ns
			3.0 V		3	15	
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2.2 V		4	15	ns
			3.0 V		3	15	
$t_{rise,ana}$	Port output rise time, port pins with shared analog functions	C_L = 20 pF	2.2 V		6	15	ns
			3.0 V		4	15	
$t_{fall,ana}$	Port output fall time, port pins with shared analog functions	C_L = 20 pF	2.2 V		6	15	ns
			3.0 V		4	15	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit, and the port might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
(5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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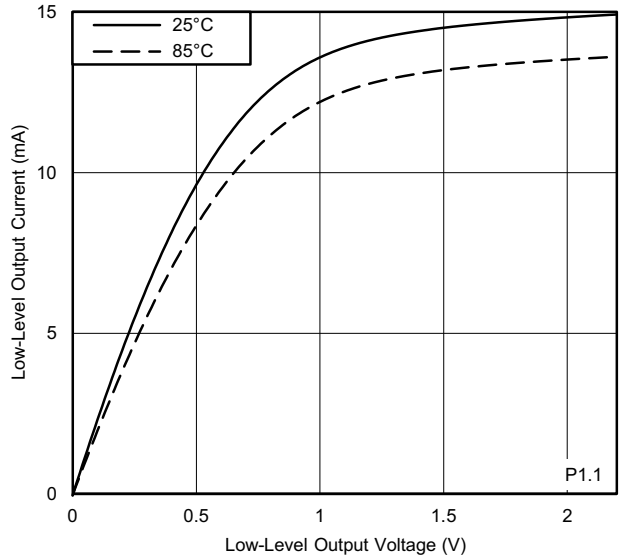
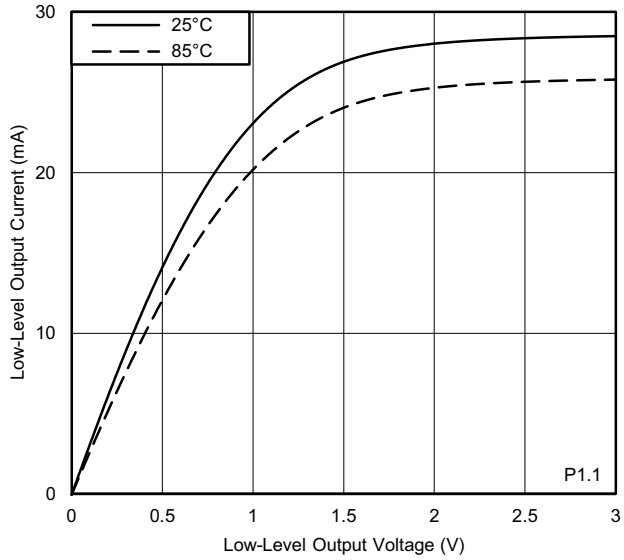
5.13.5.1 Typical Characteristics, Digital Outputs



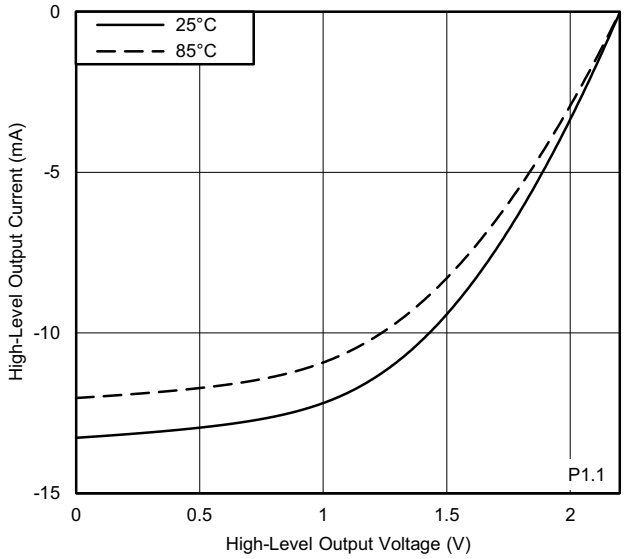
V_{CC} = 2.2 V

図 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage



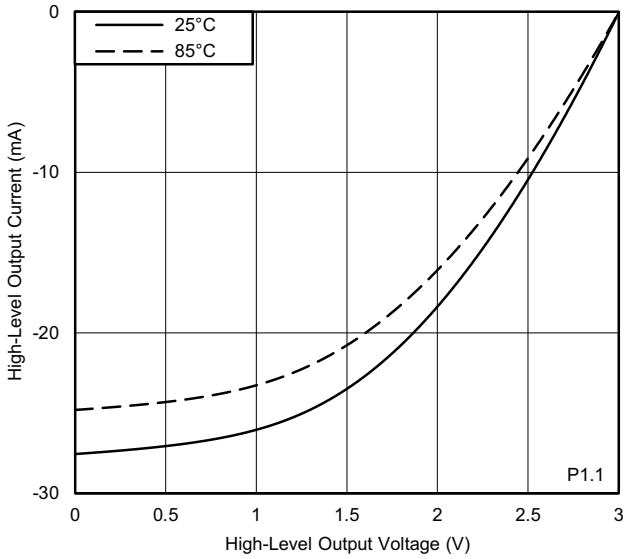
V_{CC} = 3.0 V

図 5-9. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 2.2 V

図 5-10. Typical High-Level Output Current vs High-Level Output Voltage



V_{CC} = 3.0 V

図 5-11. Typical High-Level Output Current vs High-Level Output Voltage

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5.13.6 LEA

Table 5-13 lists the characteristics of the LEA.

Table 5-13. Low-Energy Accelerator (LEA) Performance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{LEA}	Frequency for specified performance	MCLK			16		MHz
W_LEA_FFT	LEA subsystem energy on fast Fourier transform	Complex FFT 128 pt. Q.15 with random data in LEA-RAM	V_{CORE} = 3 V, MCLK = 16 MHz		350		nJ
W_LEA_FIR	LEA subsystem energy on finite impulse response	Real FIR on random Q.31 data with 128 taps on 24 points	V_{CORE} = 3 V, MCLK = 16 MHz		2.6		µJ
W_LEA_ADD	LEA subsystem energy on additions	On 32 Q.31 elements with random value out of LEA-RAM with linear address increment	V_{CORE} = 3 V, MCLK = 16 MHz		6.6		nJ

5.13.7 Timer_A and Timer_B

Table 5-14 lists the characteristics of Timer_A.

Table 5-14. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

Table 5-15 lists the characteristics of Timer_B.

Table 5-15. Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V, 3.0 V			16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

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5.13.8 eUSCI

Table 5-16 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-16. eUSCI (UART Mode) Clock Frequency

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			4	MHz

Table 5-17 lists the switching characteristics of the eUSCI in UART mode.

Table 5-17. eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0	2.2 V, 3.0 V	5		30	ns
		UCGLITx = 1		20		90	
		UCGLITx = 2		35		160	
		UCGLITx = 3		50		220	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-18 lists the supported clock frequency of the eUSCI in SPI master mode.

Table 5-18. eUSCI (SPI Master Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		16	MHz

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Table 5-19 lists the switching characteristics of the eUSCI in SPI master mode.

Table 5-19. eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10		1			UCxCLK cycles
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10		1			UCxCLK cycles
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V			60	ns
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V			80	ns
$t_{SU,MI}$	SOMI input data setup time		2.2 V	40			ns
			3.0 V	40			ns
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0			ns
			3.0 V	0			ns
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			11	ns
			3.0 V			10	ns
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.2 V		0		ns
			3.0 V		0		ns

(1) $f_{UCxCLK} = 1/2\ t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in 図 5-12 and 図 5-13.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in 図 5-12 and 図 5-13.

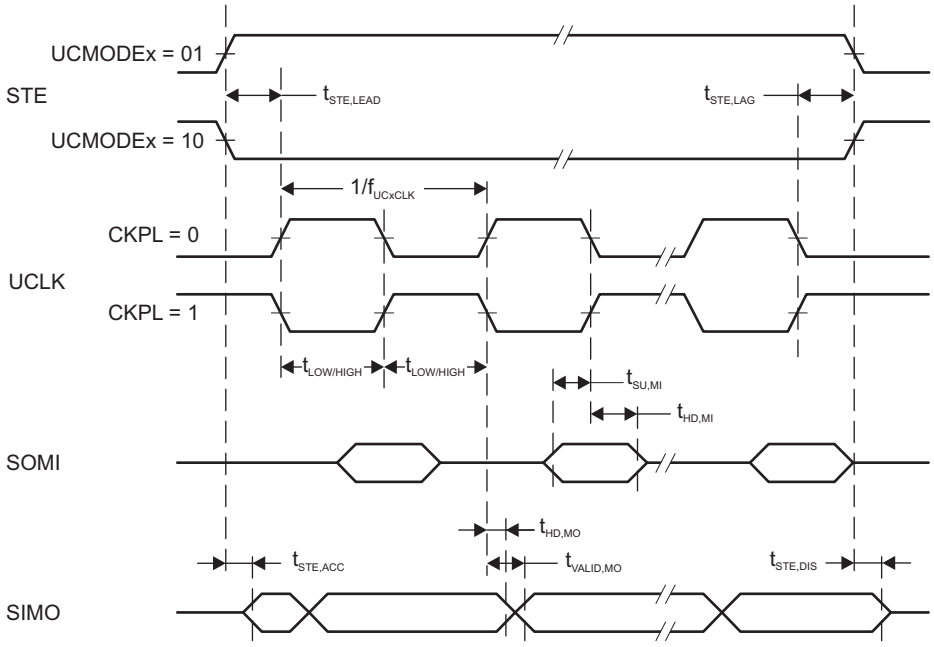

図 5-12. SPI Master Mode, CKPH = 0

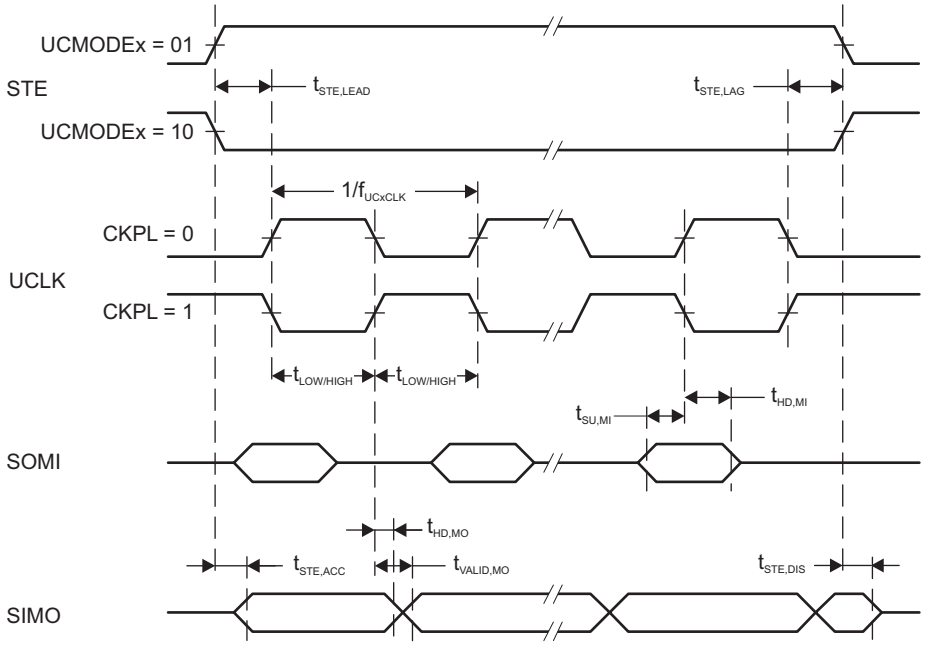

図 5-13. SPI Master Mode, CKPH = 1

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Table 5-20 lists the switching characteristics of the eUSCI in SPI slave mode.

Table 5-20. eUSCI (SPI Slave Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.2 V	45		ns
			3.0 V	40		
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2.2 V	2		ns
			3.0 V	3		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.2 V		45	ns
			3.0 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.2 V		50	ns
			3.0 V		45	
$t_{SU,SI}$	SIMO input data setup time		2.2 V	4		ns
			3.0 V	4		
$t_{HD,SI}$	SIMO input data hold time		2.2 V	7		ns
			3.0 V	7		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		35	ns
			3.0 V		35	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF	2.2 V	0		ns
			3.0 V	0		

(1) $f_{UCxCLK} = 1/2\ t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in 図 5-14 and 図 5-15.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in 図 5-14 and 図 5-15.

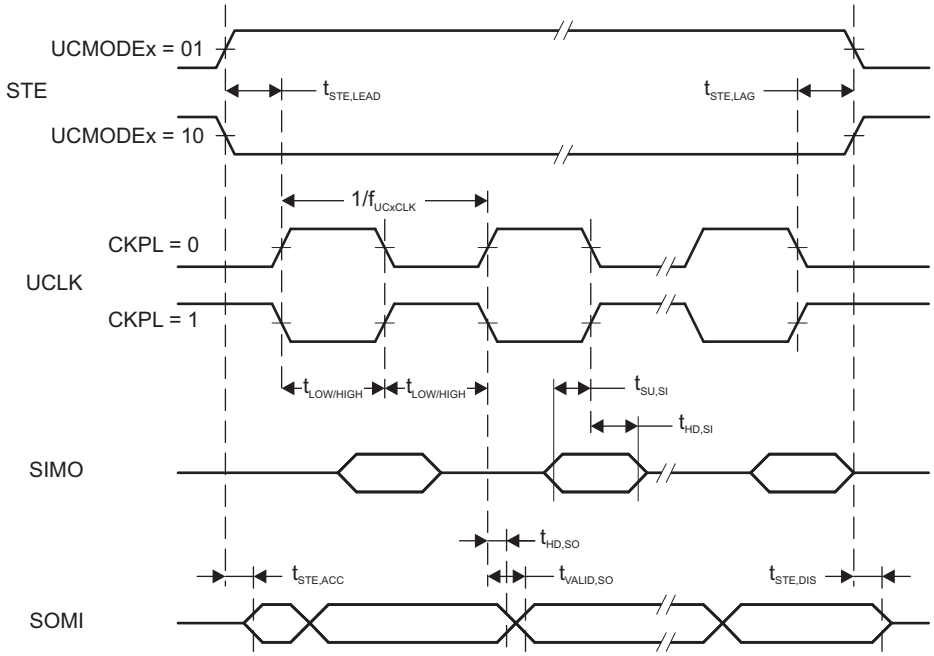

図 5-14. SPI Slave Mode, CKPH = 0

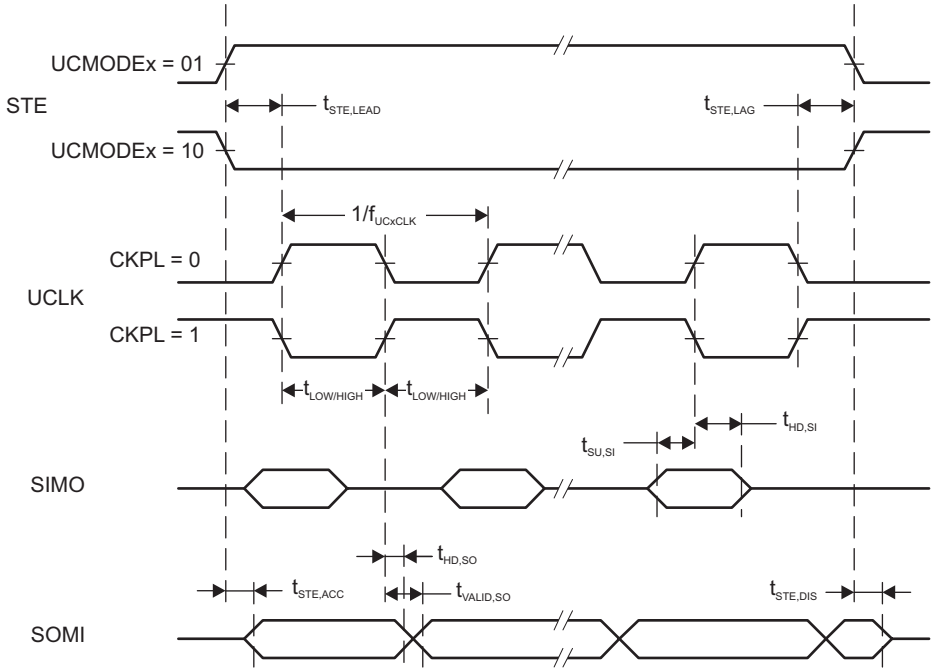

図 5-15. SPI Slave Mode, CKPH = 1

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Table 5-21 lists the switching characteristics of the eUSCI in I²C mode.

Table 5-21. eUSCI (I²C Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 5-16)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				16	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3.0 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3.0 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3.0 V	100			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2.2 V, 3.0 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{BUF}	Bus free time between a STOP and START condition	f_{SCL} = 100 kHz		4.7			us
		f_{SCL} > 100 kHz		1.3			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2.2 V, 3.0 V	50		250	ns
		UCGLITx = 1		25		125	
		UCGLITx = 2		12.5		62.5	
		UCGLITx = 3		6.3		31.5	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2.2 V, 3.0 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

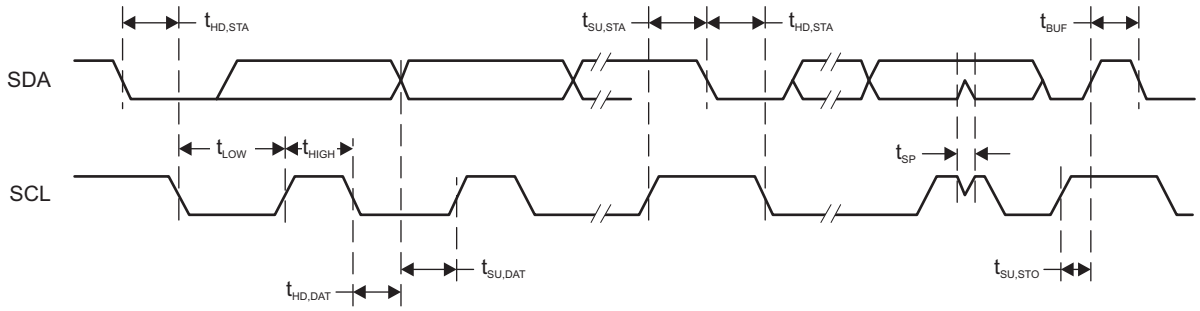

図 5-16. I²C Mode Timing

5.13.9 Segment LCD Controller

Table 5-22 lists the recommended operating conditions for the LCD controller.

Table 5-22. LCD_C Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC,LCD_C,CP\ en,3.6}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.6 V	LCDCPEN = 1, 0000b < VLCDx ≤ 1111b (charge pump enabled, V_{LCD} ≤ 3.6 V)	2.2		3.6	V
$V_{CC,LCD_C,CP\ en,3.3}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.3 V	LCDCPEN = 1, 0000b < VLCDx ≤ 1100b (charge pump enabled, V_{LCD} ≤ 3.3 V)	2.0		3.6	V
$V_{CC,LCD_C,int.\ bias}$	Supply voltage range, internal biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD_C,ext.\ bias}$	Supply voltage range, external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD_C,VLCDEXT}$	Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.0		3.6	V
V_{LCDCAP}	External LCD voltage at LCDCAP, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.4		3.6	V
C_{LCDCAP}	Capacitor value on LCDCAP when charge pump enabled	LCDCPEN = 1, VLCDx > 0000b (charge pump enabled)	$4.7_{-20\%}$	4.7	$10_{+20\%}$	µF
$f_{ACLK,in}$	ACLK input frequency range		30	32.768	40	kHz
f_{LCD}	LCD frequency range	f_{FRAME} = (1 / (2 × mux)) × f_{LCD} with mux = 1 (static) to 8	0		1024	Hz
$f_{FRAME,4mux}$	LCD frame frequency range	$f_{FRAME,4mux}$(MAX) = (1 / (2 × 4)) × f_{LCD}(MAX) = (1 / (2 × 4)) × 1024 Hz			128	Hz
C_{Panel}	Panel capacitance	f_{LCD} = 1024 Hz, all common lines equally loaded			10000	pF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, VLCDEXT = 1	2.4		V_{CC} + 0.2	V
$V_{R23,1/3bias}$	Analog input voltage at R23	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R13}	V_{R03} + 2/3 × (V_{R33} – V_{R03})	V_{R33}	V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R03}	V_{R03} + 1/3 × (V_{R33} – V_{R03})	V_{R23}	V
$V_{R13,1/2bias}$	Analog input voltage at R13 with 1/2 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1	V_{R03}	V_{R03} + 1/2 × (V_{R33} – V_{R03})	V_{R33}	V
V_{R03}	Analog input voltage at R03	R0EXT = 1	V_{SS}			V
V_{LCD} – V_{R03}	Voltage difference between V_{LCD} and R03	LCDCPEN = 0, R0EXT = 1	2.4		V_{CC} + 0.2	V
V_{LCDREF}	External LCD reference voltage applied at LCDREF	VLCDREFx = 01	0.8	1.0	1.2	V

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Table 5-23 lists the electrical characteristics the LCD controller.

Table 5-23. LCD_C Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{LCD,0}$	LCD voltage	VLCDx = 0000, VLCDEXT = 0	2.4 V to 3.6 V		V_{CC}		V
$V_{LCD,1}$		LCDCPEN = 1, VLCDx = 0001b	2 V to 3.6 V	2.49	2.60	2.72	
$V_{LCD,2}$		LCDCPEN = 1, VLCDx = 0010b	2 V to 3.6 V		2.66		
$V_{LCD,3}$		LCDCPEN = 1, VLCDx = 0011b	2 V to 3.6 V		2.72		
$V_{LCD,4}$		LCDCPEN = 1, VLCDx = 0100b	2 V to 3.6 V		2.78		
$V_{LCD,5}$		LCDCPEN = 1, VLCDx = 0101b	2 V to 3.6 V		2.84		
$V_{LCD,6}$		LCDCPEN = 1, VLCDx = 0110b	2 V to 3.6 V		2.90		
$V_{LCD,7}$		LCDCPEN = 1, VLCDx = 0111b	2 V to 3.6 V		2.96		
$V_{LCD,8}$		LCDCPEN = 1, VLCDx = 1000b	2 V to 3.6 V		3.02		
$V_{LCD,9}$		LCDCPEN = 1, VLCDx = 1001b	2 V to 3.6 V		3.08		
$V_{LCD,10}$		LCDCPEN = 1, VLCDx = 1010b	2 V to 3.6 V		3.14		
$V_{LCD,11}$		LCDCPEN = 1, VLCDx = 1011b	2 V to 3.6 V		3.20		
$V_{LCD,12}$		LCDCPEN = 1, VLCDx = 1100b	2 V to 3.6 V		3.26		
$V_{LCD,13}$		LCDCPEN = 1, VLCDx = 1101b	2.2 V to 3.6 V		3.32		
$V_{LCD,14}$		LCDCPEN = 1, VLCDx = 1110b	2.2 V to 3.6 V		3.38		
$V_{LCD,15}$		LCDCPEN = 1, VLCDx = 1111b	2.2 V to 3.6 V	3.32	3.44	3.6	
$V_{LCD,7,0.8}$	LCD voltage with external reference of 0.8 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V_{LCDREF} = 0.8 V	2 V to 3.6 V		2.96 × 0.8 V		V
$V_{LCD,7,1.0}$	LCD voltage with external reference of 1.0 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V_{LCDREF} = 1.0 V	2 V to 3.6 V		2.96 × 1.0 V		V
$V_{LCD,7,1.2}$	LCD voltage with external reference of 1.2 V	LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, V_{LCDREF} = 1.2 V	2.2 V to 3.6 V		2.96 × 1.2 V		V
ΔV_{LCD}	Voltage difference between consecutive VLCDx settings	$\Delta V_{LCD} = V_{LCD,x} - V_{LCD,x-1}$ with x = 0010b to 1111b		40	60	80	mV
$I_{CC,Peak,CP}$	Peak supply currents due to charge pump activities	LCDCPEN = 1, VLCDx = 1111b external, with decoupling capacitor on DVCC supply ≥1 µF	2.2 V		600		µA
$t_{LCD,CP,on}$	Time to charge C_{LCD} when discharged	C_{LCD} = 4.7 µF, LCDCPEN = 0→1, VLCDx = 1111b	2.2 V		100	500	ms
$I_{CP,Load}$	Maximum charge pump load current	LCDCPEN = 1, VLCDx = 1111b	2.2 V	50			µA
$R_{LCD,Seg}$	LCD driver output impedance, segment lines	LCDCPEN = 0, I_{LOAD} = ±10 µA	2.2 V			10	kΩ
$R_{LCD,COM}$	LCD driver output impedance, common lines	LCDCPEN = 0, I_{LOAD} = ±10 µA	2.2 V			10	kΩ

5.13.10 ADC12_B

Table 5-24 lists the power and input requirements of the ADC.

Table 5-24. 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{(Ax)}$	Analog input voltage range(1)	All ADC12 analog input pins Ax		0		AVCC	V
$I_{(ADC12_B)}$ single-ended mode	Operating supply current into AVCC and DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		145	199	µA
		$f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	2.2 V		140	190	
$I_{(ADC12_B)}$ differential mode	Operating supply current into AVCC and DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 1, REFON = 0, ADC12SHTx= 0, ADC12DIV = 0	3.0 V		175	245	µA
			2.2 V		170	230	
$I_{(ADC12_B)}$ single-ended low-power mode	Operating supply current into AVCC and DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK/4, ADC12ON = 1, ADC12PWRMD = 1, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		85	125	µA
		$f_{ADC12CLK}$ = MODCLK/4, ADC12ON = 1, ADC12PWRMD = 1, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	2.2 V		83	120	
$I_{(ADC12_B)}$ differential low-power mode	Operating supply current into AVCC and DVCC terminals(2) (3)	$f_{ADC12CLK}$ = MODCLK/4, ADC12ON = 1, ADC12PWRMD = 1, ADC12DIF = 1, REFON = 0, ADC12SHTx= 0, ADC12DIV = 0	3.0 V		110	165	µA
			2.2 V		109	160	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		10	15	pF
R_I	Input MUX ON resistance	$0\ V \le V_{(Ax)} \le AV_{CC}$	>2 V		0.5	4	kΩ
			<2 V		1	10	

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference supply current is not included in current consumption parameter I(ADC12_B).
(3) Approximately 60% (typical) of the total current into the AVCC and DVCC terminal is from AVCC.

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Table 5-25 lists the timing requirements of the ADC.

Table 5-25. 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	Frequency for specified performance	For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0, If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here		0.45		5.4	MHz
$f_{ADC12CLK}$	Frequency for reduced performance	Linearity parameters have reduced performance			32.768		kHz
$f_{ADC12OSC}$	Internal oscillator(1)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK		4	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK, ADC12WINC = 0		2.6		3.5	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			See (2)		
$t_{ADC12ON}$	Turnon settling time of the ADC	See (3)				100	ns
$t_{ADC12OFF}$	Time ADC must be off before can be turned on again	Note: $t_{ADC12OFF}$ must be met to make sure that $t_{ADC12ON}$ time holds.		100			ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 4 kΩ, C_I = 15 pF, C_{pext}= 8 pF(4)	All pulse sample mode (ADC12SHP = 1) and extended sample mode (ADC12SHP = 0) with buffered reference (ADC12VRSEL = 0x1, 0x3, 0x5, 0x7, 0x9, 0xB, 0xD, 0xF)	1			µs
			Extended sample mode (ADC12SHP = 0) with unbuffered reference (ADC12VRSEL= 0x0, 0x2, 0x4, 0x6, 0xC, 0xE)	See (5)			

(1) The ADC12OSC is sourced directly from MODOSC in the UCS.
(2) 14 × 1 / $f_{ADC12CLK}$. If ADC12WINC = 1 then 15 × 1 / $f_{ADC12CLK}$.
(3) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(4) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB: $t_{sample} = \ln(2^{n+2}) \times (R_S + R_I) \times (C_I + C_{pext})$, where n = ADC resolution = 12, R_S= external source resistance, C_{pext} = external parasitic capacitance.
(5) 6 × 1 / $f_{ADC12CLK}$

Table 5-26 lists the linearity parameters of the ADC.

Table 5-26. 12-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL) for differential input	With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15), $1.2\ V \le (V_{R+} - V_{R-}) \le AV_{CC}$			±1.8	LSB
	Integral linearity error (INL) for single-ended inputs	With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15), $1.2\ V \le (V_{R+} - V_{R-}) \le AV_{CC}$			±2.2	
E_D	Differential linearity error (DNL)	With external voltage reference (ADC12VRSEL = 0x2, 0x3, 0x4, 0x14, 0x15),	–0.99		+1.0	LSB
E_O	Offset error(1) (2)	ADC12VRSEL = 0x1 without TLV calibration, TLV calibration data can be used to improve the parameter(3)		±0.5	±1.5	mV
E_G	Gain error	With internal voltage reference V_{REF} = 2.5 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2%	±1.7%	
		With internal voltage reference V_{REF} = 1.2 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2%	±2.5%	
		With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, V_{R+} = 2.5 V, V_{R-} = AVSS		±1	±3	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V_{R+} = 2.5 V, V_{R-} = AVSS		±2	±27	
E_T	Total unadjusted error	With internal voltage reference V_{REF} = 2.5 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2%	±1.8%	
		With internal voltage reference V_{REF} = 1.2 V (ADC12VRSEL = 0x1, 0x7, 0x9, 0xB, or 0xD)		±0.2%	±2.6%	
		With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, V_{R+} = 2.5 V, V_{R-} = AVSS		±1	±5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), V_{R+} = 2.5 V, V_{R-} = AVSS		±1	±28	

(1) Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.
(2) Offset increases as I_R drop increases when V_{R-} is AVSS.
(3) For details, see the *Device Descriptor Table* section in the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide.

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Table 5-27 lists the dynamic performance characteristics of the ADC with an external reference.

Table 5-27. 12-Bit ADC, Dynamic Performance With External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Number of no missing code output-code bits		12			bits
SNR	Signal-to-noise with differential inputs	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		71		dB
	Signal-to-noise with single-ended inputs	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		70		
ENOB	Effective number of bits with differential inputs (1)	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		11.4		bits
	Effective number of bits with single-ended inputs (1)	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		11.1		
	Effective number of bits with 32.768-kHz clock (reduced performance) (1)	Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, V_{R+} = 2.5 V, V_{R-} = AV_{SS}		10.9		

(1) ENOB = (SINAD – 1.76) / 6.02

Table 5-28 lists the dynamic performance characteristics of the ADC with an internal reference.

Table 5-28. 12-Bit ADC, Dynamic Performance With Internal Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Number of no missing code output-code bits		12			bits
SNR	Signal-to-noise with differential inputs	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		70		dB
	Signal-to-noise with single-ended inputs	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		69		
ENOB	Effective number of bits with differential inputs (1)	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		11.4		bits
	Effective number of bits with single-ended inputs (1)	V_{R+} = 2.5 V, V_{R-} = AV_{SS}		11.0		
	Effective number of bits with 32.768-kHz clock (reduced performance) (1)	Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, V_{R+} = 2.5 V, V_{R-} = AV_{SS}		10.9		

(1) ENOB = (SINAD – 1.76) / 6.02

Table 5-29 lists the characteristics of the temperature sensor and the $V_{1/2}$.

Table 5-29. 12-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SENSOR}	Temperature sensor voltage (1) (2)	ADC12ON = 1, ADC12TCMAP = 1, T_A = 0°C		700		mV
TC_{SENSOR}	See (2)	ADC12ON = 1, ADC12TCMAP = 1		2.5		mV/°C
$t_{SENSOR(sample)}$	Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected (3)	ADC12ON = 1, ADC12TCMAP = 1, Error of conversion result ≤1 LSB	30			µs
$V_{1/2}$	AVCC voltage divider for ADC12BATMAP = 1 on MAX input channel	ADC12ON = 1, ADC12BATMAP = 1	47.5%	50%	52.5%	
$I_{V1/2}$	Current for battery monitor during sample time	ADC12ON = 1, ADC12BATMAP = 1		38	72	µA
$t_{V1/2\ (sample)}$	Sample time required if ADC12BATMAP = 1 and channel MAX is selected (4)	ADC12ON = 1, ADC12BATMAP = 1	1.7			µs

(1) The temperature sensor offset can be as much as ±30°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as V_{SENSE} = TC_{SENSOR} × (Temperature, °C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 250 kΩ. The sample time required includes the sensor on-time, $t_{SENSOR(on)}$.
(4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V1/2(sample)}$; no additional on time is needed.

Table 5-30 lists the characteristics of the external reference for the ADC.

Table 5-30. 12-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{R+}	Positive external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
V_{R-}	Negative external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	0		1.2	V
$V_{R+} - V_{R-}$	Differential external reference voltage input	$V_{R+} > V_{R-}$	1.2		AV_{CC}	V
I_{VeREF+}, I_{VeREF-}	Static input current singled-ended input mode	1.2 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 0, ADC12PWRMD = 0			±10	µA
		1.2 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 0, ADC12PWRMD = 01			±2.5	
I_{VeREF+}, I_{VeREF-}	Static input current differential input mode	1.2 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 1, ADC12PWRMD = 0			±20	µA
		1.2 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 1, ADC12PWRMD = 1			±5	
I_{VeREF+}	Peak input current with single-ended input	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC12DIF = 0			1.5	mA
I_{VeREF+}	Peak input current with differential input	0 V ≤ V_{eREF+} ≤ V_{AVCC}, ADC12DIF = 1			3	mA
$C_{VeREF+/-}$	Capacitance at VeREF+ or VeREF- terminal	See [2]	10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance (C_I) is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) Connect two decoupling capacitors, 10 µF and 470 nF, from VeREF+ or VeREF– to AVSS to decouple the dynamic current required for an external reference source if it is used for the ADC12_B. Also see the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide.

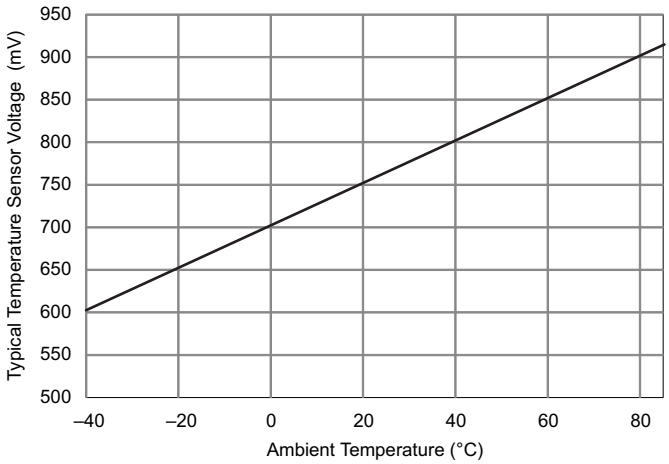

図 5-17. Typical Temperature Sensor Voltage

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5.13.11 Reference

Table 5-31 lists the characteristics of the internal reference.

Table 5-31. REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1	2.7 V		2.5	±1.5%	V
		REFVSEL = {1} for 2.0 V, REFON = 1	2.2 V		2.0	±1.5%	
		REFVSEL = {0} for 1.2 V, REFON = 1	1.8 V		1.2	±1.8%	
Noise	RMS noise at VREF (1)	From 0.1 Hz to 10 Hz, REFVSEL = {0}			30	130	µV
$V_{OS_BUF_INT}$	VREF ADC BUF_INT buffer offset(2)	T_A = 25°C, ADC on, REFVSEL = {0}, REFON = 1, REFOUT = 0		–16		+16	mV
$V_{OS_BUF_EXT}$	VREF ADC BUF_EXT buffer offset(3)	T_A = 25°C, REFVSEL = {0} , REFOUT = 1, REFON = 1 or ADC on		–16		+16	mV
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into AVCC terminal(4)	REFON = 1	3 V		19	26	µA
$I_{REF+_ADC_BUF}$	Operating supply current into AVCC terminal(4)	ADC ON, REFOUT = 0, REFVSEL = {0, 1, or 2}, ADC12PWRMD = 0	3 V		247	400	µA
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0			1053	1820	
		ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1			153	240	
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1			581	1030	
		ADC OFF, REFON = 1, REFOUT = 1, REFVSEL = {0, 1, 2}			1105	1890	
$I_{O(VREF+)}$	VREF maximum load current, VREF+ terminal	REFVSEL = {0, 1, 2}, AV_{CC} = $AV_{CC(min)}$ for each reference level, REFON = REFOUT = 1		–1000		+10	µA
$\Delta V_{out}/\Delta I_{o(VREF+)}$	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2}, $I_{O(VREF+)}$ = +10 µA or –1000 µA, AV_{CC} = $AV_{CC(min)}$ for each reference level, REFON = REFOUT = 1				1500	µV/mA
$C_{VREF+/-}$	Capacitance at VREF+ and VREF- terminals	REFON = REFOUT = 1		0		100	pF
TC_{REF+}	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, T_A = –40°C to 85°C(5)			24	50	ppm/K
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1			100	400	µV/V
PSRR_AC	Power supply rejection ratio (AC)	dAV_{CC}= 0.1 V at 1 kHz			3.0		mV/V
t_{SETTLE}	Settling time of reference voltage(6)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0 → 1			40	80	µs
T_{buf_settle}	Settling time of ADC reference voltage buffer(6)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 1			0.4	2	us

(1) Internal reference noise affects ADC performance when ADC uses the internal reference. See Designing With the MSP430FR59xx and MSP430FR58xx ADC for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) Buffer offset affects ADC gain error and thus total unadjusted error.
(3) Buffer offset affects ADC gain error and thus total unadjusted error.
(4) The internal reference current is supplied through the AVCC terminal.
(5) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(6) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.13.12 Comparator

Table 5-32 lists the characteristics of the comparator.

Table 5-32. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{AVCC_COMP}	Comparator operating supply current into AVCC, excludes reference resistor ladder	CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)	2.2 V, 3.0 V		12	16	µA
		CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)			10	14	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 30°C			0.1	0.3	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 85°C			0.3	1.3	
$I_{AVCC_COMP_REF}$	Quiescent current of resistor ladder into AVCC, including REF module current	CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 1, CEREFACC = 0	2.2 V, 3.0 V		31	38	µA
		CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 1, CEREFACC = 1			16	19	
V_{REF}	Reference voltage level	CERSx = 11, CEREFLx = 01, CEREFACC = 0	1.8 V	1.152	1.2	1.248	V
		CERSx = 11, CEREFLx = 10, CEREFACC = 0	2.2 V	1.92	2.0	2.08	
		CERSx = 11, CEREFLx = 11, CEREFACC = 0	2.7 V	2.40	2.5	2.60	
		CERSx = 11, CEREFLx = 01, CEREFACC = 1	1.8 V	1.10	1.2	1.245	
		CERSx = 11, CEREFLx = 10, CEREFACC = 1	2.2 V	1.90	2.0	2.08	
		CERSx = 11, CEREFLx = 11, CEREFACC = 1	2.7 V	2.35	2.5	2.60	
V_{IC}	Common-mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CEPWRMD = 00		–16		16	mV
		CEPWRMD = 01		–12		12	
		CEPWRMD = 10		–37		37	
C_{IN}	Input capacitance	CEPWRMD = 00 or CEPWRMD = 01			10		pF
		CEPWRMD = 10			10		
R_{SIN}	Series input resistance	ON (switch closed)			1	3	kΩ
		OFF (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV			193	330	ns
		CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV			230	400	
		CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV			5	15	µs
$t_{PD,filter}$	Propagation delay with filter active	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00			700	1000	ns
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01			1.0	1.9	µs
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10			2.0	3.7	
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11			4.0	7.7	

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Table 5-32. Comparator_E (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{EN_CMP}	Comparator enable time	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 00			0.9	1.5	µs
		CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 01			0.9	1.5	
		CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 10			15	65	
$t_{EN_CMP_VREF}$	Comparator and reference ladder and reference voltage enable time	CEON = 0 → 1, CEREFLX = 10, CERSx = 10 or 11, CEREF0 = CEREF1 = 0x0F, REFON = 0			120	220	µs
$t_{EN_CMP_RL}$	Comparator and reference ladder enable time	CEON = 0 → 1, CEREFLX = 10, CERSx = 10, REFON = 1, CEREF0 = CEREF1 = 0x0F			10	30	
V_{CE_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

5.13.13 FRAM

Table 5-33 lists the characteristics of the FRAM.

Table 5-33. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			T_J	MIN	TYP	MAX	UNIT
	Read and write endurance			10^{15}			cycles
$t_{Retention}$	Data retention duration		25°C	100			years
			70°C	40			
			85°C	10			
I_{WRITE}	Current to write into FRAM (1)				I_{READ}		nA
I_{ERASE}	Erase current (2)				N/A (3)		nA
t_{WRITE}	Write time (4)				t_{READ}		ns
t_{READ}	Read time (5)	NWAITSx = 0			1 / f_{SYSTEM}		ns
		NWAITSx = 1			2 / f_{SYSTEM}		

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption, $I_{AM,FRAM}$.
(2) FRAM does not require a special erase sequence.
(3) N/A = Not applicable
(4) Writing into FRAM is as fast as reading.
(5) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

5.13.14 USS

Table 5-34 lists the USS recommended operating conditions.

Table 5-34. USS Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PV_{CC}	Analog supply voltage at PVCC pins for LDO operation		2.2		3.6	V
PV_{CC}	Analog supply voltage at PVCC pins for USS operation		2.2		3.6	V

Table 5-35 lists the characteristics of the USS LDO.

Table 5-35. USS LDO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC\text{-}LDO}$	Analog supply voltage at PVCC pins		2.2		3.6	V
V_{USS}	USS voltage	$0 \le I_{LOAD} \le I_{LOAD,MAX}$	1.52	1.6	1.65	V
$t_{holdoff}$	Hold off delay on power up	LBHDEL = 0		0		µs
		LBHDEL = 1		100		
		LBHDEL = 2		200		
		LBHDEL = 3		300		
$t_{time\text{-}out}$	Time-out on transition from OFF to READY			160 + $t_{holdoff}$		µs

Table 5-36 lists the characteristics of the USS crystal.

Table 5-36. USSXTAL

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N_{phase_osc}	Integrated phase noise	f_{osc} = 4 MHz or 8 MHz, range = 10 kHz to 4 MHz		–74		dBc
FRQ_{XTAL}	Resonator frequency		4		8	MHz
DC_{osc}	Duty cycle		35%		65%	
I_{osc}	OSC supply current	f_{osc} = 4 MHz or 8 MHz, C_L = 18 pF, C_S = 4 pF, fully settled, ceramic resonator		180		µA
		f_{osc} = 4 MHz or 8 MHz, C_L = 12 pF (4 MHz) or 16 pF (8 MHz), C_S = 7 pF, fully settled, crystal resonator		240		
A_{osc}	Oscillation allowance	f_{osc} = 4 MHz, C_L = 18 pF, C_S = 4 pF, ceramic resonator		1500		Ω
		f_{osc} = 4 MHz, C_L = 12 pF, C_S = 7 pF, crystal resonator		1000		
		f_{osc} = 8 MHz, C_L = 18 pF, C_S = 4 pF, ceramic resonator		500		
		f_{osc} = 8 MHz, C_L = 16 pF, C_S = 7 pF, crystal resonator		350		
T_{start_osc}	Start-up time (gate)	f_{osc} = 4 MHz, crystal resonator		2.8	4.6	ms
		f_{osc} = 8 MHz, crystal resonator		1	1.9	
		f_{osc} = 4 MHz, ceramic resonator		0.14	0.17	
		f_{osc} = 8 MHz, ceramic resonator		0.08	0.12	

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Table 5-37 lists the characteristics of the USS HSPLL.

Table 5-37. USS HSPLL

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL_CLK_{in}	Input clock to HSPLL		4		8	MHz
PLL_CLK_{out}	Output clock from HSPLL		68		80	MHz
$LOCK_{pwr}$	Lock time from PLL power up	Reference clock = PLL_CLK_{in}, Sequence: Set USS.CTL.USSPWRUP bit = 1, then measure the time between PSQ_PLLUP (internal control signal) is set to 1 and HSPLL.CTL.PLL_LOCK is set to 1			64	cycles

Table 5-38 lists the characteristics of the USS SDHS.

Table 5-38. USS SDHS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{sdhs}	SDHS power domain supply voltage	$V_{sdhs} = V_{uss}$		1.52	1.6	1.65	V
$I_{sdhs_product}$	Operating supply current into AVCC and DVCC	Includes PLL, PGA, SDHS, and DTC, modulator clock = 80 MHz, output data rate = 8 Msps			5.2		mA
f_{mod}	Modulator clock			68		80	MHz
BW_{mod}	Frequency at –3-dB SNR	Modulator clock = 80 MHz, modulator only (no filter is enabled)			1.5		MHz
SNR	Signal-to-noise ratio	Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 1000 mVpp, PVCC = 3.0 V, f_{mod} = 80 MHz, OSR = 20	58.5	62.5		dB
		Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 760 mVpp, PVCC = 2.5 V, f_{mod} = 80 MHz, OSR = 20	57.5	62		
		Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 200 mVpp, PVCC = 2.5 V, f_{mod} = 80 MHz, OSR = 20	54.5	57		
		Bandwidth from 200kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 100 mVpp, PVCC = 2.5 V, f_{mod} = 80 MHz, OSR = 20	49	53		
		Bandwidth from 200 kHz to 1.5 MHz, PGA gain: a gain from the PGA gain table for the maximum SNR	Input signal level = 30 mVpp, PVCC = 2.5 V, f_{mod} = 80 MHz, OSR = 20	38.5	43		
t_{MOD_Settle}	SDHS settling time (PGA + modulator)	TM2 – TM1, AUTOSSDIS = 0, 1% of settled DC level				40	µs
		TM2 – TM1, AUTOSSDIS = 1, 1% of settled DC level				40	
$DROUT_{sdhs}$	Output data rate					8	Msps

Table 5-39 lists the characteristics of the USS PHY outputs.

Table 5-39. USS PHY Output Stage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVCC	PHY supply voltage	PVCC = V_{CC}, PVSS = V_{SS}	2.2		3.6	V
R_{DSonT}	Output impedance of CH0OUT and CH1OUT for high and low sides (trimmed at 3-V PV_{DD})	PVCC ≥ 2.5 V		3		Ω
R_{Term}	Termination impedance of CH0OUT and CH1OUT toward PVSS (trimmed)	PVCC ≥ 2.5 V		3		Ω
DrvM	High-side to low-side drive mismatch (trimmed)	PVCC ≥ 2.5 V		5%	12.5%	
TermM	Termination to drive mismatch (trimmed)	PVCC ≥ 2.5 V		5%	12.5%	
f_{MAX}	Maximum output frequency	PVCC = V_{CC} (2.5 V to 3.6 V)	4.5			MHz
C_{SUPP}	Supply buffering capacitance (low ESR type)	PVCC = V_{CC}	22	100		µF
R_{SUPP}	Series resistance to C_{SUPP}	PVCC = V_{CC}		22		Ω

Table 5-40 lists the characteristics of the USS PHY inputs.

Table 5-40. USS PHY Input Stage, Multiplexer

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage on CH0IN or CH1IN	PVCC = V_{CC}, PVSS = V_{SS}	PVSS – 0.3		1.8	V

Table 5-41 lists the characteristics of the USS PGA.

Table 5-41. USS PGA

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PV_{cc}	Supply voltage			2.2		3.6	V
G_N	Gain (1)			–6.5		30.8	dB
V_{inr1}	Input range	2.2 V ≤ PVCC		30		800	mVpp
V_{inr2}	Input range	2.5 V ≤ PVCC		30		1000	mVpp
$V_{inrperf}$	Recommended input range for maximum performance	2.5 V ≤ PVCC		30		800	mVpp
G_{tol}	Gain tolerance	Full PGA gain range, V_{OUT} = 600 mV		–1.5		1.5	dB
G_{Tdrift}	Gain drift with temperature	Full PGA gain range, V_{OUT} = 600 mV			0.0019		dB/°C
G_{Vdrift}	Gain drift with voltage	Full PGA gain range, V_{OUT} = 600 mV			0.15		dB/V
t_{SET}	Gain settling time	Gain setting: from 0 dB to 6 dB, to ±5%			0.65	1.4	µs
DC_{offset}	DC offset (PGA and SDHS)	Full PGA gain range, measured at SDHS output			5.5		mV
DC_{drift}	DC offset drift (PGA and SDHS)	Full PGA gain range, measured at SDHS output			4.7		µV/°C
PSRR_AC	AC power supply rejection ratio	V_{CC} = 3 V + 50 mVpp × sin (2π × f_C) where f_C = 1 MHz, V_{IN} = ground, PSRR_AC = 20log(V_{OUT} / 50 mV)	PGA gain = 0 dB		–41		dB
			PGA gain = 10 dB		–37		
			PGA gain = 30 dB		–19		

(1) See the *PGA Gain* table in the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide.

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Table 5-42 lists the characteristics of the USS bias voltage generator.

Table 5-42. USS Bias Voltage Generator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{exc_bias}	Excitation bias voltage (coupling capacitors)	PVCC = V_{CC} (2.2 V to 3.6 V)	EXCBIAS = 0		200		mV
			EXCBIAS = 1		300		
			EXCBIAS = 2		400		
			EXCBIAS = 3		600		
R_{VBE}	Impedance of excitation bias generator	PVCC = V_{CC} (2.2 V to 3.6 V)	BIMP = 0		450		Ω
			BIMP = 1		850		
			BIMP = 2		1450		
			BIMP = 3		2900		
t_{SBE}	Excitation bias settling time	PVCC = V_{CC} (2.2 V to 3.6 V), to 0.1% end value, R_{ET} = 200 Ω, C_K + C_{0P} = 1 nF, BIMP = 2			20		µs
V_{pga_bias}	PGA bias voltage (coupling capacitors)	PVCC = V_{CC} (2.2 V to 3.6 V)	PGABIAS = 0		750		mV
			PGABIAS = 1		800		
			PGABIAS = 2		900		
			PGABIAS = 3		950		
R_{VBA}	Impedance of acquisition bias generator	PVCC = V_{CC} (2.2 V to 3.6 V)	BIMP = 0		500		Ω
			BIMP = 1		900		
			BIMP = 2		1500		
			BIMP = 3		2950		
t_{SBA}	Acquisition bias settling time	PVCC = V_{CC} (2.2 V to 3.6 V), to 0.1% end value, R_{ET} = 200 Ω, C_K + C_{0P} = 1 nF, BIMP = 2			22		µs

5.13.15 Emulation and Debug

Table 5-43 lists the characteristics of the JTAG and SBW interface.

Table 5-43. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
I_{JTAG}	Supply current adder when JTAG active (but not clocked)	2.2 V, 3.0 V		40	100	µA
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3.0 V	0		10	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3.0 V	0.04		15	µs
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	2.2 V, 3.0 V			110	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG(2)	2.2 V	0		16	MHz
		3.0 V	0		16	
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3.0 V	20	35	50	kΩ
f_{TCLK}	TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f_{SYSTEM})				16	MHz
$t_{TCLK,Low/High}$	TCLK low or high clock pulse duration, no FRAM access				25	ns
$f_{TCLK,FRAM}$	TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f_{SYSTEM} with no FRAM wait states)				4	MHz
$t_{TCLK,FRAM,Low/High}$	TCLK low or high clock pulse duration, including FRAM accesses				100	ns

(1) Tools that access the Spy-Bi-Wire and the BSL interfaces must wait for the $t_{SBW,En}$ time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Overview

The TI MSP430FR60xx(1) family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes, is optimized to achieve extended battery life for example in portable measurement applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The device is an MSP430FR6xx family device with Ultrasonic Sensing Solution (USS), Low-Energy Accelerator (LEA), up to six 16-bit timers, up to six eUSCIs that support UART, SPI, and I^2C, a comparator, a hardware multiplier, an AES accelerator, a 6-channel DMA, an RTC module with alarm capabilities, up to 76 I/O pins, and a high-performance 12-bit ADC. The MSP430FR60xx(1) devices also include an LCD module with contrast control for displays with up to 264 segments.

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. The peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

6.3 Ultrasonic Sensing Solution (USS) Module

The USS module provides a high-precision ultrasonic sensing solution. The USS module is a sophisticated system that consists of six submodules:

- UUPS (universal USS power supply)
- HSPLL (high-speed PLL) with oscillator
- ASQ (acquisition sequencer)
- PHY (physical interface)
- PPG (programmable pulse generator) with low-output-impedance driver
- PGA (programmable gain amplifier)
- SDHS (sigma-delta high-speed ADC) with DTC (data transfer controller)

The submodules have different roles, and together they enable high-precision data acquisition in ultrasonic applications. See the dedicated chapter for each submodule in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

The USS module performs complete measurement sequence without CPU involvement to achieve ultra-low power consumption for ultrasonic metrology. 図 6-1 shows the USS subsystem block diagram. The USS module has dedicated I/O pins without secondary functions. See the *Ultrasonic Sensing Solution (USS)* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide* for details.

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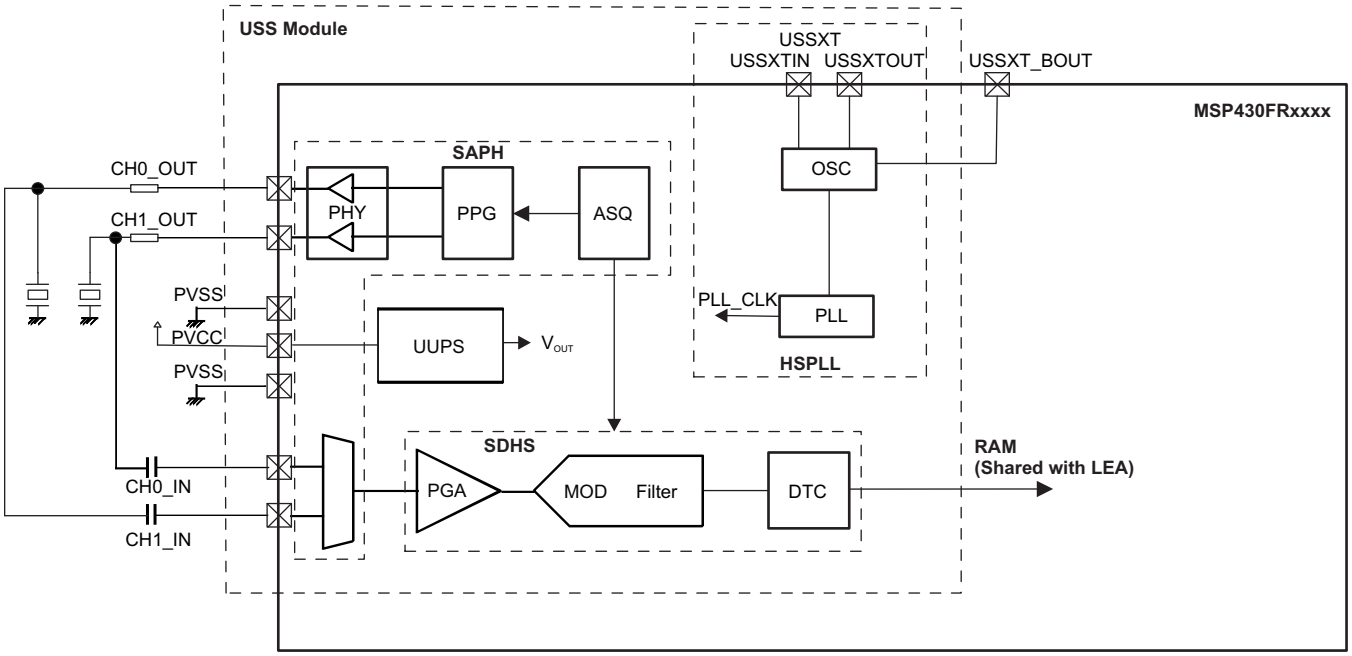

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図 6-1. USS Subsystem Block Diagram

6.4 Low-Energy Accelerator (LEA) for Signal Processing

The LEA is a hardware engine designed for operations that involve vector-based signal processing, such as FIR, IIR, and FFT. The LEA offers fast performance and low energy consumption when performing vector-based digital signal processing computations. For performance benchmarks comparing LEA to using the CPU or other processors, see *Benchmarking the Signal Processing Capabilities of the Low-Energy Accelerator*.

The LEA requires MCLK to be operational; therefore, LEA operates only in active mode or LPM0. While the LEA is running, the LEA data operations are performed on a shared 4KB of RAM out of the 8KB of total RAM (see 表 6-47). This shared RAM can also be used by the regular application. The MSP CPU and the LEA can run simultaneously and independently unless they access the same system RAM.

Direct access to LEA registers is not supported, and TI offers the optimized Digital Signal Processing (DSP) Library for MSP Microcontrollers for the operations that the LEA module supports.

6.5 Operating Modes

The MCU has one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 to LPM4, service the request, and return to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption. 表 6-1 lists the operating modes and the clocks and peripherals that are available in each.

表 6-1. Operating Modes

MODE	AM		LPM0		LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	ACTIVE	ACTIVE, FRAM OFF(1)	CPU OFF(2)		CPU OFF	STANDBY	STANDBY	OFF	RTC ONLY	SHUTDOWN WITH SVS	SHUTDOWN WITHOUT SVS
Maximum system clock	16 MHz		16 MHz		16 MHz	50 kHz	50 kHz	0(3)	50 kHz	0(3)	
Typical current consumption, T_A = 25°C	103 µA/MHz	65 µA/MHz	70 µA at 1 MHz		35 µA at 1 MHz	0.7 µA	0.4 µA	0.3 µA	0.25 µA	0.2 µA	0.02 µA
Typical wake-up time	N/A		instant		6 µs	6 µs	7 µs	7 µs	250 µs	250 µs	1000 µs
Wake-up events	N/A		all		all	LF RTC I/O Comp	LF RTC I/O Comp	I/O Comp	RTC I/O	I/O	
CPU	on		off		off	off	off	off	reset	reset	
USS	on		on		off	off	off	off	reset	reset	
LEA	on		on(4)	off	off	off	off	off	reset	reset	
FRAM	**on**	off(1)	standby (or off(1))		off	off	off	off	off	off	
High-frequency peripherals	**available**		**available**		**available**	off	off	off	reset	reset	
Low-frequency peripherals	**available**		**available**		**available**	**available**	**available**(5)	off	RTC MTIF	reset	
Unclocked peripherals(6)	**available**		**available**		**available**	**available**	**available**(5)	**available**(5)	reset	reset	
MCLK	**on**		**on(4)**	**off**	off	off	off	off	off	off	
SMCLK	optional(7)		optional(7)		optional(7)	off	off	off	off	off	
ACLK	**on**		**on**		**on**	**on**	**on**	off	off	off	
Full retention	**yes**		**yes**		**yes**	**yes**	**yes**	**yes**	no	no	

(1) FRAM is disabled in the FRAM controller (FRCTL_A).
(2) Disabling the FRAM through the FRAM controller (FRCTL_A) allows the application to lower the LPM current consumption but the wake-up time increases when FRAM is accessed (for example, to fetch an interrupt vector). For a wakeup that does not involve FRAM (for example, a DMA transfer to RAM) the wake-up time is not increased.
(3) All clocks disabled
(4) Only while the LEA is performing a task enabled by the CPU during AM. The LEA cannot be enabled in LPM0.
(5) See 6.5.2, which describes the use of peripherals in LPM3 and LPM4.
(6) *Unclocked peripherals* are peripherals that do not require a clock source to operate; for example, the comparator and REF, or the eUSCI when operated as an SPI slave.
(7) Controlled by SMCLKOFF.

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表 6-1. Operating Modes (continued)

MODE	AM		LPM0	LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	ACTIVE	ACTIVE, FRAM OFF(1)	CPU OFF(2)	CPU OFF	STANDBY	STANDBY	OFF	RTC ONLY	SHUTDOWN WITH SVS	SHUTDOWN WITHOUT SVS
SVS	always		always	always	optional(8)	optional(8)	optional(8)	optional(8)	on(9)	off(10)
Brownout	**always**		**always**	**always**	**always**	**always**	**always**	**always**	**always**	

(8) Activated SVS (SVSHE = 1) results in higher current consumption. SVS is not included in typical current consumption.
(9) SVSHE = 1
(10) SVSHE = 0

6.5.1 Peripherals in Low-Power Modes

Peripherals can be in different states that affect the achievable power modes of the device. The states depend on the operational modes of the peripherals (see 表 6-2). The states are:

- A peripheral is in a "high-frequency state" if it requires or uses a clock with a "high" frequency of more than 50 kHz.
- A peripheral is in a "low-frequency state" if it requires or uses a clock with a "low" frequency of 50 kHz or less.
- A peripheral is in an "unclocked state" if it does not require or use an internal clock.

If the CPU requests a power mode that does not support the current state of all active peripherals, the device does not enter the requested power mode, but it does enter a power mode that still supports the current state of the peripherals, except if an external clock is used. If an external clock is used, the application must use the correct frequency range for the requested power mode.

表 6-2. Peripheral States

PERIPHERAL	IN HIGH-FREQUENCY STATE (1)	IN LOW-FREQUENCY STATE (2)	IN UNCLOCKED STATE (3)
WDT	Clocked by SMCLK	Clocked by ACLK	Not applicable
DMA (4)	Not applicable	Not applicable	Waiting for a trigger
RTC_C	Not applicable	Clocked by LFXT	Not applicable
LCD_C	Not applicable	Clocked by ACLK or VLOCLK	Not applicable
Timer_A, TAx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
Timer_B, TBx	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Ax in UART mode	Clocked by SMCLK	Clocked by ACLK	Waiting for first edge of START bit
eUSCI_Ax in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Ax in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
eUSCI_Bx in I^2C master mode	Clocked by SMCLK or clocked by external clock >50 kHz	Clocked by ACLK or clocked by external clock ≤50 kHz	Not applicable
eUSCI_Bx in I^2C slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Waiting for START condition or clocked by external clock ≤50 kHz
eUSCI_Bx in SPI master mode	Clocked by SMCLK	Clocked by ACLK	Not applicable
eUSCI_Bx in SPI slave mode	Clocked by external clock >50 kHz	Clocked by external clock ≤50 kHz	Clocked by external clock ≤50 kHz
ADC12_B	Clocked by SMCLK or by MODOSC	Clocked by ACLK	Waiting for a trigger
REF_A	Not applicable	Not applicable	Always
COMP_E	Not applicable	Not applicable	Always
CRC (5)	Not applicable	Not applicable	Not applicable
MPY (5)	Not applicable	Not applicable	Not applicable
AES (5)	Not applicable	Not applicable	Not applicable

(1) Peripherals are in a state that requires or uses a clock with a "high" frequency of more than 50 kHz
(2) Peripherals are in a state that requires or uses a clock with a "low" frequency of 50 kHz or less.
(3) Peripherals are in a state that does not require or does not use an internal clock.
(4) The DMA always transfers data in active mode but can wait for a trigger in any low-power mode. A DMA trigger during a low-power mode causes a temporary transition into active mode for the time of the transfer.
(5) This peripheral operates during active mode only and will delay the transition into a low-power mode until its operation is completed.

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6.5.2 Idle Currents of Peripherals in LPM3 and LPM4

Most peripherals can be operational in LPM3 if clocked by ACLK. Some modules are operational in LPM4, because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To reduce the idle current adder, certain peripherals are grouped together. To achieve optimal current consumption, use modules within one group and limit the number of groups with active modules. 表 6-3 lists the peripheral groups. Modules not listed in this table are either already included in the standard LPM3 current consumption or cannot be used in LPM3 or LPM4.

The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C); see the I_{IDLE} current parameters in for details.

表 6-3. Peripheral Groups

GROUP A	GROUP B	GROUP C
Timer TA1	Timer TA0	Timer TA4
Timer TA2	Timer TA3	eUSCI_A2
Timer TB0	Comparator	eUSCI_A3
eUSCI_A0	ADC12_B	eUSCI_B1
eUSCI_A1	REF_A	LCD_C
eUSCI_B0		

6.6 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address, and signatures are in the address range 0FFFFh to 0FF80h. 図 6-2 summarizes the content of this address range.

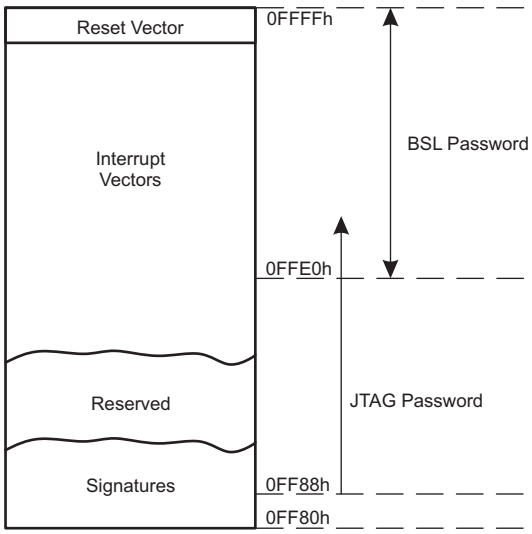

図 6-2. Interrupt Vectors, Signatures and Passwords

The power-up start address or reset vector is at 0FFFFh to 0FFFEh. It contains the 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh and extend to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. 表 6-4 shows the device-specific interrupt vector locations.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as BSL password (if enabled by the corresponding signature).

The signatures start at 0FF80h and extend to higher addresses. Signatures are evaluated during device start-up. 表 6-5 shows the device-specific signature locations.

A JTAG password can be programmed starting from address 0FF88h and extending to higher addresses. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password. The length of the JTAG password depends on the JTAG signature.

See the chapter *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide* for details.

表 6-4. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, brownout, supply supervisor External reset $\overline{\text{RST}}$ Watchdog time-out (watchdog mode) WDT, FRCTL MPU, CS, PMM password violation FRAM uncorrectable bit error detection MPU segment violation Software POR, BOR	SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW UBDIFG MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG PMMPORIFG, PMMBORIFG (SYSRSTIV)(1) (2)	Reset	0FFFEh	Highest
System NMI Vacant memory access JTAG mailbox FRAM access time error FRAM write protection error FRAM bit error detection MPU segment violation	VMAIFG JMBINIFG, JMBOUTIFG ACCTEIFG, WPIFG CBDIFG, UBDIFG MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG (SYSSNIV)(1) (3)	(Non)maskable	0FFFCh	
User NMI External NMI Oscillator fault LEA RAM access conflict	NMIIFG, OFIFG DACCESSIFG (SYSUNIV)(1) (3)	(Non)maskable	0FFFAh	
Comparator_E	CEIFG, CEIIFG (CEIV)(1)	Maskable	0FFF8h	
TB0	TB0CCR0.CCIFG	Maskable	0FFF6h	
TB0	TB0CCR1.CCIFG to TB0CCR6.CCIFG, TB0CTL.TBIFG (TB0IV)(1)	Maskable	0FFF4h	
Watchdog timer (interval timer mode)	WDTIFG	Maskable	0FFF2h	
eUSCI_A0 receive or transmit	UCA0IFG: UCRXIFG, UCTXIFG (SPI mode) UCA0IFG: UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA0IV)(1)	Maskable	0FFF0h	
eUSCI_B0 receive or transmit	UCB0IFG: UCRXIFG, UCTXIFG (SPI mode) UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB0IV)(1)	Maskable	0FFEEh	
ADC12_B	ADC12IFG0 to ADC12IFG31 ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC21OVIFG, ADC12TOVIFG (ADC12IV)(1) (4)	Maskable	0FFECh	
TA0	TA0CCR0.CCIFG	Maskable	0FFEAh	

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space.
(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot disable it.
(4) Only on devices with ADC, otherwise reserved.

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表 6-4. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
TA0	TA0CCR1.CCIFG, TA0CCR2.CCIFG, TA0CTL.TAIFG (TA0IV)(1)	Maskable	0FFE8h	
eUSCI_A1 receive or transmit	UCA1IFG: UCRXIFG, UCTXIFG (SPI mode) UCA1IFG: UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA1IV)(1)	Maskable	0FFE6h	
DMA	DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG (DMAIV)(1)	Maskable	0FFE4h	
TA1	TA1CCR0.CCIFG	Maskable	0FFE2h	
TA1	TA1CCR1.CCIFG, TA1CCR2.CCIFG, TA1CTL.TAIFG (TA1IV)(1)	Maskable	0FFE0h	
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)	Maskable	0FFDEh	
TA2	TA2CCR0.CCIFG	Maskable	0FFDCh	
TA2	TA2CCR1.CCIFG TA2CTL.TAIFG (TA2IV)(1)	Maskable	0FFDAh	
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)	Maskable	0FFD8h	
TA3	TA3CCR0.CCIFG	Maskable	0FFD6h	
TA3	TA3CCR1.CCIFG TA3CTL.TAIFG (TA3IV)(1)	Maskable	0FFD4h	
I/O port P3	P3IFG.0 to P3IFG.7 (P3IV)(1)	Maskable	0FFD2h	
I/O port P4	P4IFG.0 to P4IFG.2 (P4IV)(1)	Maskable	0FFD0h	
LCD_C	LCD_C Interrupt Flags (LCDCIV)(1)	Maskable	0FFCEh	
RTC_C	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV)(1)	Maskable	0FFCCh	
AES	AESRDYIFG	Maskable	0FFCAh	
TA4	TA4CCR0.CCIFG	Maskable	0FFC8h	
TA4	TA4CCR1.CCIFG TA4CTL.TAIFG (TA4IV)(1)	Maskable	0FFC6h	
I/O port P5	P5IFG.0 to P5IFG.2 (P5IV)(1)	Maskable	0FFC4h	
I/O port P6	P6IFG.0 to P6IFG.2 (P6IV)(1)	Maskable	0FFC2h	
eUSCI_A2 receive or transmit	UCA2IFG: UCRXIFG, UCTXIFG (SPI mode) UCA2IFG: UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA2IV)(1)	Maskable	0FFC0h	
eUSCI_A3 receive or transmit	UCA3IFG: UCRXIFG, UCTXIFG (SPI mode) UCA3IFG: UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode) (UCA3IV)(1)	Maskable	0FFBEh	
eUSCI_B1 receive or transmit	UCB1IFG: UCRXIFG, UCTXIFG (SPI mode) UCB1IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I^2C mode) (UCB1IV)(1)	Maskable	0FFBCh	

表 6-4. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
I/O Port P7	P7IFG.0 to P7IFG.2 (P7IV)(1)	Maskable	0FFBAh	
I/O Port P8	P8IFG.0 to P8IFG.2 (P8IV)(1)	Maskable	0FFB8h	
I/O Port P9	P9IFG.0 to P9IFG.2 (P9IV)(1)	Maskable	0FFB6h	
LEA	CMDIFG, SDIIFG, OORIFG, TIFG, COVLIFG (LEAIV)(1)	Maskable	0FFB4h	
UUPS	PTMOUT, PREQIG (IIDX)(1)	Maskable	0FFB2h	
HSPLL	PLLUNLOCK (IIDX)(1)	Maskable	0FFB0h	
SAPH	DATAERR, TAMTO, SEQDN, PNGDN (IIDX)(1)	Maskable	0FFAEh	
SDHS	OVF, ACQDONE, SSTRG, DTRDY, WINHI, WINLO (IIDX)(1)	Maskable	0FFACh	Lowest

表 6-5. Signatures

SIGNATURE	WORD ADDRESS
IP Encapsulation Signature2	0FF8Ah
IP Encapsulation Signature1(1)	0FF88h
BSL Signature2	0FF86h
BSL Signature1	0FF84h
JTAG Signature2	0FF82h
JTAG Signature1	0FF80h

(1) Must not contain 0AAAAh if used as the JTAG password.

6.7 Bootloader (BSL)

The BSL can program the FRAM or RAM using a UART serial interface (FRxxxx devices) or an I^2C interface (FRxxxx1 devices). Access to the device memory through the BSL is protected by an user-defined password. 表 6-6 lists the pins that are required for use of the BSL. BSL entry requires a specific entry sequence on the $\overline{RST}$/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 FRAM Device Bootloader (BSL) User's Guide*. More information on the BSL can be found at www.ti.com/tool/mspbsl.

表 6-6. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{RST}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P2.0	Devices with UART BSL (FRxxxx): Data transmit
P2.1	Devices with UART BSL (FRxxxx): Data receive
P1.6	Devices with I^2C BSL (FRxxxx1): Data
P1.7	Devices with I^2C BSL (FRxxxx1): Clock
VCC	Power supply
VSS	Ground supply

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6.8 JTAG Operation

6.8.1 JTAG Standard Interface

The MSP family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP development tools and device programmers. 表 6-7 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

表 6-7. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION (1)	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
DVCC	N/A	Power supply
DVSS	N/A	Ground supply

(1) N/A = not applicable

6.8.2 Spy-Bi-Wire (SBW) Interface

In addition to the standard JTAG interface, the MSP family supports the 2-wire SBW interface. SBW can be used to interface with MSP development tools and device programmers. 表 6-8 lists the SBW interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

表 6-8. SBW Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION (1)	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
DVCC	N/A	Power supply
DVSS	N/A	Ground supply

(1) N/A = not applicable

6.9 FRAM Controller A (FRCTL_A)

The FRAM can be programmed through the JTAG port, SBW, the BSL, or in-system by the CPU. Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

注

Wait States

For MCLK frequencies > 8 MHz, wait states must be configured following the flow described in the "Wait State Control" section of the *FRAM Controller A (FRCTRL_A)* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see *MSP430™ FRAM Technology – How To and Best Practices*.

6.10 RAM

The RAM is made up of three sectors: Sector 0 = 2KB, Sector 1 = 2KB, Sector 2 = 4KB (shared with LEA). Each sector can be individually powered down in LPM3 and LPM4 to save leakage. All data in the sector is lost when a sector is powered down.

6.11 Tiny RAM

Tiny RAM is 22 bytes of RAM in addition to the complete RAM (see 表 6-47). This memory is always available, even in LPM3 and LPM4, while the complete RAM can be powered down in LPM3 and LPM4. Tiny RAM can be used to hold data or a very small stack when the complete RAM is powered down in LPM3 and LPM4. No memory is available in LPMx.5.

6.12 Memory Protection Unit (MPU) Including IP Encapsulation

The FRAM can be protected by the MPU from inadvertent CPU execution, read access, or write access. Features of the MPU include:

- IP encapsulation with programmable boundaries in steps of 1KB (prevents reads from outside the application; for example, through JTAG or by non-IP software).
- Main memory partitioning is programmable up to three segments in steps of 1KB.
- Access rights of each segment can be individually selected (main and information memory).
- Access violation flags with interrupt capability for easy servicing of access violations.

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6.13 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be controlled using all instructions. For complete module descriptions, see the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

6.13.1 Digital I/O

Up to ten 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input is available for all pins of ports P1 to P9.
- Read and write access to port control registers is supported by all instructions.
- Ports P1 and P2 (PA), P3 and P4 (PB), P5 and P6 (PC), P7 and P8 (PD), or P9 (PE) can be accessed byte-wise or word-wise in pairs.
- No cross currents during start-up.

注

Configuration of Digital I/Os After BOR Reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and their module functions disabled. To enable the I/O functionality after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section of the *Digital I/O* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

6.13.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch-crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK). ACLK can be sourced from a 32-kHz watch crystal (LFXT1), the internal VLO, or a digital external low-frequency (<50-kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal DCO, a 32-kHz watch crystal (LFXT1), the internal VLO, or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

6.13.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device . The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a safe level and below a user-selectable level. SVS circuitry is available on the primary and core supplies.

6.13.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

6.13.5 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock (RTC) with the following features:

- Calendar mode with leap year correction
- General-purpose counter mode

The internal calendar compensates for months with fewer than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

6.13.6 Measurement Test Interface (MTIF)

The MTIF module provides a simple pulse-based test interface that is used to implement consumption monitoring of "legal relevant data" with high integrity. MTIF consists of the a pulse generator, a pulse counter, and a pulse interface. MTIF has following features:

- Independent passwords for generator counter and pulse interface
- Pulse rates up to 1016 pulses per second (p/s)
- Pulse frame duration from 1/16 s to 16 s
- Count capacity up to 65535 (16 bit)
- Operating in LPM3.5 with 200 nA
- 2-pin interface with MTIF_OUT_IN and MTIF_PIN_EN

6.13.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. 表 6-9 lists the clocks that can source the WDT_A module.

表 6-9. WDT_A Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	LFMODCLK

6.13.8 System Module (SYS)

The SYS module manages many system functions within the device. These functions include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader (BSL) entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. 表 6-10 lists the SYS module interrupt vector registers.

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表 6-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		MPUPW MPU password violation (PUC)	22h	
		CSPW CS password violation (PUC)	24h	
		MPUSEGIPIFG encapsulated IP memory segment violation (PUC)	26h	
		Reserved	28h	
		MPUSEG1IFG segment 1 memory violation (PUC)	2Ah	
		MPUSEG2IFG segment 2 memory violation (PUC)	2Ch	
		MPUSEG3IFG segment 3 memory violation (PUC)	2Eh	
		Reserved	30h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		Reserved	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		FRAM access time error	06h	
		MPUSEGIPIFG encapsulated IP memory segment violation	08h	
		Reserved	0Ah	
		MPUSEG1IFG segment 1 memory violation	0Ch	
		MPUSEG2IFG segment 2 memory violation	0Eh	
		MPUSEG3IFG segment 3 memory violation	10h	
		VMAIFG vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		FRAM Write Protection Detection	1Ah	
		LEA time-out fault	1Ch	
		LEA command fault	1Eh	Lowest

表 6-10. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG NMI pin	02h	Highest
		OFIFG oscillator fault	04h	
		DACCESSIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

6.13.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 6-11 lists the available triggers for the DMA.

表 6-11. DMA Trigger Assignments(1)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4	CHANNEL 5
0	DMAREQ	DMAREQ	DMAREQ	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG	TA3CCR0 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG	TA4CCR0 CCIFG
10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	AES Trigger 0	AES Trigger 0	AES Trigger 0	AES Trigger 0	AES Trigger 0	AES Trigger 0
12	AES Trigger 1	AES Trigger 1	AES Trigger 1	AES Trigger 1	AES Trigger 1	AES Trigger 1
13	AES Trigger 2	AES Trigger 2	AES Trigger 2	AES Trigger 2	AES Trigger 2	AES Trigger 2
14	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG	UCA2RXIFG	UCA2RXIFG	UCA2RXIFG
15	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG	UCA2TXIFG	UCA2TXIFG	UCA2TXIFG
16	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG	UCA3RXIFG	UCA3RXIFG	UCA3RXIFG
17	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG	UCA3TXIFG	UCA3TXIFG	UCA3TXIFG
18	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I^2C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I^2C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I^2C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I^2C)
19	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I^2C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I^2C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I^2C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I^2C)
20	UCB0RXIFG1 (I^2C)	UCB0RXIFG1 (I^2C)	UCB0RXIFG1 (I^2C)	UCB1RXIFG1 (I^2C)	UCB1RXIFG1 (I^2C)	UCB1RXIFG1 (I^2C)
21	UCB0TXIFG1 (I^2C)	UCB0TXIFG1 (I^2C)	UCB0TXIFG1 (I^2C)	UCB1TXIFG1 (I^2C)	UCB1TXIFG1 (I^2C)	UCB1TXIFG1 (I^2C)
22	UCB0RXIFG2 (I^2C)	UCB0RXIFG2 (I^2C)	UCB0RXIFG2 (I^2C)	UCB1RXIFG2 (I^2C)	UCB1RXIFG2 (I^2C)	UCB1RXIFG2 (I^2C)
23	UCB0TXIFG2 (I^2C)	UCB0TXIFG2 (I^2C)	UCB0TXIFG2 (I^2C)	UCB1TXIFG2 (I^2C)	UCB1TXIFG2 (I^2C)	UCB1TXIFG2 (I^2C)
24	UCB0RXIFG3 (I^2C)	UCB0RXIFG3 (I^2C)	UCB0RXIFG3 (I^2C)	UCB1RXIFG3 (I^2C)	UCB1RXIFG3 (I^2C)	UCB1RXIFG3 (I^2C)
25	UCB0TXIFG3 (I^2C)	UCB0TXIFG3 (I^2C)	UCB0TXIFG3 (I^2C)	UCB1TXIFG3 (I^2C)	UCB1TXIFG3 (I^2C)	UCB1TXIFG3 (I^2C)
26	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion	ADC12 end of conversion
27	LEA ready	LEA ready	LEA ready	LEA ready	LEA ready	LEA ready
28	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready	MPY ready	MPY ready	MPY ready

(1) If a reserved trigger source is selected, no trigger is generated.

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表 6-11. DMA Trigger Assignments[(1)] (continued)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4	CHANNEL 5
30	DMA2IFG	DMA0IFG	DMA1IFG	DMA5IFG	DMA3IFG	DMA4IFG
31	DMAE0	DMAE0	DMAE0	DMAE0	DMAE0	DMAE0

6.13.10 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_A0, eUSCI_A1, eUSCI_A2, and eUSCI_A3 modules support SPI (3- or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_B0 and eUSCI_B1 modules support SPI (3- or 4-pin) and I^2C.

Four eUSCI_A modules and two eUSCI_B modules are implemented.

6.13.11 TA0, TA1, and TA4

TA0, TA1, and TA4 are 16-bit timers and counters (Timer_A type) with three (TA0 and TA1) or two (TA4) capture/compare registers each. Each timer can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-12, 表 6-13, and 表 6-14). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

表 6-12. TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.4, P4.5, P5.5	TA0CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.4. P4.5, P5.5	$\overline{\text{TA0CLK}}$	INCLK				
P2.3	TA0.0	CCI0A	CCR0	TA0	TA0.0	P2.3
P2.7	TA0.0	CCI0B				P2.7
	DVSS	GND				
	DVCC	V_{CC}				
P7.4	TA0.1	CCI1A	CCR1	TA1	TA0.1	P7.4
	COUT (internal)	CCI1B				ADC12(internal)[(1)] ADC12SHSx = {1}
	DVSS	GND				
	DVCC	V_{CC}				
P7.7	TA0.2	CCI2A	CCR2	TA2	TA0.2	P7.7
	ACLK (internal)	CCI2B				UUPS Trigger (USSPWRUP) UUPS.CTL.USSPWRUPSEL = {2}
	DVSS	GND				
	DVCC	V_{CC}				

(1) Only on devices with ADC.

表 6-13. TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.4, P4.5	TA1CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.4. P4.5	$\overline{\text{TA1CLK}}$	INCLK				
P1.0	TA1.0	CCI0A	CCR0	TA0	TA1.0	P1.0
P9.0	TA1.0	CCI0B				P9.0
	DVSS	GND				
	DVCC	V_{CC}				
P7.5	TA1.1	CCI1A	CCR1	TA1	TA1.1	P7.5
	COUT (internal)	CCI1B				ADC12(internal)(1) ADC12SHSx = {4}
	DVSS	GND				
	DVCC	V_{CC}				
P8.4	TA1.2	CCI2A	CCR2	TA2	TA1.2	P8.4
	ACLK (internal)	CCI2B				ASQ Trigger (ASQTRIG) SAPH.ASCTL0.TRIGSEL= {2}
	DVSS	GND				
	DVCC	V_{CC}				

(1) Only on devices with ADC.

表 6-14. TA4 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
PJ.1,P4.6	TA4CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
PJ.1, P4.6	$\overline{\text{TA4CLK}}$	INCLK				
P1.1	TA4.0	CCI0A	CCR0	TA0	TA4.0	P1.1
P2.5	TA4.0	CCI0B				P2.5
	DVSS	GND				
	DVCC	V_{CC}				
P7.6	TA4.1	CCI1A	CCR1	TA1	TA4.1	P7.6
P2.6	TA4.1	CCI1B				P2.6
	DVSS	GND				ADC12(internal)(1) ADC12SHSx = {7}
	DVCC	V_{CC}				

(1) Only on devices with ADC.

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6.13.12 TA2 and TA3

TA2 and TA3 are 16-bit timers and counters (Timer_A type) with two capture/compare registers each and with internal connections only. Each timer can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-15 and 表 6-16). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

表 6-15. TA2 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
Reserved	INCLK			
TA3 CCR0 output (internal)	CCI0A	CCR0	TA0	TA3 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V_{CC}			
Reserved	CCI1A	CCR1	TA1	ADC12(internal)(1) ADC12SHSx = {5}
COUT (internal)	CCI1B			PPG Trigger (PPGTRIG) SAPH.PGCTL.TRSEL= {2}
DVSS	GND			
DVCC	V_{CC}			

(1) Only on devices with ADC

表 6-16. TA3 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
Reserved	INCLK			
TA2 CCR0 output (internal)	CCI0A	CCR0	TA0	TA2 CCI0A input
ACLK (internal)	CCI0B			
DVSS	GND			
DVCC	V_{CC}			
Reserved	CCI1A	CCR1	TA1	ADC12(internal)(1) ADC12SHSx = {6}
COUT (internal)	CCI1B			
DVSS	GND			
DVCC	V_{CC}			

(1) Only on devices with ADC

6.13.13 TB0

TB0 is a 16-bit timer and counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-17). TB0 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

表 6-17. TB0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.4, P4.6	TB0CLK	TBCLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.4, P4.6	$\overline{\text{TB0CLK}}$	INCLK				
P7.2	TB0.0	CCI0A	CCR0	TB0	TB0.0	P7.2
P3.0	TB0.0	CCI0B				P3.0
	DVSS	GND				ADC12 (internal)(1) ADC12SHSx = {2}
	DVCC	V_{CC}				
P7.3	TB0.1	CCI1A	CCR1	TB1	TB0.1	P7.3
	COUT (internal)	CCI1B				P3.1
	DVSS	GND				ADC12 (internal)(1) ADC12SHSx = {3}
	DVCC	V_{CC}				
P8.0	TB0.2	CCI2A	CCR2	TB2	TB0.2	P8.0
	ACLK (internal)	CCI2B				P3.2
	DVSS	GND				
	DVCC	V_{CC}				
P8.1	TB0.3	CCI3A	CCR3	TB3	TB0.3	P8.1
P3.3	TB0.3	CCI3B				P3.3
	DVSS	GND				
	DVCC	V_{CC}				
P1.4	TB0.4	CCI4A	CCR4	TB4	TB0.4	P1.4
P3.5	TB0.4	CCI4B				P3.5
	DVSS	GND				
	DVCC	V_{CC}				
P1.5	TB0.5	CCI5A	CCR5	TB5	TB0.5	P1.5
P3.6	TB0.5	CCI5B				P3.6
	DVSS	GND				
	DVCC	V_{CC}				
PJ.3	TB0.6	CCI6A	CCR6	TB6	TB0.6	PJ.3
P3.7	TB0.6	CCI6B				P3.7
	DVSS	GND				
	DVCC	V_{CC}				

(1) Only on devices with ADC.

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6.13.14 ADC12_B

The ADC12_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, a reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

表 6-18 lists the external trigger sources.

表 6-19 lists the available multiplexing between internal and external analog inputs.

表 6-18. ADC12_B Trigger Signal Connections

ADC12SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC12SC)
001	1	TA0 CCR1 output
010	2	TB0 CCR0 output
011	3	TB0 CCR1 output
100	4	TA1 CCR1 output
101	5	TA2 CCR1 output
110	6	TA3 CCR1 output
111	7	TA4 CCR1 output

表 6-19. ADC12_B External and Internal Signal Mapping

CONTROL BIT IN ADC12CTL3 REGISTER	EXTERNAL ADC INPUT (CONTROL BIT = 0)	INTERNAL ADC INPUT (CONTROL BIT = 1)
ADC12BATMAP	A31	Battery monitor
ADC12TCMAP	A30	Temperature sensor
ADC12CH0MAP	A29	N/A (1)
ADC12CH1MAP	A28	N/A (1)
ADC12CH2MAP	A27	N/A (1)
ADC12CH3MAP	A26	N/A (1)

(1) N/A = No internal signal is available on this device.

6.13.15 USS

表 6-20 lists the available UUPS triggers.

表 6-20. UUPS Trigger Signal Connections

UUPS.CTL.USSPWRUPSEL BINARY	CONNECTED TRIGGER SOURCE
00	Software (UUPS.CTL.USSPWRUP)
01	RTC (any enabled interrupt events)
10	TA0 CCR2 output
11	P1.7

表 6-21 lists the available PPG triggers.

表 6-21. PPG Trigger Signal Connections

SAPH.PGCTL.TRSEL BINARY	CONNECTED TRIGGER SOURCE
00	Software (SAPH.PPGTRIG.PPGTRIG)
01	ASQ (Acquisition Sequencer)
10	TA2 CCR1 output
11	Reserved

表 6-22 lists the available ASQ triggers.

表 6-22. ASQ Trigger Signal Connections

SAPH.ASCTL0.TRIGSEL BINARY	CONNECTED TRIGGER SOURCE
00	Software (SAPH.ASQTRIG.ASQTRIG)
01	PSQ (Power Sequencer)
10	TA1 CCR2 output
11	Reserved

6.13.16 Comparator_E

The primary function of the Comparator_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.13.17 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.13.18 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC32 module signature is based on the ISO 3309 standard.

6.13.19 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

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6.13.20 True Random Seed

The device descriptor information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

6.13.21 Shared Reference (REF)

The REF module generates critical reference voltages that can be used by the various analog peripherals in the device.

6.13.22 LCD_C

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static and 2-mux to 8-mux LCDs are supported. The module can provide an LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments in static, 2-, 3-, and 4-mux modes.

To reduce system noise, the charge pump can be temporarily disabled. 表 6-23 lists the available automatic charge pump disable options.

表 6-23. LCD Automatic Charge Pump Disable Bits (LCDCPDISx)

CONTROL BIT	DESCRIPTION
LCDCPDIS0	LCD charge pump disable during ADC12 conversion 0b = LCD charge pump not automatically disabled during conversion. 1b = LCD charge pump automatically disabled during conversion.
LCDCPDIS1 to LCDCPDIS7	No functionality.

6.13.23 Embedded Emulation

6.13.23.1 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.13.23.2 EnergyTrace++ Technology

The devices implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology lets the user observe information about the internal states of the microcontroller. These states include the CPU Program Counter (PC), the on or off status of the peripherals and system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

The activity of the following modules can be observed:

- LEA is running
- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REFBG or REFGEN active and BG in static mode.
- COMP is on.

- AES is encrypting or decrypting.
- eUSCI_A0 is transferring (receiving or transmitting) data.
- eUSCI_A1 is transferring (receiving or transmitting) data.
- eUSCI_A2 is transferring (receiving or transmitting) data.
- eUSCI_A3 is transferring (receiving or transmitting) data.
- eUSCI_B0 is transferring (receiving or transmitting) data.
- eUSCI_B1 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.
- TA4 is counting.
- LCD_C is running.
- USS status

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6.14 Input/Output Diagrams

6.14.1 Port Function Select Registers (PySEL1 , PySEL0)

Port pins are multiplexed with peripheral module functions as described in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*. The functions of each port pin are controlled by its port function select registers, PySEL1 and PySEL0, where y = port number. The bits in the registers are mapped to the pins in the port. The primary module function, secondary module function, and tertiary module function of the pins are determined by the configuration of the PySEL1.x and PySEL0.x bits (see 表 6-24). For example, P1SEL1.0 and P1SEL0.0 determine the primary module function, secondary module function, and tertiary module function of the P1.0 pin, which is in port 1. The module functions may also require the PxDIR bits to be configured according to the direction needed for the module function.

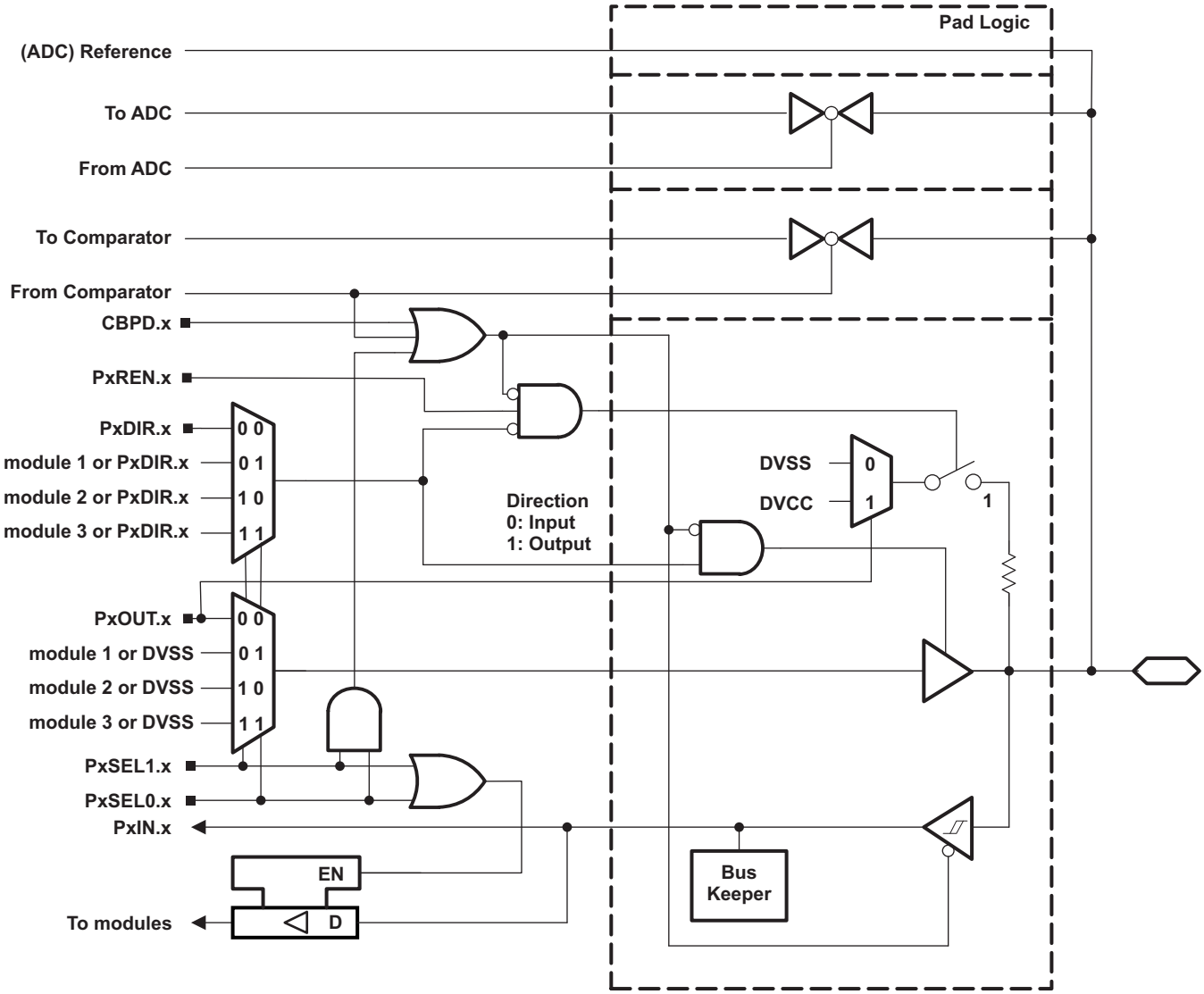
表 6-24. I/O Function Selection

I/O FUNCTIONS	PySEL1.x	PySEL1.x
General-purpose I/O is selected	0	0
Primary module function is selected	0	1
Secondary module function is selected	1	0
Tertiary module function is selected	1	1

See the port pin function tables in the following sections for the configurations of the function and direction for each pin.

6.14.2 Port P1 (P1.0 and P1.1) Input/Output With Schmitt Trigger

図 6-3 shows the port diagram. 表 6-25 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-3. Port P1 (P1.0 to P1.1) Diagram

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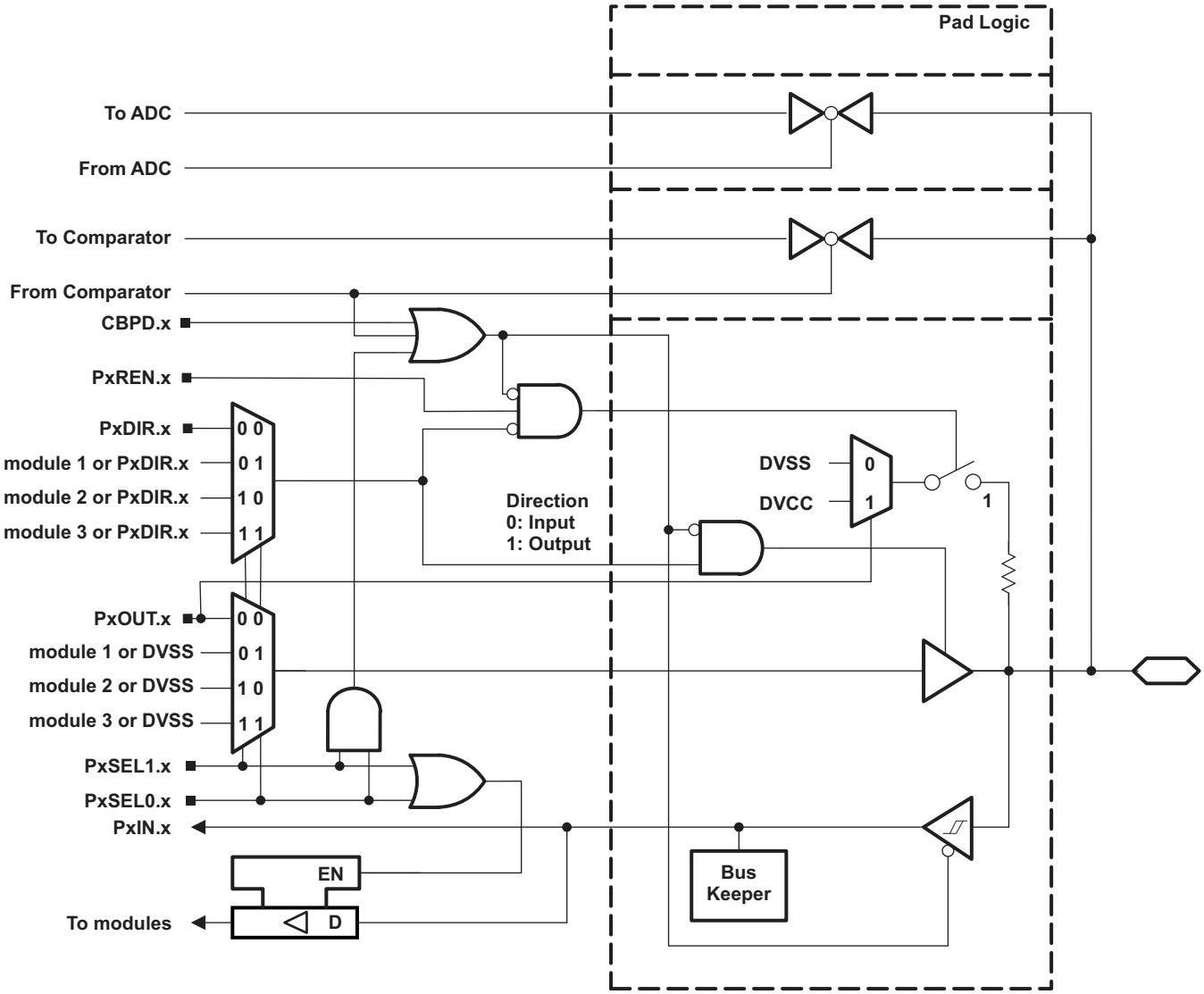
表 6-25. Port P1 (P1.0 to P1.1) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/UCA1CLK/TA1.0/A0/C0/ VREF-/VeREF-	0	P1.0 (I/O)	I: 0; O: 1	0	0
		UCA1CLK	X[2]	0	1
		TA1.CCI0A	0	1	0
		TA1.0	1		
		A0, C0, VREF-, VeREF-[3][4]	X	1	1
P1.1/UCA1STE/TA4.0/A1/C1/ VREF+/VeREF+	1	P1.1 (I/O)	I: 0; O: 1	0	0
		UCA1STE	X[2]	0	1
		TA4.CCI0A	0	1	0
		TA4.0	1		
		A1, C1, VREF+, VeREF+[3][4]	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

6.14.3 Port P1 (P1.2 to P1.7) Input/Output With Schmitt Trigger

図 6-4 shows the port diagram. 表 6-26 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-4. Port P1 (P1.2 to P1.7) Diagram

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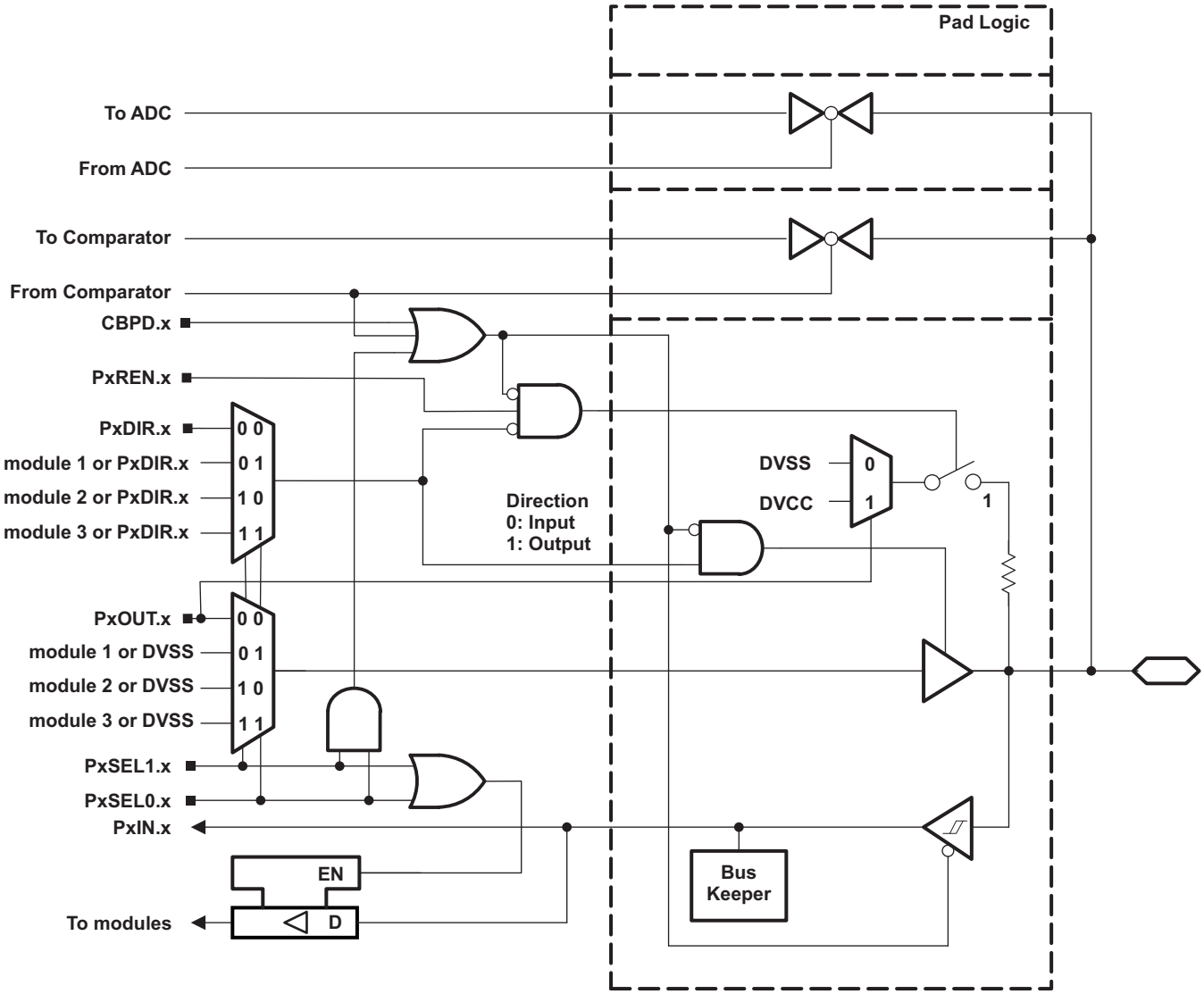
表 6-26. Port P1 (P1.2 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.2/UCA1SIMO/UCA1TXD/A8/C8	2	P1.2 (I/O)	I: 0; O: 1	0	0
		UCA1SIMO/UCA1TXD	X[2]	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		A8, C8[3][4]	X	1	1
P1.3/UCA1SOMI/UCA1RXD/A9/C9	3	P1.3 (I/O)	I: 0; O: 1	0	0
		UCA1SOMI/UCA1RXD	X[2]	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		A9, C9[3][4]	X	1	1
P1.4/TB0.4/UCB0STE/A2/C2	4	P1.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI4A	0	0	1
		TB0.4	1		
		UCB0STE	X[5]	1	0
		A2, C2[3][4]	X	1	1
P1.5/TB0.5/UCB0CLK/A3/C3	5	P1.5(I/O)	I: 0; O: 1	0	0
		TB0.CCI5A	0	0	1
		TB0.5	1		
		UCB0CLK	X[5]	1	0
		A3, C3[3][4]	X	1	1
P1.6/UCB0SIMO/UCB0SDA/A4/C4	6	P1.6(I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		UCB0SIMO/UCB0SDA	X[5]	1	0
		A4, C4[3][4]	X	1	1
P1.7/USSTRG/UCB0SOMI/UCB0SCL/ A5/C5	7	P1.7(I/O)	I: 0; O: 1	0	0
		USSTRG (independent function)	0	X	1
				1	X
		Internally tied to DVSS	1	0	1
		UCB0SOMI/UCB0SCL	X[5]	1	0
		A5, C5[3][4]	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.
(5) Direction controlled by eUSCI_B0 module.

6.14.4 Port P2 (P2.0 to P2.3) Input/Output With Schmitt Trigger

図 6-5 shows the port diagram. 表 6-27 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-5. Port P2 (P2.0 to P2.3) Diagram

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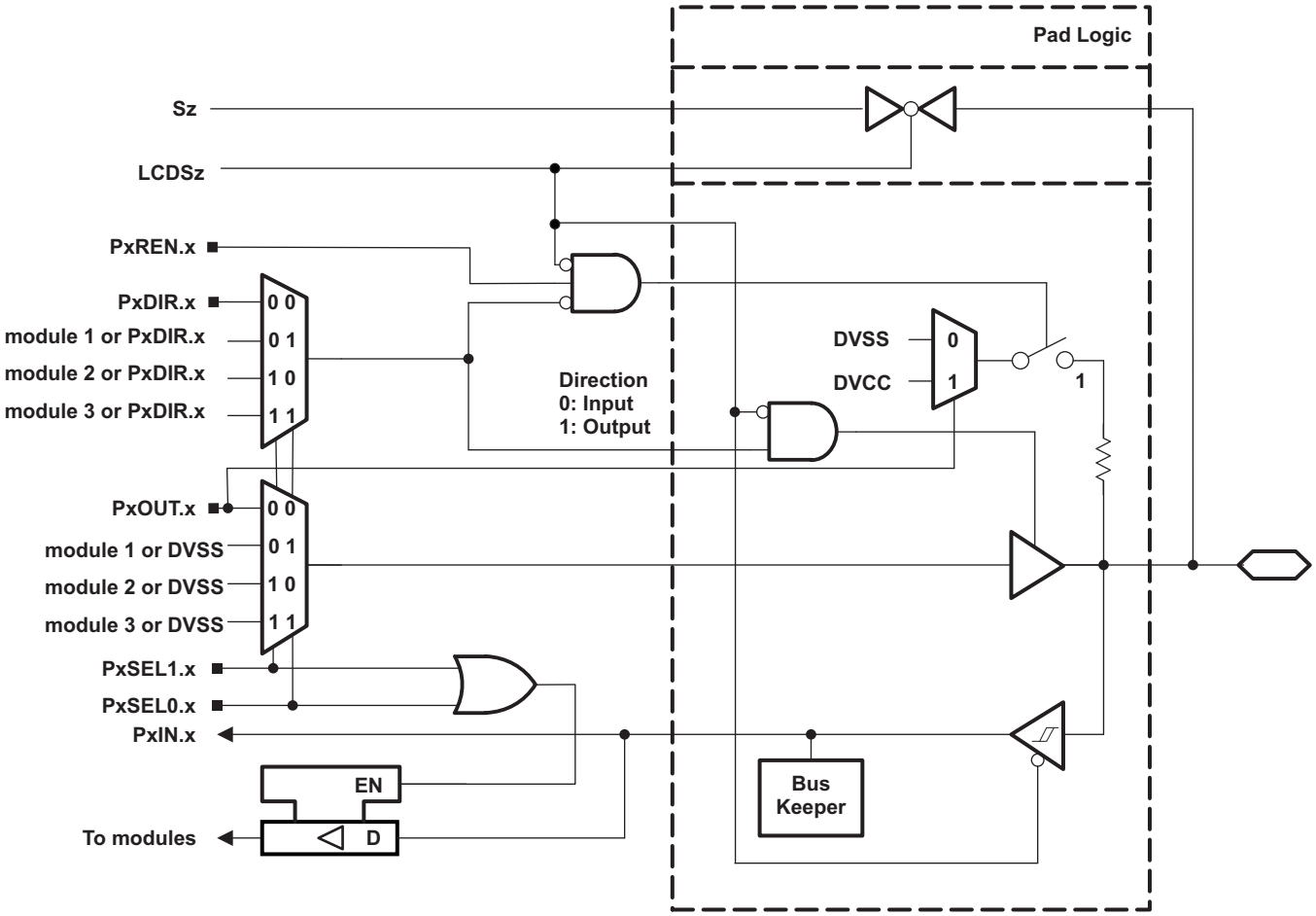
表 6-27. Port P2 (P2.0 to P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.0/UCA0SIMO/UCA0TXD/A6/C6	0	P2.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		UCA0SIMO/UCA0TXD	X[2]	1	0
		A6, C6[3][4]	X	1	1
P2.1/UCA0SOMI/UCA0RXD/A7/C7	1	P2.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		UCA0SOMI/UCA0RXD	X[2]	1	0
		A7, C7[3][4]	X	1	1
P2.2/COUT/UCA0CLK/A14/C14	2	P2.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		COUT	1		
		UCA0CLK	X[2]	1	0
		A14, C14[3][4]	X	1	1
P2.3/TA0.0/UCA0STE/A15/C15	3	P2.3(I/O)	I: 0; O: 1	0	0
		TA0.CCI0A	0	0	1
		TA0.0	1		
		UCA0STE	X[2]	1	0
		A15, C15[3][4]	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.

6.14.5 Port P2 (P2.4 to P2.7) Input/Output With Schmitt Trigger

図 6-6 shows the port diagram. 表 6-28 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-6. Port P2 (P2.4 to P2.7) Diagram

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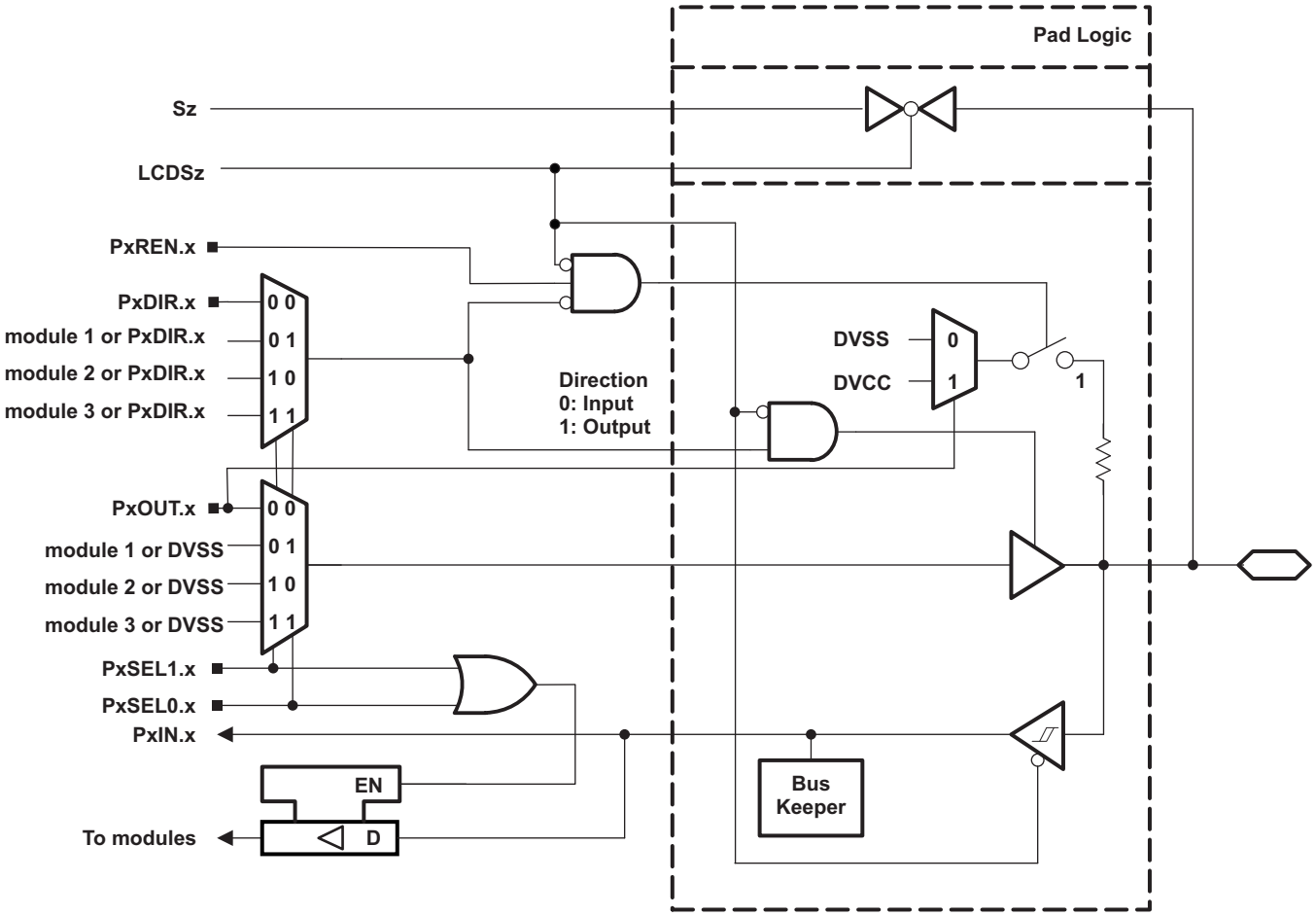
表 6-28. Port P2 (P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	LCDSz
P2.4/TA0LCK/TB0CLK/TA1CLK/LCDS32	4	P2.4 (I/O)	I: 0; O: 1	0	0	0
		TA0LCK	0	0	1	0
		Internally tied to DVSS	1			
		TB0LCK	0	1	0	0
		Internally tied to DVSS	1			
		TA1LCK	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P2.5/TA4.0/LCDS31	5	P2.5 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TA4.CCI0B	0	1	0	0
		TA4.0	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P2.6/TA4.1/LCDS30	6	P2.6 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TA4.CCI1B	0	1	0	0
		TA4.1	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P2.7/TA0.0/LCDS21	7	P2.7 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TA0.CCI0B	0	1	0	0
		TA0.0	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

6.14.6 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

図 6-7 shows the port diagram. 表 6-29 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-7. Port P3 (P3.0 to P3.7) Diagram

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表 6-29. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	LCDSz
P3.0/TB0.0/LCDS29	0	P3.0 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TB0.CCI0B	0	1	0	0
		TB0.0	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P3.1/TB0.1/LCDS28	1	P3.1 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		TB0.1	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P3.2/TB0.2/LCDS27	2	P3.2 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		TB0.2	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P3.3/TB0.3/LCDS26	3	P3.3 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TB0.CCI3B	0	1	0	0
		TB0.3	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P3.4/TB0OUTH/LCDS25	4	P3.4 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TB0OUTH	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

表 6-29. Port P3 (P3.0 to P3.7) Pin Functions (continued)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	LCDSz
P3.5/TB0.4/LCDS24	5	P3.5 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TB0.CCI4B	0	1	0	0
		TB0.4	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P3.6/TB0.5/LCDS23	6	P3.6 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TB0.CCI5B	0	1	0	0
		TB0.5	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P3.7/TB0.6/LCDS22	7	P3.7 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		TB0.CCI6B	0	1	0	0
		TB0.6	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

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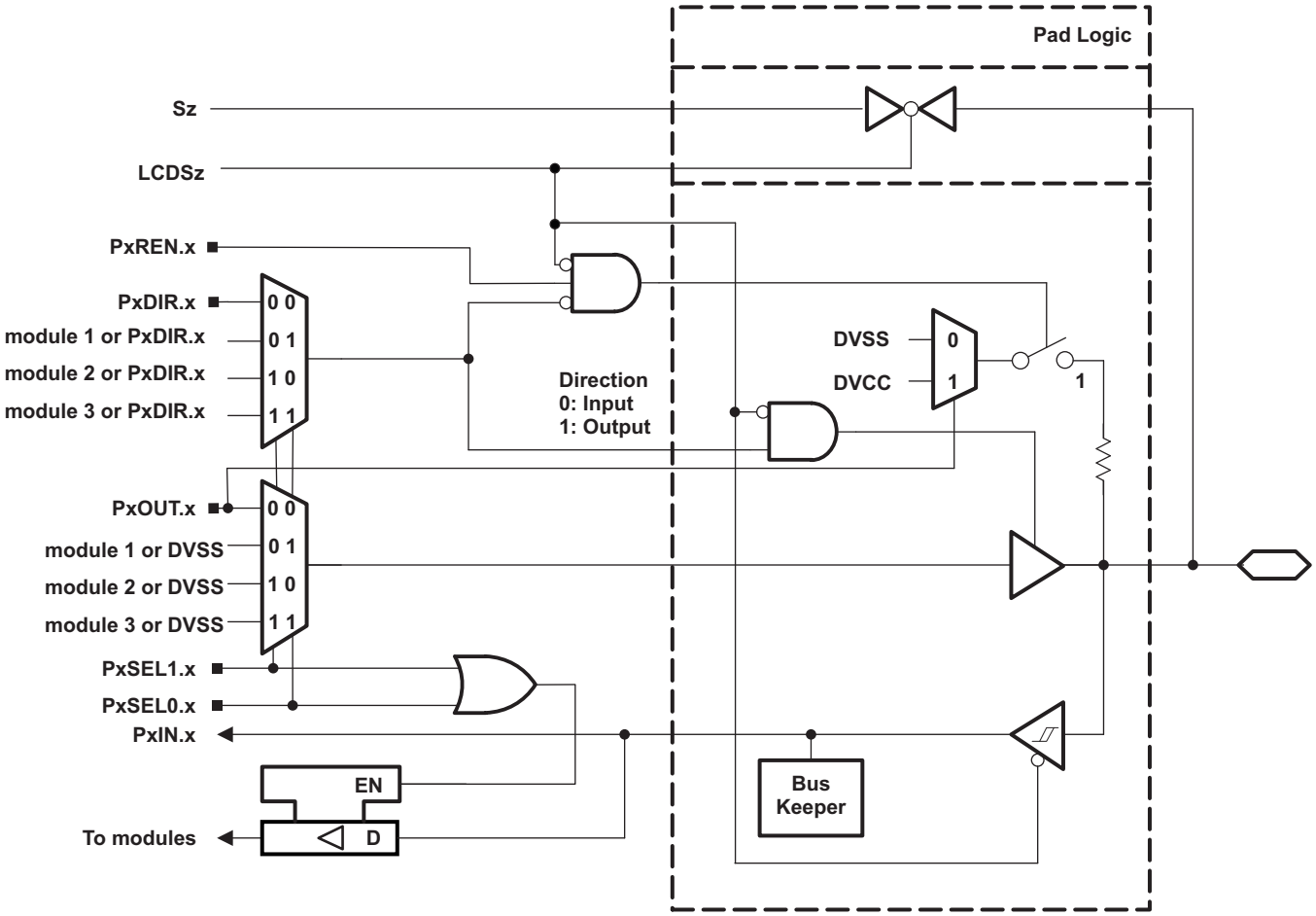
6.14.7 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

図 6-8 shows the port diagram. 表 6-30 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-8. Port P4 (P4.0 to P4.7) Diagram

表 6-30. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P4DIR.x	P4SEL1.x	P4SEL0.x	LCDSz
P4.0/RTCCLK/LCDS16	0	P4.0 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		RTCCLK	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

表 6-30. Port P4 (P4.0 to P4.7) Pin Functions (continued)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P4DIR.x	P4SEL1.x	P4SEL0.x	LCDSz
P4.1/UCA0CLK/LCDS15	1	P4.1 (I/O)	I: 0; O: 1	0	0	0
		UCA0CLK	X(3)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P4.2/UCA0STE/LCDS14	2	P4.2 (I/O)	I: 0; O: 1	0	0	0
		UCA0STE	X(3)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P4.3/UCA0SIMO/UCA0TXD/LCDS13	3	P4.3 (I/O)	I: 0; O: 1	0	0	0
		UCA0SIMO/UCA0TXD	X(3)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P4.4/UCA0SOMI/UCA0RXD/LCDS12	4	P4.4 (I/O)	I: 0; O: 1	0	0	0
		UCA0SOMI/UCA0RXD	X(3)	0	1	0
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P4.5/TA0LCK/TA1CLK/LCDS11	5	P4.5 (I/O)	I: 0; O: 1	0	0	0
		TA0CLK	0	0	1	0
		Internally tied to DVSS	1			
		TA1CLK	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P4.6/TB0CLK/TA4CLK/LCDS10	6	P4.6 (I/O)	I: 0; O: 1	0	0	0
		TB0CLK	0	0	1	0
		Internally tied to DVSS	1			
		TA4CLK	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(3) Direction controlled by eUSCI_A0 module.

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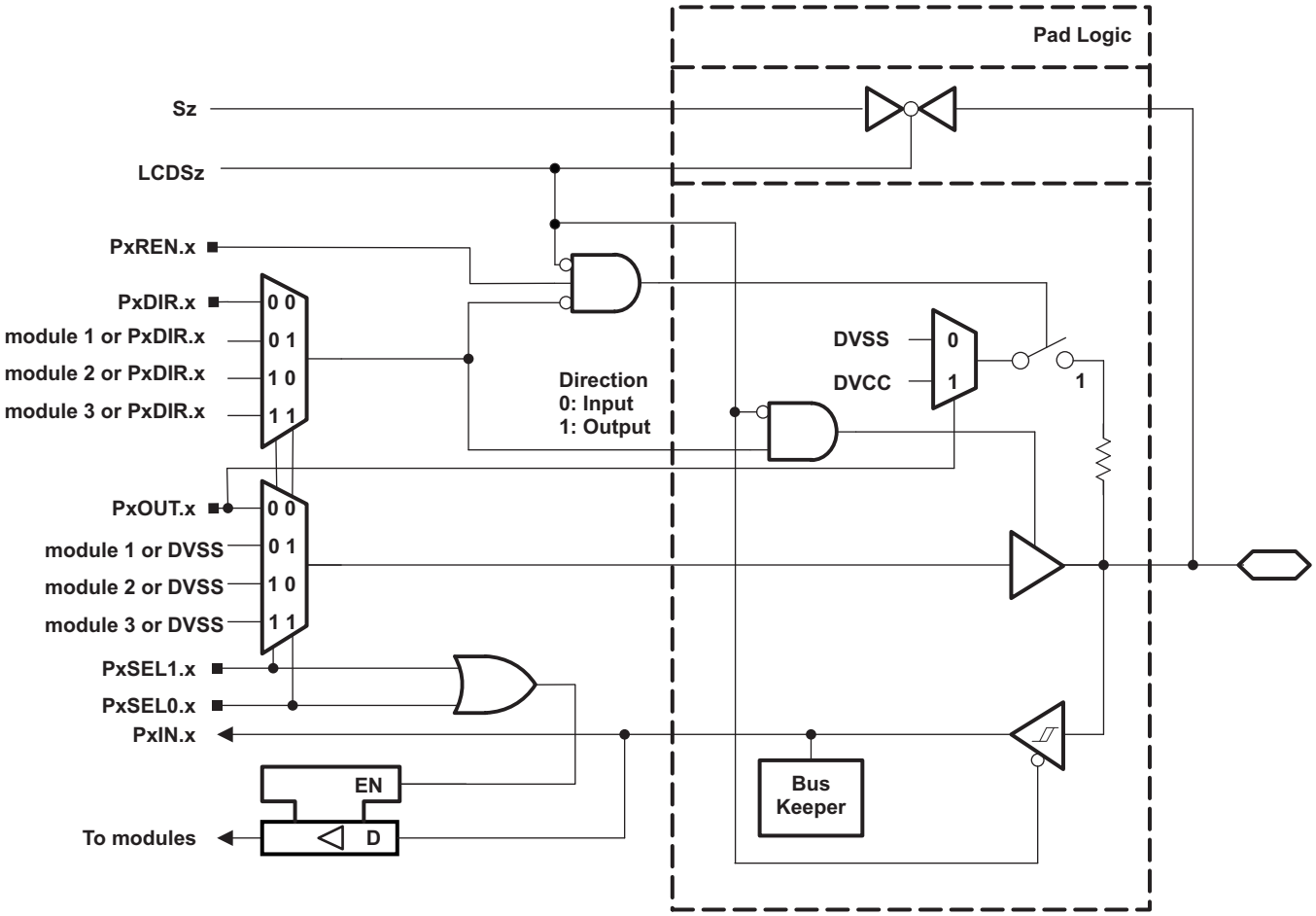
表 6-30. Port P4 (P4.0 to P4.7) Pin Functions (continued)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P4DIR.x	P4SEL1.x	P4SEL0.x	LCDSz
P4.7/DMAE0/LCDS9	7	P4.7 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		DMAE0	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

6.14.8 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger

図 6-9 shows the port diagram. 表 6-31 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-9. Port P5 (P5.0 to P5.7) Diagram

表 6-31. Port P5 (P5.0 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P5DIR.x	P5SEL1.x	P5SEL0.x	LCDSz
P5.0/UCA2SIMO/UCA2TXD/LCDS8	0	P5.0 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCA2SIMO/UCA2TXD	X(2)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

(1) X = Don't care
(2) Direction controlled by eUSCI_A3 module.
(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

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表 6-31. Port P5 (P5.0 to P5.7) Pin Functions (continued)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P5DIR.x	P5SEL1.x	P5SEL0.x	LCDSz
P5.1/UCA2SOMI/UCA2RXD/LCDS7	1	P5.1 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCA2SOMI/UCA2RXD	X(2)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.2/UCA2CLK/LCDS6	2	P5.2 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCA2CLK	X(2)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.3/UCA2STE/LCDS5	3	P5.3 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCA2STE	X(2)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.4/UCB1CLK/LCDS4	4	P5.4 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1CLK	X(4)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.5/TA0CLK/UCB1SIMO/UCB1SDA/LCDS3	5	P5.5 (I/O)	I: 0; O: 1	0	0	0
		TA0CLK	0	0	1	0
		Internally tied to DVSS	1			
		UCB1SIMO/UCB1SDA	X(4)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1
P5.6/UCB1SOMI/UCB1SCL/LCDS2	6	P5.6 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1SOMI/UCB1SCL	X(4)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

(4) Direction controlled by eUSCI_B1 module.

表 **6-31. Port P5 (P5.0 to P5.7) Pin Functions (continued)**

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P5DIR.x	P5SEL1.x	P5SEL0.x	LCDSz
P5.7/UCB1STE/LCDS1	7	P5.7 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		UCB1STE	X(4)	1	0	0
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (3)	X	X	X	1

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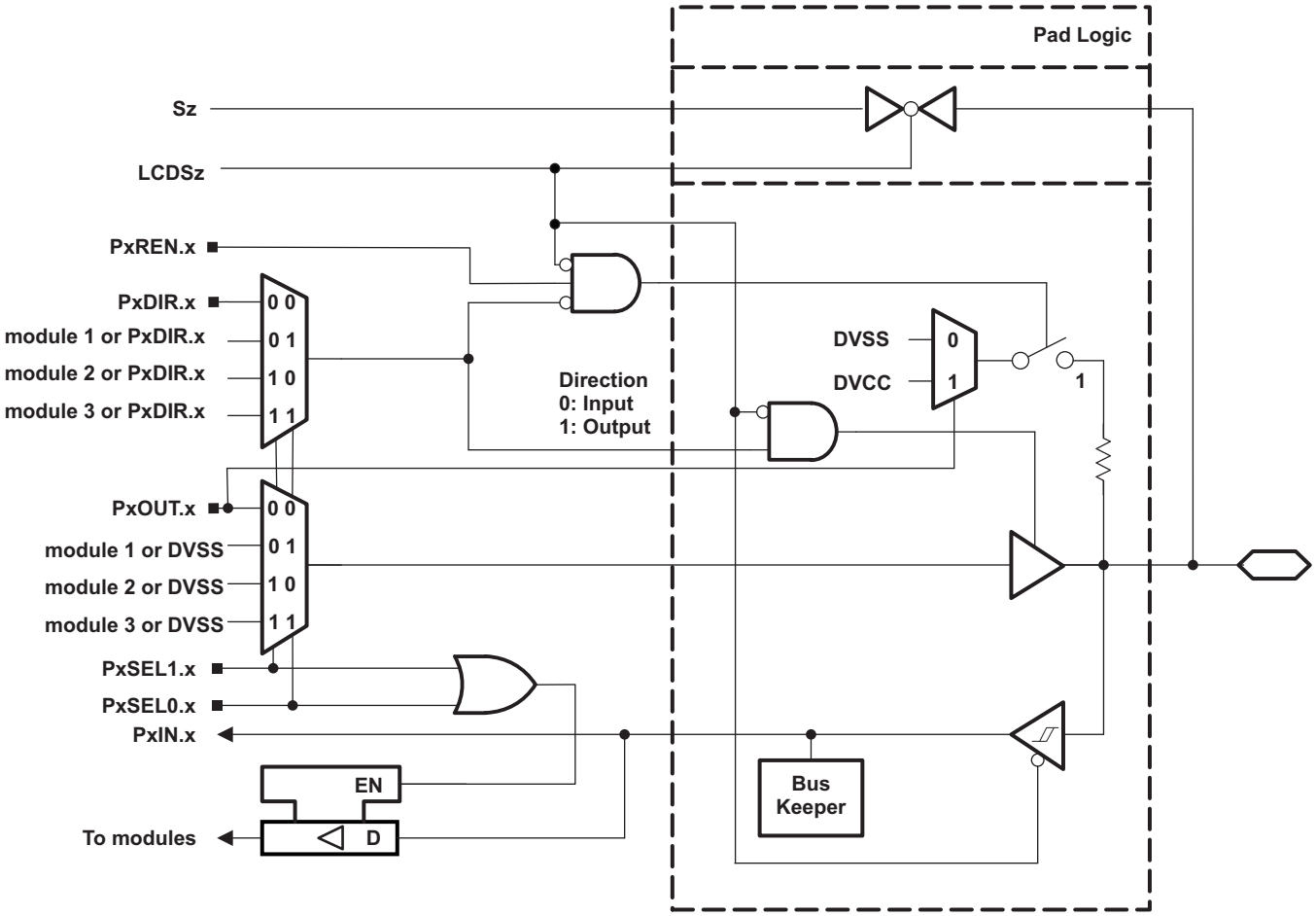
6.14.9 Port P6 (P6.0) Input/Output With Schmitt Trigger

図 6-10 shows the port diagram. 表 6-32 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-10. Port P6 (P6.0) Diagram

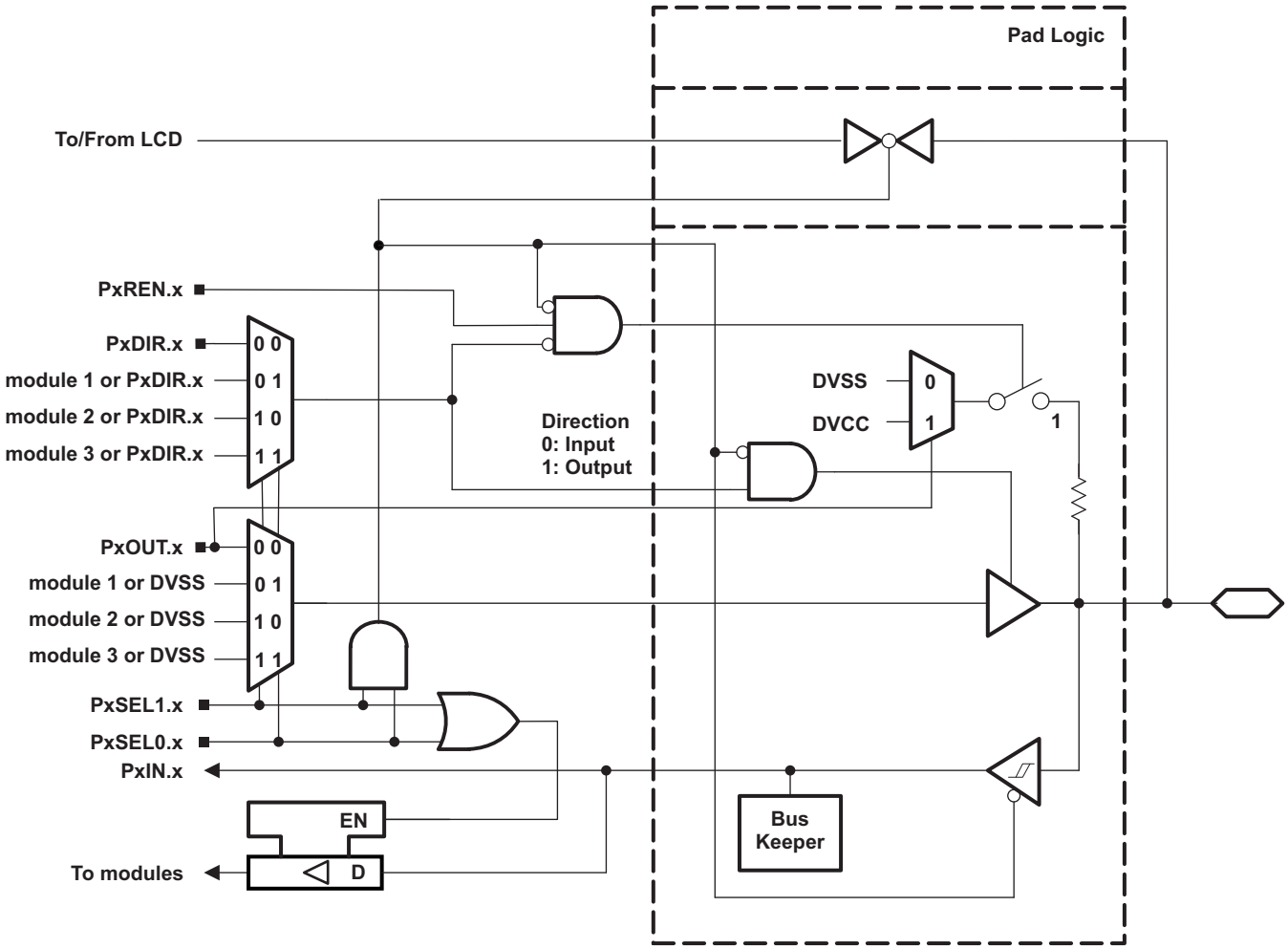
表 6-32. Port P6 (P6.0) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P6DIR.x	P6SEL1.x	P6SEL0.x	LCDSz
P6.0/COUT/LCDS0	0	P6.0 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		COUT	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

6.14.10 Port P6 (P6.1 to P6.5) Input/Output With Schmitt Trigger

図 6-11 shows the port diagram. 表 6-33 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-11. Port P6 (P6.1 to P6.5) Diagram

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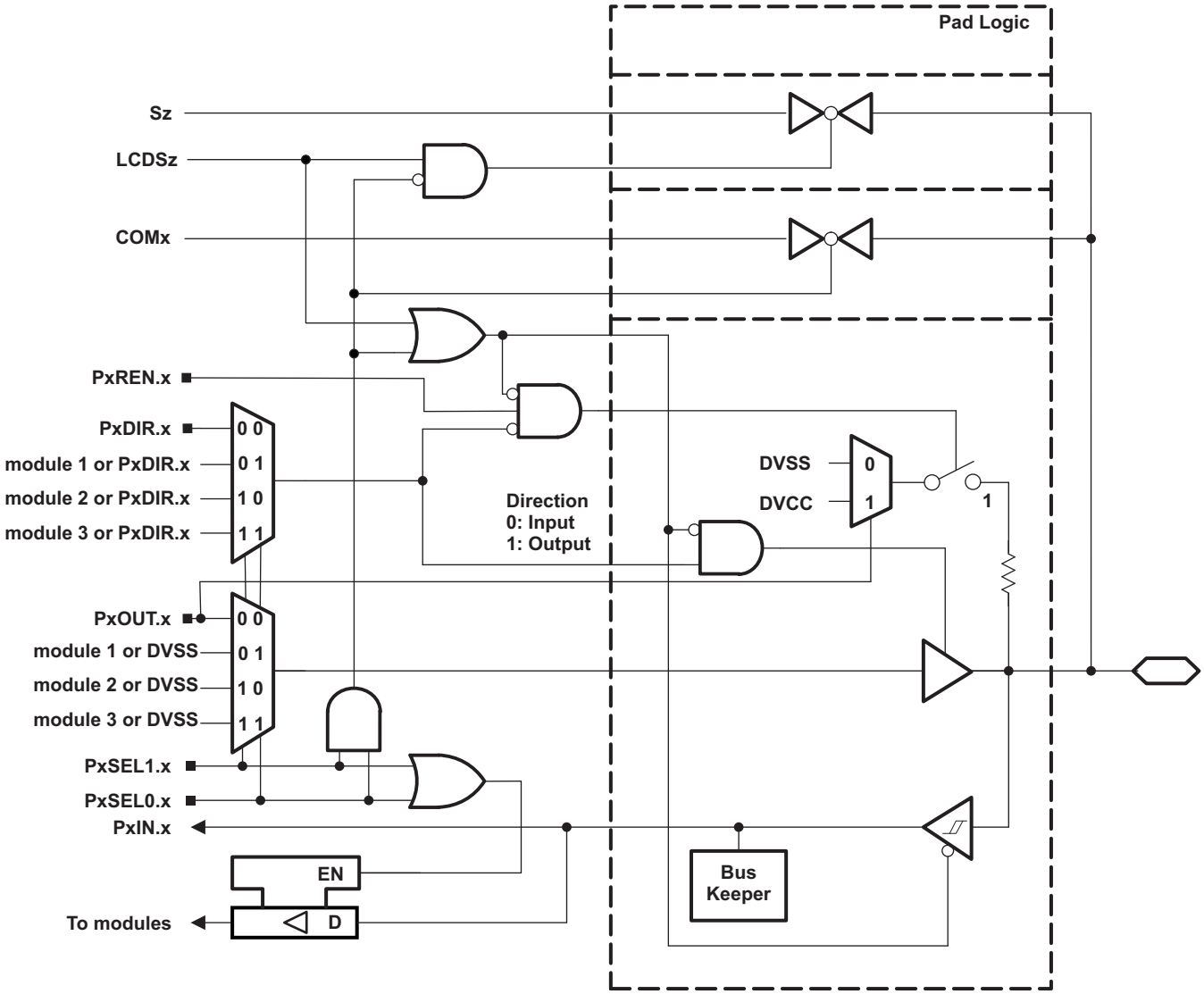
表 6-33. Port P6 (P6.1 to P6.5) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.1/R03	1	P6.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		R03 (2)	X	1	1
P6.2/R13/LCDREF	2	P6.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		R13/LCDREF (2)	X	1	1
P6.3/R23	3	P6.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		R23 (2)	X	1	1
P6.4/COM0	4	P6.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		COM0 (2)	X	1	1
P6.5/COM1	5	P6.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		COM1 (2)	X	1	1

(1) X = Don't care
(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.14.11 Port P6 (P6.6 and P6.7) Input/Output With Schmitt Trigger

図 6-12 shows the port diagram. 表 6-34 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-12. Port P6 (P6.6 and P6.7) Diagram

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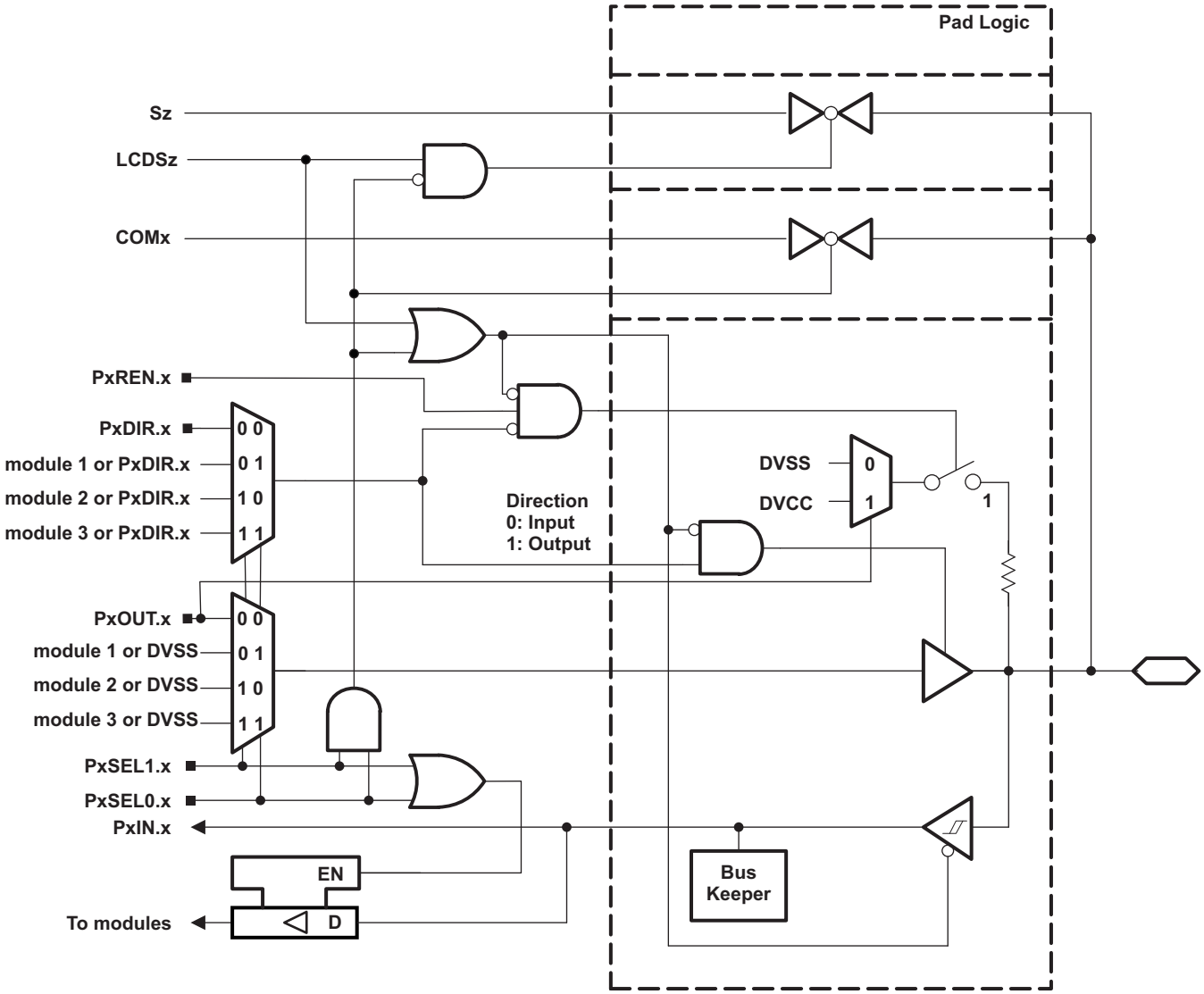
表 6-34. Port P6 (P6.6 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS			
			P6DIR.x	P6SEL1.x	P6SEL0.x	LCDSz
P6.6/COM2/LCDS38	6	P6.6(I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		COM2 (1)	X	1	1	0
		Sz (2)	X	X	0	1
				0	X	
P6.7/COM3/LCDS37	7	P6.7(I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		COM3 (1)	X	1	1	0
		Sz (2)	X	X	0	1
				0	X	

(1) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

6.14.12 Port P7 (P7.0 to P7.3) Input/Output With Schmitt Trigger

図 6-13 shows the port diagram. 表 6-35 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-13. Port P7 (P7.0 to P7.3) Diagram

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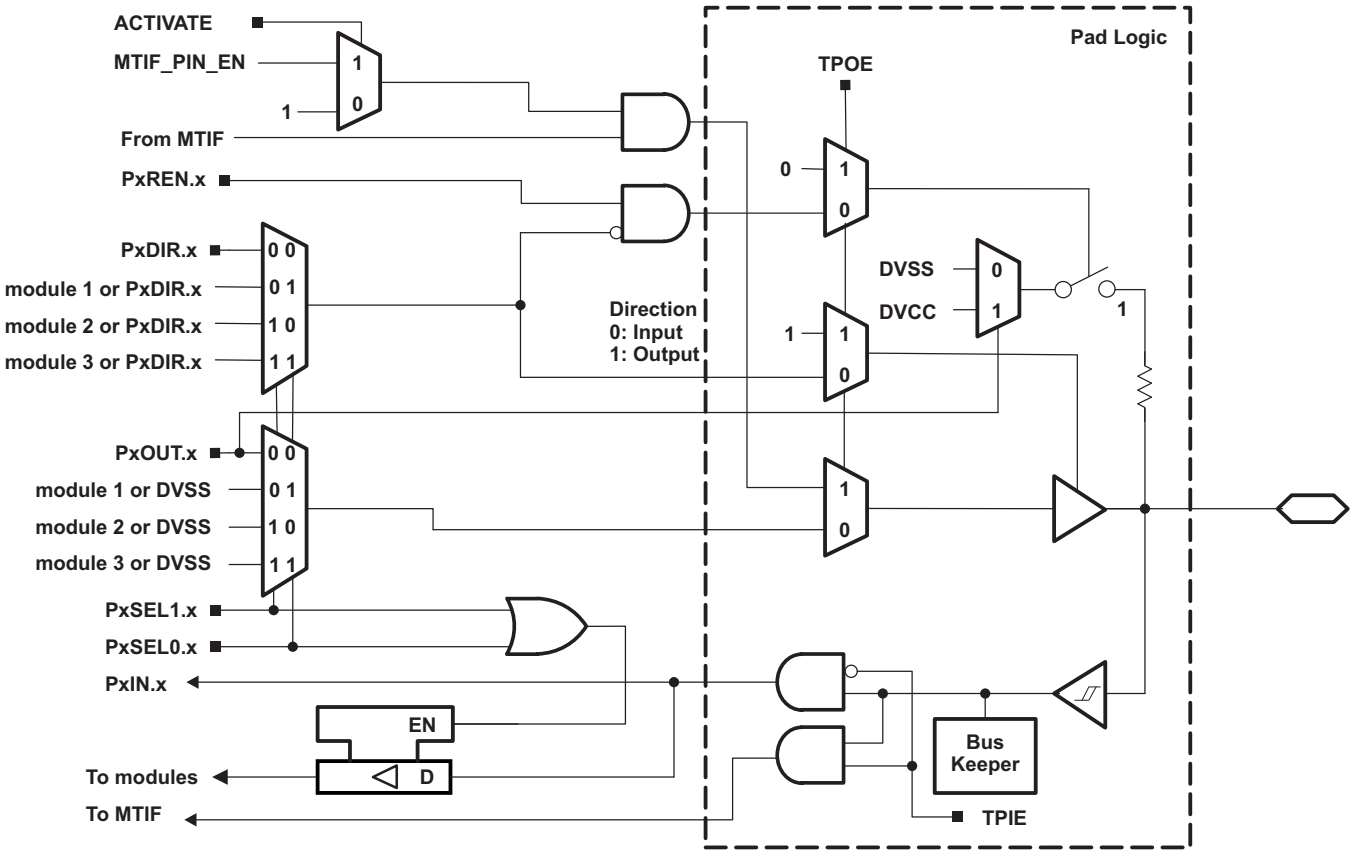
表 6-35. Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS			
			P7DIR.x	P7SEL1.x	P7SEL0.x	LCDSz
P7.0/UCA2SIMO/UCA2TXD/ ACLK/COM4/LCDS36	0	P7.0(I/O)	I: 0; O: 1	0	0	0
		UCA2SIMO/UCA2TXD	X(1)	0	1	0
		N/A	0	1	0	0
		ACLK	1			
		COM4(2)	X	1	1	0
		Sz (3)	X	X	0	1
				0	X	
P7.1/UCA2SOMI/UCA2RXD/ SMCLK/COM5/LCDS35	1	P7.1(I/O)	I: 0; O: 1	0	0	0
		UCA2SOMI/UCA2RXD	X(1)	0	1	0
		N/A	0	1	0	0
		SMCLK	1			
		COM5(2)	X	1	1	0
		Sz (3)	X	X	0	1
				0	X	
P7.2/UCA2CLK/TB0.0/COM6/ LCDS34	2	P7.2(I/O)	I: 0; O: 1	0	0	0
		UCA2CLK	X(1)	0	1	0
		TB0.CCI0A	0	1	0	0
		TB0.0	1			
		COM6(2)	X	1	1	0
		Sz (3)	X	X	0	1
				0	X	
P7.3/UCA2STE/TB0.1/COM7/ LCDS33	3	P7.3(I/O)	I: 0; O: 1	0	0	0
		UCA2STE	X(1)	0	1	0
		TB0.CCI1A	0	1	0	0
		TB0.1	1			
		COM7(2)	X	1	1	0
		Sz (3)	X	X	0	1
				0	X	

(1) Direction controlled by eUSCI_A2 module.
(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

6.14.13 Port P7 (P7.4) Input/Output With Schmitt Trigger

図 6-14 shows the port diagram. 表 6-36 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-14. Port P7 (P7.4) Diagram

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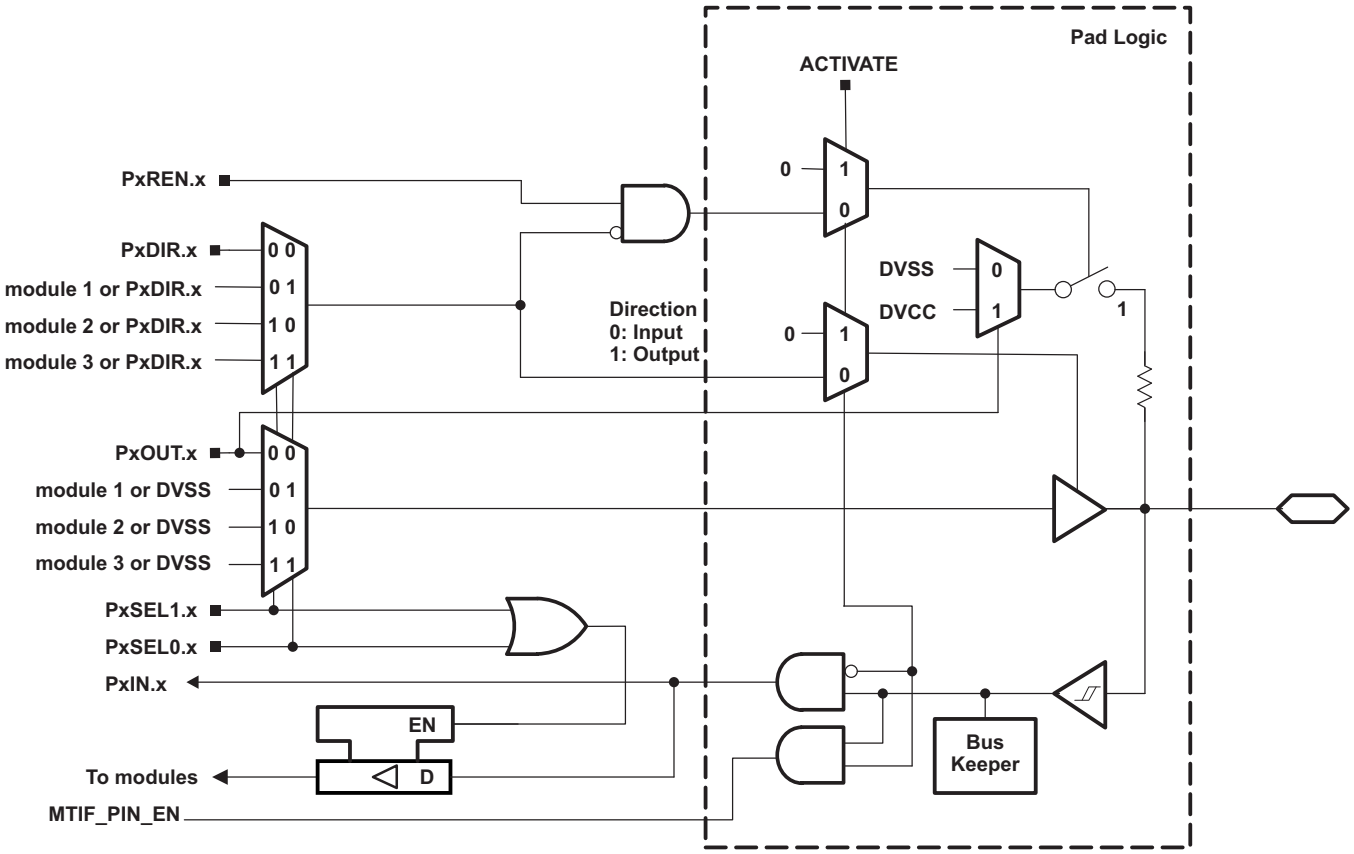
表 6-36. Port P7 (P7.4) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS						
			P7DIR.x	P7SEL1.x	P7SEL0.x	TPOE (1)	TPIE (1)	ACTIVATE (1)	Signal on MTIF_PIN_EN pin (2)
P7.4/TA0.1/ MTIF_OUT_IN	4	P7.4(I/O)	I: 0; O: 1	0	0	0	0	X	X
		TA0.CCI1A	0	0	1	0	0	X	X
		TA0.1	1						
		N/A	0	1	0	0	0	X	X
		Internally tied to DVSS	1						
		N/A	0	1	1	0	0	X	X
		Internally tied to DVSS	1						
		MTIF_IN	X	X	X	0	1	X	X
		MTIF_OUT (1)	X	X	X	1	X	0	X
		Internally tied to DVSS (1)	X	X	X	1	X	1	0
		MTIF_OUT (1)	X	X	X	1	X	1	1

(1) See MTIF.TPCTL register
(2) When P7.5 pin is configured as MTIF_PIN_EN (See 表 6-37 for details)

6.14.14 Port P7 (P7.5) Input/Output With Schmitt Trigger

図 6-15 shows the port diagram. 表 6-37 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-15. Port P7 (P7.5) Diagram

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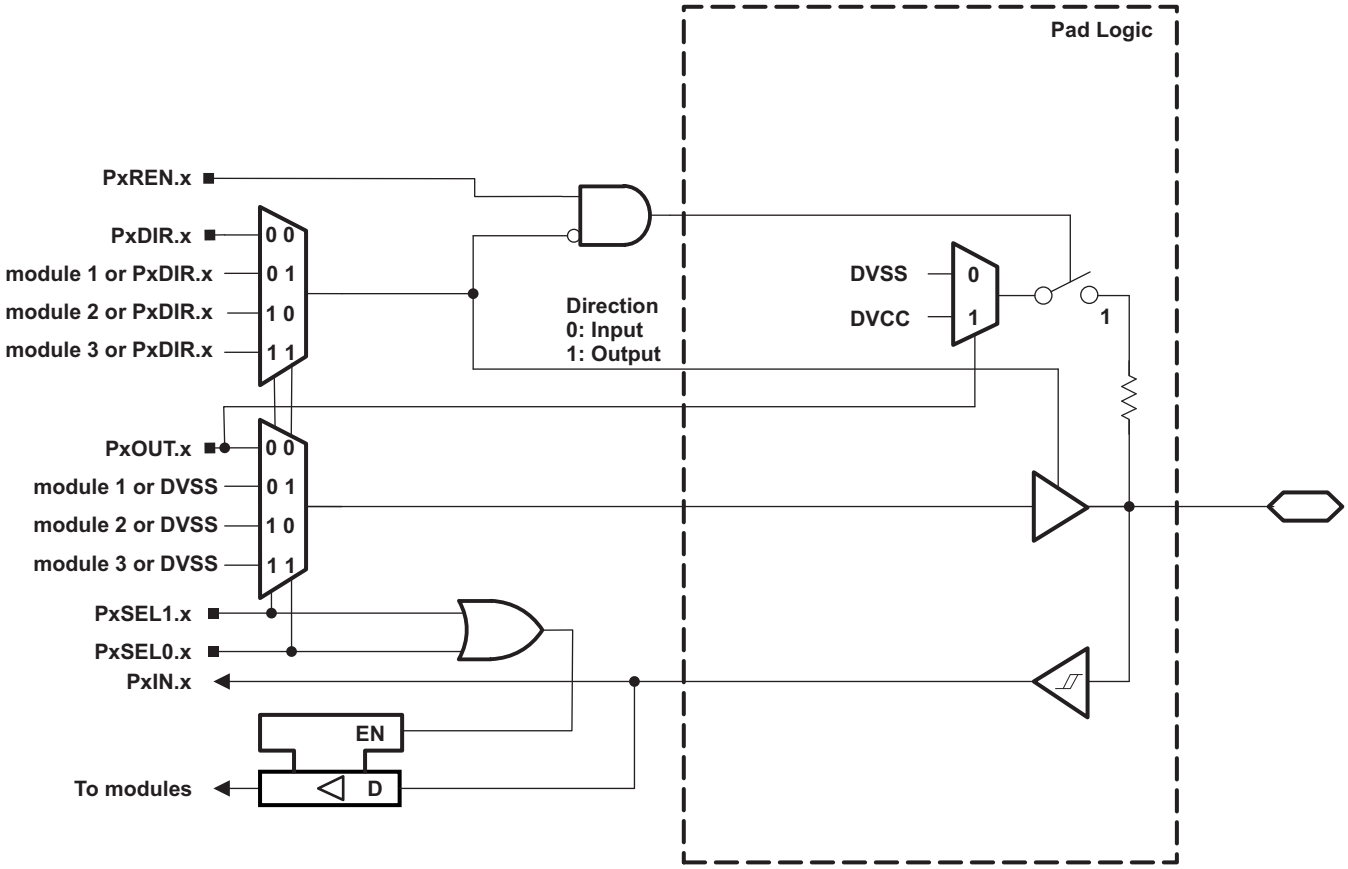
表 6-37. Port P7 (P7.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS			
			P7DIR.x	P7SEL1.x	P7SEL0.x	ACTIVATE (1)
P7.5/TA1.1/MTIF_PIN_EN	5	P7.5(I/O)	I: 0; O: 1	0	0	0
		TA1.CCI1A	0	0	1	0
		TA1.1	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		MTIF_PIN_EN	X	X	X	1

(1) See MTIF.TPCTL register

6.14.15 Port P7 (P7.6 and P7.7) Input/Output With Schmitt Trigger

図 6-16 shows the port diagram. 表 6-38 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-16. Port P7 (P7.6 and P7.7) Diagram

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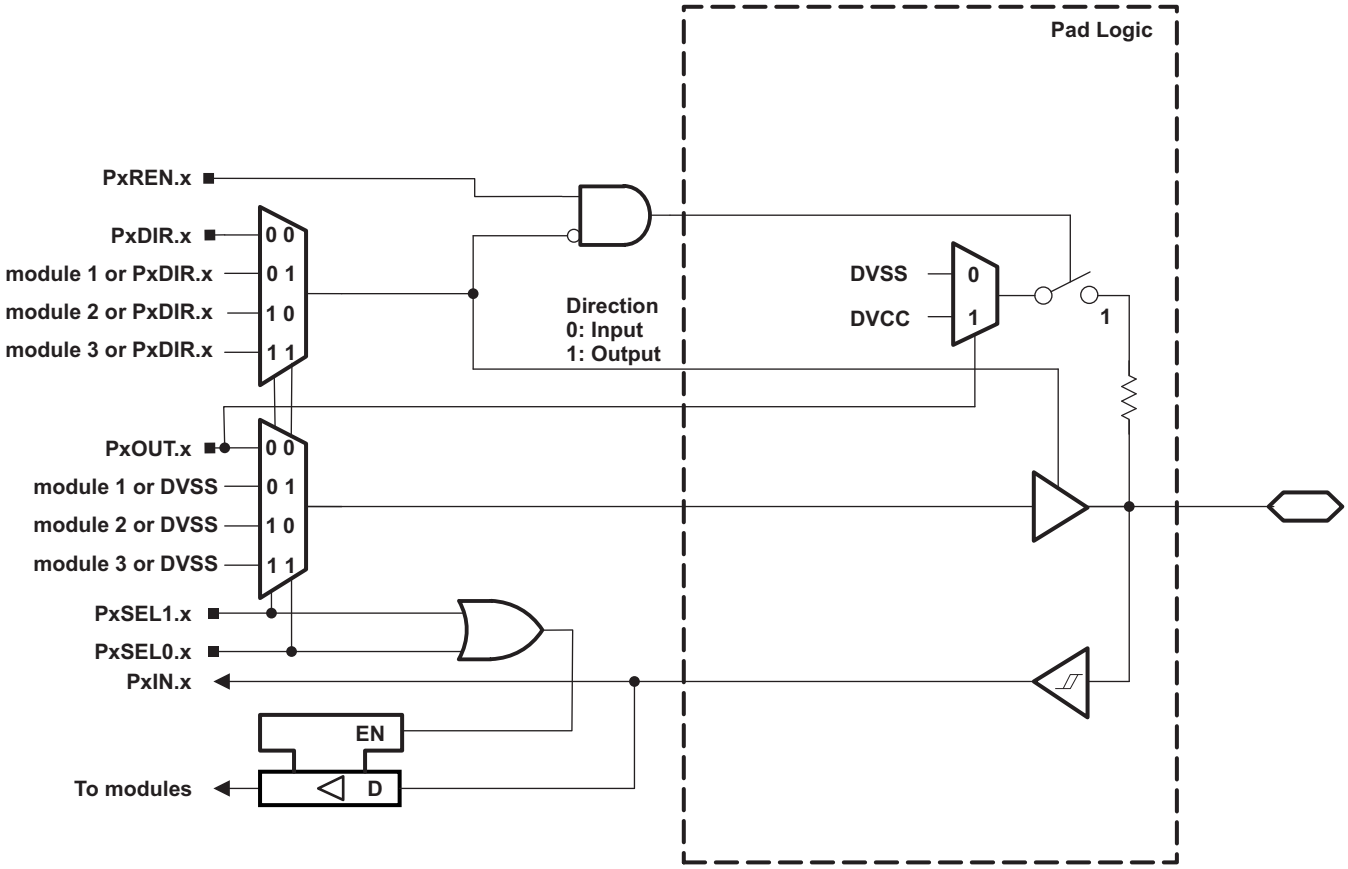
表 6-38. Port P7 (P7.6 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P7DIR.x	P7SEL1.x	P7SEL0.x
P7.6/TA4.1/DMAE0/COUT	6	P7.6(I/O)	I: 0; O: 1	0	0
		TA4.CCI1A	0	0	1
		TA4.1	1		
		DMAE0	0	1	0
		Internally tied to DVSS	1		
		N/A	0	1	1
		COUT	1		
P7.7/TA0.2/TB0OUTH/COUT	7	P7.7(I/O)	I: 0; O: 1	0	0
		TA0.CCI2A	0	0	1
		TA0.2	1		
		TB0OUTH	0	1	0
		Internally tied to DVSS	1		
		N/A	0	1	1
		COUT	1		

6.14.16 Port P8 (P8.0 to P8.3) Input/Output With Schmitt Trigger

図 6-17 shows the port diagram. 表 6-39 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-17. Port P8 (P8.0 to P8.3) Diagram

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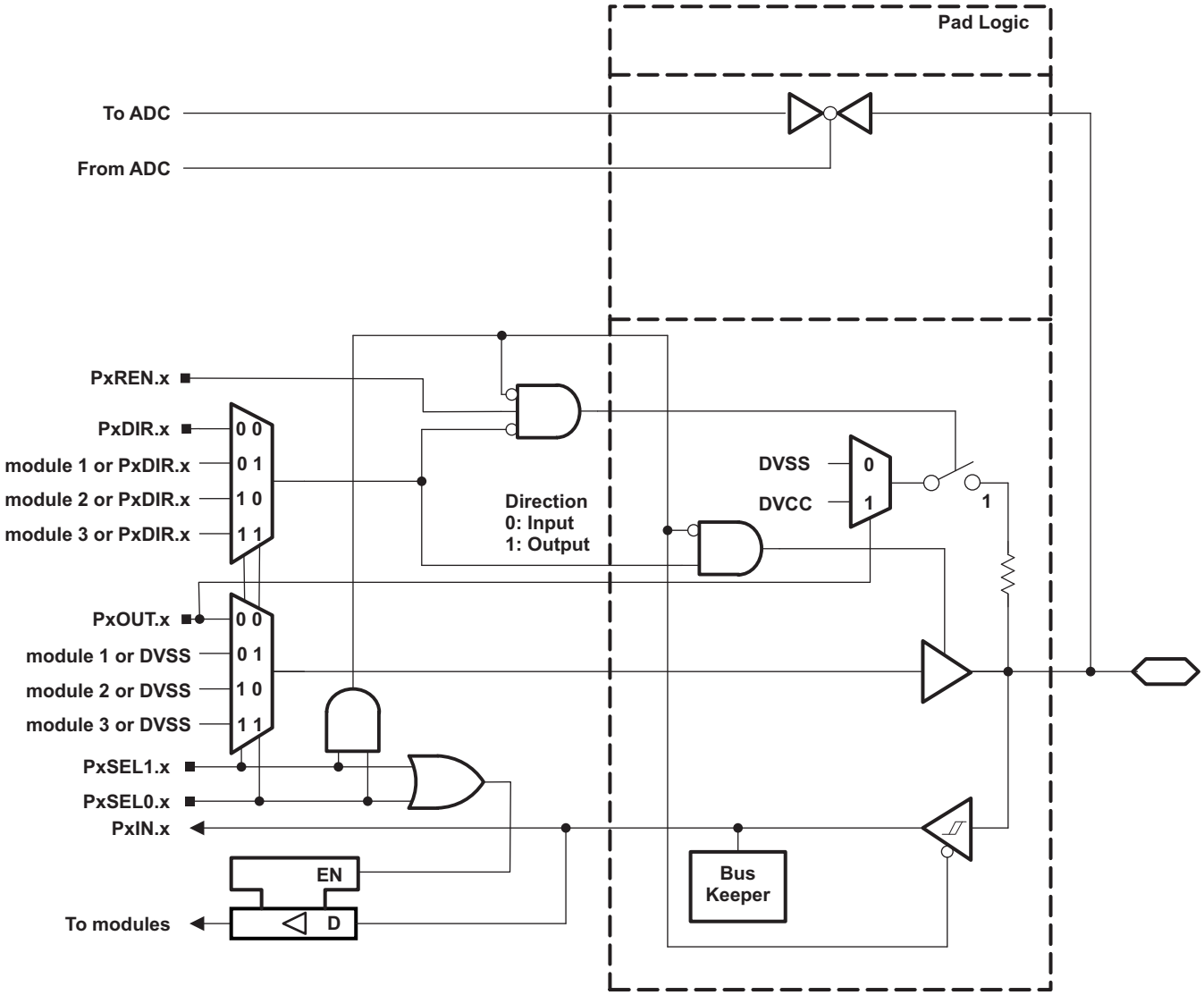
表 6-39. Port P8 (P8.0 to P8.3) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.0/UCA3STE/TB0.2/DMAE0	0	P8.0(I/O)	I: 0; O: 1	0	0
		UCA3STE	X(1)	0	1
		TB0.CCI2A	0	1	0
		TB0.2	1		
		DMAE0	0	1	1
		Internally tied to DVSS	1		
P8.1/UCA3CLK/TB0.3/TB0OUTH	1	P8.1(I/O)	I: 0; O: 1	0	0
		UCA3CLK	X(1)	0	1
		TB0.CCI3A	0	1	0
		TB0.3	1		
		TB0OUTH	0	1	1
		Internally tied to DVSS	1		
P8.2/UCA3SOMI/UCA3RXD/MCLK	2	P8.2(I/O)	I: 0; O: 1	0	0
		UCA3SOMI/UCA3RXD	X(1)	0	1
		N/A	0	1	0
		MCLK	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P8.3/UCA3SIMO/UCA3TXD/RTCCLK	3	P8.3(I/O)	I: 0; O: 1	0	0
		/UCA3SIMO/UCA3TXD	X(1)	0	1
		N/A	0	1	0
		RTCCLK	1		
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) Direction controlled by eUSCI_A3 module.

6.14.17 Port P8 (P8.4 to P8.7) Input/Output With Schmitt Trigger

図 6-18 shows the port diagram. 表 6-40 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-18. Port P8 (P8.4 to P8.7) Diagram

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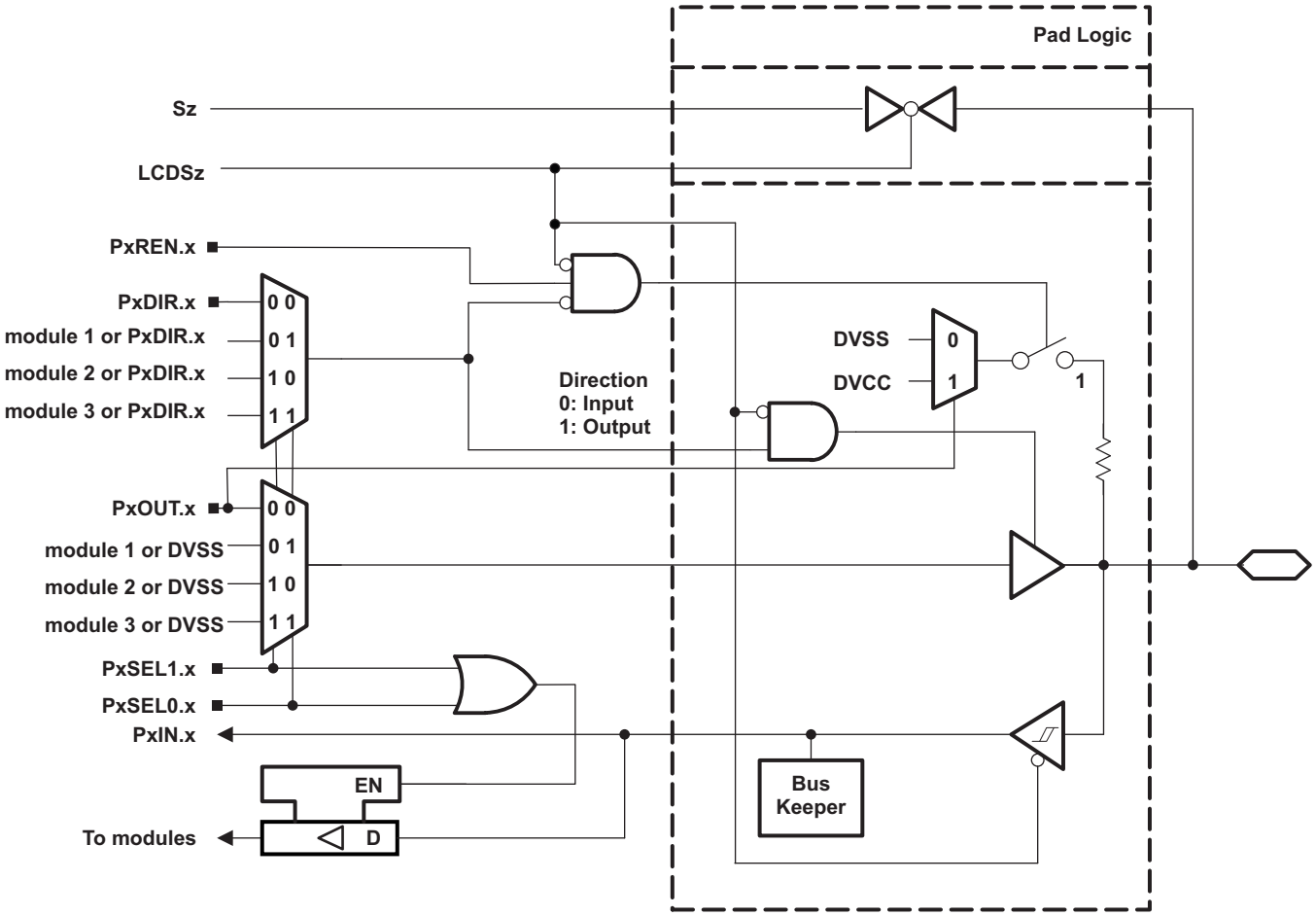
表 6-40. Port P8 (P8.4 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.4/UCB1CLK/TA1.2/A10	4	P8.4(I/O)	I: 0; O: 1	0	0
		UCB1CLK	X(1)	0	1
		TA1.CCI2A	0	1	0
		TA1.2	1		
		A10(2)	X	1	1
P8.5/UCB1SIMO/UCB1SDA/A11	5	P8.5(I/O)	I: 0; O: 1	0	0
		UCB1SIMO/UCB1SDA	X(1)	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		A11(2)	X	1	1
P8.6/UCB1SOMI/UCB1SCL/A12	6	P8.6(I/O)	I: 0; O: 1	0	0
		UCB1SOMI/UCB1SCL	X(1)	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		A12(2)	X	1	1
P8.7/UCB1STE/USSXT_BOUT/A13	7	P8.7(I/O)	I: 0; O: 1	0	0
		UCB1STE	X(1)	0	1
		N/A	0	1	0
		USSXT_BOUT(3)	1		
		A13(2)	X	1	1

(1) Direction controlled by eUSCI_B1 module.
(2) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) USSXTHSPLL.PLLXTLCTL.XTOUTOFF bit must also be set to 0.

6.14.18 Port P9 (P9.0 to P9.3) Input/Output With Schmitt Trigger

図 6-19 shows the port diagram. 表 6-41 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-19. Port P9 (P9.0 to P9.3) Diagram

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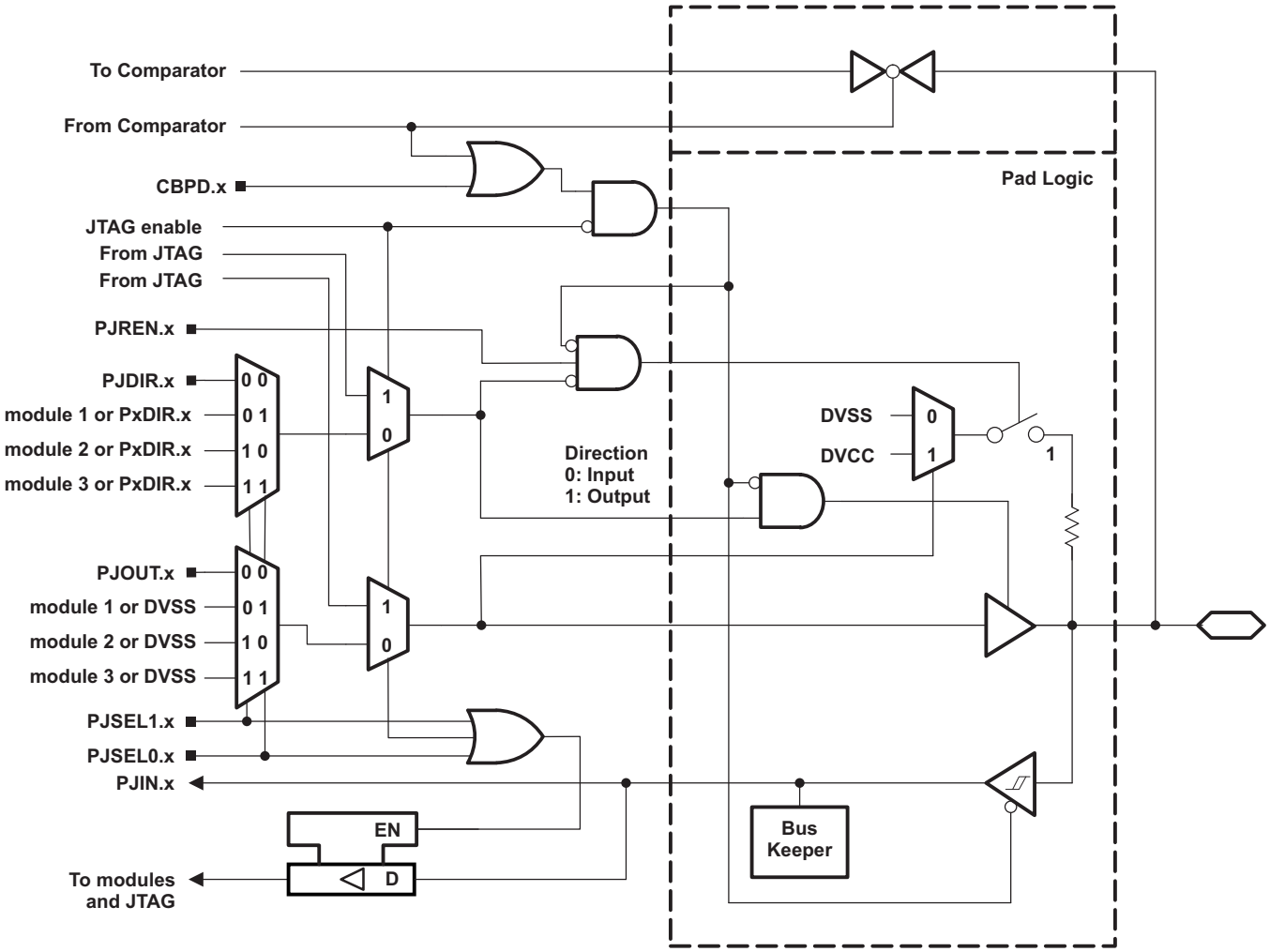
表 6-41. Port P9 (P9.0 to P9.3) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P9DIR.x	P9SEL1.x	P9SEL0.x	LCDSz
P9.0/TA1.0/LCDS20	0	P9.0 (I/O)	I: 0; O: 1	0	0	0
		TA1.CCI0B	0	0	1	0
		TA1.0	1			
		N/A	0	1	0	0
		Internally tied to DVSS	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P9.1/SMCLK/LCDS19	1	P9.1 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		SMCLK	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P9.2/MCLK/LCDS18	2	P9.2 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		MCLK	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1
P9.3/ACLK/LCDS17	3	P9.3 (I/O)	I: 0; O: 1	0	0	0
		N/A	0	0	1	0
		Internally tied to DVSS	1			
		N/A	0	1	0	0
		ACLK	1			
		N/A	0	1	1	0
		Internally tied to DVSS	1			
		Sz (2)	X	X	X	1

(1) X = Don't care
(2) Associated LCD segment is package dependent. Refer to the pin diagrams and signal descriptions in 4.1.

6.14.19 Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

図 6-20 shows the port diagram. 表 6-42 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-20. Port PJ (PJ.0 to PJ.3) Diagram

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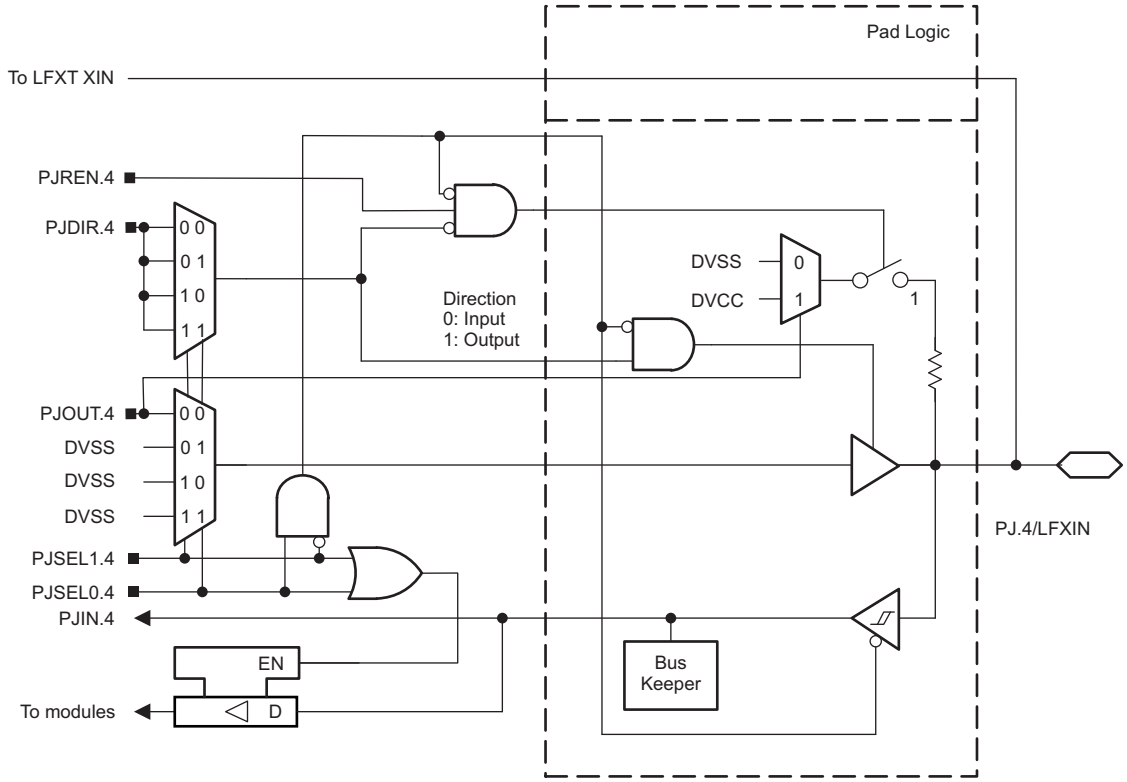
表 6-42. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[1]			
			PJDIR.x	PJSEL1.x	PJSEL0.x	CEPDx (Cx)
PJ.0/TDO/ACLK/SRSCG1/DMAE0/C10	0	PJ.0 (I/O)[2]	I: 0; O: 1	0	0	0
		TDO[3]	X	X	X	0
		N/A	0	0	1	0
		ACLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit SCG1	1			
		DMAE0	0	1	1	0
		Internally tied to DVSS	1			
		C10[4]	X	X	X	1
PJ.1/TDI/TCLK/SMCLK/SRSCG0/TA4CLK/C11	1	PJ.1 (I/O)[2]	I: 0; O: 1	0	0	0
		TDI/TCLK[3] [5]	X	X	X	0
		N/A	0	0	1	0
		SMCLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit SCG0	1			
		TA4CLK	0	1	1	0
		Internally tied to DVSS	1			
		C11[4]	X	X	X	1
PJ.2/TMS/MCLK/SROSCOFF/TB0OUTH/C12	2	PJ.2 (I/O)[2]	I: 0; O: 1	0	0	0
		TMS[3] [5]	X	X	X	0
		N/A	0	0	1	0
		MCLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit OSCOFF	1			
		TB0OUTH	0	1	1	0
		Internally tied to DVSS	1			
		C12[4]	X	X	X	1
PJ.3/TCK/RTCCLK/SRCPUOFF/TB0.6/C13	3	PJ.3 (I/O)[2]	I: 0; O: 1	0	0	0
		TCK[3] [5]	X	X	X	0
		N/A	0	0	1	0
		RTCCLK	1			
		N/A	0	1	0	0
		CPU Status Register Bit CPUOFF	1			
		TB0.CCI6A	0	1	1	0
		TB0.6	1			
		C13[4]	X	X	X	1

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made through the SYS module or by the Spy-Bi-Wire four-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPDx bits have an effect in these cases.
(4) Setting the CEPDx bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables The output driver and input buffer for that pin, regardless of the state of the associated CEPDx bit.
(5) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.14.20 Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

図 6-21 and 図 6-22 show the port diagrams. 表 6-43 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-21. Port PJ (PJ.4) Diagram

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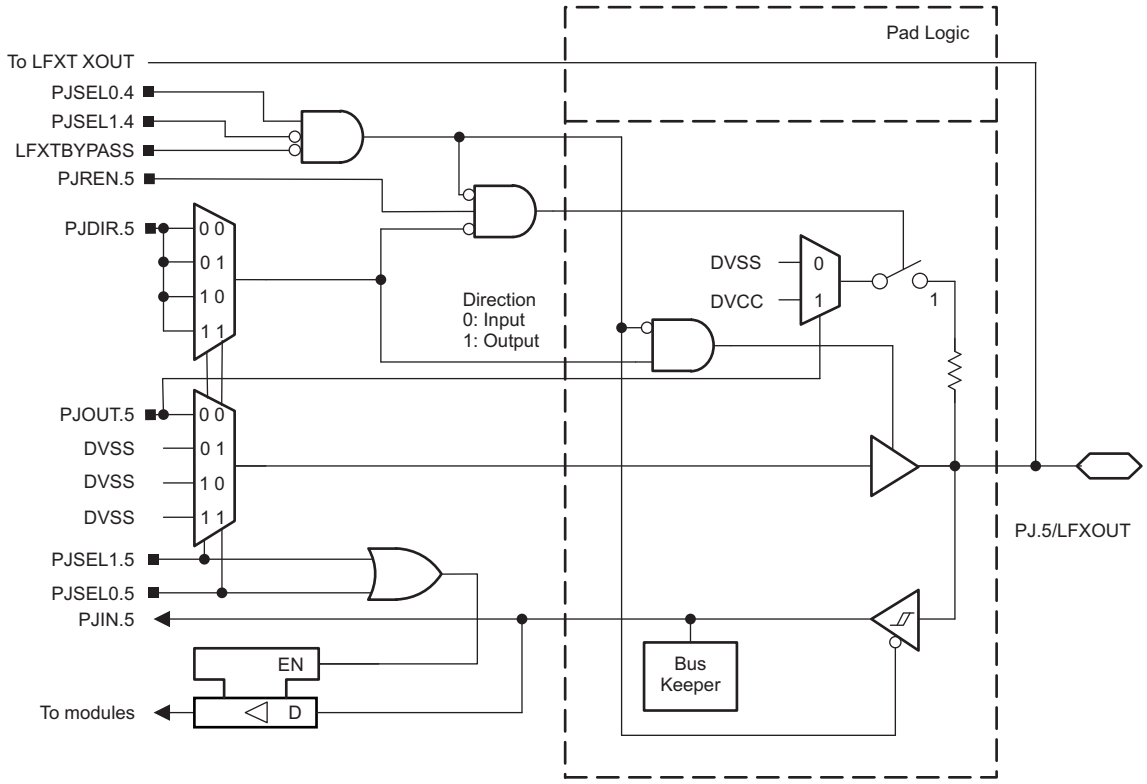

NOTE: Functional representation only.

図 6-22. Port PJ (PJ.5) Diagram

表 6-43. Port PJ (PJ.4 and PJ.5) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			PJDIR.x	PJSEL1.5	PJSEL0.5	PJSEL1.4	PJSEL0.4	LFXT BYPASS
PJ.4/LFXIN	4	PJ.4 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		LFXIN crystal mode[2]	X	X	X	0	1	0
		LFXIN bypass mode[2]	X	X	X	0	1	1
PJ.5/LFXOUT	5	PJ.5 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1[3]
		N/A	0	see[4]	see[4]	0	0	0
						1	X	
						X	X	1[3]
		Internally tied to DVSS	1	see[4]	see[4]	0	0	0
						1	X	
						X	X	1[3]
		LFXOUT crystal mode[2]	X	X	X	0	1	0

(1) X = Don't care
(2) If PJSEL1.4 = 0 and PJSEL0.4 = 1, the general-purpose I/O is disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.
(4) If PJSEL0.5 = 1 or PJSEL1.5 = 1, the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

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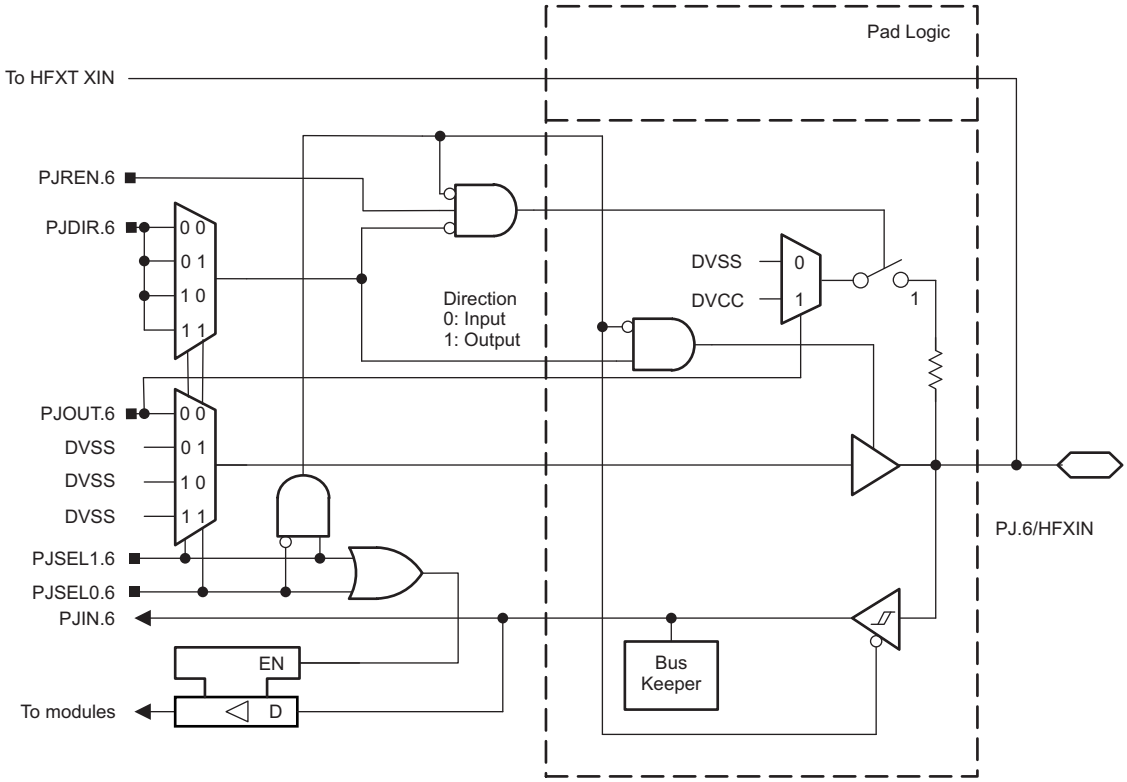
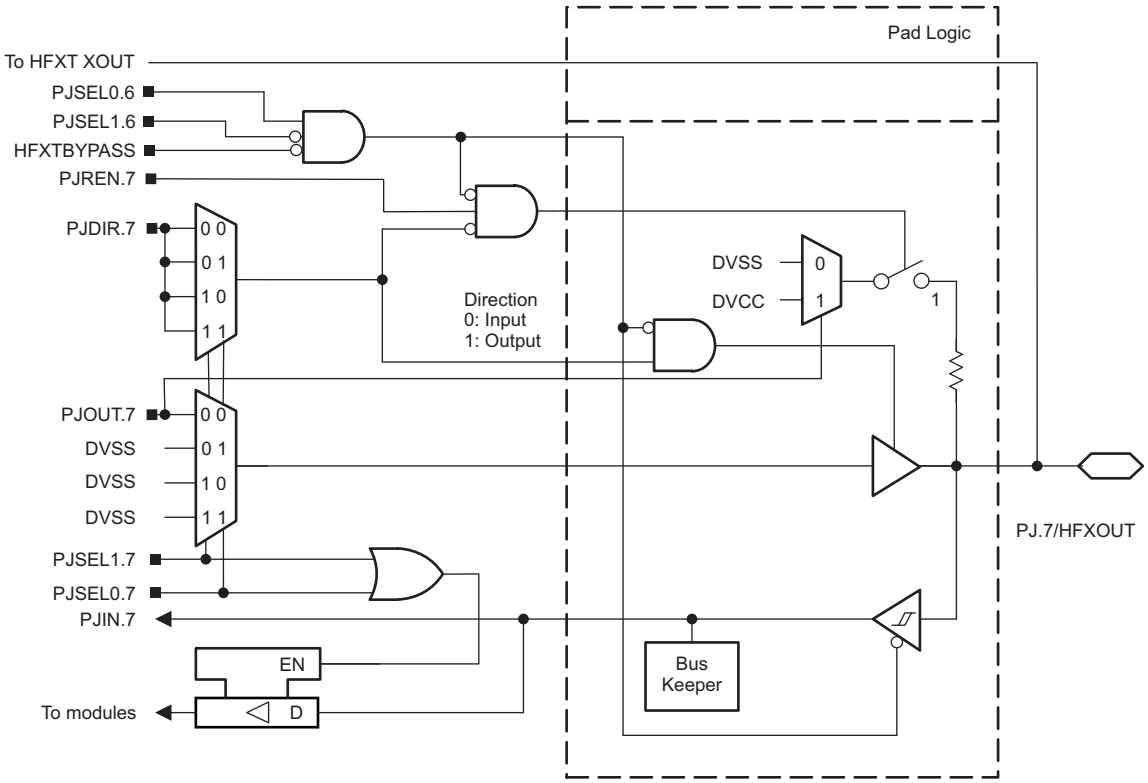
6.14.21 Port PJ (PJ.6 and PJ.7) Input/Output With Schmitt Trigger

図 6-23 and 図 6-24 show the port diagrams. 表 6-44 summarizes the selection of the pin function.



NOTE: Functional representation only.

図 6-23. Port PJ (PJ.6) Diagram



NOTE: Functional representation only.

図 6-24. Port PJ (PJ.7) Diagram

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表 6-44. Port PJ (PJ.6 and PJ.7) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			PJDIR.x	PJSEL1.7	PJSEL0.7	PJSEL1.6	PJSEL0.6	HFXTBYPASS
PJ.6/HFXIN	6	PJ.6 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		HFXIN crystal mode[2]	X	X	X	0	1	0
		HFXIN bypass mode[2]	X	X	X	0	1	1
PJ.7/HFXOUT	7	PJ.7 (I/O)[3]	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1[4]
		N/A	0	see [3]	see [3]	0	0	0
						1	X	
						X	X	1[4]
		Internally tied to DVSS	1	see [3]	see [3]	0	0	0
						1	X	
						X	X	1[4]
		HFXOUT crystal mode[2]	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are do not care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.
(3) With PJSEL0.7 = 1 or PJSEL1.7 =1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output the pin is actively pulled to zero.
(4) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.

6.15 Device Descriptors (TLV)

表 6-45 lists the Device IDs.

表 6-45. Device IDs

DEVICE	PACKAGE	DEVICE ID	
		01A05h	01A04h
MSP430FR6047	PZ	82h	EAh
MSP430FR60471	PZ	82h	EEh
MSP430FR6045	PZ	82h	EBh
MSP430FR6037	PZ	82h	ECh
MSP430FR60371	PZ	82h	EFh
MSP430FR6035	PZ	82h	EDh

表 6-46 lists the contents of the device descriptor tag-length-value (TLV) structure.

表 6-46. Device Descriptors(1)

	DESCRIPTION	MSP430FR60xx (UART BSL)		MSP430FR60xx1 (I^2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
Info Block	Info length	01A00h	06h	01A00h	06h
	CRC length	01A01h	06h	01A01h	06h
	CRC value	01A02h	Per unit	01A02h	Per unit
		01A03h	Per unit	01A03h	Per unit
	Device ID	01A04h	See 表 6-45.	01A04h	See 表 6-45.
		01A05h			
	Hardware revision	01A06h	Per unit	01A06h	Per unit
	Firmware revision	01A07h	Per unit	01A07h	Per unit
Die Record	Die record tag	01A08h	08h	01A08h	08h
	Die record length	01A09h	0Ah	01A09h	0Ah
	Lot/wafer ID	01A0Ah	Per unit	01A0Ah	Per unit
		01A0Bh	Per unit	01A0Bh	Per unit
		01A0Ch	Per unit	01A0Ch	Per unit
		01A0Dh	Per unit	01A0Dh	Per unit
	Die X position	01A0Eh	Per unit	01A0Eh	Per unit
		01A0Fh	Per unit	01A0Fh	Per unit
	Die Y position	01A10h	Per unit	01A10h	Per unit
		01A11h	Per unit	01A11h	Per unit
	Test results	01A12h	Per unit	01A12h	Per unit
		01A13h	Per unit	01A13h	Per unit

(1) NA = Not applicable, Per unit = content can differ from device to device

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表 6-46. Device Descriptors[(1)] (continued)

	DESCRIPTION	MSP430FR60xx (UART BSL)		MSP430FR60xx1 (I^2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
ADC12 Calibration	ADC12 calibration tag	01A14h	11h	01A14h	11h
	ADC12 calibration length	01A15h	10h	01A15h	10h
	ADC gain factor[(2)]	01A16h	Per unit	01A16h	Per unit
		01A17h	Per unit	01A17h	Per unit
	ADC offset[(3)]	01A18h	Per unit	01A18h	Per unit
		01A19h	Per unit	01A19h	Per unit
	ADC 1.2-V reference temperature sensor 30°C	01A1Ah	Per unit	01A1Ah	Per unit
		01A1Bh	Per unit	01A1Bh	Per unit
	ADC 1.2-V reference temperature sensor 85°C	01A1Ch	Per unit	01A1Ch	Per unit
		01A1Dh	Per unit	01A1Dh	Per unit
	ADC 2.0-V reference temperature sensor 30°C	01A1Eh	Per unit	01A1Eh	Per unit
		01A1Fh	Per unit	01A1Fh	Per unit
	ADC 2.0-V reference temperature sensor 85°C	01A20h	Per unit	01A20h	Per unit
		01A21h	Per unit	01A21h	Per unit
	ADC 2.5-V reference temperature sensor 30°C	01A22h	Per unit	01A22h	Per unit
		01A23h	Per unit	01A23h	Per unit
	ADC 2.5-V reference temperature sensor 85°C	01A24h	Per unit	01A24h	Per unit
		01A25h	Per unit	01A25h	Per unit
REF Calibration	REF calibration tag	01A26h	12h	01A26h	12h
	REF calibration length	01A27h	06h	01A27h	06h
	REF 1.2-V reference	01A28h	Per unit	01A28h	Per unit
		01A29h	Per unit	01A29h	Per unit
	REF 2.0-V reference	01A2Ah	Per unit	01A2Ah	Per unit
		01A2Bh	Per unit	01A2Bh	Per unit
	REF 2.5-V reference	01A2Ch	Per unit	01A2Ch	Per unit
		01A2Dh	Per unit	01A2Dh	Per unit

(2) ADC gain: The gain correction factor is measured at room temperature using a 2.5-V external voltage reference without internal buffer (ADC12VRSEL = 0x2, 0x4, or 0xE). Other settings (for example, using internal reference) can result in different correction factors.
(3) ADC offset: the offset correction factor is measured at room temperature using ADC12VRSEL= 0x2 or 0x4, an external reference, V_{R+} = external 2.5 V, V_{R-} = AVSS.

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表 6-46. Device Descriptors[(1)] (continued)

	DESCRIPTION	MSP430FR60xx (UART BSL)		MSP430FR60xx1 (I^2C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
Random Number	128-bit random number tag	01A2Eh	15h	01A2Eh	15h
	Random number length	01A2Fh	10h	01A2Fh	10h
	128-bit random number[(4)]	01A30h	Per unit	01A30h	Per unit
		01A31h	Per unit	01A31h	Per unit
		01A32h	Per unit	01A32h	Per unit
		01A33h	Per unit	01A33h	Per unit
		01A34h	Per unit	01A34h	Per unit
		01A35h	Per unit	01A35h	Per unit
		01A36h	Per unit	01A36h	Per unit
		01A37h	Per unit	01A37h	Per unit
		01A38h	Per unit	01A38h	Per unit
		01A39h	Per unit	01A39h	Per unit
		01A3Ah	Per unit	01A3Ah	Per unit
		01A3Bh	Per unit	01A3Bh	Per unit
		01A3Ch	Per unit	01A3Ch	Per unit
		01A3Dh	Per unit	01A3Dh	Per unit
		01A3Eh	Per unit	01A3Eh	Per unit
		01A3Fh	Per unit	01A3Fh	Per unit
BSL Configuration	BSL tag	01A40h	1Ch	01A40h	1Ch
	BSL length	01A41h	02h	01A41h	02h
	BSL interface	01A42h	00h	01A42h	01h
	BSL interface configuration	01A43h	00h	01A43h	48h

(4) 128-bit random number: The random number is generated during production test using the Microsoft® CryptGenRandom() function.

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6.16 Memory Map

表 6-47 summarizes the memory organization for all device variants.

表 6-47. Memory Organization(1)

		MSP430FR6047(1), FR6037(1)	MSP430FR6045, FR6035
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Total Size	256KB 00FFFFh to 00FF80h 043FFFh to 004000h	128KB 00FFFFh to 00FF80h 0023FFFh to 004000h
RAM (shared with LEA) (Sector 2) Block 0	Size	4KB (003BFFh to 002C00h) 003BFFh to 002C00h	4KB (003BFFh to 002C00h) 003BFFh to 002C00h
System RAM (Sector 1) (Sector 0) Main: base location Main: interrupt vectors	Size	4KB (002BFFh to 002400h) (0023FFh to 001C00h) 002BFFh to 001C00h 002BFFh to 002B80h	4KB (002BFFh to 002400h) (0023FFh to 001C00h) 002BFFh to 001C00h 002BFFh to 002B80h
Device descriptor info (TLV) (FRAM)	Size	256 B 001AFFh to 001A00h	256 B 001AFFh to 001A00h
TI calibration and configuration (FRAM)	Size	256 B 0019FFh to 001900h	256 B 0019FFh to 001900h
Bootloader (BSL) memory (ROM)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 000020h	4KB 000FFFh to 000020h
Tiny RAM	Size	22 B 000001Fh to 00000Ah	22 B 000001Fh to 00000Ah
Reserved	Size	10 B 000009h to 000000h	10 B 000009h to 000000h

(1) All address space not listed is considered vacant memory.

6.16.1 Peripheral File Map

For complete module register descriptions, see the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*. Table 6-48 lists the base and end addresses of the registers for each peripheral.

Table 6-48. Peripherals

MODULE NAME	BASE ADDRESS	END ADDRESS
Special Functions (see Table 6-49)	0100h	011Fh
PMM (see Table 6-50)	0120h	013Fh
FRAM Control (see Table 6-51)	0140h	014Fh
CRC (see Table 6-52)	0150h	0157h
RAM Control (see Table 6-53)	0158h	0159h
Watchdog (see Table 6-54)	015Ch	015Dh
CS (see Table 6-55)	0160h	016Fh
SYS (see Table 6-56)	0180h	019Fh
Shared Reference (see Table 6-57)	01B0h	01B1h
Digital I/O (see Table 6-58)	0200h	033Fh
TA0 (see Table 6-59)	0340h	036Fh
TA1 (see Table 6-60)	0380h	03AFh
TB0 (see Table 6-61)	03C0h	03EFh
TA2 (see Table 6-62)	0400h	042Fh
TA3 (see Table 6-63)	0440h	046Fh
RTC_C (see Table 6-64)	04A0h	04BFh
32-Bit Hardware Multiplier (see Table 6-65)	04C0h	04EFh
DMA (see Table 6-66)	0500h	056Fh
MPU Control (see Table 6-67)	05A0h	05AFh
eUSCI_A0 (see Table 6-68)	05C0h	05DFh
eUSCI_A1 (see Table 6-69)	05E0h	05FFh
eUSCI_A2 (see Table 6-70)	0600h	061Fh
eUSCI_A3 (see Table 6-71)	0620h	063Fh
eUSCI_B0 (see Table 6-72)	0640h	066Fh
eUSCI_B1 (see Table 6-73)	0680h	06AFh
TA4 (see Table 6-74)	07C0h	07EFh
ADC12_B (see Table 6-75)	0800h	089Fh
Comparator E (see Table 6-76)	08C0h	08CFh
CRC32 (see Table 6-77)	0980h	09AFh
AES256 (see Table 6-78)	09C0h	09CFh
LCD_C (see Table 6-79)	0A00h	0A5Fh
LEA (see Table 6-80)	0A80h	0AFFh
SAPH (1) (see Table 6-81)	0E00h	0E7Fh
SDHS (1) (see Table 6-82)	0E80h	0EBFh
UUPS (1) (see Table 6-83)	0EC0h	0EDFh
HSPLL (1) (see Table 6-84)	0EE0h	0EFFh
MTIF (see Table 6-85)	0F00h	0F1Fh

(1) Not available in MSP430FR6037, MSP430FR6035, and MSP430FR60371

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Table 6-49. Special Functions Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Enable	SFRIE1	0100h
Interrupt Flag	SFRIFG1	0102h
Reset Pin Control	SFRRPCR	0104h

Table 6-50. PMM Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
PMM Control 0	PMMCTL0	0120h
PMM Interrupt Flag	PMMIFG	012Ah
Power Mode 5 Control 0	PM5CTL0	0130h

Table 6-51. FRAM Control Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
FRAM Controller A Control 0	FRCTL0	0140h
General Control 0	GCCTL0	0144h
General Control 1	GCCTL1	0146h

Table 6-52. CRC Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
CRC Data In	CRCDI	0150h
CRC Data In Reverse Byte	CRCDIRB	0152h
CRC Initialization and Result	CRCINIRES	0154h
CRC Result Reverse	CRCRESR	0156h

Table 6-53. RAM Control Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
RAM Controller Control 0	RCCTL0	0158h
RAM Controller Control 1	RCCTL1	015Ah

Table 6-54. Watchdog Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Watchdog Timer Control	WDTCTL	015Ch

Table 6-55. CS Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Clock System Control 0	CSCTL0	0160h
Clock System Control 1	CSCTL1	0162h
Clock System Control 2	CSCTL2	0164h
Clock System Control 3	CSCTL3	0166h
Clock System Control 4	CSCTL4	0168h
Clock System Control 5	CSCTL5	016Ah
Clock System Control 6	CSCTL6	016Ch

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Table 6-56. SYS Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
System Control	SYSCTL	0180h
JTAG Mailbox Control	SYSJMBC	0186h
JTAG Mailbox Input	SYSJMBI0	0188h
JTAG Mailbox Input	SYSJMBI1	018Ah
JTAG Mailbox Output	SYSJMBO0	018Ch
JTAG Mailbox Output	SYSJMBO1	018Eh
User NMI Vector Generator	SYSUNIV	019Ah
System NMI Vector Generator	SYSSNIV	019Ch
Reset Vector Generator	SYSRSTIV	019Eh

Table 6-57. Shared Reference Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
REF Control 0	REFCTL0	01B0h

Table 6-58. Digital I/O Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Port A Input	PAIN	0200h
Port 1 Input	P1IN	0200h
Port 2 Input	P2IN	0201h
Port A Output	PAOUT	0202h
Port 1 Output	P1OUT	0202h
Port 2 Output	P2OUT	0203h
Port A Direction	PADIR	0204h
Port 1 Direction	P1DIR	0204h
Port 2 Direction	P2DIR	0205h
Port A Resistor Enable	PAREN	0206h
Port 1 Resistor Enable	P1REN	0206h
Port 2 Resistor Enable	P2REN	0207h
Port A Select 0	PASEL0	020Ah
Port 1 Select 0	P1SEL0	020Ah
Port 2 Select 0	P2SEL0	020Bh
Port A Select 1	PASEL1	020Ch
Port 1 Select 1	P1SEL1	020Ch
Port 2 Select 1	P2SEL1	020Dh
Port 1 Interrupt Vector	P1IV	020Eh
Port A Complement Select	PASELC	0216h
Port 1 Complement Select	P1SELC	0216h
Port 2 Complement Select	P2SELC	0217h
Port A Interrupt Edge Select	PAIES	0218h
Port 1 Interrupt Edge Select	P1IES	0218h
Port 2 Interrupt Edge Select	P2IES	0219h
Port A Interrupt Enable	PAIE	021Ah
Port 1 Interrupt Enable	P1IE	021Ah
Port 2 Interrupt Enable	P2IE	021Bh
Port A Interrupt Flag	PAIFG	021Ch
Port 1 Interrupt Flag	P1IFG	021Ch
Port 2 Interrupt Flag	P2IFG	021Dh

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Table 6-58. Digital I/O Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Port 2 Interrupt Vector	P2IV	021Eh
Port B Input	PBIN	0220h
Port 3 Input	P3IN	0220h
Port 4 Input	P4IN	0221h
Port B Output	PBOUT	0222h
Port 3 Output	P3OUT	0222h
Port 4 Output	P4OUT	0223h
Port B Direction	PBDIR	0224h
Port 3 Direction	P3DIR	0224h
Port 4 Direction	P4DIR	0225h
Port B Resistor Enable	PBREN	0226h
Port 3 Resistor Enable	P3REN	0226h
Port 4 Resistor Enable	P4REN	0227h
Port B Select 0	PBSEL0	022Ah
Port 3 Select 0	P3SEL0	022Ah
Port 4 Select 0	P4SEL0	022Bh
Port B Select 1	PBSEL1	022Ch
Port 3 Select 1	P3SEL1	022Ch
Port 4 Select 1	P4SEL1	022Dh
Port 3 Interrupt Vector	P3IV	022Eh
Port B Complement Select	PBSELC	0236h
Port 3 Complement Select	P3SELC	0236h
Port 4 Complement Select	P4SELC	0237h
Port B Interrupt Edge Select	PBIES	0238h
Port 3 Interrupt Edge Select	P3IES	0238h
Port 4 Interrupt Edge Select	P4IES	0239h
Port B Interrupt Enable	PBIE	023Ah
Port 3 Interrupt Enable	P3IE	023Ah
Port 4 Interrupt Enable	P4IE	023Bh
Port B Interrupt Flag	PBIFG	023Ch
Port 3 Interrupt Flag	P3IFG	023Ch
Port 4 Interrupt Flag	P4IFG	023Dh
Port 4 Interrupt Vector	P4IV	023Eh
Port C Input	PCIN	0240h
Port 5 Input	P5IN	0240h
Port 6 Input	P6IN	0241h
Port C Output	PCOUT	0242h
Port 5 Output	P5OUT	0242h
Port 6 Output	P6OUT	0243h
Port C Direction	PCDIR	0244h
Port 5 Direction	P5DIR	0244h
Port 6 Direction	P6DIR	0245h
Port C Resistor Enable	PCREN	0246h
Port 5 Resistor Enable	P5REN	0246h
Port 6 Resistor Enable	P6REN	0247h
Port C Select 0	PCSEL0	024Ah
Port 5 Select 0	P5SEL0	024Ah

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Table 6-58. Digital I/O Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Port 6 Select 0	P6SEL0	024Bh
Port C Select 1	PCSEL1	024Ch
Port 5 Select 1	P5SEL1	024Ch
Port 6 Select 1	P6SEL1	024Dh
Port 5 Interrupt Vector	P5IV	024Eh
Port C Complement Select	PCSELC	0256h
Port 5 Complement Select	P5SELC	0256h
Port 6 Complement Select	P6SELC	0257h
Port C Interrupt Edge Select	PCIES	0258h
Port 5 Interrupt Edge Select	P5IES	0258h
Port 6 Interrupt Edge Select	P6IES	0259h
Port C Interrupt Enable	PCIE	025Ah
Port 5 Interrupt Enable	P5IE	025Ah
Port 6 Interrupt Enable	P6IE	025Bh
Port C Interrupt Flag	PCIFG	025Ch
Port 5 Interrupt Flag	P5IFG	025Ch
Port 6 Interrupt Flag	P6IFG	025Dh
Port 6 Interrupt Vector	P6IV	025Eh
Port D Input	PDIN	0260h
Port 7 Input	P7IN	0260h
Port 8 Input	P8IN	0261h
Port D Output	PDOUT	0262h
Port 7 Output	P7OUT	0262h
Port 8 Output	P8OUT	0263h
Port D Direction	PDDIR	0264h
Port 7 Direction	P7DIR	0264h
Port 8 Direction	P8DIR	0265h
Port D Resistor Enable	PDREN	0266h
Port 7 Resistor Enable	P7REN	0266h
Port 8 Resistor Enable	P8REN	0267h
Port D Select 0	PDSEL0	026Ah
Port 7 Select 0	P7SEL0	026Ah
Port 8 Select 0	P8SEL0	026Bh
Port D Select 1	PDSEL1	026Ch
Port 7 Select 1	P7SEL1	026Ch
Port 8 Select 1	P8SEL1	026Dh
Port 7 Interrupt Vector	P7IV	026Eh
Port D Complement Select	PDSELC	0276h
Port 7 Complement Select	P7SELC	0276h
Port 8 Complement Select	P8SELC	0277h
Port D Interrupt Edge Select	PDIES	0278h
Port 7 Interrupt Edge Select	P7IES	0278h
Port 8 Interrupt Edge Select	P8IES	0279h
Port D Interrupt Enable	PDIE	027Ah
Port 7 Interrupt Enable	P7IE	027Ah
Port 8 Interrupt Enable	P8IE	027Bh
Port D Interrupt Flag	PDIFG	027Ch

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Table 6-58. Digital I/O Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Port 7 Interrupt Flag	P7IFG	027Ch
Port 8 Interrupt Flag	P8IFG	027Dh
Port 8 Interrupt Vector	P8IV	027Eh
Port E Input	PEIN	0280h
Port 9 Input	P9IN	0280h
Port E Output	PEOUT	0282h
Port 9 Output	P9OUT	0282h
Port E Direction	PEDIR	0284h
Port 9 Direction	P9DIR	0284h
Port E Resistor Enable	PEREN	0286h
Port 9 Resistor Enable	P9REN	0286h
Port E Select 0	PESEL0	028Ah
Port 9 Select 0	P9SEL0	028Ah
Port E Select 1	PESEL1	028Ch
Port 9 Select 1	P9SEL1	028Ch
Port 9 Interrupt Vector	P9IV	028Eh
Port E Complement Select	PESELC	0296h
Port 9 Complement Select	P9SELC	0296h
Port E Interrupt Edge Select	PEIES	0298h
Port 9 Interrupt Edge Select	P9IES	0298h
Port E Interrupt Enable	PEIE	029Ah
Port 9 Interrupt Enable	P9IE	029Ah
Port E Interrupt Flag	PEIFG	029Ch
Port 9 Interrupt Flag	P9IFG	029Ch
Port J Input	PJIN	0320h
Port J Output	PJOUT	0322h
Port J Direction	PJDIR	0324h
Port J Resistor Enable	PJREN	0326h
Port J Select 0	PJSEL0	032Ah
Port J Select 1	PJSEL1	032Ch
Port J Complement Select	PJSELC	0336h

Table 6-59. TA0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A0 Control	TA0CTL	0340h
Timer_A0 Capture/Compare Control	TA0CCTL0	0342h
Timer_A0 Capture/Compare Control	TA0CCTL1	0344h
Timer_A0 Capture/Compare Control	TA0CCTL2	0346h
Timer_A0 Counter	TA0R	0350h
Timer_A0 Capture/Compare	TA0CCR0	0352h
Timer_A0 Capture/Compare	TA0CCR1	0354h
Timer_A0 Capture/Compare	TA0CCR2	0356h
Timer_A0 Expansion 0	TA0EX0	0360h
Timer_A0 Interrupt Vector	TA0IV	036Eh

Table 6-60. TA1 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A1 Control	TA1CTL	0380h
Timer_A1 Capture/Compare Control	TA1CCTL0	0382h
Timer_A1 Capture/Compare Control	TA1CCTL1	0384h
Timer_A1 Capture/Compare Control	TA1CCTL2	0386h
Timer_A1 Counter	TA1R	0390h
Timer_A1 Capture/Compare	TA1CCR0	0392h
Timer_A1 Capture/Compare	TA1CCR1	0394h
Timer_A1 Capture/Compare	TA1CCR2	0396h
Timer_A1 Expansion 0	TA1EX0	03A0h
Timer_A1 Interrupt Vector	TA1IV	03AEh

Table 6-61. TB0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_B0 Control	TB0CTL	03C0h
Timer_B0 Capture/Compare Control	TB0CCTL0	03C2h
Timer_B0 Capture/Compare Control	TB0CCTL1	03C4h
Timer_B0 Capture/Compare Control	TB0CCTL2	03C6h
Timer_B0 Capture/Compare Control	TB0CCTL3	03C8h
Timer_B0 Capture/Compare Control	TB0CCTL4	03CAh
Timer_B0 Capture/Compare Control	TB0CCTL5	03CCh
Timer_B0 Capture/Compare Control	TB0CCTL6	03CEh
Timer_B0 Counter	TB0R	03D0h
Timer_B0 Capture/Compare	TB0CCR0	03D2h
Timer_B0 Capture/Compare	TB0CCR1	03D4h
Timer_B0 Capture/Compare	TB0CCR2	03D6h
Timer_B0 Capture/Compare	TB0CCR3	03D8h
Timer_B0 Capture/Compare	TB0CCR4	03DAh
Timer_B0 Capture/Compare	TB0CCR5	03DCh
Timer_B0 Capture/Compare	TB0CCR6	03DEh
Timer_B0 Expansion 0	TB0EX0	03E0h
Timer_B0 Interrupt Vector	TB0IV	03EEh

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Table 6-62. TA2 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A2 Control	TA2CTL	0400h
Timer_A2 Capture/Compare Control	TA2CCTL0	0402h
Timer_A2 Capture/Compare Control	TA2CCTL1	0404h
Timer_A2 Counter	TA2R	0410h
Timer_A2 Capture/Compare	TA2CCR0	0412h
Timer_A2 Capture/Compare	TA2CCR1	0414h
Timer_A2 Expansion 0	TA2EX0	0420h
Timer_A2 Interrupt Vector	TA2IV	042Eh

Table 6-63. TA3 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A3 Control	TA3CTL	0440h
Timer_A3 Capture/Compare Control	TA3CCTL0	0442h
Timer_A3 Capture/Compare Control	TA3CCTL1	0444h
Timer_A3 Counter	TA3R	0450h
Timer_A3 Capture/Compare	TA3CCR0	0452h
Timer_A3 Capture/Compare	TA3CCR1	0454h
Timer_A3 Expansion 0	TA3EX0	0460h
Timer_A3 Interrupt Vector	TA3IV	046Eh

Table 6-64. RTC_C Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Real-Time Clock Control 0	RTCCTL0	04A0h
Real-Time Clock Control 1, 3	RTCCTL13	04A2h
Real-Time Clock Offset Calibration	RTCOCAL	04A4h
Real-Time Clock Temperature Compensation	RTCTCMP	04A6h
Real-Time Clock Prescale Timer 0 Control	RTCPS0CTL	04A8h
Real-Time Clock Prescale Timer 1 Control	RTCPS1CTL	04AAh
Real-Time Clock Prescale Timer Counter	RTCPS	04ACh
Prescale Timer 0 Counter Value	RT0PS	04ACh
Prescale Timer 1 Counter Value	RT1PS	04ADh
Real-Time Clock Interrupt Vector	RTCIV	04AEh
Real-Time Clock Seconds and Minutes	RTCTIM0	04B0h
Real-Time Clock Hour, Day of Week	RTCTIM1	04B2h
Real-Time Clock Date	RTCDATE	04B4h
Real-Time Clock Year	RTCYEAR	04B6h
Real-Time Clock Minute and Hour	RTCAMINHR	04B8h
Real-Time Clock Alarm Day of Week and Day	RTCADOWDAY	04BAh
Binary-to-BCD Conversion	BIN2BCD	04BCh
BCD-to-Binary Conversion	BCD2BIN	04BEh

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Table 6-65. 32-Bit Hardware Multiplier Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
16-bit operand one – multiply	MPY	04C0h
16-bit operand one – signed multiply	MPYS	04C2h
16-bit operand one – multiply accumulate	MAC	04C4h
16-bit operand one – signed multiply accumulate	MACS	04C6h
16-bit operand two	OP2	04C8h
16x16-bit result low word	RESLO	04CAh
16x16-bit result high word	RESHI	04CCh
16x16-bit sum extension	SUMEXT	04CEh
32-bit operand 1 – multiply – low word	MPY32L	04D0h
32-bit operand 1 – multiply – high word	MPY32H	04D2h
32-bit operand 1 – signed multiply – low word	MPYS32L	04D4h
32-bit operand 1 – signed multiply – high word	MPYS32H	04D6h
32-bit operand 1 – multiply accumulate – low word	MAC32L	04D8h
32-bit operand 1 – multiply accumulate – high word	MAC32H	04DAh
32-bit operand 1 – signed multiply accumulate – low word	MACS32L	04DCh
32-bit operand 1 – signed multiply accumulate – high word	MACS32H	04DEh
32-bit operand 2 – low word	OP2L	04E0h
32-bit operand 2 – high word	OP2H	04E2h
32x32-bit result 0 – least significant word	RES0	04E4h
32x32-bit result 1	RES1	04E6h
32x32-bit result 2	RES2	04E8h
32x32-bit result 3 – most significant word	RES3	04EAh
MPY32 control 0	MPY32CTL0	04ECh

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Table 6-66. DMA Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
DMA Control 0	DMACTL0	0500h
DMA Control 1	DMACTL1	0502h
DMA Control 2	DMACTL2	0504h
DMA Control 4	DMACTL4	0508h
DMA Interrupt Vector	DMAIV	050Eh
DMA Channel 0 Control	DMA0CTL	0510h
DMA Channel 0 Source Address	DMA0SA	0512h
DMA Channel 0 Destination Address	DMA0DA	0516h
DMA Channel 0 Transfer Size	DMA0SZ	051Ah
DMA Channel 1 Control	DMA1CTL	0520h
DMA Channel 1 Source Address	DMA1SA	0522h
DMA Channel 1 Destination Address	DMA1DA	0526h
DMA Channel 1 Transfer Size	DMA1SZ	052Ah
DMA Channel 2 Control	DMA2CTL	0530h
DMA Channel 2 Source Address	DMA2SA	0532h
DMA Channel 2 Destination Address	DMA2DA	0536h
DMA Channel 2 Transfer Size	DMA2SZ	053Ah
DMA Channel 3 Control	DMA3CTL	0540h
DMA Channel 3 Source Address	DMA3SA	0542h
DMA Channel 3 Destination Address	DMA3DA	0546h
DMA Channel 3 Transfer Size	DMA3SZ	054Ah
DMA Channel 4 Control	DMA4CTL	0550h
DMA Channel 4 Source Address	DMA4SA	0552h
DMA Channel 4 Destination Address	DMA4DA	0556h
DMA Channel 4 Transfer Size	DMA4SZ	055Ah
DMA Channel 5 Control	DMA5CTL	0560h
DMA Channel 5 Source Address	DMA5SA	0562h
DMA Channel 5 Destination Address	DMA5DA	0566h
DMA Channel 5 Transfer Size	DMA5SZ	056Ah

Table 6-67. MPU Control Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Memory Protection Unit Control 0	MPUCTL0	05A0h
Memory Protection Unit Control 1	MPUCTL1	05A2h
Memory Protection Unit Segmentation Border 2 Register	MPUSEGB2	05A4h
Memory Protection Unit Segmentation Border 1 Register	MPUSEGB1	05A6h
Memory Protection Unit Segmentation Access Management Register	MPUSAM	05A8h
Memory Protection Unit IP Control 0 Register	MPUIPC0	05AAh
Memory Protection Unit IP Encapsulation Segment Border 2 Register	MPUIPSEGB2	05ACh
Memory Protection Unit IP Encapsulation Segment Border 1 Register	MPUIPSEGB1	05AEh

Table 6-68. eUSCI_A0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A0 Control Word Register 0	UCA0CTLW0	05C0h
eUSCI_A0 Control Word Register 1	UCA0CTLW1	05C2h
eUSCI_A0 Baud Rate Control Word	UCA0BRW	05C6h
eUSCI_A0 Modulation Control Word	UCA0MCTLW	05C8h
eUSCI_A0 Status Register	UCA0STATW	05CAh
eUSCI_A0 Receive Buffer	UCA0RXBUF	05CCh
eUSCI_A0 Transmit Buffer	UCA0TXBUF	05CEh
eUSCI_A0 Auto Baud Rate Control	UCA0ABCTL	05D0h
eUSCI_A0 IrDA Control Word	UCA0IRCTL	05D2h
eUSCI_A0 Interrupt Enable	UCA0IE	05DAh
eUSCI_A0 Interrupt Flag	UCA0IFG	05DCh
eUSCI_A0 Interrupt Vector	UCA0IV	05DEh

Table 6-69. eUSCI_A1 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A1 Control Word Register 0	UCA1CTLW0	05E0h
eUSCI_A1 Control Word Register 1	UCA1CTLW1	05E2h
eUSCI_A1 Baud Rate Control Word	UCA1BRW	05E6h
eUSCI_A1 Modulation Control Word	UCA1MCTLW	05E8h
eUSCI_A1 Status Register	UCA1STATW	05EAh
eUSCI_A1 Receive Buffer	UCA1RXBUF	05ECh
eUSCI_A1 Transmit Buffer	UCA1TXBUF	05EEh
eUSCI_A1 Auto Baud Rate Control	UCA1ABCTL	05F0h
eUSCI_A1 IrDA Control Word	UCA1IRCTL	05F2h
eUSCI_A1 Interrupt Enable	UCA1IE	05FAh
eUSCI_A1 Interrupt Flag	UCA1IFG	05FCh
eUSCI_A1 Interrupt Vector	UCA1IV	05FEh

Table 6-70. eUSCI_A2 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A2 Control Word Register 0	UCA2CTLW0	0600h
eUSCI_A2 Control Word Register 1	UCA2CTLW1	0602h
eUSCI_A2 Baud Rate Control Word	UCA2BRW	0606h
eUSCI_A2 Modulation Control Word	UCA2MCTLW	0608h
eUSCI_A2 Status Register	UCA2STATW	060Ah
eUSCI_A2 Receive Buffer	UCA2RXBUF	060Ch
eUSCI_A2 Transmit Buffer	UCA2TXBUF	060Eh
eUSCI_A2 Auto Baud Rate Control	UCA2ABCTL	0610h
eUSCI_A2 IrDA Control Word	UCA2IRCTL	0612h
eUSCI_A2 Interrupt Enable	UCA2IE	061Ah
eUSCI_A2 Interrupt Flag	UCA2IFG	061Ch
eUSCI_A2 Interrupt Vector	UCA2IV	061Eh

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Table 6-71. eUSCI_A3 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_A3 Control Word Register 0	UCA3CTLW0	0620h
eUSCI_A3 Control Word Register 1	UCA3CTLW1	0622h
eUSCI_A3 Baud Rate Control Word	UCA3BRW	0626h
eUSCI_A3 Modulation Control Word	UCA3MCTLW	0628h
eUSCI_A3 Status Register	UCA3STATW	062Ah
eUSCI_A3 Receive Buffer	UCA3RXBUF	062Ch
eUSCI_A3 Transmit Buffer	UCA3TXBUF	062Eh
eUSCI_A3 Auto Baud Rate Control	UCA3ABCTL	0630h
eUSCI_A3 IrDA Control Word	UCA3IRCTL	0632h
eUSCI_A3 Interrupt Enable	UCA3IE	063Ah
eUSCI_A3 Interrupt Flag	UCA3IFG	063Ch
eUSCI_A3 Interrupt Vector	UCA3IV	063Eh

Table 6-72. eUSCI_B0 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_B0 Control Word Register 0	UCB0CTLW0	0640h
eUSCI_B0 Control Word Register 1	UCB0CTLW1	0642h
eUSCI_B0 Baud Rate Control Word	UCB0BRW	0646h
eUSCI_B0 Status Register	UCB0STATW	0648h
eUSCI_B0 Byte Counter Threshold	UCB0TBCNT	064Ah
eUSCI_B0 Receive Buffer	UCB0RXBUF	064Ch
eUSCI_B0 Transmit Buffer	UCB0TXBUF	064Eh
eUSCI_B0 I2C Own Address 0	UCB0I2COA0	0654h
eUSCI_B0 I2C Own Address 1	UCB0I2COA1	0656h
eUSCI_B0 I2C Own Address 2	UCB0I2COA2	0658h
eUSCI_B0 I2C Own Address 3	UCB0I2COA3	065Ah
eUSCI_B0 I2C Received Address	UCB0ADDRX	065Ch
eUSCI_B0 I2C Address Mask	UCB0ADDMASK	065Eh
eUSCI_B0 I2C Slave Address	UCB0I2CSA	0660h
eUSCI_B0 Interrupt Enable	UCB0IE	066Ah
eUSCI_B0 Interrupt Flag	UCB0IFG	066Ch
eUSCI_B0 Interrupt Vector	UCB0IV	066Eh

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Table 6-73. eUSCI_B1 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
eUSCI_B1 Control Word Register 0	UCB1CTLW0	0680h
eUSCI_B1 Control Word Register 1	UCB1CTLW1	0682h
eUSCI_B1 Baud Rate Control Word	UCB1BRW	0686h
eUSCI_B1 Status Register	UCB1STATW	0688h
eUSCI_B1 Byte Counter Threshold	UCB1TBCNT	068Ah
eUSCI_B1 Receive Buffer	UCB1RXBUF	068Ch
eUSCI_B1 Transmit Buffer	UCB1TXBUF	068Eh
eUSCI_B1 I2C Own Address 0	UCB1I2COA0	0694h
eUSCI_B1 I2C Own Address 1	UCB1I2COA1	0696h
eUSCI_B1 I2C Own Address 2	UCB1I2COA2	0698h
eUSCI_B1 I2C Own Address 3	UCB1I2COA3	069Ah
eUSCI_B1 I2C Received Address	UCB1ADDRX	069Ch
eUSCI_B1 I2C Address Mask	UCB1ADDMASK	069Eh
eUSCI_B1 I2C Slave Address	UCB1I2CSA	06A0h
eUSCI_B1 Interrupt Enable	UCB1IE	06AAh
eUSCI_B1 Interrupt Flag	UCB1IFG	06ACh
eUSCI_B1 Interrupt Vector	UCB1IV	06AEh

Table 6-74. TA4 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Timer_A4 Control	TA4CTL	07C0h
Timer_A4 Capture/Compare Control	TA4CCTL0	07C2h
Timer_A4 Capture/Compare Control	TA4CCTL1	07C4h
Timer_A4 Counter	TA4R	07D0h
Timer_A4 Capture/Compare	TA4CCR0	07D2h
Timer_A4 Capture/Compare	TA4CCR1	07D4h
Timer_A4 Expansion 0	TA4EX0	07E0h
Timer_A4 Interrupt Vector	TA4IV	07EEh

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Table 6-75. ADC12_B Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
ADC12_B Control 0	ADC12CTL0	0800h
ADC12_B Control 1	ADC12CTL1	0802h
ADC12_B Control 2	ADC12CTL2	0804h
ADC12_B Control 3	ADC12CTL3	0806h
ADC12_B Window Comparator Low Threshold Register	ADC12LO	0808h
ADC12_B Window Comparator High Threshold Register	ADC12HI	080Ah
ADC12_B Interrupt Flag 0	ADC12IFGR0	080Ch
ADC12_B Interrupt Flag 1	ADC12IFGR1	080Eh
ADC12_B Interrupt Flag 2	ADC12IFGR2	0810h
ADC12_B Interrupt Enable 0	ADC12IER0	0812h
ADC12_B Interrupt Enable 1	ADC12IER1	0814h
ADC12_B Interrupt Enable 2	ADC12IER2	0816h
ADC12_B Interrupt Vector	ADC12IV	0818h
ADC12_B Memory Control 0	ADC12MCTL0	0820h
ADC12_B Memory Control 1	ADC12MCTL1	0822h
ADC12_B Memory Control 2	ADC12MCTL2	0824h
ADC12_B Memory Control 3	ADC12MCTL3	0826h
ADC12_B Memory Control 4	ADC12MCTL4	0828h
ADC12_B Memory Control 5	ADC12MCTL5	082Ah
ADC12_B Memory Control 6	ADC12MCTL6	082Ch
ADC12_B Memory Control 7	ADC12MCTL7	082Eh
ADC12_B Memory Control 8	ADC12MCTL8	0830h
ADC12_B Memory Control 9	ADC12MCTL9	0832h
ADC12_B Memory Control 10	ADC12MCTL10	0834h
ADC12_B Memory Control 11	ADC12MCTL11	0836h
ADC12_B Memory Control 12	ADC12MCTL12	0838h
ADC12_B Memory Control 13	ADC12MCTL13	083Ah
ADC12_B Memory Control 14	ADC12MCTL14	083Ch
ADC12_B Memory Control 15	ADC12MCTL15	083Eh
ADC12_B Memory Control 16	ADC12MCTL16	0840h
ADC12_B Memory Control 17	ADC12MCTL17	0842h
ADC12_B Memory Control 18	ADC12MCTL18	0844h
ADC12_B Memory Control 19	ADC12MCTL19	0846h
ADC12_B Memory Control 20	ADC12MCTL20	0848h
ADC12_B Memory Control 21	ADC12MCTL21	084Ah
ADC12_B Memory Control 22	ADC12MCTL22	084Ch
ADC12_B Memory Control 23	ADC12MCTL23	084Eh
ADC12_B Memory Control 24	ADC12MCTL24	0850h
ADC12_B Memory Control 25	ADC12MCTL25	0852h
ADC12_B Memory Control 26	ADC12MCTL26	0854h
ADC12_B Memory Control 27	ADC12MCTL27	0856h
ADC12_B Memory Control 28	ADC12MCTL28	0858h
ADC12_B Memory Control 29	ADC12MCTL29	085Ah
ADC12_B Memory Control 30	ADC12MCTL30	085Ch
ADC12_B Memory Control 31	ADC12MCTL31	085Eh
ADC12_B Memory 0	ADC12MEM0	0860h
ADC12_B Memory 1	ADC12MEM1	0862h

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Table 6-75. ADC12_B Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
ADC12_B Memory 2	ADC12MEM2	0864h
ADC12_B Memory 3	ADC12MEM3	0866h
ADC12_B Memory 4	ADC12MEM4	0868h
ADC12_B Memory 5	ADC12MEM5	086Ah
ADC12_B Memory 6	ADC12MEM6	086Ch
ADC12_B Memory 7	ADC12MEM7	086Eh
ADC12_B Memory 8	ADC12MEM8	0870h
ADC12_B Memory 9	ADC12MEM9	0872h
ADC12_B Memory 10	ADC12MEM10	0874h
ADC12_B Memory 11	ADC12MEM11	0876h
ADC12_B Memory 12	ADC12MEM12	0878h
ADC12_B Memory 13	ADC12MEM13	087Ah
ADC12_B Memory 14	ADC12MEM14	087Ch
ADC12_B Memory 15	ADC12MEM15	087Eh
ADC12_B Memory 16	ADC12MEM16	0880h
ADC12_B Memory 17	ADC12MEM17	0882h
ADC12_B Memory 18	ADC12MEM18	0884h
ADC12_B Memory 19	ADC12MEM19	0886h
ADC12_B Memory 20	ADC12MEM20	0888h
ADC12_B Memory 21	ADC12MEM21	088Ah
ADC12_B Memory 22	ADC12MEM22	088Ch
ADC12_B Memory 23	ADC12MEM23	088Eh
ADC12_B Memory 24	ADC12MEM24	0890h
ADC12_B Memory 25	ADC12MEM25	0892h
ADC12_B Memory 26	ADC12MEM26	0894h
ADC12_B Memory 27	ADC12MEM27	0896h
ADC12_B Memory 28	ADC12MEM28	0898h
ADC12_B Memory 29	ADC12MEM29	089Ah
ADC12_B Memory 30	ADC12MEM30	089Ch
ADC12_B Memory 31	ADC12MEM31	089Eh

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Table 6-76. Comparator_E Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Comparator Control Register 0	CECTL0	08C0h
Comparator Control Register 1	CECTL1	08C2h
Comparator Control Register 2	CECTL2	08C4h
Comparator Control Register 3	CECTL3	08C6h
Comparator Interrupt Control	CEINT	08CCh
Comparator Interrupt Vector Word	CEIV	08CEh

Table 6-77. CRC32 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
CRC32 Data Input Word 0	CRC32DIW0	0980h
CRC32 Data Input Word 1	CRC32DIW1	0982h
CRC32 Data In Reverse Word 1	CRC32DIRBW1	0984h
CRC32 Data In Reverse Word 0	CRC32DIRBW0	0986h
CRC32 Initialization and Result Word 0	CRC32INIRESW0	0988h
CRC32 Initialization and Result Word 1	CRC32INIRESW1	098Ah
CRC32 Result Reverse Word 1	CRC32RESRW1	098Ch
CRC32 Result Reverse Word 0	CRC32RESRW0	098Eh
CRC16 Data Input	CRC16DIW0	0990h
CRC16 Data In Reverse	CRC16DIRBW0	0996h
CRC16 Init and Result	CRC16INIRESW0	0998h
CRC16 Result Reverse	CRC16RESRW0	099Eh

Table 6-78. AES256 Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
AES Accelerator Control 0	AESACTL0	09C0h
AES Accelerator Control 1	AESACTL1	09C2h
AES Accelerator Status	AESASTAT	09C4h
AES Accelerator Key	AESAKEY	09C6h
AES Accelerator Data In	AESADIN	09C8h
AES Accelerator Data Out	AESADOUT	09CAh
AES Accelerator XORed Data In	AESAXDIN	09CCh
AES Accelerator XORed Data In	AESAXIN	09CEh

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Table 6-79. LCD_C Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
LCD_C control 0	LCDCCTL0	0A00h
LCD_C control 1	LCDCCTL1	0A02h
LCD_C blinking control	LCDCBLKCTL	0A04h
LCD_C memory control	LCDCMEMCTL	0A06h
LCD_C Voltage Control	LCDCVCTL	0A08h
LCD_C port control 0	LCDCPCTL0	0A0Ah
LCD_C port control 1	LCDCPCTL1	0A0Ch
LCD_C port control 2 (≥256 segments)	LCDCPCTL2	0A0Eh
LCD_C port control 3 (384 segments)	LCDCPCTL3	0A10h
LCD_C charge pump control	LCDCCPCTL	0A12h
LCD_C interrupt vector	LCDCIV	0A1Eh
LCDMX = 0 ... 4		
LCD memory 1	LCDM1	0A20h
LCD memory 2	LCDM2	0A21h
LCD memory 3	LCDM3	0A22h
LCD memory 4	LCDM4	0A23h
LCD memory 5	LCDM5	0A24h
LCD memory 6	LCDM6	0A25h
LCD memory 7	LCDM7	0A26h
LCD memory 8	LCDM8	0A27h
LCD memory 9	LCDM9	0A28h
LCD memory 10	LCDM10	0A29h
LCD memory 11	LCDM11	0A2Ah
LCD memory 12	LCDM12	0A2Bh
LCD memory 13	LCDM13	0A2Ch
LCD memory 14	LCDM14	0A2Dh
LCD memory 15	LCDM15	0A2Eh
LCD memory 16	LCDM16	0A2Fh
LCD memory 17	LCDM17	0A30h
LCD memory 18	LCDM18	0A31h
LCD memory 19	LCDM19	0A32h
LCD memory 20	LCDM20	0A33h
LCD blinking memory 1	LCDM33_LCDBM1	0A40h
LCD blinking memory 2	LCDM34_LCDBM2	0A41h
LCD blinking memory 3	LCDM35_LCDBM3	0A42h
LCD blinking memory 4	LCDM36_LCDBM4	0A43h
LCD blinking memory 5	LCDM37_LCDBM5	0A44h
LCD blinking memory 6	LCDM38_LCDBM6	0A45h
LCD blinking memory 7	LCDM39_LCDBM7	0A46h
LCD blinking memory 8	LCDM40_LCDBM8	0A47h
LCD blinking memory 9	LCDM41_LCDBM9	0A48h
LCD blinking memory 10	LCDM42_LCDBM10	0A49h
LCD blinking memory 11	LCDM43_LCDBM11	0A4Ah
LCD blinking memory 11	LCDM44_LCDBM12	0A4Bh
LCD blinking memory 13	LCDM45_LCDBM13	0A4Ch
LCD blinking memory 14	LCDM46_LCDBM14	0A4Dh
LCD blinking memory 15	LCDM47_LCDBM15	0A4Eh

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Table 6-79. LCD_C Registers (continued)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
LCD blinking memory 16	LCDM48_LCDBM16	0A4Fh
LCD blinking memory 17	LCDM49_LCDBM17	0A50h
LCD blinking memory 18	LCDM50_LCDBM18	0A51h
LCD blinking memory 19	LCDM51_LCDBM19	0A52h
LCD blinking memory 20	LCDM52_LCDBM20	0A53h
LCDMX = 5 ... 8		
LCD memory 1	LCDM1	0A20h
LCD memory 2	LCDM2	0A21h
LCD memory 3	LCDM3	0A22h
LCD memory 4	LCDM4	0A23h
LCD memory 5	LCDM5	0A24h
LCD memory 6	LCDM6	0A25h
LCD memory 7	LCDM7	0A26h
LCD memory 8	LCDM8	0A27h
LCD memory 9	LCDM9	0A28h
LCD memory 10	LCDM10	0A29h
LCD memory 11	LCDM11	0A2Ah
LCD memory 12	LCDM12	0A2Bh
LCD memory 13	LCDM13	0A2Ch
LCD memory 14	LCDM14	0A2Dh
LCD memory 15	LCDM15	0A2Eh
LCD memory 16	LCDM16	0A2Fh
LCD memory 17	LCDM17	0A30h
LCD memory 18	LCDM18	0A31h
LCD memory 19	LCDM19	0A32h
LCD memory 20	LCDM20	0A33h
LCD memory 21	LCDM21	0A34h
LCD memory 22	LCDM22	0A35h
LCD memory 23	LCDM23	0A36h
LCD memory 24	LCDM24	0A37h
LCD memory 25	LCDM25	0A38h
LCD memory 26	LCDM26	0A39h
LCD memory 27	LCDM27	0A3Ah
LCD memory 28	LCDM28	0A3Bh
LCD memory 29	LCDM29	0A3Ch
LCD memory 30	LCDM30	0A3Dh
LCD memory 31	LCDM31	0A3Eh
LCD memory 32	LCDM32	0A3Fh
LCD memory 33	LCDM33_LCDBM1	0A40h
LCD memory 34	LCDM34_LCDBM2	0A41h
LCD memory 35	LCDM35_LCDBM3	0A42h
LCD memory 36	LCDM36_LCDBM4	0A43h

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Table 6-80. LEA Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
LEA Capability Register	LEACAP	0A80h
Configuration Register 0	LEACNF0	0A84h
Configuration Register 1	LEACNF1	0A88h
Configuration Register 2	LEACNF2	0A8Ch
Memory Bottom Register	LEAMB	0A90h
Memory Top Register	LEAMT	0A94h
Code Memory Access	LEACMA	0A98h
Code Memory Control	LEACMCTL	0A9Ch
LEA Command Status	LEACMDSTAT	0AA8h
LEA Source 1 Status	LEAS1STAT	0AACh
LEA Source 0 Status	LEAS0STAT	0AB0h
LEA Result Status	LEADSTSTAT	0AB4h
PM Control Register	LEAPMCTL	0AC0h
PM Result Register	LEAPMDST	0AC4h
PM Source 1 Register	LEAPMS1	0AC8h
PM Source 0 Register	LEAPMS0	0ACCh
PM Command Buffer	LEAPMCB	0AD0h
Interrupt Flag and Set	LEAIFGSET	0AF0h
Interrupt Enable	LEAIE	0AF4h
Interrupt Flag and Clear	LEAIFG	0AF8h
Interrupt Vector	LEAIV	0AFCh

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Table 6-81. SAPH Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index	SAPHIIDX	0E00h
Masked Interrupt Satus	SAPHMIS	0E02h
Raw Interrupt Status	SAPHRIS	0E04h
Interrupt Mask	SAPHIMSC	0E06h
Interrupt Clear	SAPHICR	0E08h
Interrupt Set	SAPHISR	0E0Ah
Module-Descriptor Low Word	SAPHDESCLO	0E0Ch
Module-Descriptor High Word	SAPHDESCHI	0E0Eh
Key	SAPHKEY	0E10h
Physical Interface Output Control #0	SAPHOCTL0	0E12h
Physical Interface Output Control #1	SAPHOCTL1	0E14h
Physical Interface Output Function Select	SAPHOSEL	0E16h
Channel 0 Pull UpTrim	SAPHCH0PUT	0E20h
Channel 0 Pull DownTrim	SAPHCH0PDT	0E22h
Channel 0 Termination Trim	SAPHCH0TT	0E24h
Channel 1 Pull UpTrim	SAPHCH1PUT	0E26h
Channel 1 Pull DownTrim	SAPHCH1PDT	0E28h
Channel 1 Termination Trim	SAPHCH1TT	0E2Ah
Mode Configuration Register	SAPHMCNF	0E2Ch
Trim Access Control	SAPHTACTL	0E2Eh
Physical Interface Input Control #0	SAPHICTL0	0E30h
Bias Control	SAPHBCTL	0E34h
PPG Count	SAPHPGC	0E40h
Pulse Generator Low Period	SAPHPGLPER	0E42h
Pulse Generator High Period	SAPHPGHPER	0E44h
PPG Control	SAPHPGCTL	0E46h
PPG Software Trigger	SAPHPPGTRIG	0E48h
A-SEQ control 0	SAPHASCTL0	0E60h
A-SEQ control 1	SAPHASCTL1	0E62h
ASQ Software Trigger	SAPHASQTRIG	0E64h
ASQ ping output polarity	SAPHAPOL	0E66h
ASQ ping pause level	SAPHAPLEV	0E68h
ASQ ping pause impedance	SAPHAPHIZ	0E6Ah
A-SEQ start to 1st ping	SAPHATM_A	0E6Eh
ASQ start to ADC arm	SAPHATM_B	0E70h
Count for the TIMEMARK C Event	SAPHATM_C	0E72h
ASQ start to ADC trig	SAPHATM_D	0E74h
ASQ start to restart	SAPHATM_E	0E76h
ASQ start to time-out	SAPHATM_F	0E78h
Time Base Control	SAPHTBCTL	0E7Ah
Acquisition Timer Low Part	SAPHATIMLO	0E7Ch
Acquisition Timer High Part	SAPHATIMHI	0E7Eh

Table 6-82. SDHS Registers(1)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index Register	SDHSIIDX	0E80h
Masked Interrupt Status and Clear Register	SDHSMIS	0E82h
Raw Interrupt Status	SDHSRIS	0E84h
Interrupt Mask Register	SDHSIMSC	0E86h
Interrupt Clear	SDHSICR	0E88h
Interrupt Set Register	SDHSISR	0E8Ah
SDHS Descriptor Register L	SDHSDESCLO	0E8Ch
SDHS Descriptor Register H	SDHSDESCHI	0E8Eh
SDHS Control Register 0	SDHSCTL0	0E90h
SDHS Control Register 1	SDHSCTL1	0E92h
SDHS Control Register 2	SDHSCTL2	0E94h
SDHS Control Register 3	SDHSCTL3	0E96h
SDHS Control Register 4	SDHSCTL4	0E98h
SDHS Control Register 5	SDHSCTL5	0E9Ah
SDHS Control Register 6	SDHSCTL6	0E9Ch
SDHS Control Register 7	SDHSCTL7	0E9Eh
SDHS Data Converstion Register	SDHSDT	0EA2h
SDHS Window Comparator High Threshold Register	SDHSWINHITH	0EA4h
SDHS Window Comparator Low Threshold Register	SDHSWINLOTH	0EA6h
DTC destination address	SDHSDTCDA	0EA8h

(1) Not available in MSP430FR6037, MSP430FR6035, and MSP430FR60371

Table 6-83. UUPS Registers(1)

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index Register	UUPSIIDX	0EC0h
Masked Interrupt Status	UUPSMIS	0EC2h
Raw Interrupt Status	UUPSRIS	0EC4h
Interrupt Mask Register	UUPSIMSC	0EC6h
Interrupt Clear	UUPSICR	0EC8h
Interrupt Flag Set	UUPSISR	0ECAh
UUPS Descriptor Register L	UUPSDESCLO	0ECCh
UUPS Descriptor Register H	UUPSDESCHI	0ECEh
UUPS Control	UUPSCTL	0ED0h

(1) Not available in MSP430FR6037, MSP430FR6035, and MSP430FR60371

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Table 6-84. HSPLL Registers[(1)]

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Interrupt Index Register	HSPLLIIDX	0EE0h
Masked Interrupt Status	HSPLLMIS	0EE2h
Raw Interrupt Status	HSPLLRIS	0EE4h
Interrupt Mask Register	HSPLLIMSC	0EE6h
Interrupt Flag Clear	HSPLLICR	0EE8h
Interrupt Flag Set	HSPLLISR	0EEAh
HSPLL Descriptor Register L	HSPLLDESCLO	0EECh
HSPLL Descriptor Register H	HSPLLDESCHI	0EEEh
HSPLL Control Register	HSPLLCTL	0EF0h
USSXT Control Register	HSPLLUSSXTLCTL	0EF2h

(1) Not available in MSP430FR6037, MSP430FR6035, and MSP430FR60371

Table 6-85. MTIF Registers

REGISTER DESCRIPTION	ACRONYM	ADDRESS
Pulse Generator Configuration	MTIFPGCNF	0F00h
Pulse Generator Value	MTIFPGKVAL	0F02h
Pulse Generator Control	MTIFPGCTL	0F04h
Pulse Generator Status	MTIFPGSR	0F06h
Pulse Counter Configuration	MTIFPCCNF	0F08h
Pulse Counter Value	MTIFPCR	0F0Ah
Pulse Counter Control	MTIFPCCTL	0F0Ch
Pulse Counter Status	MTIFPCSR	0F0Eh
Measurement Test Port Control	MTIFTPCTL	0F10h

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6.17 Identification

6.17.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in the Device Descriptor structure (see 6.15).

6.17.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in the Device Descriptor structure.

6.17.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in *MSP430 Programming With the JTAG Interface*.

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7 Applications, Implementation, and Layout

注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section describes the recommended guidelines when designing with the MSP MCU. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin (see 図 7-1). Higher-value capacitors may be used but can affect supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital to analog circuits on the board and to achieve high analog accuracy.

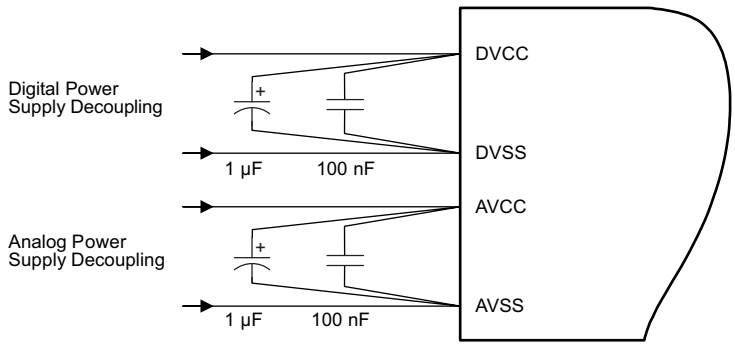

図 7-1. Power Supply Decoupling

For PVCC and PVSS, TI recommends connecting a combination of a 1-µF plus a 22-µF low-ESR ceramic decoupling capacitor between the PVCC and PVSS pins and a serial 22-Ω resistor to filter low-frequency noise on the supply line (see 図 7-2).

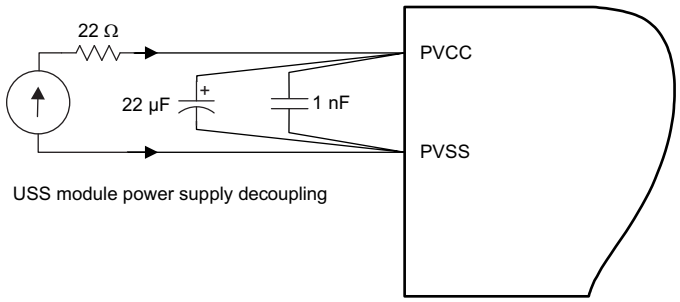

図 7-2. Power Supply Decoupling for PVCC and PVSS

7.1.2 External Oscillator (HFXT and LFXT)

Depending on the device variant (see 3), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, they must be terminated according to 4.6.

図 7-3 shows a typical connection diagram.

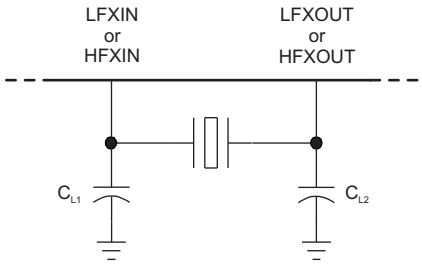

図 7-3. Typical Crystal Connection

See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP MCUs.

7.1.3 USS Oscillator (USSXT)

Depending on the device variant (see 3), the device with USS module supports a high-frequency crystal on the USSXT pins. External bypass capacitors for the crystal oscillator pins are required. Serially connect a 22-Ω resistor close to the USSXTOUT pin (see 図 7-4). The USSXT does not support bypass mode, so it is not possible to apply digital clock signals to the USSXTIN pin. Never connect the USSXTIN pin to a power supply line (AVCC, DVCC, or PVCC). If the USSXT pins are not used, terminate them according to 4.6.

図 7-4 shows a typical connection diagram.

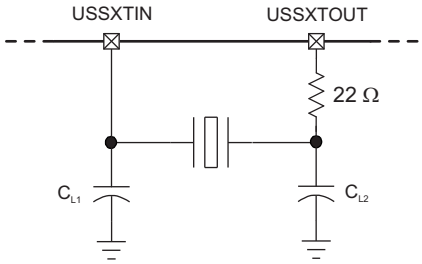

図 7-4. Typical Crystal Connection

Consider the following items for the USSXT layout:

- Keep the trace of USSXTIN and USSXTOUT as short as possible. If one must be longer than the other, keep USSXTIN shorter, because USSXTIN is more sensitive to EMI.
- Make the ground shield open ended without making a loop.
- Use a ground plane to reduce the impedance of the ground trace.
- If USSXT_BOUT is used, keep coupling to USSXTIN and CH0_IN to a minimum.
- If USSXT_BOUT is feeding other clock or device inputs, apply a small capacitor (10 pF) as the line termination load at the end of the line. This avoids reflection artifacts on sensitive inputs (for example, HFXTIN).

図 7-5 shows the recommended PCB layout.

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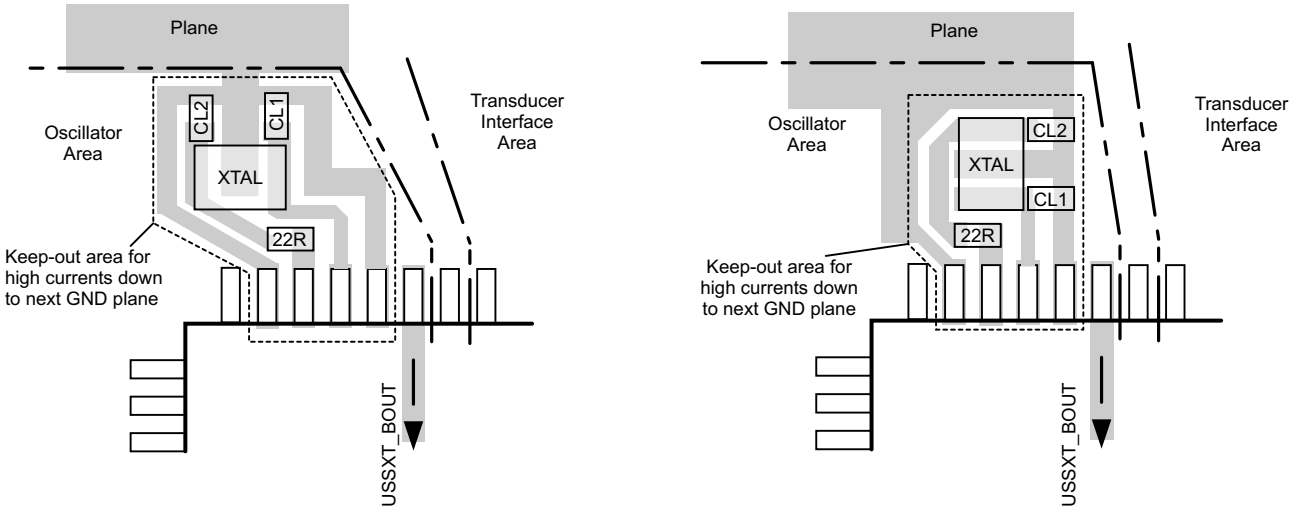

図 7-5. USSXT PCB Layout Recommendation

7.1.4 Transducer Connection to the USS Module

図 7-6 shows a typical connection of two transducers to the USS output and input pins. TI recommends 1% error tolerance for the external termination resistors (Rterm0 and Rterm1) and the AC coupling capacitors (Cac0 and Cac1). Typical value of the termination resistors is in the range of 150 to 400 Ω, the AC coupling capacitors are 1 to 2 nF. Actual values should be determined to meet the requirements of each application.

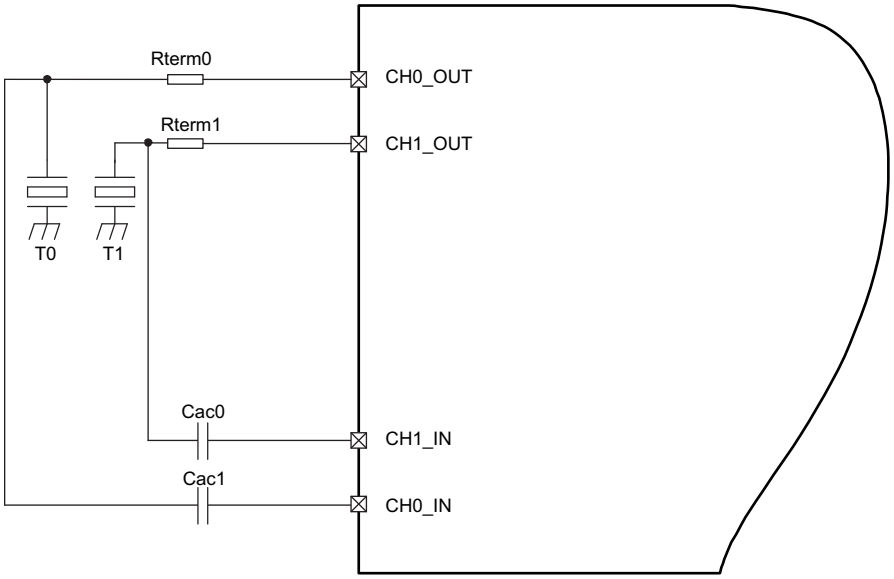

図 7-6. Typical Transducer Connection

7.1.5 Charge Pump Control of Input Multiplexer

図 7-7 shows the control logic of the charge pump control of the input multiplexer of CHx_IN. The charge pump is enabled as long the SAPH_AMCNF.CPEO is high and during the arming of the SDHS. Use the CPDA bit to control the CP during data acquisition.

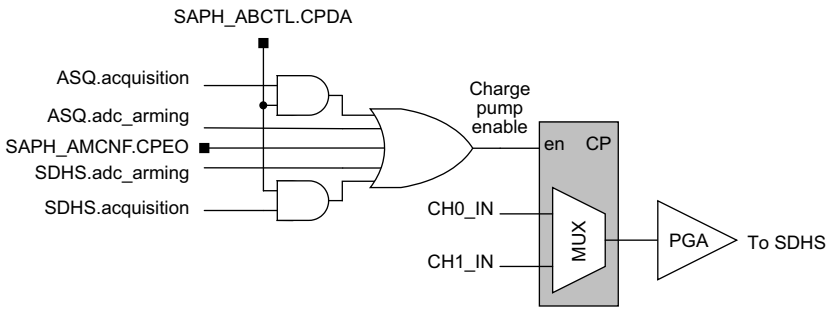

図 7-7. Control Of Input Multiplexer

7.1.6 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 図 7-8 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 図 7-9 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC} sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The V_{CC} sense feature senses the local V_{CC} present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 図 7-8 and 図 7-9 show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.

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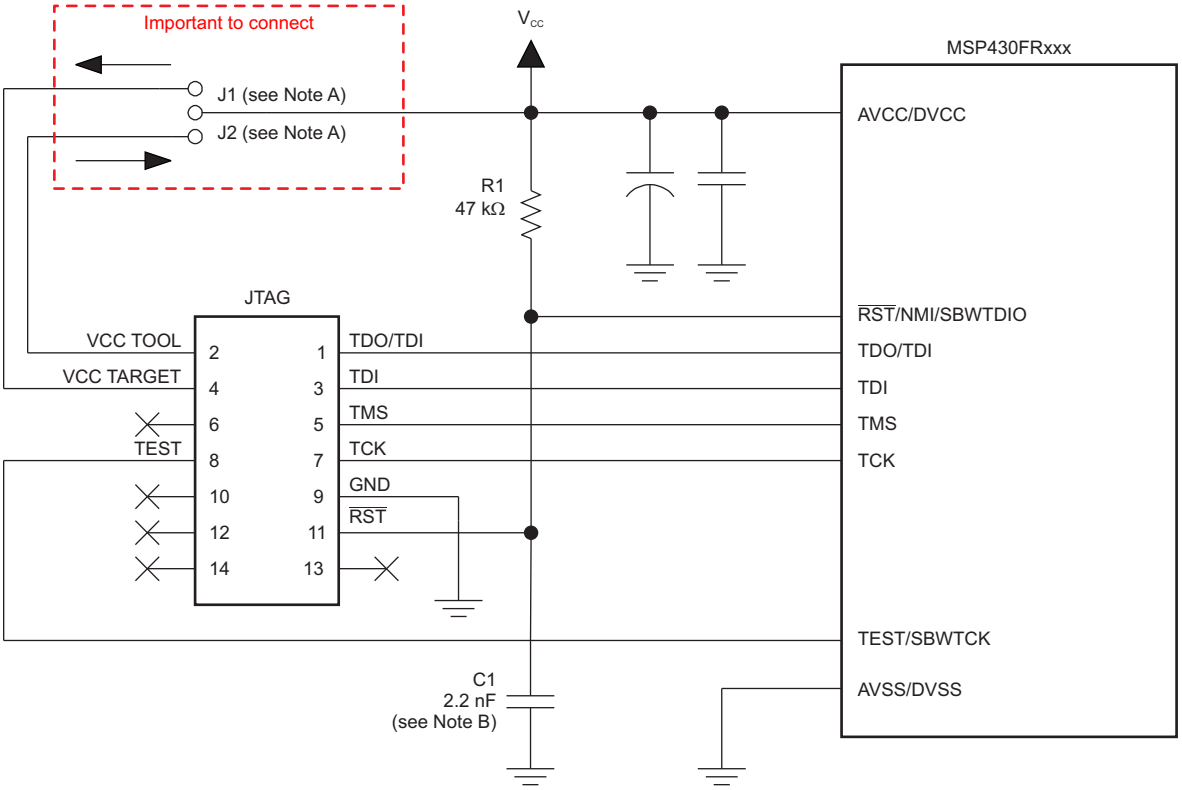

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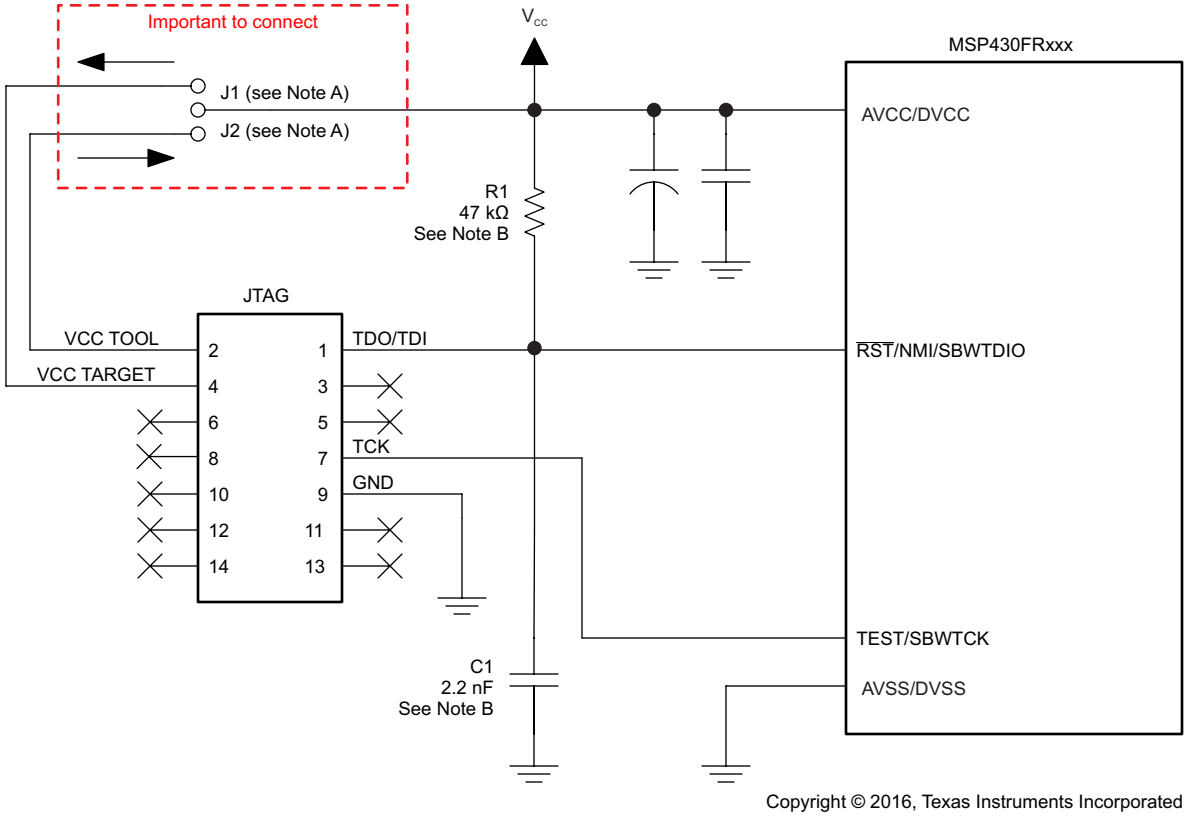
A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
B. The upper limit for C1 is 2.2 nF when using current TI tools.

図 7-8. Signal Connections for 4-Wire JTAG Communication



A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

図 7-9. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.7 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the SFRRPCR register.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide* for more information on the referenced control registers and bits.

7.1.8 Unused Pins

For details on the connection of unused pins, see 4.6.

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7.1.9 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.10 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in Section 5.1. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC12_B Peripheral

7.2.1.1 Partial Schematic

図 7-10 shows the recommended connections for the reference input pins.

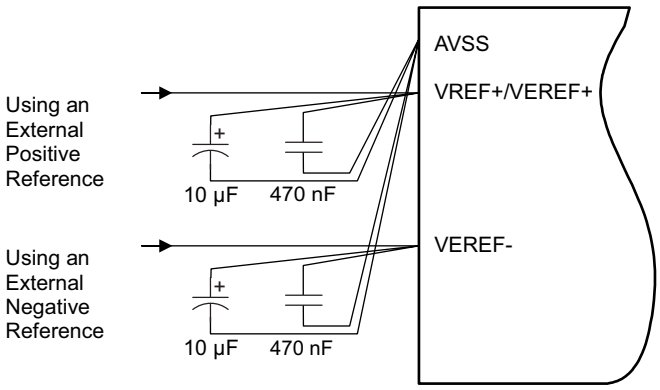

図 7-10. ADC12_B Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in 7.1.1 combined with the connections shown in 図 7-10 prevent these offsets.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommend to achieve high accuracy.

図 7-10 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the $I_{O(VREF+)}$ specification of the REF module.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor buffers the reference pin and filter any low-frequency ripple. A 470-nF bypass capacitor filters out any high-frequency noise.

7.2.1.3 Detailed Design Procedure

For additional design information, see *Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC*.

7.2.1.4 Layout Guidelines

Component that are shown in the partial schematic (see 図 7-10) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

7.2.2 LCD_C Peripheral

7.2.2.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and whether the on-chip charge pump is employed. Also, there is a fair amount of flexibility as to how the segment (Sx) and common (COMx) signals are connected to the MCU, which can provide unique benefits. Because LCD connections are application-specific, it is difficult to provide a single one-fits-all schematic. However, for examples and how-to circuit design guidance, see *Designing With MSP430™ MCUs and Segment LCDs*.

7.2.2.2 Design Requirements

Due to the flexibility of the LCD_C peripheral module to accommodate various segment-based LCDs, selecting the correct display for the application in combination with determining specific design requirements is often an iterative process. TI strongly recommends reviewing the LCD_C peripheral module chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide* and *Designing With MSP430™ MCUs and Segment LCDs* during the initial design requirements and decision process.

7.2.2.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_C peripheral module and the display. Two basic design processes can be employed for this step, although in reality often a balanced co-design approach is recommended:

- PCB layout-driven design, optimizing signal routing
- Software-driven design, focusing on optimizing computational overhead

For a detailed discussion of the design procedure as well as for design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, see *Designing With MSP430™ MCUs and Segment LCDs* and the *LCD_C Controller* chapter in the *MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide*.

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7.2.2.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane beneath the LCD traces and guard traces alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, place the externally provided capacitor on the LCDCAP pin as close as possible to the MCU. Connect the capacitor to the device using a short and direct trace and also have a solid connection to the ground plane that supplies the V_{SS} pins of the MCU.

For an example layouts and a more in-depth discussion, see *Designing With MSP430™ MCUs and Segment LCDs*.

8 デバイスおよびドキュメントのサポート

8.1 使い始めと次の手順

MSPファミリのマイクロコントローラ、および開発に役立つツールやライブラリの詳細については、「Getting Started」ページを参照してください。

8.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP　MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

XMS - 実験段階のデバイスで、最終的なデバイスの電気的仕様を表しているとは限りません。

MSP - 完全に認定済みの量産版デバイスです。

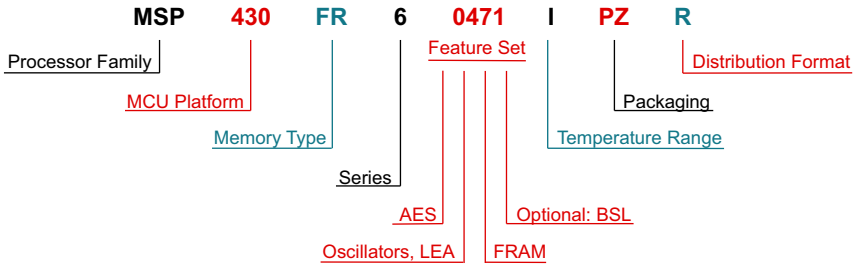
XMSデバイスは、次の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方を図 8-1に示します。



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon			
MCU Platform	430 = 16-Bit Low-Power Platform			
Memory Type	FR = FRAM			
Series	6 = FRAM 6 Series up to 16 MHz with LCD			
Feature Set	**First Digit: Feature** 0 = AES	**Second Digit: Oscillators, LEA** 4 = HFXT + LFXT + LEA + USS 3 = HFXT + LFXT + LEA 2 = HFXT + LFXT 1 = LFXT	**Third Digit: FRAM (KB)** 7 = 256 6 = 192 5 = 128 4 = 96 3 = 64	**Optional Fourth Digit: BSL** 1 = I^2C No value = UART
Temperature Range	I = –40°C to 85°C			
Packaging	http://www.ti.com/packaging			
Distribution Format	T = Small reel R = Large reel No markings = Tube or tray			

図 8-1. デバイスの項目表記

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8.3 ツールとソフトウェア

これらのマイクロコントローラでサポートされているデバッグ機能の一覧を、表 8-1に示します。利用可能な機能の詳細については、『MSP430用Code Composer Studio™ IDEユーザー・ガイド』を参照してください。使用法の詳細については、以下のドキュメントを参照してください。

『拡張エミュレーション・モジュール(EEM)とCode Composer Studio™ IDEによる高度なデバッグ』

『MSP430™の高度な電力最適化: ULP Advisor™ ソフトウェアおよびEnergyTrace™テクノロジ』

表 8-1. ハードウェアの特長

MSPのアーキテクチャ	4線式 JTAG	2線式 JTAG	ブレーク・ポイント (N)	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMx.5デバッグ・サポート	EnergyTrace++
MSP430Xv2	○	○	3	○	○	×	×	○	○

設計キットと評価モジュール

MSP430FR6047 超音波センシング評価モジュール EVM430-FR6047評価キットは、超音波センシング・アプリケーション(スマート水量計など)でのMSP430FR6047の性能を評価するため使用可能な、開発プラットフォームです。

MSP-TS430PZ100E 100ピン・ターゲット開発基板 MSP-TS430PZ100E はスタンドアロンの 100 ピン ZIF ソケット・ターゲット・ボードで、JTAG インターフェイスまたは Spy Bi-Wire (2 線式の JTAG) プロトコルによる MSP430 MCU イン・システムのプログラムとデバッグに使用することができます。

ソフトウェア

MSP430Ware™ソフトウェア MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存のMSP430用設計リソースの完全なコレクションに加えて、MSP430WareソフトウェアにはMSP430ドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430Wareソフトウェアは、Code Composer Studio IDEのコンポーネントとして、またはスタンドアロンのパッケージとして利用可能です。

MSP430FR604x(1)、MSP430FR603x(1)のサンプル・コード すべてのMSPデバイス用に、内蔵する各ペリフェラルをさまざまな用途のニーズに合わせて構成するためのCコード・サンプルが用意されています。

MSPドライバ・ライブラリ ドライバ・ライブラリの抽象化APIで、使いやすい関数呼び出しが用意されており、MSP430ハードウェアのビットやバイトのレベルを意識せずに、より高水準の開発作業に集中できます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTrace™テクノロジ MSP430マイクロコントローラ用のEnergyTraceテクノロジは、エネルギーを基準としたコード解析ツールで、アプリケーションのエネルギー・プロファイルを測定して表示し、消費電力が極めて低くなるよう最適化するため役立ちます。

ULP (超低消費電力) Advisor ULP Advisor™ソフトウェアは、MSP430およびMSP432マイクロコントローラ独自の超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorは、マイクロコントローラの熟練した開発者でも、新しい開発者でも使用でき、包括的なULPチェックリストと照らし合わせてコードのチェックを行い、アプリケーションの性能を最大限まで発揮できるようにします。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

MSP MCU用の固定小数点数値演算ライブラリ MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

MSP430™ MCU用の浮動小数点数値演算ライブラリ 低消費電力かつ低コストのマイクロコントローラ分野で継続的な革新を行うため、TIはMSPMATHLIBを提供しています。このスカラー関数の浮動小数点数値演算ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、最高26倍の性能を実現します。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer StudioとIAR IDEの両方に組み込まれています。数値演算ライブラリと関連ベンチマークの詳細については、ユーザー・ガイドを参照してください。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境 Code Composer Studioは、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。Code Composer Studioは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。IDEは直感的で、アプリケーションの開発フローの各段階を、すべて同一のユーザー・インターフェイスで実行できます。使い慣れたユーティリティとインターフェイスにより、ユーザーは従来より迅速に作業を開始できます。Code Composer Studioは、Eclipseソフトウェア・フレームワークの利点と、TIの先進的な組み込みデバッグ機能の利点を組み合わせ、組み込み製品の開発者向けの魅力的な、豊富な機能を持つ開発環境を実現します。CCSをMSP MCUとともに使用すると、MSPマイクロコントローラを最大限に活用するための、ユニークで強力な一連のプラグインや組み込みソフトウェア・ユーティリティを利用できます。

コマンドライン・プログラマ MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txtまたは.hex) をMSPマイクロコントローラへ直接ダウンロードできます。

MSP MCUプログラマおよびデバッガ MSP-FETは強力なエミュレーション開発ツールで、多くの場合、デバッグ・プローブと呼ばれています。ユーザーはこのツールを使用して、MSP低消費電力マイクロコントローラ(MCU)のアプリケーション開発を迅速に開始できます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。MSP-FETは、ホスト・コンピュータとターゲットMSPの間で、デバッグ通信経路を提供します。さらに、MSP-FETはコンピュータのUSBインターフェイスとMSP UARTの間で、バックチャネルUART接続も提供します。これにより、MSPプログラマは、コンピュータ上で動作している端末ソフトウェアとMSPとの間で、シリアル通信を簡単に実行できます。またMSP-FETは、UARTやI^2C通信プロトコルを経由するBSLを使用して、プログラム(多くの場合、ファームウェアと呼ばれます)をMSPターゲットにロードできます。

MSP-GANG量産プログラマ MSP Gang ProgrammerはMSP430またはMSP432用のデバイス・プログラマで、8つまでの同一のMSP430またはMSP432フラッシュまたはFRAMデバイスを同時にプログラムできます。MSP Gang Programmerは、標準のRS-232またはUSB接続を使用してホストPCに接続でき、柔軟なプログラミング・オプションにより、プロセスを完全にカスタマイズ可能です。MSP Gang Programmer には、Gang Splitter と呼ばれる拡張ボードが付属しており、MSP Gang Programmer と複数のターゲット・デバイスとの間で相互接続機能を実装します。拡張ボードと、8つのターゲット・デバイスとを接続するため、8本のケーブルが付属しています(JTAGまたはSpy-Bi-Wireコネクタ経由)。PCを使用してプログラムすることも、スタンドアロンのデバイスとしてプログラムすることもできます。PC側のグラフィカル・ユーザー・インターフェイスも用意されており、DLLベースです。

8.4 ドキュメントのサポート

次のドキュメントには、MSP430FR604x(1)、MSP430FR603x(1) MCUについて記載されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでお使いの製品のフォルダへ移動します(プロダクト・フォルダへのリンクについては、 8.5を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430FR6047デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR60471デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR6045デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR6037デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR60371デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430FR6035デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

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ユーザー・ガイド

『MSP430FR58xx、MSP430FR59xx、MSP430FR6xxファミリ・ユーザー・ガイド』 このデバイス・ファミリで利用可能なすべてのモジュールとペリフェラルについての詳細情報です。

『MSP430™ FRAMデバイス・ブートローダ(BSL)ユーザー・ガイド』 MSP430マイクロコントローラ(MCU)に搭載されたブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430 MCUの組み込みメモリと通信できます。必要に応じて、プログラム可能メモリ(FRAMメモリ)とデータ・メモリ(RAM)の両方を変更できます。

『JTAGインターフェイスによるMSP430™のプログラミング』 このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430™ハードウェア・ツール ユーザー・ガイド』 このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。FETは、MSP430超低消費電力マイクロコントローラ用のプログラム開発ツールです。

アプリケーション・レポート

『MSP430™ 32kHz水晶発振器』 適切な水晶振動子、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器に重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430™ システム・レベルESDの考慮事項』 シリコン・テクノロジがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まっていくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。(1) コンポーネント・レベルESDテストとシステム・レベルESDテスト、その違い、コンポーネント・レベルESD評価ではシステム・レベルの耐性が保証されない理由。(2) 筐体、ケーブル、PCBレイアウト、オンボードのESD保護デバイスなど各レベルにおいてシステム・レベルのESD保護を行うための、一般的な設計ガイドライン。(3) System Efficient ESD Design (SEED)の概要、システム・レベルESD耐性を達成するオンボードおよびオンチップESD保護のコデザイン手法、サンプル・シミュレーションとテスト結果。現実世界でのシステム・レベルのESD保護設計の例のいくつかと、その結果についても解説します。

8.5 関連リンク

表 8-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 8-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430FR6047	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR60471	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR6045	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR6037	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR60371	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430FR6035	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

8.6 商標

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, Code Composer Studio are trademarks of Texas Instruments.
Arm, Cortex are registered trademarks of Arm Limited.
Microsoft is a registered trademark of Microsoft Corporation.
All other trademarks are the property of their respective owners.

8.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

8.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430FR6035IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6035
MSP430FR6035IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6035
MSP430FR6035IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6035
MSP430FR6035IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6035
MSP430FR60371IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60371
MSP430FR60371IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60371
MSP430FR60371IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60371
MSP430FR60371IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60371
MSP430FR6037IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6037
MSP430FR6037IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6037
MSP430FR6037IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6037
MSP430FR6037IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6037
MSP430FR6045IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6045
MSP430FR6045IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6045
MSP430FR6045IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6045
MSP430FR6045IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6045
MSP430FR60471IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60471
MSP430FR60471IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60471
MSP430FR60471IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60471
MSP430FR60471IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR60471
MSP430FR6047IPZ	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6047

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430FR6047IPZ.A	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6047
MSP430FR6047IPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6047
MSP430FR6047IPZR.A	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	FR6047

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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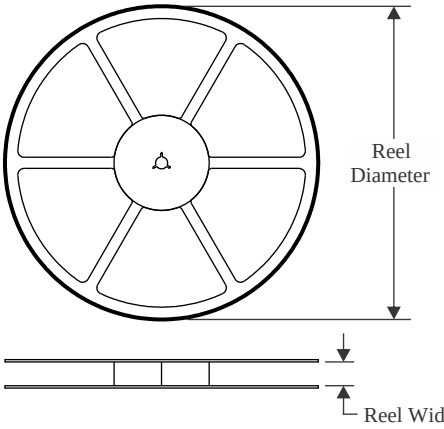
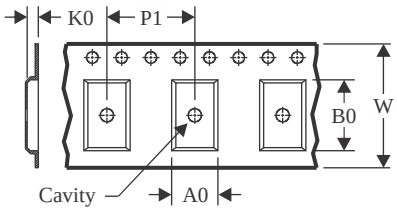
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

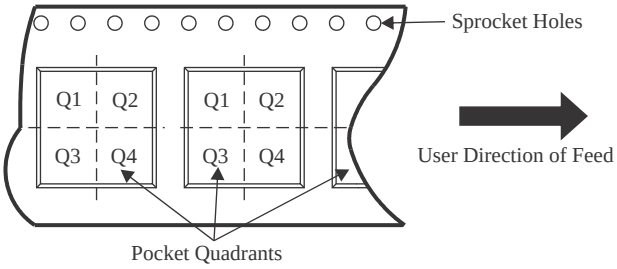


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

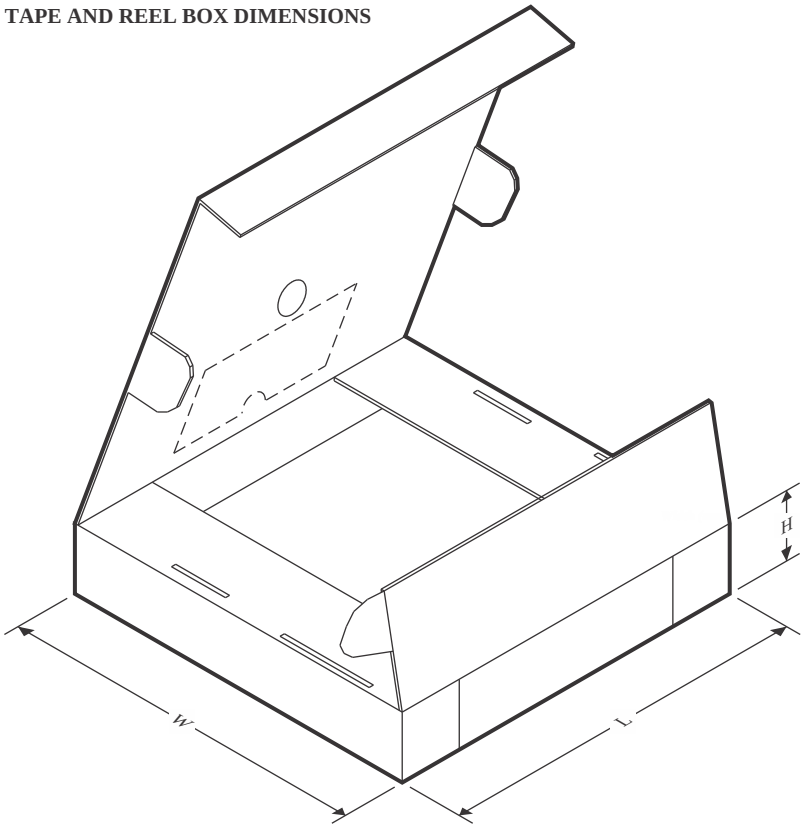
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR6035IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FR60371IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FR6037IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FR6045IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FR60471IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FR6047IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2

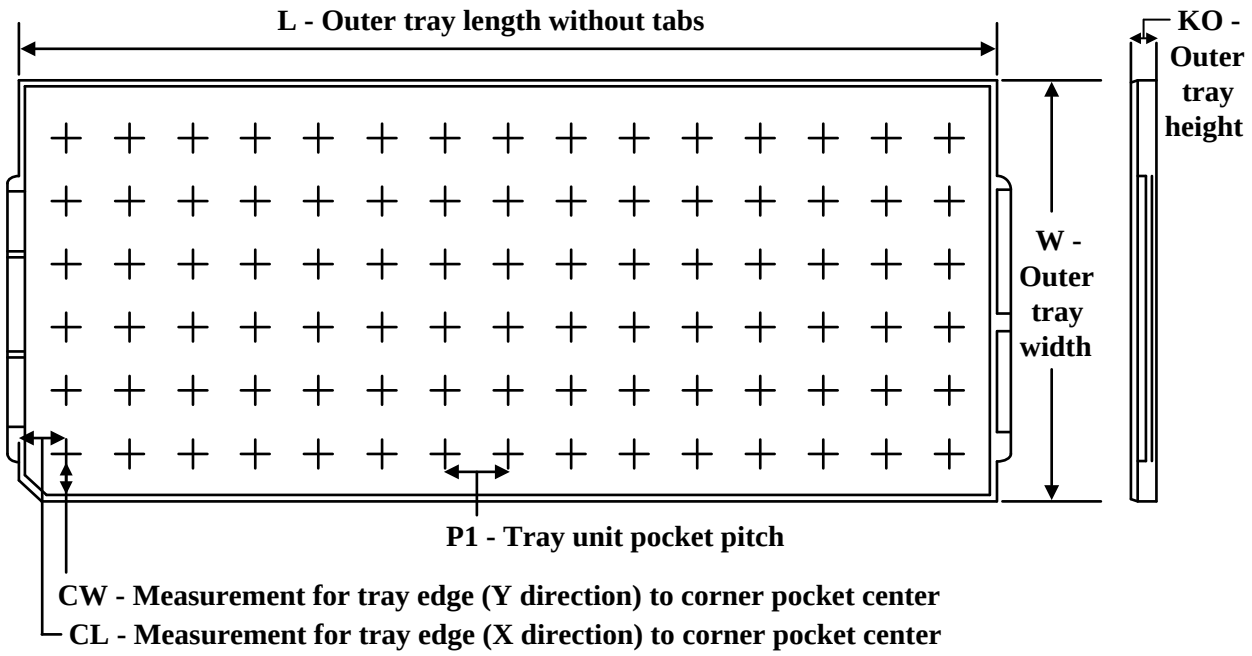
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR6035IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FR60371IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FR6037IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FR6045IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FR60471IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0
MSP430FR6047IPZR	LQFP	PZ	100	1000	350.0	350.0	43.0

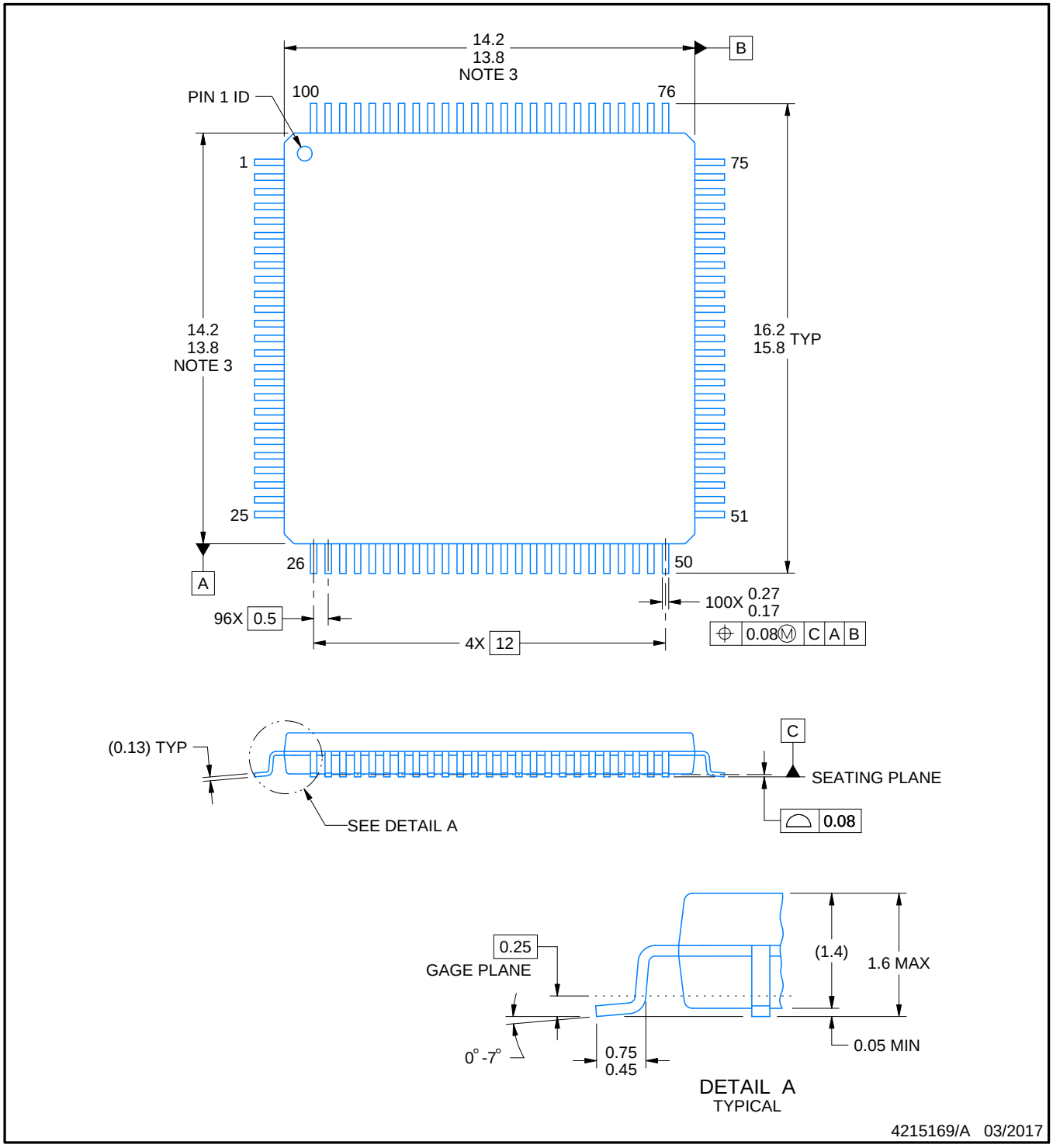
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

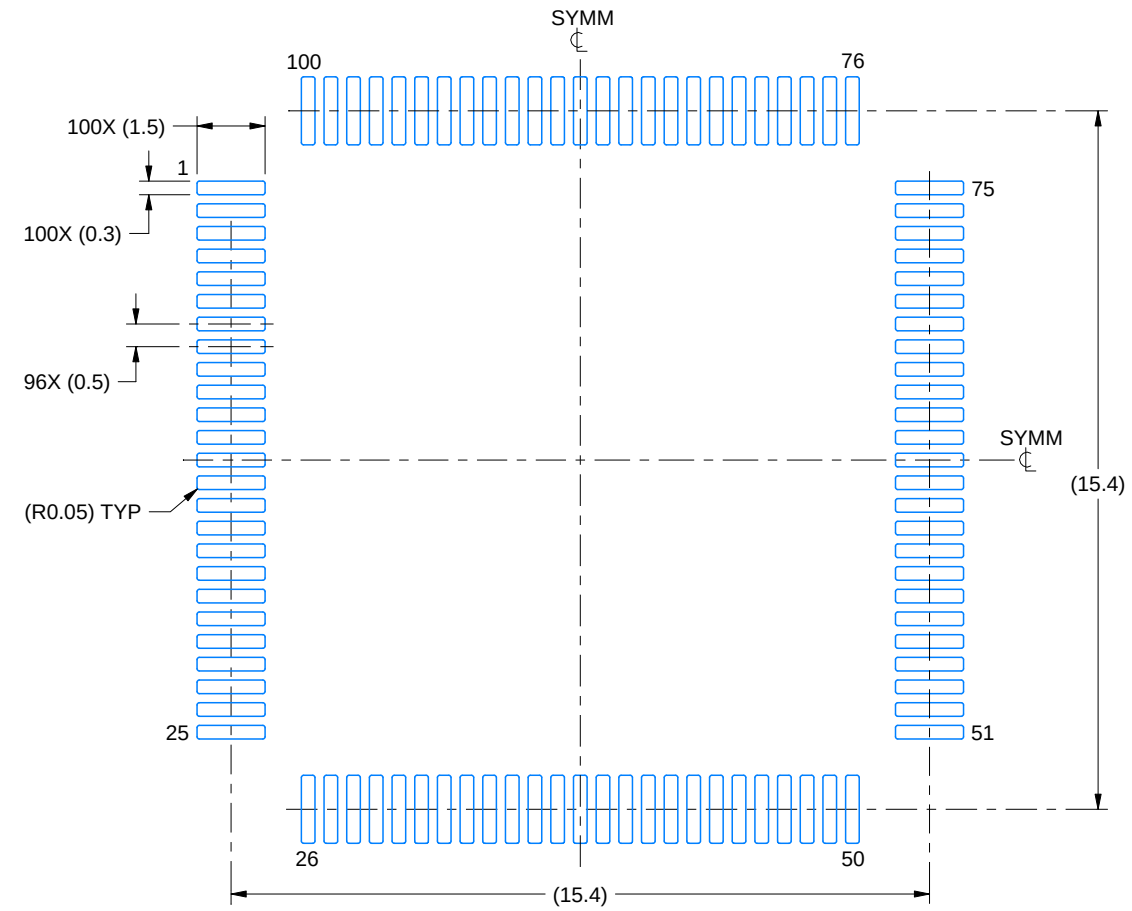
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430FR6035IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6035IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR60371IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR60371IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6037IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6037IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6045IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6045IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR60471IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR60471IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6047IPZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
MSP430FR6047IPZ.A	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45

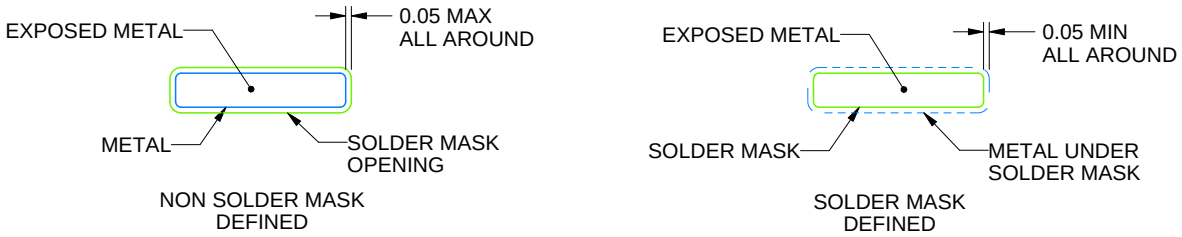


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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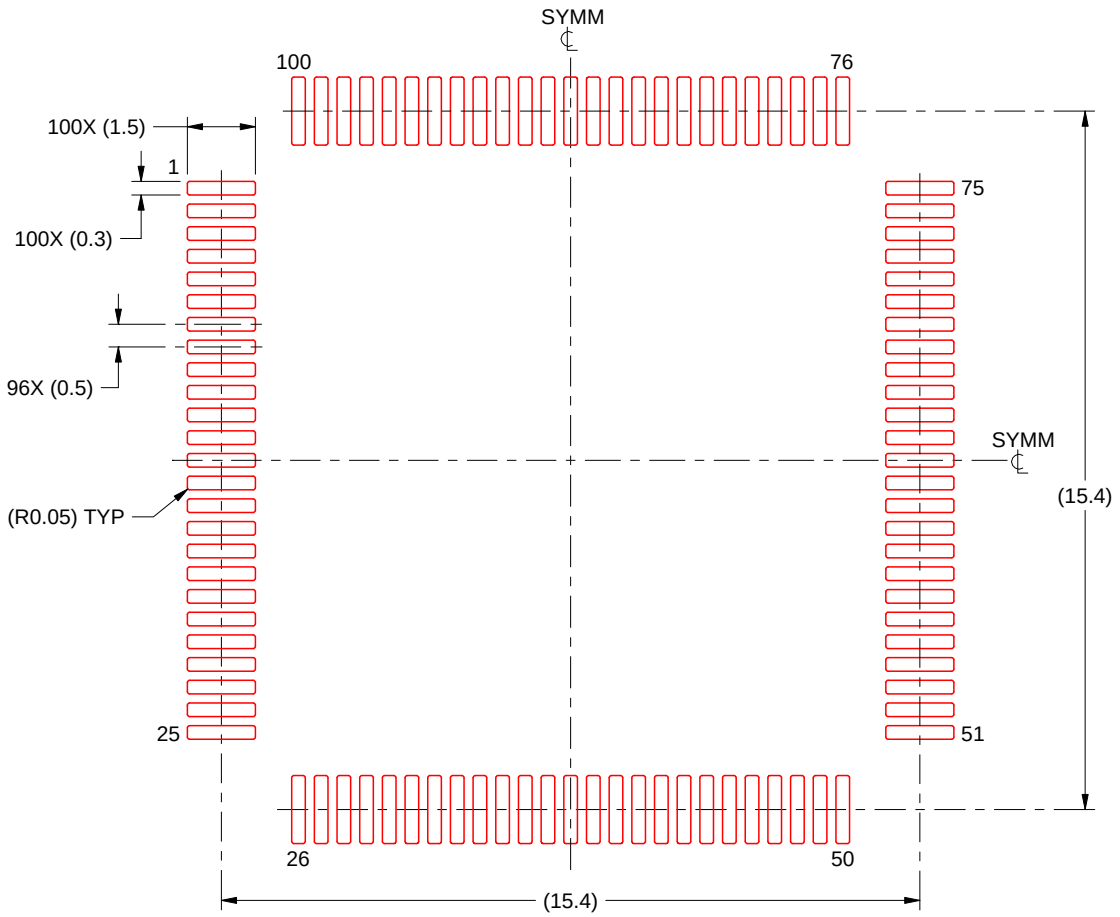
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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