

OPA164x-Q1 SoundPlus™ JFET入力、車載グレード、オーディオ・オペアンプ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み:
 - デバイス温度グレード1: 動作時周囲温度 $-40^{\circ}\text{C}\sim+125^{\circ}\text{C}$
 - デバイスHBM ESD分類レベル2
 - デバイスCDM ESD分類レベルC6
- 低ノイズ: 1kHz時に $5.1\text{nV}/\sqrt{\text{Hz}}$
- 非常に低い歪み: 1kHz時に0.00005%
- 高いスルーレート: $20\text{V}/\mu\text{s}$
- ユニティ・ゲイン安定
- 位相反転なし
- 低い静止電流:
 - チャネルごとに 1.8mA
- レール・ツー・レール出力
- 広い電源電圧範囲: $\pm 2.25\text{V}\sim\pm 18\text{V}$
- シングル、デュアル、クワッドのバージョンを利用可能

2 アプリケーション

- 車載用
- HEVおよびEVのパワートレイン
- 先進運転支援システム(ADAS)
- インフォテインメント・システム
- 車室内マイク

3 概要

OPA1641-Q1 (シングル)およびOPA1642-Q1 (デュアル)シリーズは、JFET入力、非常に低い歪み、低ノイズのオペアンプであり、オーディオ・アプリケーション向けに完全に規定されています。

レール・ツー・レール出力によりヘッドルームが増大するため、これらのデバイスはあらゆるオーディオ回路での使用に理想的です。特長として、 $5.1\text{nV}/\sqrt{\text{Hz}}$ のノイズ、低い全高調波歪み+ノイズ(THD+N) (0.00005%)、低い入力バイアス電流(2pA)、低い静止電流(チャネルごとに 1.8mA)が挙げられます。

これらのデバイスは $\pm 2.25\text{V}\sim\pm 18\text{V}$ の非常に広い電源電圧範囲で動作します。OPA164x-Q1シリーズのオペアンプはユニティ・ゲイン安定で、広い範囲の負荷条件にわたって非常に優れた動的特性を示します。

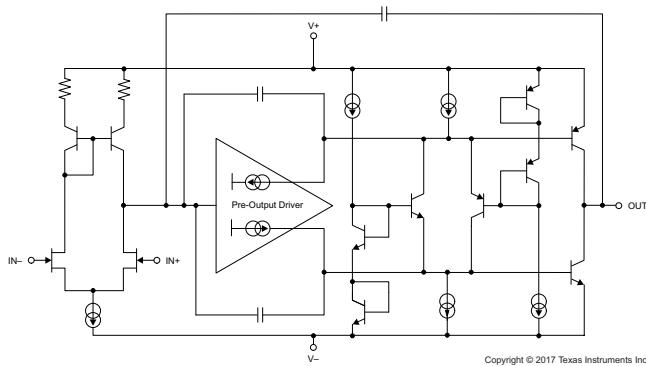
デュアル・バージョンは完全に独立した回路を使用しているため、クロストークが非常に低く、オーバードライブや過負荷時でもチャネル間の干渉が発生しません。

製品情報⁽¹⁾

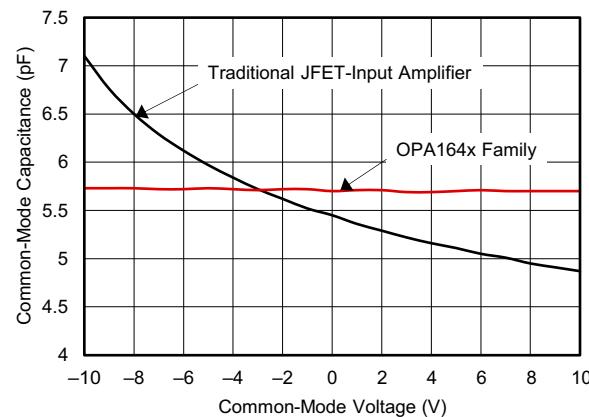
型番	パッケージ	本体サイズ(公称)
OPA1641-Q1	SOIC (8)	4.90mm×3.90mm
	VSSOP (8)	3.00mm×3.00mm
OPA1642-Q1	SOIC (8)	4.90mm×3.90mm
	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

簡略化された内部回路図



非常に安定した入力容量



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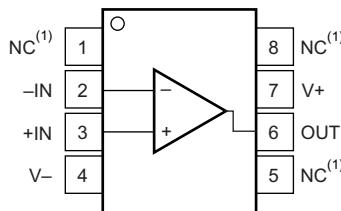
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年6月発行のものから更新	Page
• Added separate A_{OL} values for OPA1642-Q1	6

5 Pin Configuration and Functions

**OPA1641-Q1: D and DGK Packages
8-Pin SOIC and VSSOP
Top View**

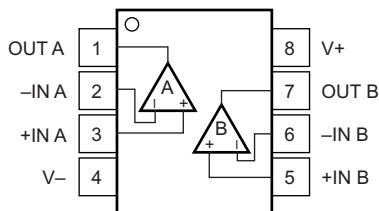


(1) NC - no internal connection

Pin Functions: OPA1641-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN	2	I	Inverting input
+IN	3	I	Noninverting input
NC	1, 5, 8	—	No connection
OUT	6	O	Output
V-	4	—	Negative (lowest) power supply
V+	7	—	Positive (highest) power supply

**OPA1642-Q1: D and DGK Packages
8-Pin SOIC and VSSOP
Top View**



Pin Functions: OPA1642-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_S	Supply voltage		40	V
V_{IN}	Input voltage ⁽²⁾	$(V-) - 0.5$	$(V+) + 0.5$	V
I_{IN}	Input current ⁽²⁾		± 10	mA
$V_{IN(DIFF)}$	Differential input voltage		$\pm V_S$	V
I_O	Output short-circuit ⁽³⁾	Continuous		
T_A	Operating temperature	-55	125	°C
T_J	Junction temperature	-65	150	°C
T_{stg}	Storage temperature	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less. The input voltage and output negative-voltage ratings can be exceeded if the input and output current ratings are followed.
- Short-circuit to $V_S / 2$ (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	± 3000
		Charged-device model (CDM), per AEC Q100-011	± 1000

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (V_+ , V_-)	Single supply	4.5		36	V
	Dual supply	± 2.25		± 18	
Specified temperature		-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	OPA1641-Q1, OPA1642-Q1		UNIT	
	D (SOIC)	DGK (VSSOP)		
	8 PINS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	180	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	75	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9	n/a	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	120	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 4.5\text{ V}$ to $36\text{ (}\pm 2.25\text{ V to }\pm 18\text{ V)}$, $R_L = 2\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE					
THD+N Total harmonic distortion + noise	$G = 1$, $f = 1\text{ kHz}$, $V_O = 3\text{ V}_{\text{RMS}}$	0.00005%			
		–126			dB
IMD Intermodulation distortion	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz), $G = 1$, $V_O = 3\text{ V}_{\text{RMS}}$	0.00004%			
		–128			dB
IMD	DIM 30 (3-kHz square wave and 15-kHz sine wave), $G = 1$, $V_O = 3\text{ V}_{\text{RMS}}$	0.00008%			
		–122			dB
	CCIF twin-tone (19 kHz and 20 kHz), $G = 1$, $V_O = 3\text{ V}_{\text{RMS}}$	0.00007%			
		–123			dB
FREQUENCY RESPONSE					
GBW Gain-bandwidth product	$G = 1$		11		MHz
SR Slew rate	$G = 1$		20		$\text{V}/\mu\text{s}$
Full-power bandwidth ⁽¹⁾	$V_O = 1\text{ V}_P$		3.2		MHz
Overload recovery time ⁽²⁾	$G = –10$		600		ns
Channel separation (dual and quad)	$f = 1\text{ kHz}$		–126		dB
NOISE					
Input voltage noise	$f = 20\text{ Hz to }20\text{ kHz}$		4.3		μV_{PP}
e_n Input voltage noise density	$f = 10\text{ Hz}$		8		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$		5.8		
	$f = 1\text{ kHz}$		5.1		
I_n Input current noise density	$f = 1\text{ kHz}$		0.8		$\text{fA}/\sqrt{\text{Hz}}$
OFFSET VOLTAGE					
V_{OS} Input offset voltage	$V_S = \pm 18\text{ V}$		1	3.5	mV
PSRR V_{OS} vs power supply	$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$		0.14	2	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT					
I_B Input bias current	$V_{CM} = 0\text{ V}$		±2	±20	pA
I_{OS} Input offset current	$V_{CM} = 0\text{ V}$		±2	±20	pA
INPUT VOLTAGE RANGE					
V_{CM} Common-mode voltage range		$(V-) – 0.1$		$(V+) – 3.5$	V
CMRR Common-mode rejection ratio	$V_{CM} = (V-) – 0.1\text{ V to } (V+) – 3.5\text{ V}$, $V_S = \pm 18\text{ V}$	120	126		dB
INPUT IMPEDANCE					
Differential			$10^{13} \parallel 8$		$\Omega \parallel \text{pF}$
Common-mode	$V_{CM} = (V-) – 0.1\text{ V to } (V+) – 3.5\text{ V}$		$10^{13} \parallel 6$		$\Omega \parallel \text{pF}$

(1) Full power bandwidth = $SR / (2\pi \times V_P)$, where SR = slew rate.

(2) See Figure 19 and Figure 20.

Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 4.5\text{ V}$ to $36\text{ (}\pm 2.25\text{ V to }\pm 18\text{ V)}$, $R_L = 2\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OPEN-LOOP GAIN						
A_{OL}	OPA1641-Q1: $(V-) + 0.2\text{ V} \leq V_O \leq (V+) - 0.2\text{ V}$, $R_L = 10\text{ k}\Omega$	120	134		dB	
	OPA1641-Q1: $(V-) + 0.35\text{ V} \leq V_O \leq (V+) - 0.35\text{ V}$, $R_L = 2\text{ k}\Omega$	114	126			
	OPA1642-Q1: $(V-) + 0.2\text{ V} \leq V_O \leq (V+) - 0.2\text{ V}$, $R_L = 10\text{ k}\Omega$	114	134			
	OPA1642-Q1: $(V-) + 0.35\text{ V} \leq V_O \leq (V+) - 0.35\text{ V}$, $R_L = 2\text{ k}\Omega$	111	126			
OUTPUT						
V_O	$R_L = 10\text{ k}\Omega$, $A_{OL} \geq 120\text{ dB (OPA1641-Q1)}$ $A_{OL} \geq 114\text{ dB (OPA1642-Q1)}$	$(V-) + 0.2$	$(V+) - 0.2$		V	
	$R_L = 2\text{ k}\Omega$, $A_{OL} \geq 114\text{ dB (OPA1641-Q1)}$ $A_{OL} \geq 111\text{ dB (OPA1642-Q1)}$	$(V-) + 0.35$	$(V+) - 0.35$			
I_{OUT}	Output current	See Typical Characteristics				
Z_O	Open-loop output impedance	See Typical Characteristics				
I_{SC}	Short-circuit current	Source	36		mA	
		Sink	-30			
C_{LOAD}	Capacitive load drive	See Typical Characteristics				
POWER SUPPLY						
V_S	Specified voltage	± 2.25	± 18		V	
I_Q	Quiescent current (per amplifier)	$I_{OUT} = 0\text{ A}$	1.8	2.3	mA	
TEMPERATURE RANGE						
Specified range		-40	125		°C	
Operating range		-55	125		°C	

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $R_L = 2 \text{ k}\Omega$ connected to midsupply, and $V_{\text{CM}} = V_{\text{OUT}} = \text{midsupply}$ (unless otherwise noted)

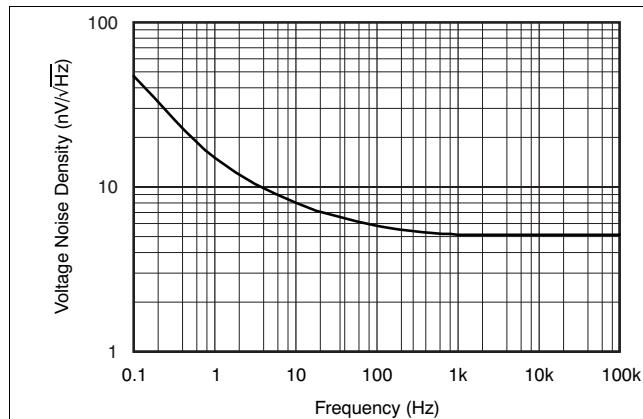


图 1. Input Voltage Noise Density vs Frequency

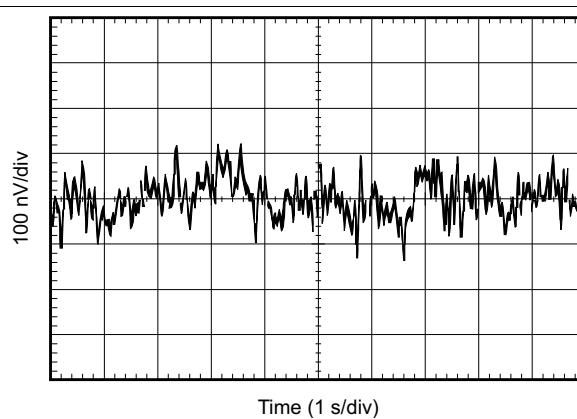


图 2. 0.1-Hz to 10-Hz Noise

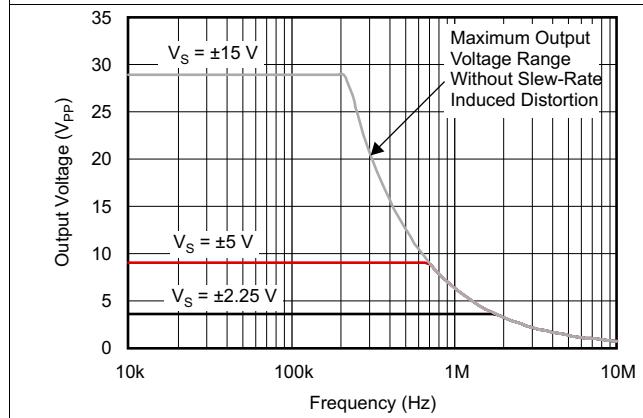


图 3. Maximum Output Voltage vs Frequency

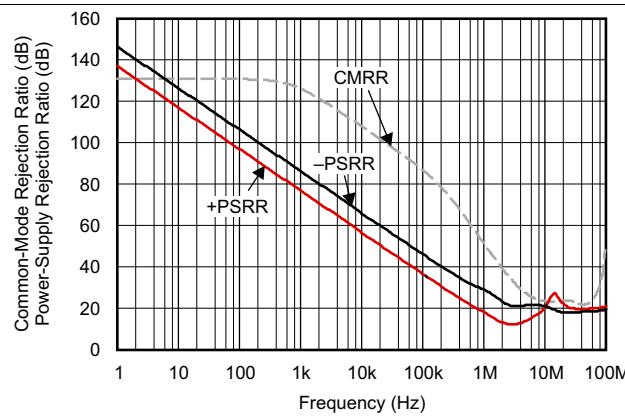


图 4. CMRR and PSRR vs Frequency
(Referred to Input)

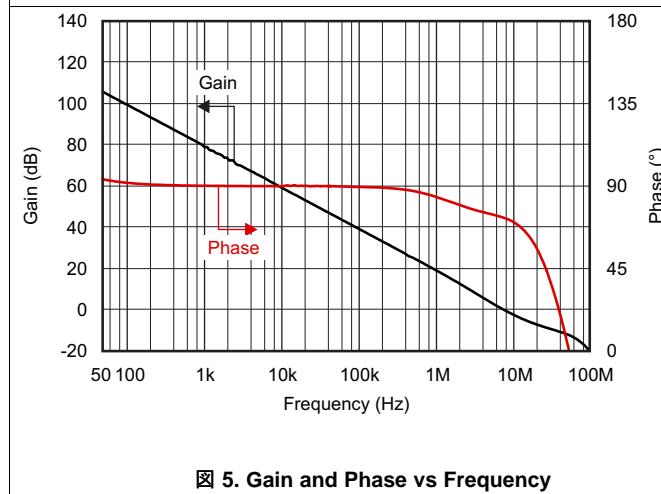


图 5. Gain and Phase vs Frequency

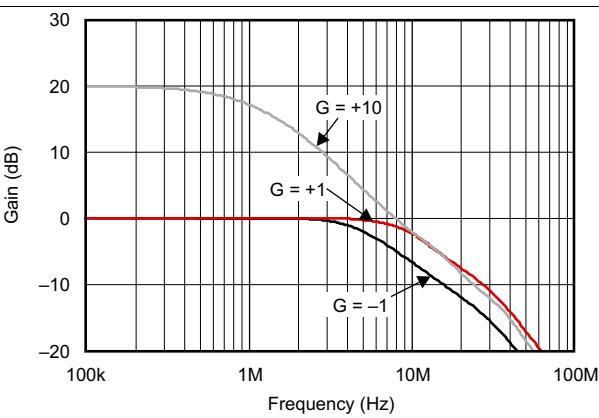
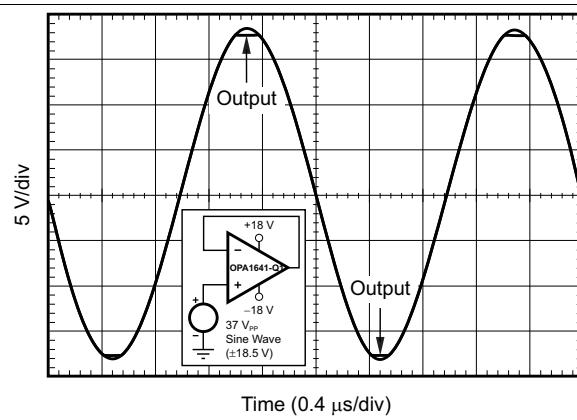
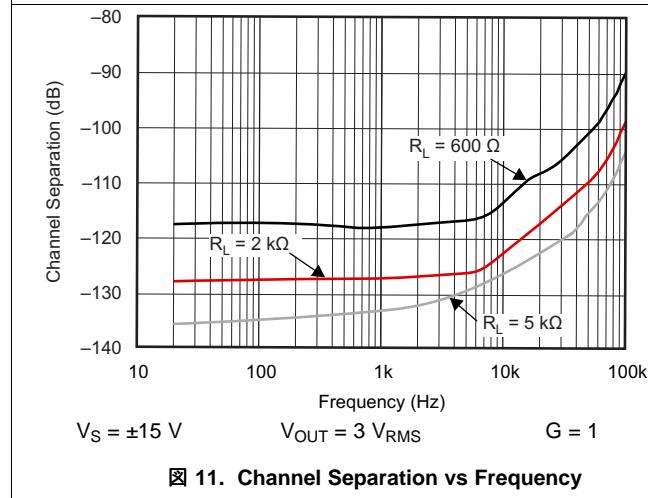
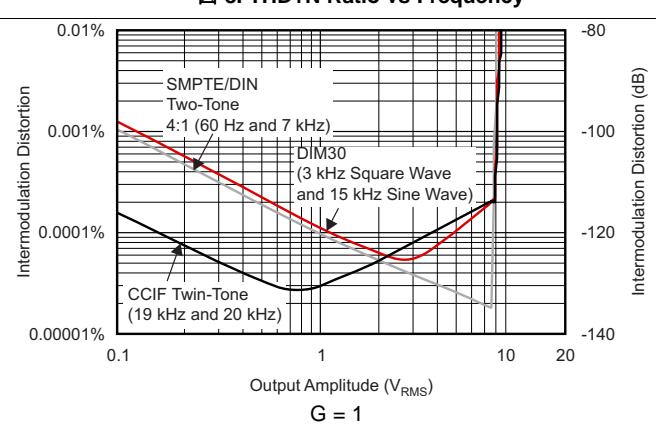
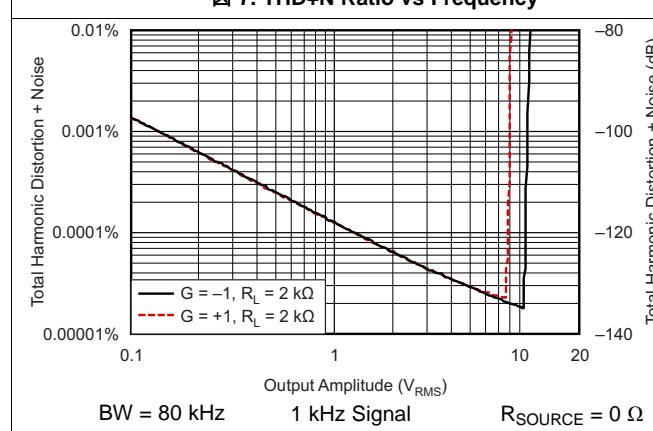
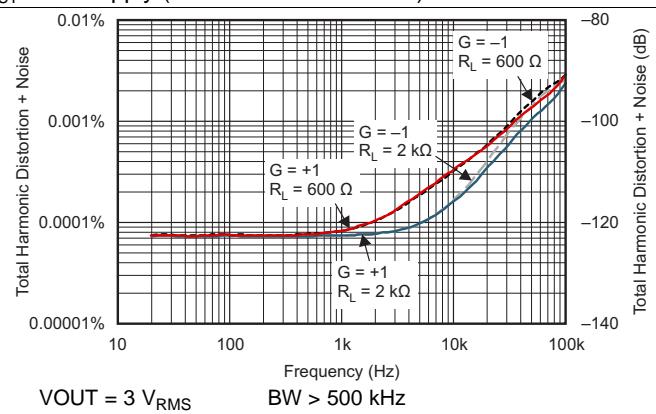
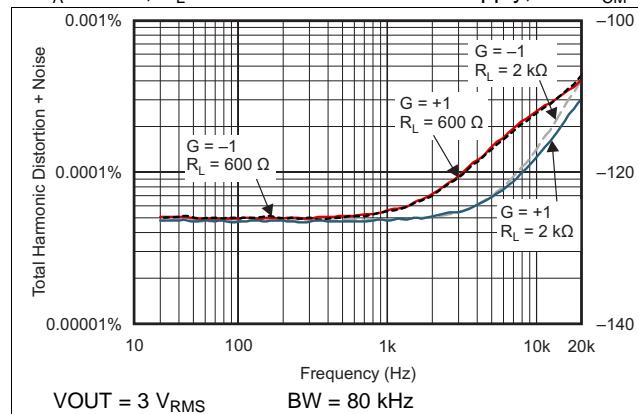


图 6. Closed-Loop Gain vs Frequency

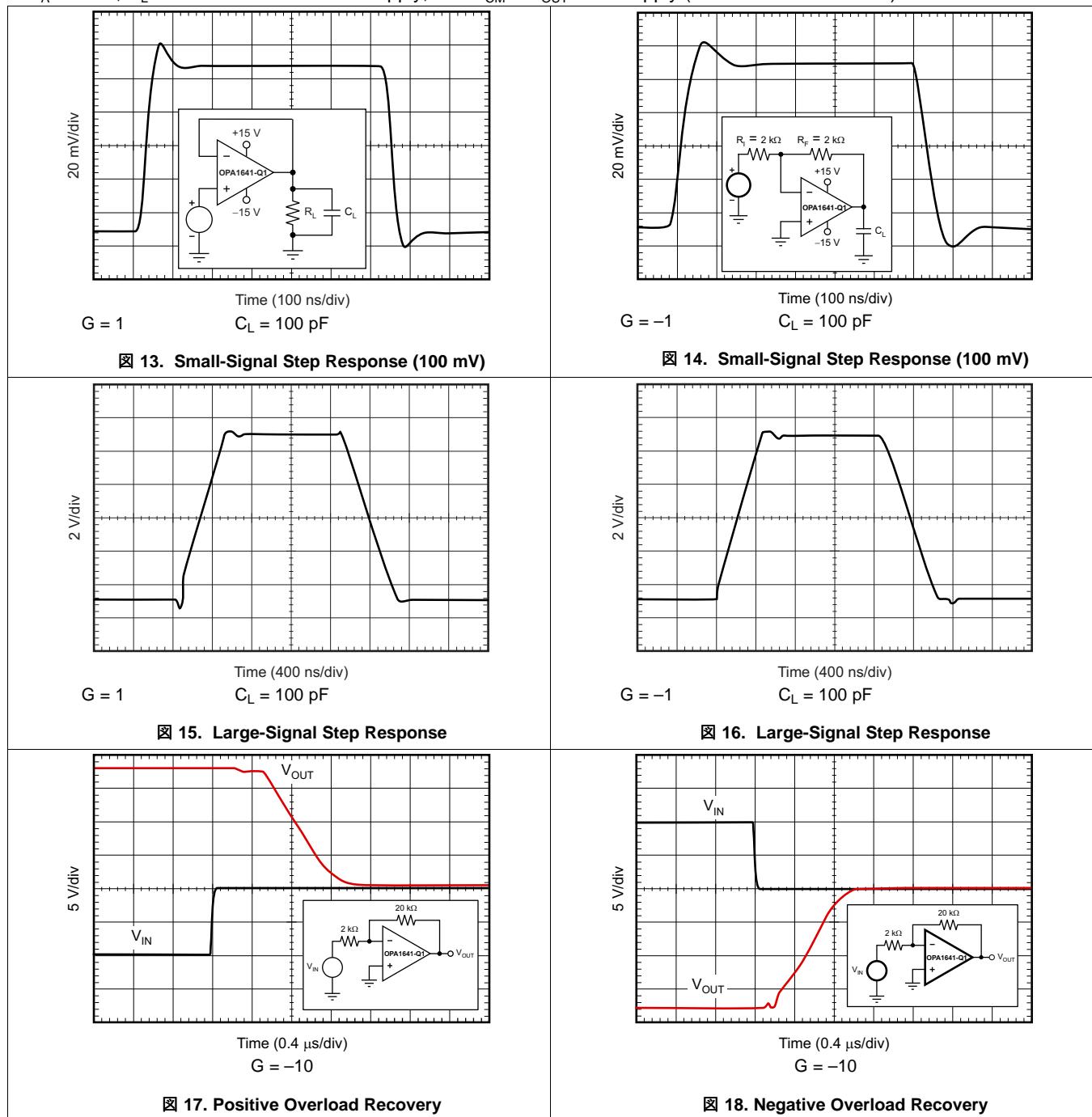
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $R_L = 2 \text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)



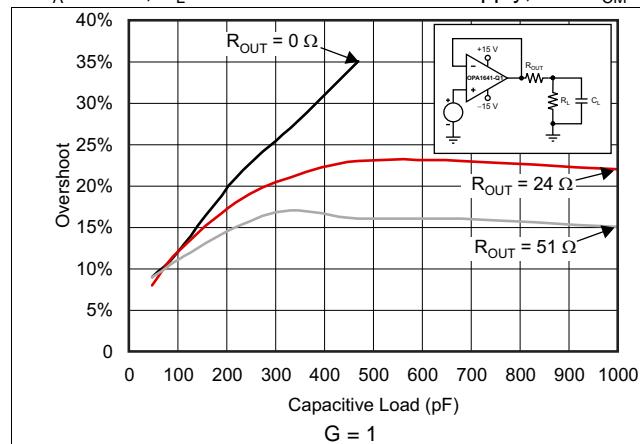
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT}$ = midsupply (unless otherwise noted)

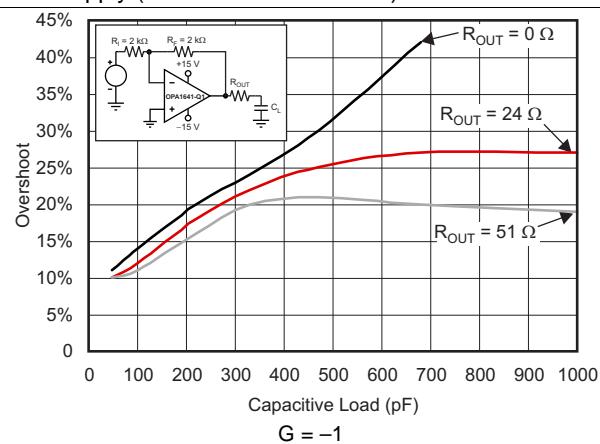


Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)



**図 19. Small-Signal Overshoot vs Capacitive Load
(100-mV Output Step)**



**図 20. Small-Signal Overshoot vs Capacitive Load
(100-mV Output Step)**

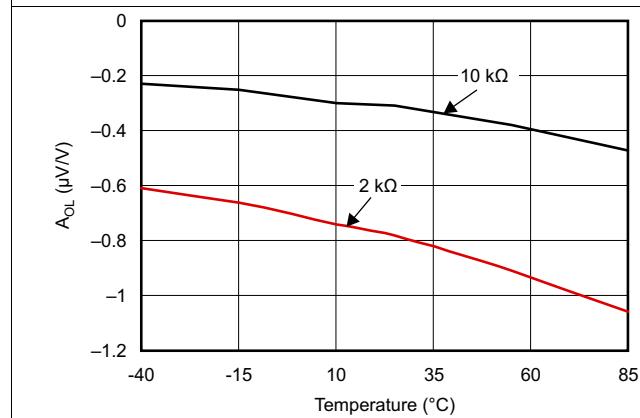


図 21. Open-Loop Gain vs Temperature

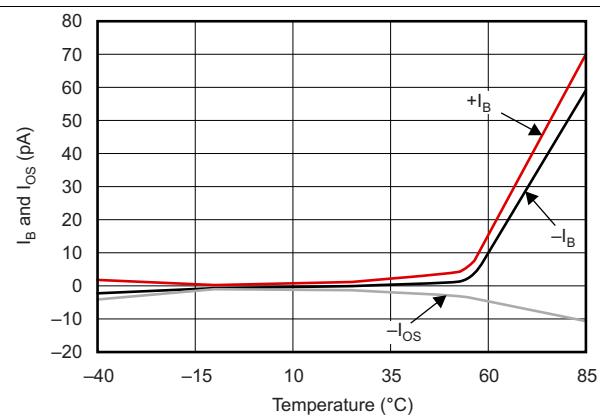


図 22. I_B and I_OS vs Temperature

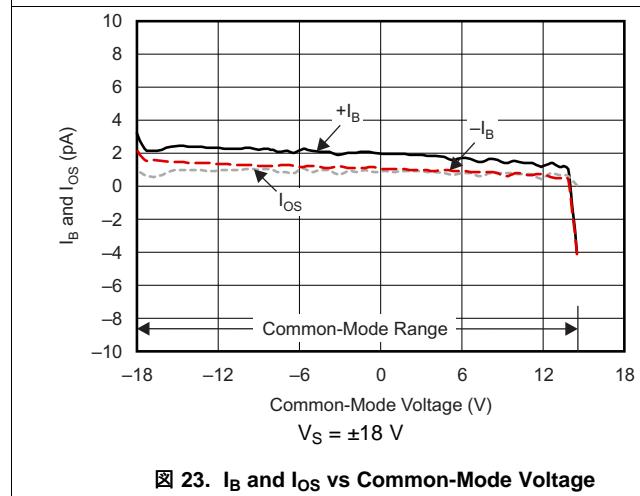


図 23. I_B and I_OS vs Common-Mode Voltage

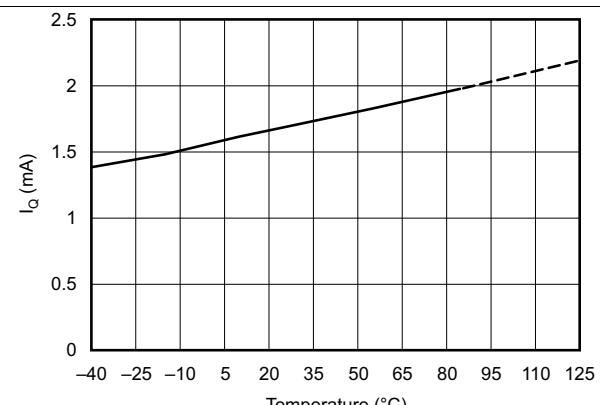


図 24. Quiescent Current vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

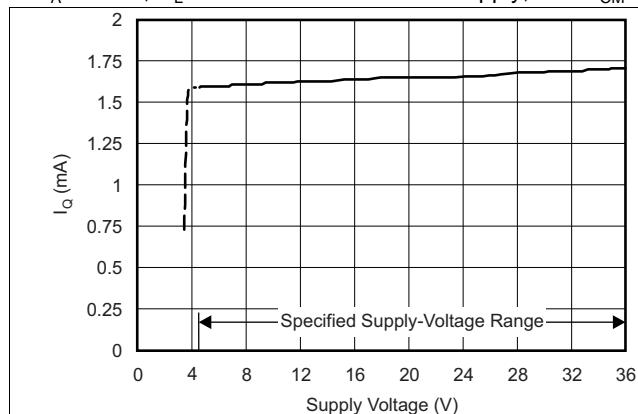
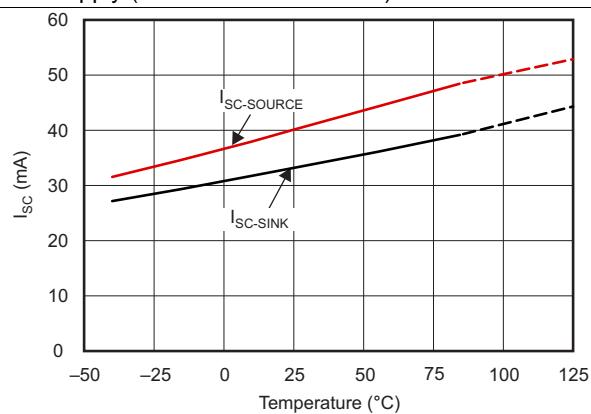


図 25. Quiescent Current vs Supply Voltage



$V_{OUT} = \text{Midsupply}$ (includes self-heating)

図 26. Short-Circuit Current vs Temperature

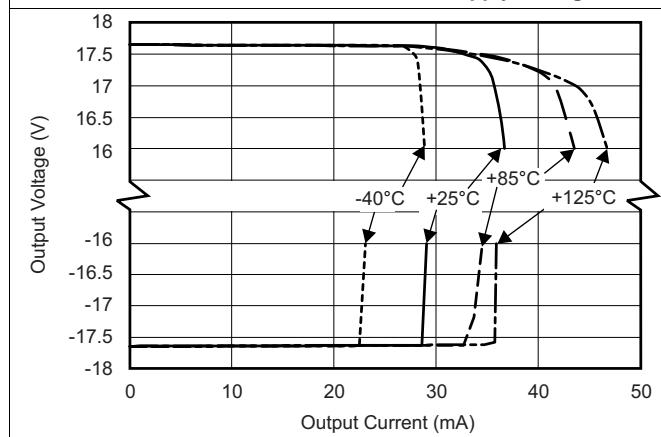


図 27. Output Voltage vs Output Current

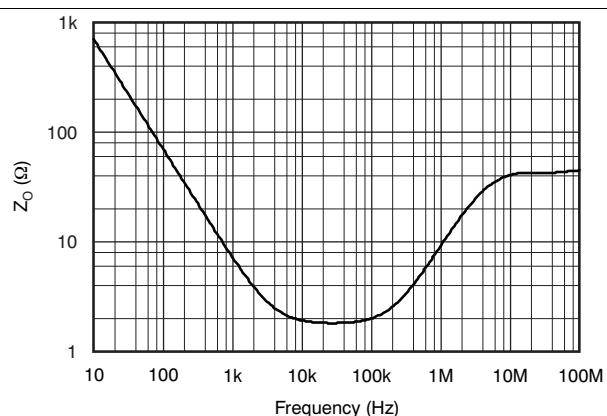


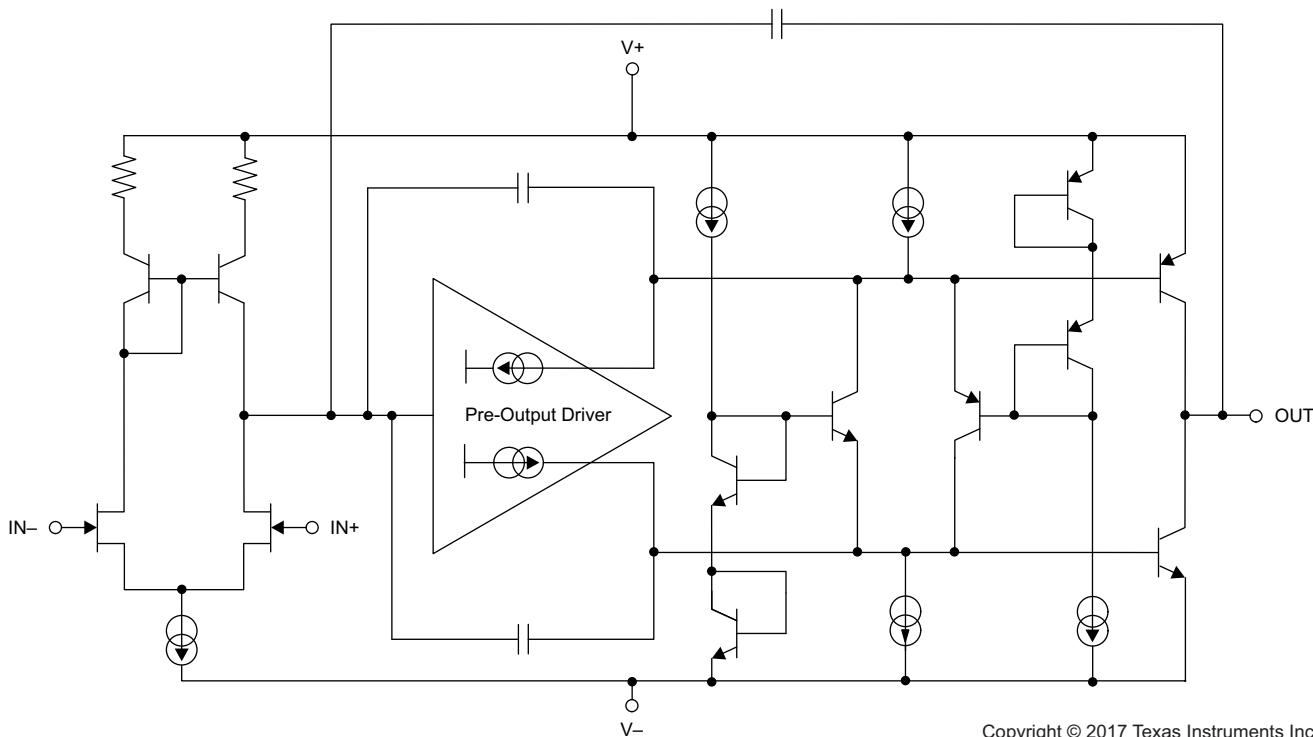
図 28. Open-Loop Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The OPA164x-Q1 family of operational amplifiers combine an ultra-low noise JFET input stage with a rail-to-rail output stage to provide high overall performance in audio applications. The internal topology is selected specifically to deliver extremely low distortion, consume limited power, and accommodate small packages. These amplifiers are well-suited for analog signal processing applications such as active filter circuits, pre-amplifiers, and tone controls. The unique input stage design and semiconductor processes used in this device deliver extremely high performance even in applications with high source impedance and wide common-mode voltage swings.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Phase Reversal Protection

The OPA164x-Q1 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA164x-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in [图 29](#).

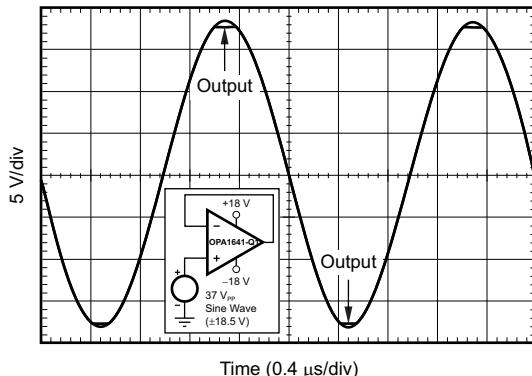


图 29. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

7.3.2 Output Current Limit

The output current of the OPA164x-Q1 series is limited by internal circuitry to 36 mA and -30 mA (sourcing and sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature; see [图 26](#).

Although uncommon for most modern audio applications to require 600- Ω load drive capability, many audio operational amplifier applications continue to specify the total harmonic distortion (THD+N) at 600- Ω load for comparative purposes. [图 7](#) and [图 8](#) provide typical THD+N measurement curves for the OPA164x-Q1 series, where the output drives a 3-V_{RMS} signal into a 600- Ω load. However, correct device operation cannot be ensured when driving 600- Ω loads at full supply. Depending on supply voltage and temperature, this operating condition can possibly trigger the output current limit circuitry of the device.

7.3.3 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report [EMI Rejection Ratio of Operational Amplifiers](#), available for download at www.ti.com.

Feature Description (continued)

The EMIRR IN+ of the OPA164x-Q1 is plotted versus frequency in [图 30](#). If available, any dual and quad operational amplifier device versions have nearly identical EMIRR IN+ performance. The OPA164x-Q1 unity-gain bandwidth is 11 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

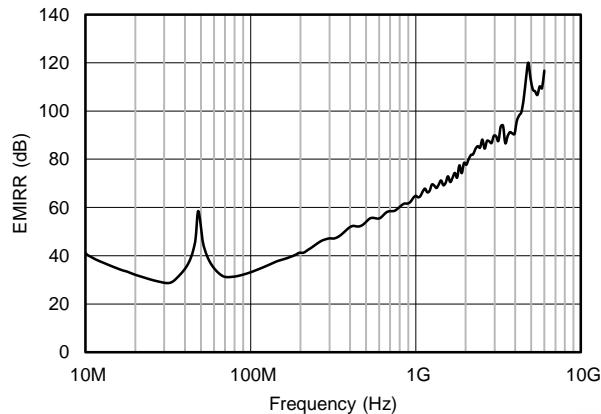


图 30. OPA164x-Q1 EMIRR vs Frequency

[表 1](#) lists the EMIRR IN+ values for the OPA164x-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in [表 1](#) can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

表 1. OPA164x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, UHF	53.1 dB
900 MHz	GSM, radio communication and navigation, GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	72.2 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	80.7 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio and satellite, S-band	86.8 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	91.7 dB
5 GHz	802.11a/n, aero communication and navigation, mobile communication, space and satellite operation, C-band	96.6 dB

7.3.3.1 EMIRR IN+ Test Configuration

図 31 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See [EMI Rejection Ratio of Operational Amplifiers](#) for more details.

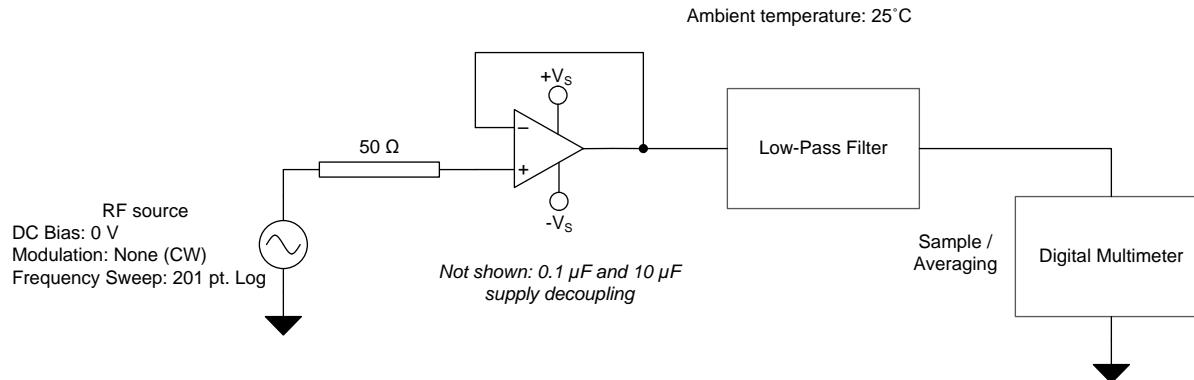


図 31. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

7.4.1 Operating Voltage

The OPA164x-Q1 series of operational amplifiers can be used with single or dual supplies from an operating range of $V_S = 4.5$ V (± 2.25 V) and up to $V_S = 36$ V (± 18 V). These devices do not require symmetrical supplies; only a minimum supply voltage of 4.5 V (± 2.25 V) is required. For V_S less than ± 3.5 V, the common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device; see [Absolute Maximum Ratings](#) for more information. Key parameters are specified over the operating temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Key parameters that vary over the supply voltage or temperature range are shown in [Typical Characteristics](#).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA164x-Q1 amplifiers are unity-gain stable, audio operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, $0.1\text{-}\mu\text{F}$ capacitors are adequate. [図 32](#) shows a simplified schematic of the OPA1641-Q1.

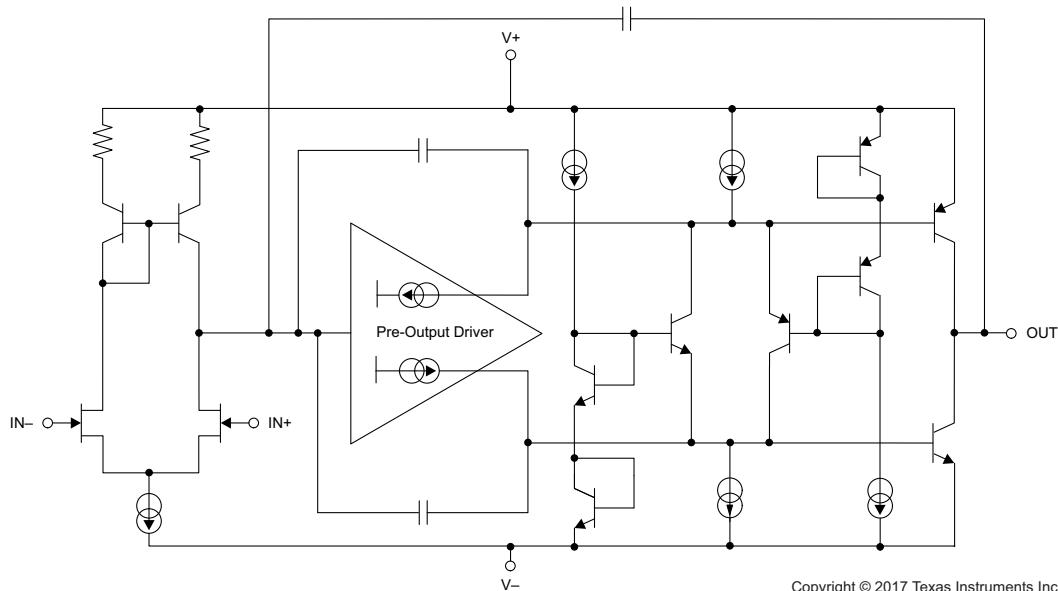


図 32. Simplified Internal Schematic

Application Information (continued)

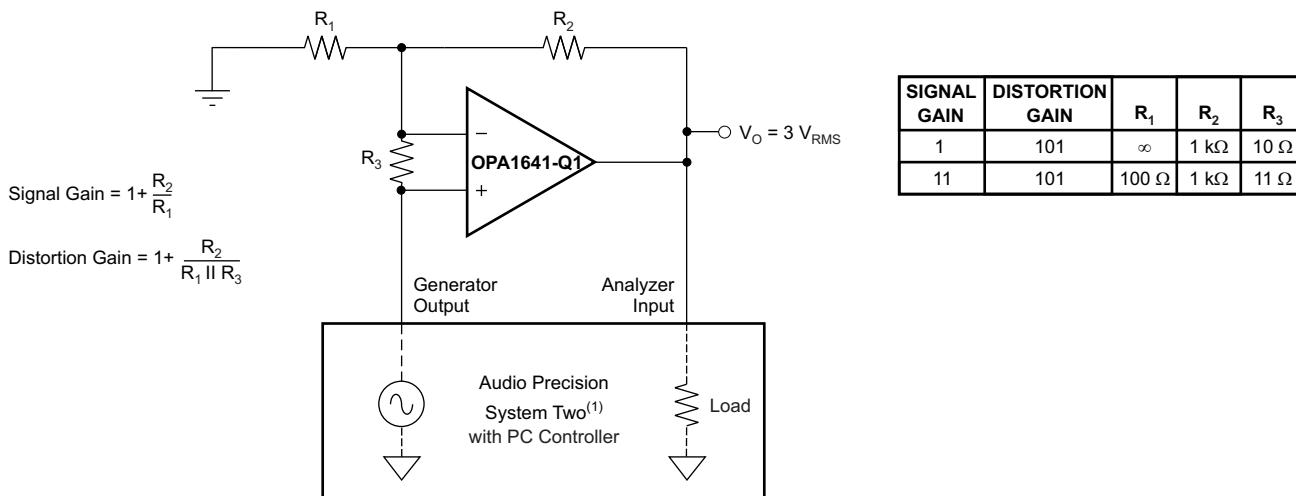
8.1.1 Total Harmonic Distortion Measurements

The OPA164x-Q1 series operational amplifiers have excellent distortion characteristics. THD + noise is below 0.00005% ($G = 1$, $V_O = 3 \text{ V}_{\text{RMS}}$, $\text{BW} = 80 \text{ kHz}$) throughout the audio frequency range, 20 Hz to 20 kHz, with a $2\text{-k}\Omega$ load (see [图 7](#)).

The distortion produced by the OPA164x-Q1 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as shown in [图 33](#)) can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. [图 33](#) shows a circuit that causes the operational amplifier distortion to be 101 times (or approximately 40 dB) greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, extending the resolution by 101. The input signal and load applied to the op amp are the same as with conventional feedback without R_3 . Keep the value of R_3 small to minimize any effect on distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this document were made with an audio precision system two distortion and noise analyzer that greatly simplifies repetitive measurements. However, the measurement technique can be performed with manual distortion measurement instruments.



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(1) For measurement bandwidth, see [图 7](#) through [图 10](#).

图 33. Distortion Test Circuit

8.1.2 Source Impedance and Distortion

In traditional JFET-input op amps, the impedance applied to the positive and negative inputs in noninverting applications must be matched for lowest distortion. Legacy methods for fabricating the JFETs in the FET input stage exhibit a varying input capacitance with applied common-mode input voltage. In inverting configurations, the input does not vary with input voltage because the inverting input is held at virtual ground. However, in noninverting applications, the inputs do vary, and the gate-to-source voltage is not constant. This effect produces increased distortion resulting from the varying capacitance for unmatched source impedances. However, the OPA164x-Q1 family of amplifiers is designed to maintain a constant input capacitance with varying common-mode voltage to prevent this mechanism of distortion. The variation of input capacitance with common-mode voltage for a traditional amplifier is compared to the OPA164x-Q1 family in [图 34](#).

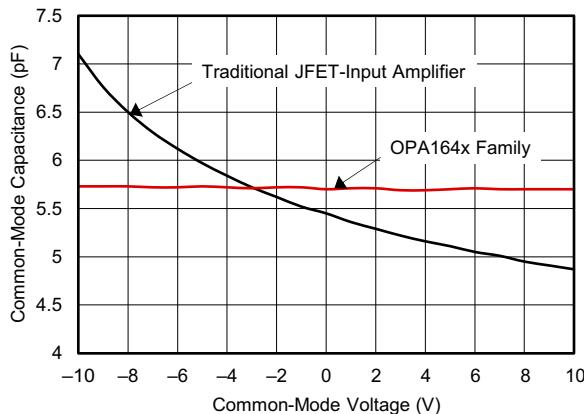


图 34. Input Capacitance of the OPA164x-Q1 Family of Amplifiers Compared to Traditional JFET-input Amplifiers

By stabilizing the input capacitance, the distortion performance of the amplifier is greatly improved for noninverting configurations with high source impedances. The measured performance of an OPA164x-Q1 amplifier is compared to a traditional JFET-input amplifier in **图 35**. The unity-gain configuration, high source impedance, and large-signal amplitude produce additional distortion in the traditional amplifier.

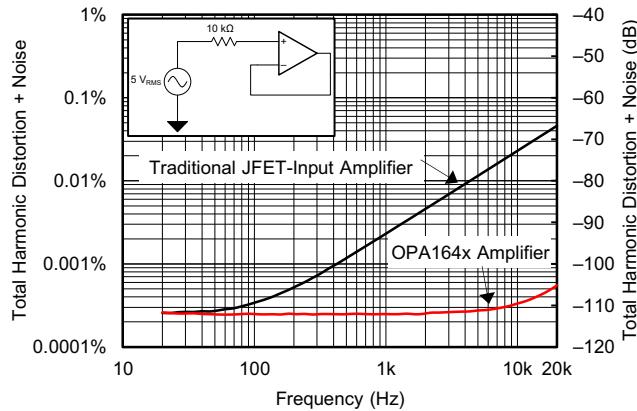


图 35. Measured THD+N of the OPA164x-Q1 Family of Amplifiers Compared to Traditional JFET-input Amplifiers

8.1.3 Capacitive Load and Stability

The dynamic characteristics of the OPA164x-Q1 are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω , for example) in series with the output.

图 19 and **图 20** illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT} . For details of analysis techniques and application circuits, see [see *Feedback Plots Define Op Amp AC Performance*](http://www.ti.com) available for download at www.ti.com

8.1.4 Power Dissipation and Thermal Protection

The OPA164x-Q1 op amps are capable of driving 2-k Ω loads with power-supply voltages of up to ± 18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8 k Ω at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance can be used, as long as the output current does not exceed 13 mA; otherwise, the device short-circuit current-protection circuit can activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA164x-Q1 series of devices improves heat dissipation compared to conventional materials. PCB layout can help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by functioning as an additional heat sink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to midsupply, the typical short-circuit current of 36 mA leads to an internal power dissipation of over 600 mW at a supply of ± 18 V. In case of a dual OPA1642-Q1 in an VSSOP-8 package (thermal resistance $R_{\theta,JA} = 180^{\circ}\text{C}/\text{W}$), such a power dissipation results in the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase destroys the device.

To prevent such excessive heating that can destroy the device, the OPA164x-Q1 series has an internal thermal shutdown circuit that shuts down the device if the die temperature exceeds approximately 180°C . When this thermal shutdown circuit activates, a built-in hysteresis of 15°C ensures that the die temperature must drop to approximately 165°C before the device switches on again.

8.1.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. [图 36](#) illustrates the ESD circuits contained in the OPA164x-Q1 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines where an internal absorption device is connected. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger (or threshold voltage) that is above the normal operating voltage of the OPA164x-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

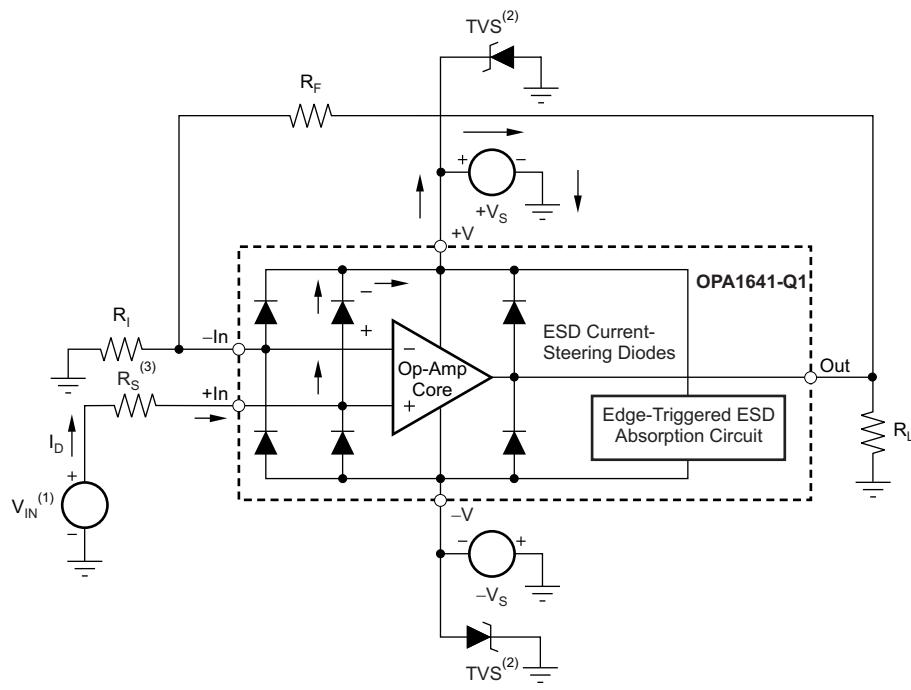
When the operational amplifier connects into a circuit as shown in [图 36](#), the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, some of the internal ESD protection circuits can be biased on and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

[图 36](#) depicts a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies $+V_S$ and $-V_S$ are at 0 V. The amplifier behavior depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes can be added to the supply pins, as shown in [图 36](#). The Zener voltage must be selected so the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



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(1) $V_{IN} = +V_S + 500$ mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR (Min)} > +V_S$

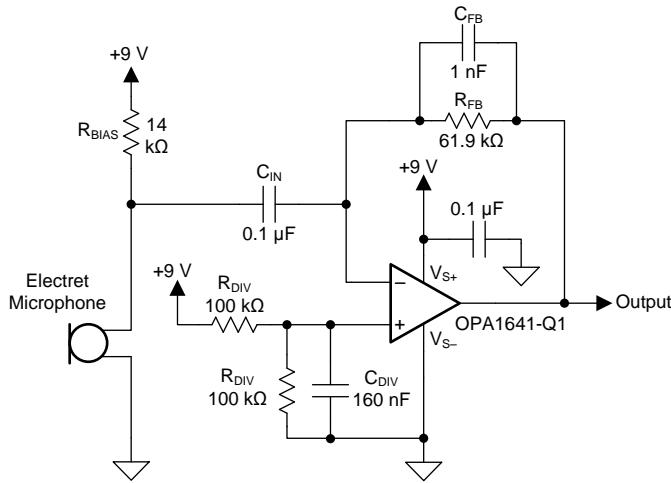
(3) Suggested value is approximately 1 k Ω .

图 36. Equivalent Internal ESD Circuitry and the Relation to a Typical Circuit Application

8.2 Typical Application

8.2.1 Single-Supply Electret Microphone Preamplifier for Speech

Electret microphones are commonly used in automotive hands-free phone systems because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The low noise and distortion of the OPA1641-Q1 makes the device a good choice for preamplifier circuits for electret microphones. The circuit shown in [図 37](#) is a single-supply preamplifier circuit for electret microphones with a bandwidth from 100 Hz to 3 kHz for capturing speech.



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図 37. Preamplifier Circuit for Electret Microphones Using a Single Power Supply Voltage

8.2.1.1 Design Requirements

- 9-V single supply
- 1-V_{RMS} output for 100-dB_{SPL} input
- Approximately 100-Hz to 3-kHz, -3-dB Bandwidth
- Microphone sensitivity: 8 μA / Pa
- Microphone operating voltage: 2 V to 10 V
- Microphone bias current: 500 μA

8.2.1.2 Detailed Design Procedure

In this circuit, the op amp is configured as a transimpedance amplifier which converts the signal current of the microphone into an output voltage. The bandwidth of this circuit is limited to the vocal range as is common in telephony systems. The gain of the circuit is determined by the feedback resistor (R_{FB}), which must be calculated according to the microphone sensitivity. For this design, a microphone output current of 8 μA per Pascal (Pa) of air pressure was selected. Using this value, the output current for a sound pressure level of 100 dB_{SPL}, or 2 Pa air pressure, is calculated in [式 1](#).

$$i_{\text{mic}} = \frac{8 \mu\text{A}}{1 \text{ Pa}} \times 2 \text{ Pa} = 16 \mu\text{A} \quad (1)$$

R_{FB} is then calculated from this current to produce 1-V_{RMS} output for a 100-dB_{SPL} input signal in [式 2](#).

$$R_{FB} = \frac{V_O}{i_{\text{mic}}} = \frac{1 \text{ V}_{\text{RMS}}}{16 \mu\text{A}} = 62500 \rightarrow 61.9 \text{ k}\Omega \quad (2)$$

The feedback capacitor (C_{FB}) is calculated to limit the bandwidth of the amplifier to 3 kHz in [式 3](#).

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot R_{FB} \cdot f_H} = \frac{1}{2 \cdot \pi \cdot (61.9 \text{ k}\Omega) \cdot (3 \text{ kHz})} = 857 \times 10^{-12} \rightarrow 1 \text{ nF} \quad (3)$$

Typical Application (continued)

R_{BIAS} is necessary to divert the microphone signal current through capacitor C_{IN} rather than flowing from the power supply (V_{CC}). Larger values of R_{BIAS} allow for a smaller capacitor to be used for C_{IN} and reduces the overall noise of the circuit. However, the maximum value for R_{BIAS} is limited by the microphone bias current and minimum operating voltage.

The value of R_{BIAS} is calculated in 式 4.

$$R_{BIAS} = \frac{V_{CC} - V_{MIC}}{I_{BIAS}} = \frac{9 \text{ V} - 2 \text{ V}}{500 \mu\text{A}} = 14 \text{ k}\Omega \quad (4)$$

Input capacitor C_{IN} forms a high-pass filter in combination with resistor R_{BIAS} . The filter corner frequency calculation is shown in 式 5 to place the high-pass corner frequency at 100 Hz.

$$C_{IN} = \frac{1}{2 \cdot \pi \cdot R_{BIAS} \cdot f_L} = \frac{1}{2 \cdot \pi \cdot (14 \text{ k}\Omega) \cdot (100 \text{ Hz})} = 113.7 \times 10^{-9} \rightarrow 100 \text{ nF} \quad (5)$$

The voltage divider network at the op amp noninverting input is used to bias the op amp output to the midsupply point ($V_{CC} / 2$) to maximize the output voltage range of the circuit. This result is easily achieved by selecting the same value for both resistors in the divider. The absolute value of those resistors is limited by the acceptable power-supply current drawn by the voltage divider. Choosing 50 μA as an acceptable limit of supply current gives a value of 100 $\text{k}\Omega$ for the resistors in the divider, as 式 6 shows.

$$R_{DIV} \geq \frac{V_{CC}}{2 \cdot I_{DIV}} \geq \frac{9 \text{ V}}{2 \cdot 50 \mu\text{A}} \geq 90 \text{ k}\Omega \rightarrow 100 \text{ k}\Omega \quad (6)$$

Finally, to minimize the additional noise contribution from the voltage divider, a capacitor is placed at the op amp noninverting input. This capacitor forms a low-pass filter with the parallel combination of the voltage divider resistors. Selecting a filter corner frequency of 20 Hz minimizes the noise contribution of the voltage divider inside the amplifier passband; see 式 7.

$$C_{DIV} = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{DIV}}{2} \right) \cdot f_L} = \frac{1}{2 \cdot \pi \cdot \left(\frac{100 \text{ k}\Omega}{2} \right) \cdot (20 \text{ Hz})} = 1.592 \times 10^{-7} \rightarrow 160 \text{ nF} \quad (7)$$

Typical Application (continued)

8.2.1.3 Application Curve

The transfer function of the microphone preamplifier circuit is shown in [図 38](#). The nominal gain of the circuit is 95.46 dB, or 59,292.5 V per amp of input current. The –3-dB bandwidth limits of the circuit are 105.7 Hz and 2.77 kHz.

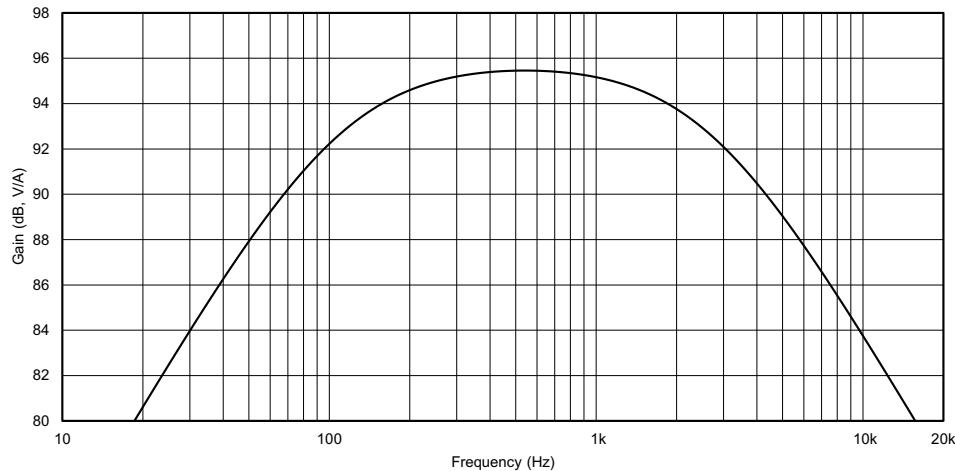


図 38. Microphone Preamplifier Transfer Function

9 Power Supply Recommendations

The OPA164x-Q1 devices are specified for operation from 4.5 V to 36 V (± 2.25 V to ± 18 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Typical Characteristics](#).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in [图 39](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

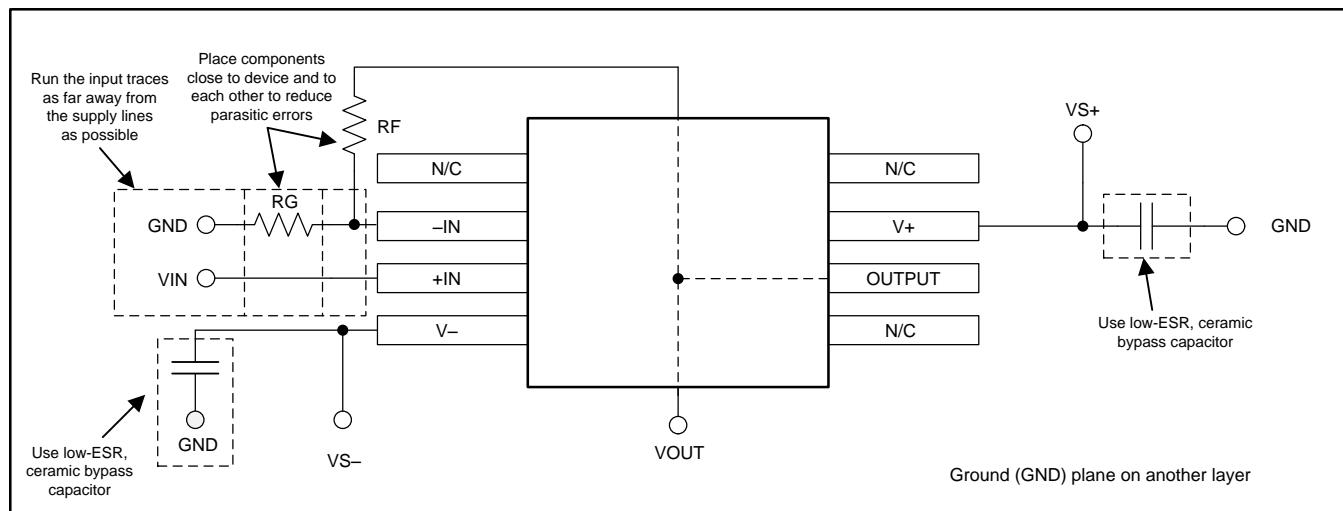
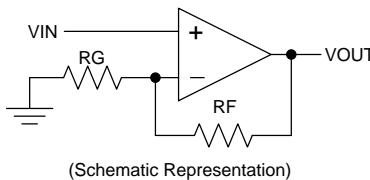


图 39. OPA1641-Q1 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINA-TIソフトウェアのフル機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクリック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™ 製) または TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI フォルダから、無料の TINA-TI ソフトウェアをダウンロードしてください。

11.1.1.2 TI Precision Designs

TI Precision Designsは、<http://www.ti.com/ww/en/analog/precision-designs/>からオンラインで入手できます。TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerにより、TIのオペアンプと、TIのベンダ・パートナーの受動部品を選択して、最適化されたフィルタを設計できます。

WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、完全な多段アクティブ・フィルタ・ソリューションの設計、最適化、シミュレーションを、わずか数分で実行できます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- 『オペアンプのゲイン安定性、第3部: ACゲイン誤差の解析』
- 『オペアンプのゲイン安定性、第2部: DCゲイン誤差の解析』
- 『完全差動アクティブ・フィルタにおける無限ゲイン、MFBフィルタ・トポロジの使用』
- 『オペアンプの性能分析』
- 『オペアンプの単一電源動作』
- 『アンプのチューニング』
- 『鉛フリー部品仕上げの保存寿命評価』

11.3 関連リンク

表 2 に、クリック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクリック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA1641-Q1	ここをクリック				
OPA1642-Q1	ここをクリック				

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer)* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てるることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.6 商標

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TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

 静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.8 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあります。ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1641AQDGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1641
OPA1641AQDGKRQ1.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1641
OPA1642AQDGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1642
OPA1642AQDGKRQ1.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1642

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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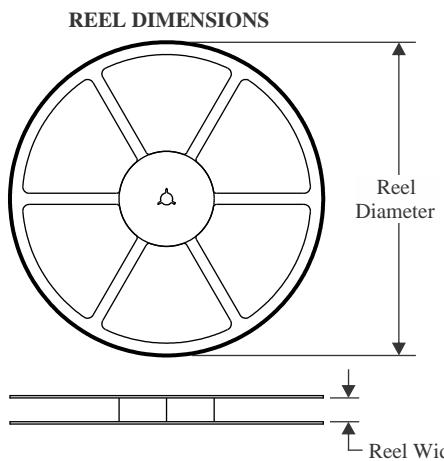
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA1641-Q1, OPA1642-Q1 :

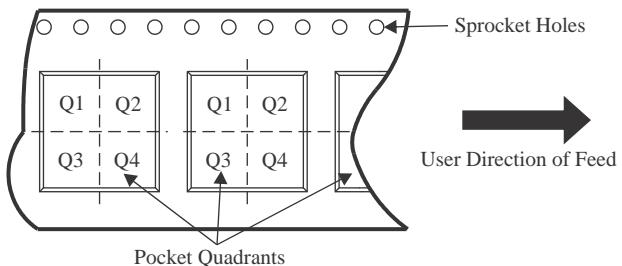
- Catalog : [OPA1641](#), [OPA1642](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

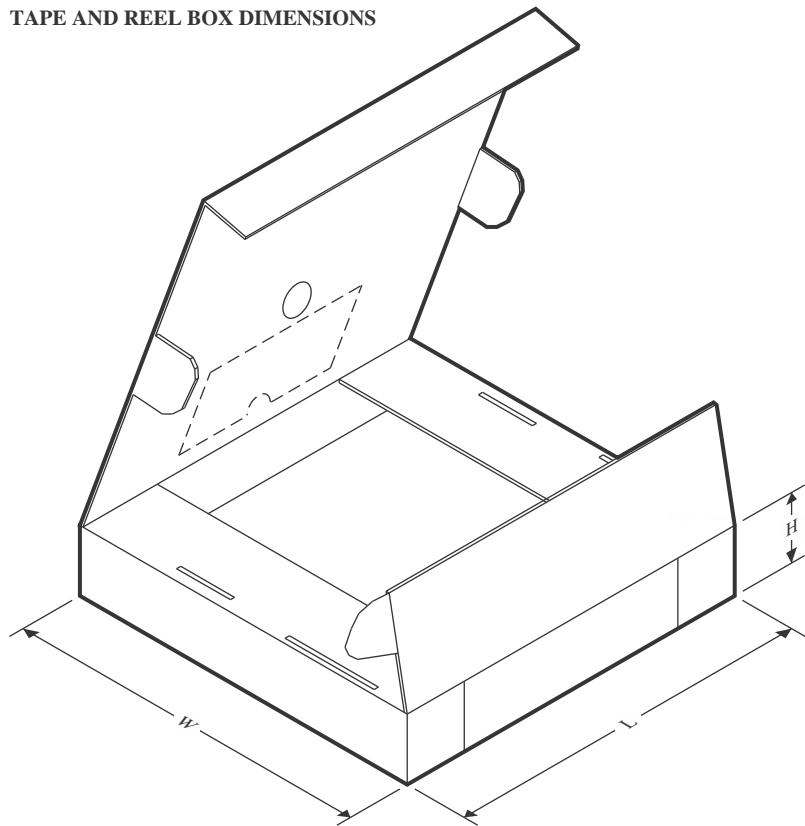
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1641AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1641AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA1642AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

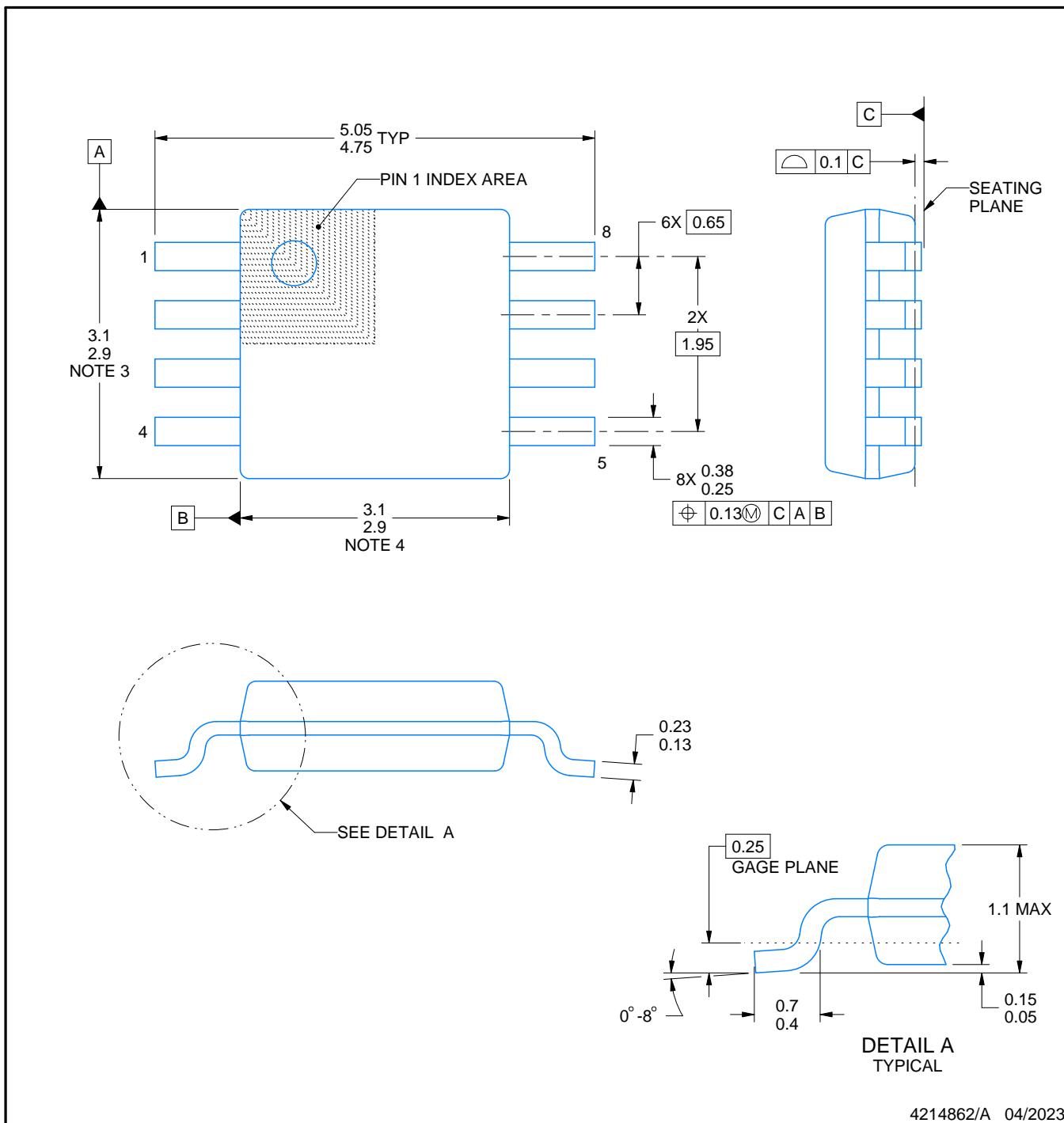
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

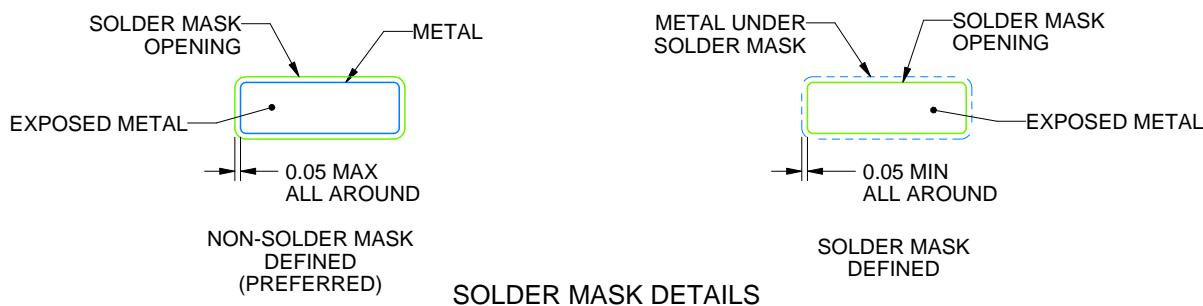
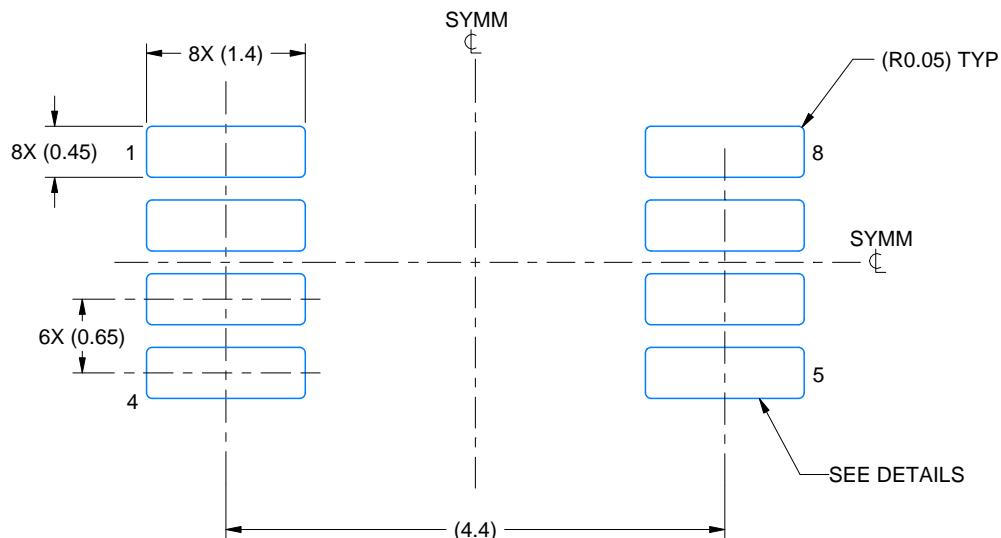
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES: (continued)

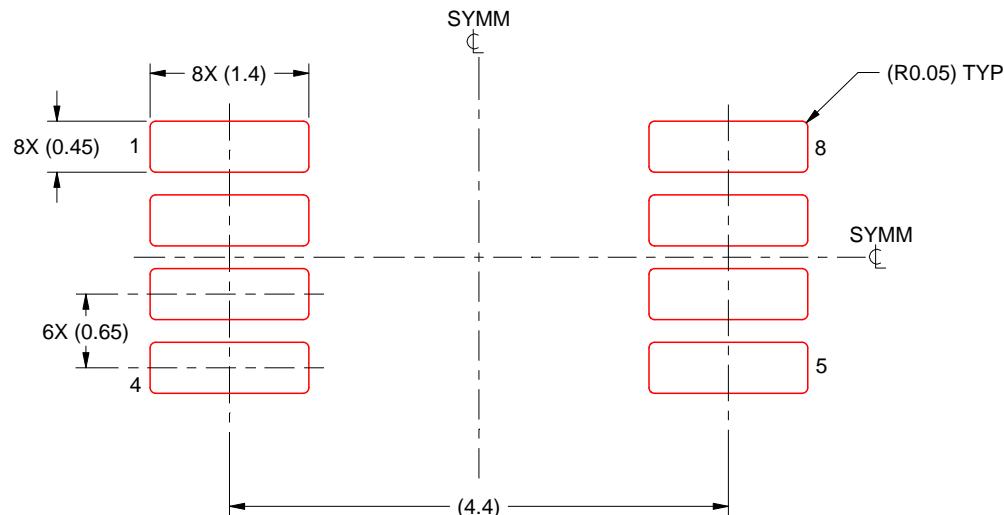
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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