

OPA1671 13MHz、低ノイズ、レール・ツー・レールのオーディオ・オペアンプ



1 特長

- 低ノイズ：
 - $4\text{nV}/\sqrt{\text{Hz}}$ (10kHz 時)
 - $4.7\text{fA}/\sqrt{\text{Hz}}$ (1kHz 時)
- 低歪み：-109dB (0.00035%)
- 広いゲイン帯域幅：13MHz
- レール・ツー・レール入出力
- 低電源電圧動作：1.7V~5.5V
- 低い入力容量
 - 差動: 6pF
 - 同相: 2.5pF
- 低入力バイアス電流：10pA
- 低消費電流：940 μA
- 業界標準パッケージ：SC-70 および SOT-23

2 アプリケーション

- マイク・プリアンプ
- 補助ライン入出力
- アクティブ・フィルタ回路
- トランスインピーダンス・アンプ
- 電圧バッファ

3 概要

OPA1671は広帯域幅、低ノイズ、低歪みのオーディオ・オペアンプで、レール・ツー・レール入出力に対応しています。電圧ノイズ、電流ノイズ、入力容量がいずれも低いため、幅広いオーディオおよび産業用途で高性能を実現します。OPA1671の独自の内部トポロジにより、歪みが極めて小さく(-109dB)、消費電流はわずか940 μA です。帯域幅が広く(13MHz)、スルーレートが高い(5V/ μs)ため、高ゲイン・オーディオおよび産業用信号コンディショニングに最適です。

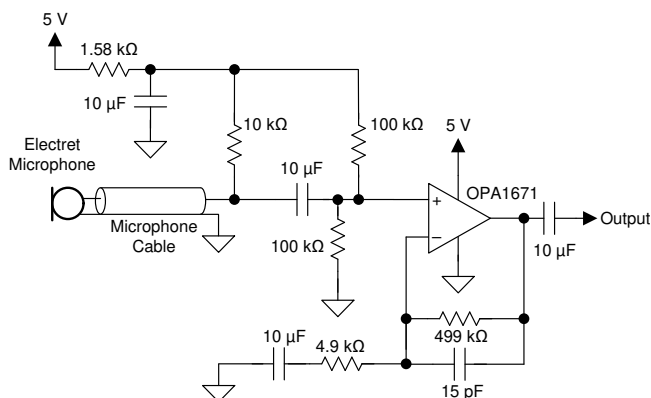
OPA1671はSC-70およびSOT-23パッケージで供給され、産業温度範囲(-40 $^{\circ}\text{C}$ ~+125 $^{\circ}\text{C}$)で仕様が規定されています。

製品情報⁽¹⁾

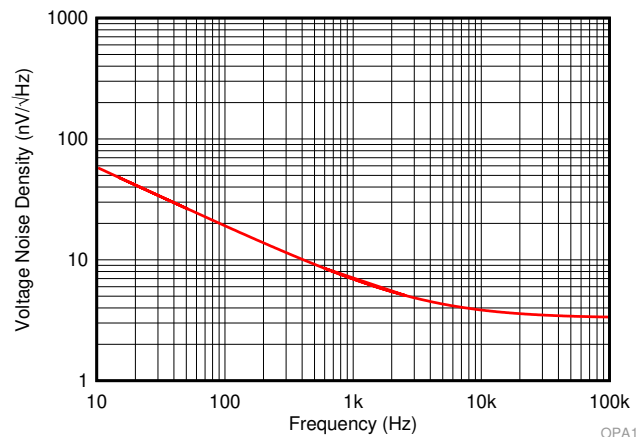
型番	パッケージ	本体サイズ(公称)
OPA1671	SC-70 (5)	2.00mm×1.25mm
	SOT-23 (5)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

エレクトレット・マイク・プリアンプ



OPA1671の電圧ノイズ密度



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4 改訂履歴

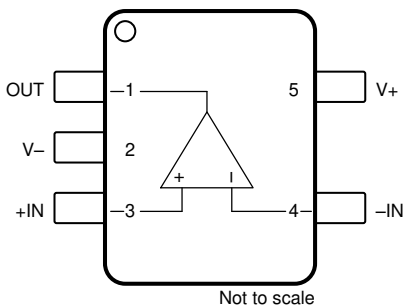
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (January 2019) から Revision B に変更	Page
• SOT-23 (DBV) パッケージと関連情報をデータシートに追加	1
• Added input offset voltage specification for $V_{CM} = (V+), (V-)$	5

2018年11月発行のものから更新	Page
• 事前情報 (プレビュー) から量産データ (アクティブ) に変更	1

5 Pin Configuration and Functions

**DBV and DCK Packages
5-Pin SOT-23 and SC-70
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V-	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		6	V
Input voltage	(V-) -0.3	(V+) +0.3	V
Output short-circuit ⁽²⁾	Continuous		
Operating temperature, T_A	-55	150	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$	1.7 (± 0.85)		5.5 (± 2.75)	V
Specified temperature, T_A	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA1671		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	214.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.4	127.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	60.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	33.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	59.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $V_S = \pm 0.85\text{ V}$ to $\pm 2.75\text{ V}$ ($V_S = 1.7\text{ V}$ to 5.5 V), $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
AUDIO PERFORMANCE								
THD+N	Total harmonic distortion + noise	$G = 1$, $f = 1\text{ kHz}$, $V_O = 1\text{ V}_{RMS}$, $V_S = 5.5\text{ V}$		0.00035%				
					-109		dB	
IMD	Intermodulation distortion	$G = 1$, $V_O = 1\text{ V}_{RMS}$, $V_S = 5.5\text{ V}$	SMPTE/DIN Two-Tone, 4:1, (60 Hz and 7 kHz)	0.00158%				
					-96		dB	
				0.0005%				
			CCIF Two-Tone (19 kHz and 20 kHz)		-106		dB	
FREQUENCY RESPONSE								
GBW	Gain-bandwidth product			13			MHz	
SR	Slew rate	4-V step, $G = 1$		5			V/ μs	
t_S	Settling time	T_O 0.1%, 2-V step, $G = 1$		0.75			μs	
		T_O 0.01%, 2-V step, $G = 1$		1				
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$		0.35			μs	
NOISE								
	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		2.4			μV_{PP}	
e_N	Input voltage noise density	$f = 10\text{ Hz}$		45			$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$		7				
		$f = 10\text{ kHz}$		4.0				
i_N	Input current noise	$f = 1\text{ kHz}$		4.7			$\text{fA}/\sqrt{\text{Hz}}$	
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	$V_{CM} = (V+)$				± 1.6	mV	
		$V_{CM} = (V-)$				± 1.6		
		$T_A = -40^\circ\text{C}$ to 125°C				± 0.25		± 1.25
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to 125°C				± 0.3	± 2.2	
PSRR	Input offset voltage versus power supply	$V_{CM} = (V-)$				± 30	± 130	
INPUT BIAS CURRENT								
I_B	Input bias current					± 10	pA	
I_{OS}	Input offset current					± 10		
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range			V-		V+	V	
CMRR	Common-mode rejection ratio	$V_S = 1.7\text{ V}$, $(V-) < V_{CM} < (V+) - 1.25\text{ V}$		74	91		dB	
		$V_S = 5.5\text{ V}$, $(V-) < V_{CM} < (V+) - 1.25\text{ V}$		80	96			
		$V_S = 1.7\text{ V}$, $V_{CM} = 0\text{ V}$ to 1.7 V		60	88			
		$V_S = 5.5\text{ V}$, $V_{CM} = 0\text{ V}$ to 5.5 V		68	102			
INPUT CAPACITANCE								
Z_{ID}	Differential			$10^{13} \parallel 6$			$\text{M}\Omega \parallel \text{pF}$	
Z_{ICM}	Common-mode			$10^{13} \parallel 2.5$			$\text{G}\Omega \parallel \text{pF}$	
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$(V-) + 50\text{ mV} < V_O < (V+) - 50\text{ mV}$, $R_L = 10\text{ k}\Omega$				97	113	dB
				$T_A = -40^\circ\text{C}$ to 125°C				
		$(V-) + 200\text{ mV} < V_O < (V+) - 200\text{ mV}$, $R_L = 2\text{ k}\Omega$				97	112	
				$T_A = -40^\circ\text{C}$ to 125°C				

Electrical Characteristics (continued)

at $V_S = \pm 0.85\text{ V}$ to $\pm 2.75\text{ V}$ ($V_S = 1.7\text{ V}$ to 5.5 V), $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	$V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$		10	20	mV
I_{SC}	Short-circuit current	Sinking, $V_S = 5.5\text{ V}$		-57		mA
		Sourcing, $V_S = 5.5\text{ V}$		66		
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$I_O = 0\text{ mA}$		0.94	1.3	mA
		$I_O = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to 125°C			1.4	

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.5\text{ V}$, $V_{CM} = V_S / 2$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

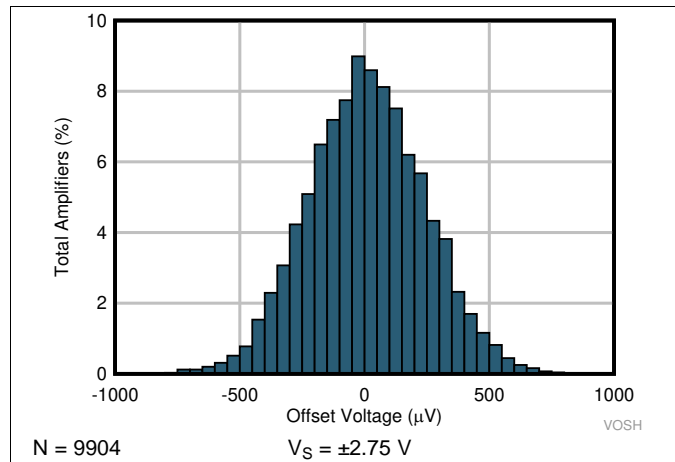


图 1. Offset Voltage Production Distribution

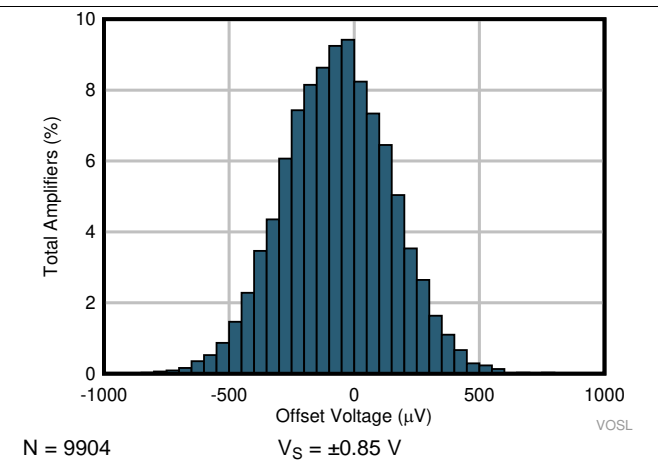


图 2. Offset Voltage Production Distribution

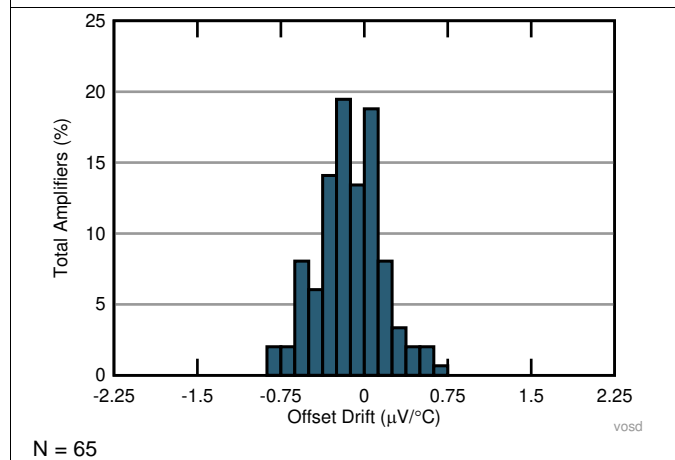


图 3. Offset Voltage Drift Distribution

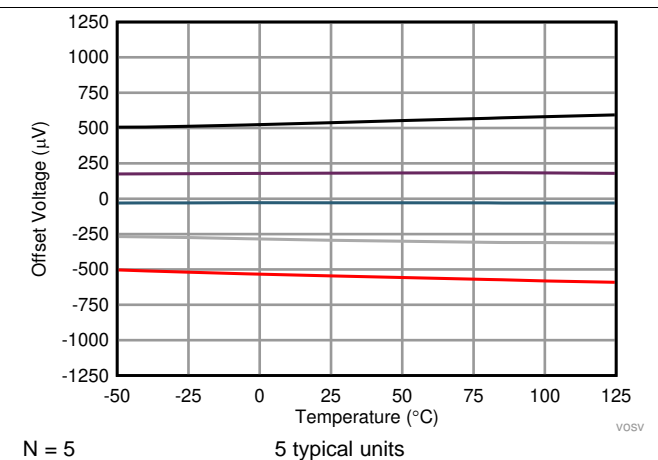


图 4. Offset Voltage vs Temperature

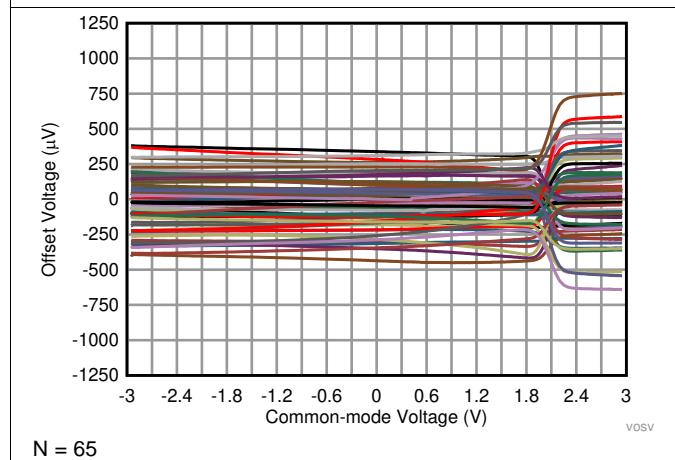


图 5. Offset Voltage vs Common Mode Voltage

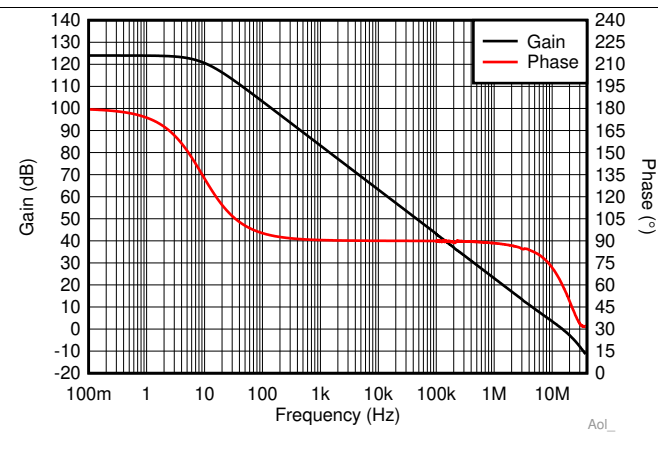
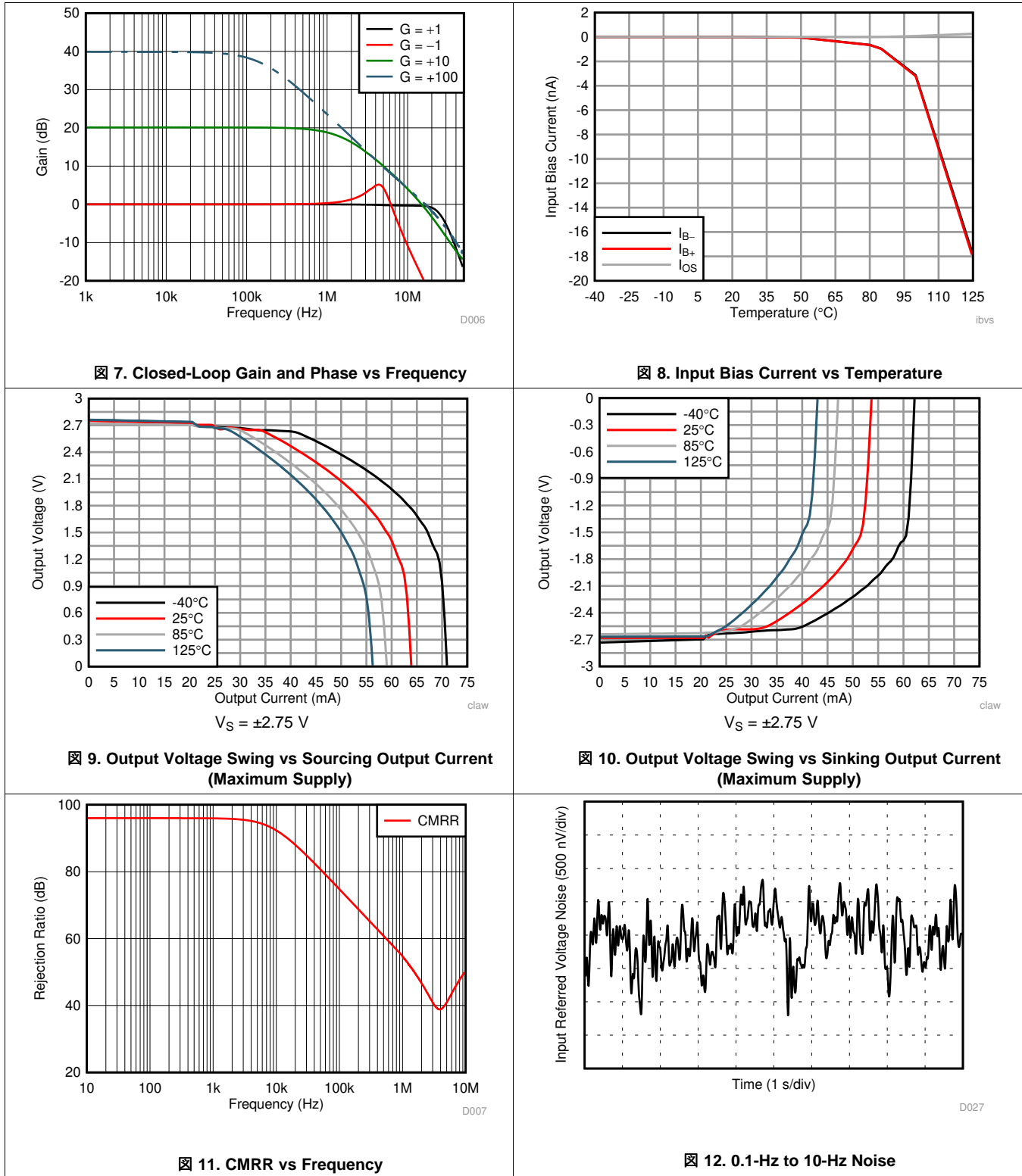


图 6. Open-Loop Gain and Phase vs Frequency

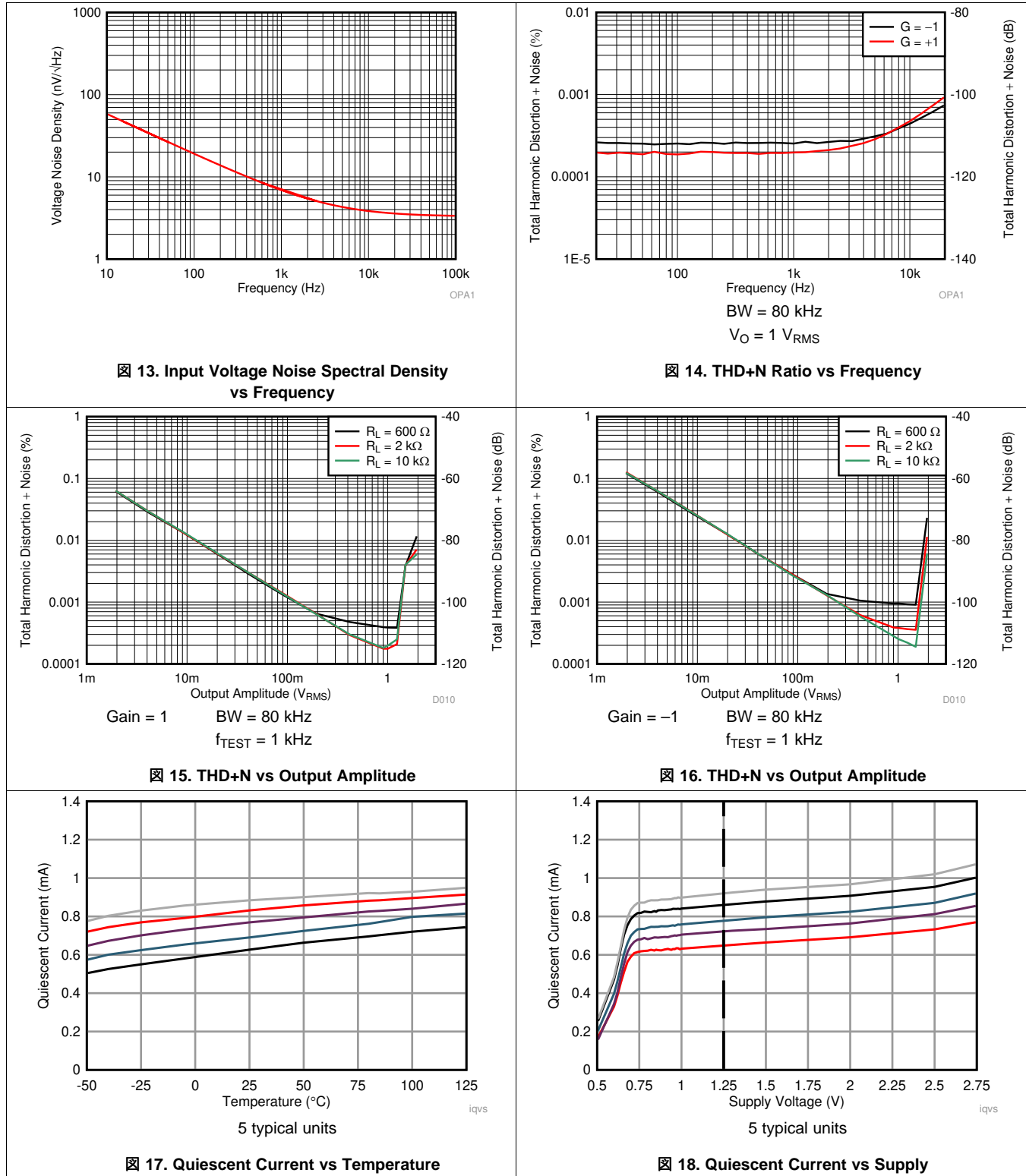
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.5\text{ V}$, $V_{CM} = V_S / 2$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)



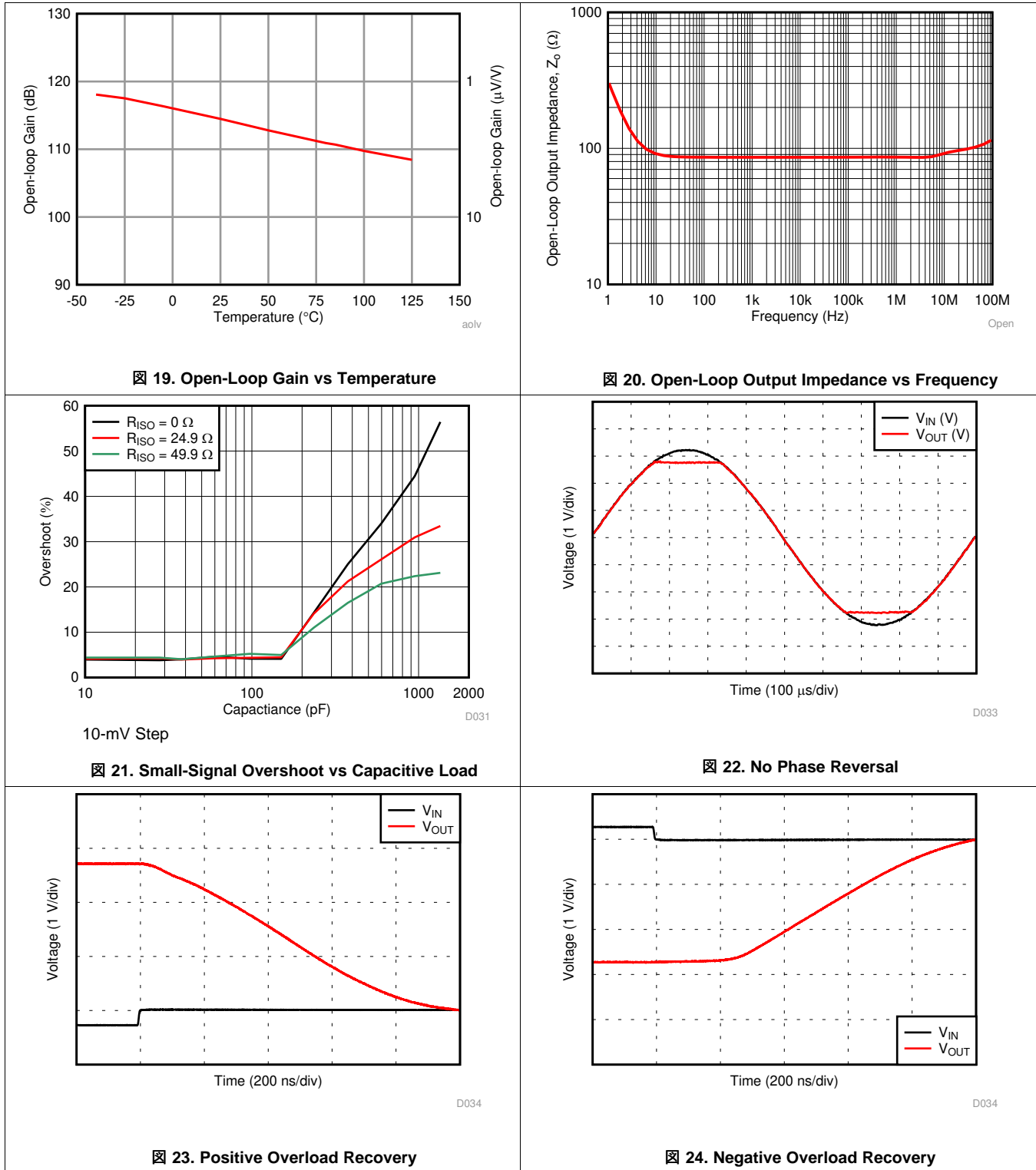
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.5\text{ V}$, $V_{CM} = V_S / 2$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)



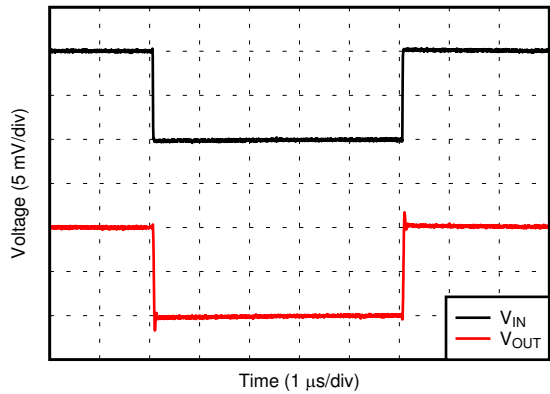
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.5\text{ V}$, $V_{CM} = V_S / 2$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)



Typical Characteristics (continued)

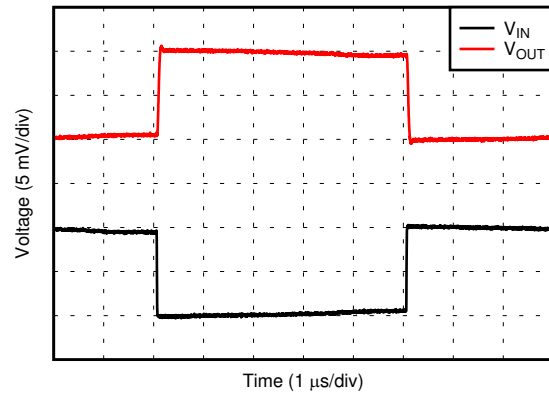
at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.5\text{ V}$, $V_{CM} = V_S / 2$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)



10-mV step $G = +1$

D035

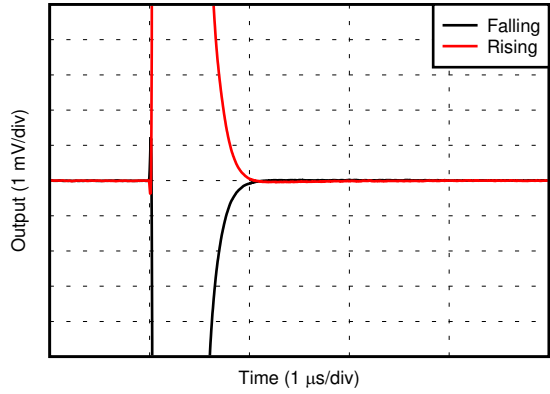
⊗ 25. Small-Signal Step Response



10-mV step $G = -1$

D035

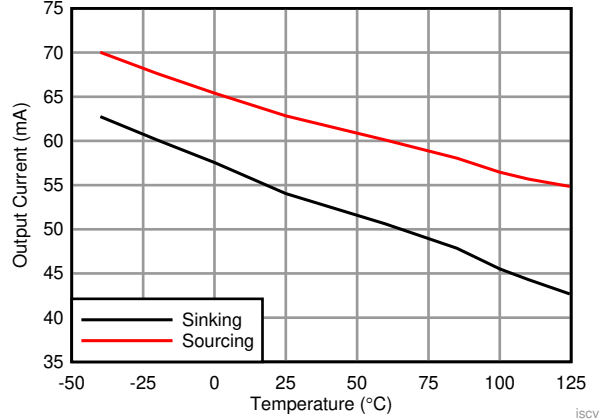
⊗ 26. Small-Signal Step Response



2-V Step

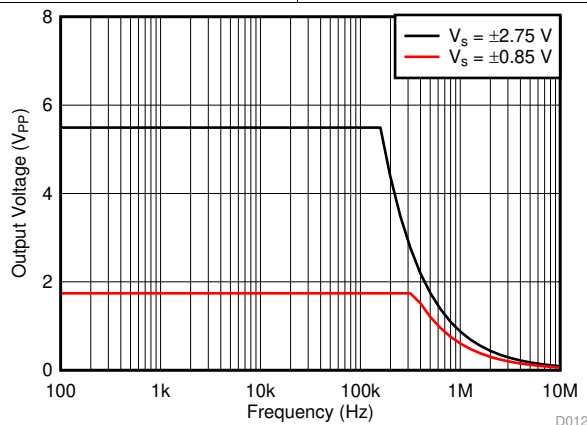
D037

⊗ 27. Settling Time



iscv

⊗ 28. Short-Circuit Current vs Temperature



D012

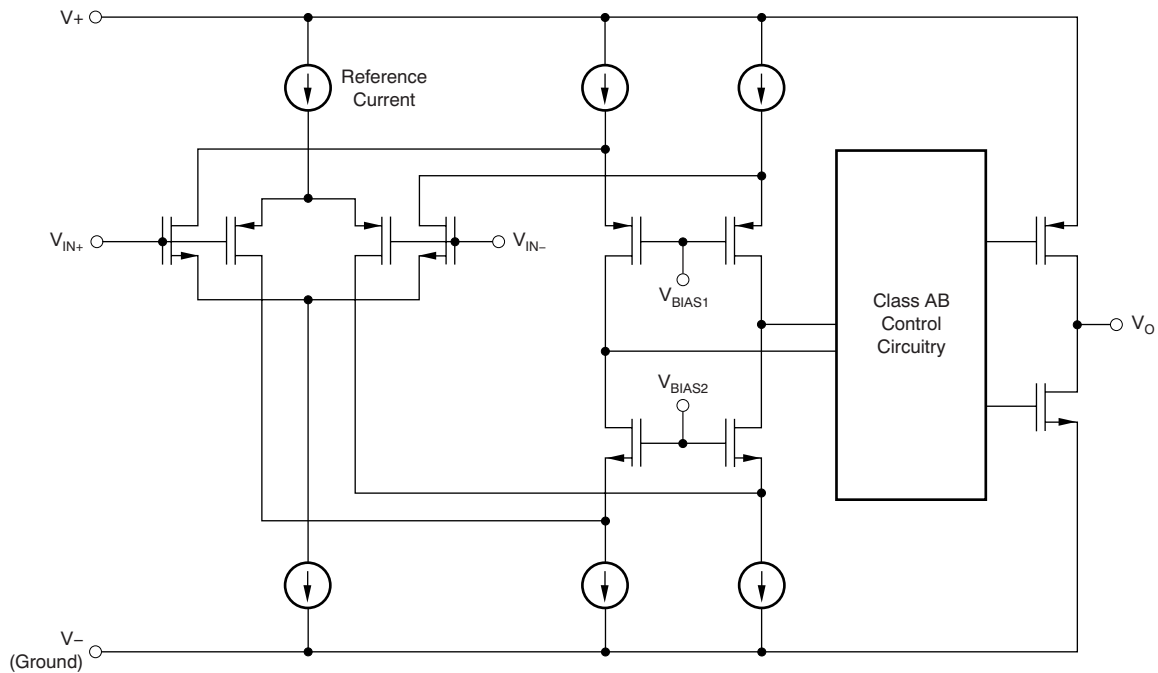
⊗ 29. Maximum Output Voltage vs Frequency

7 Detailed Description

7.1 Overview

The OPA1671 is a rail-to-rail input, very low noise operational amplifier (op amp). The OPA1671 operates from 1.7 V to 5.5 V, is unity-gain stable, and is designed for a wide range of audio and general-purpose applications. The OPA1671 strengths also include 13-MHz bandwidth and 4.0-nV/ $\sqrt{\text{Hz}}$ noise spectral density, with very low input bias current (10 pA). These strengths make the OPA1671 a great choice for a preamplifier in microphone circuits, sensor modules and buffering high-fidelity, digital-to-analog converters (DACs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA1671 op amp can be used with single or dual supplies from an operating range of $V_S = 1.7\text{ V}$ ($\pm 0.85\text{ V}$) up to 5.5 V ($\pm 2.75\text{ V}$).

注意

Supply voltages greater than 6 V can permanently damage the device (see [Absolute Maximum Ratings](#))

Key parameters that vary over the supply voltage or temperature range are shown in the [Typical Characteristics](#) section.

7.3.2 Input Bias Current

Typically, input bias current is approximately $\pm 10\text{ pA}$. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA . This limitation is easily accomplished with an input resistor, as shown in [Figure 30](#).

Unlike many operational amplifiers, there are no diodes connected between the positive and negative input terminals. As a result, differential voltages up to the full supply voltage do not cause any significantly higher current flow into the inputs.

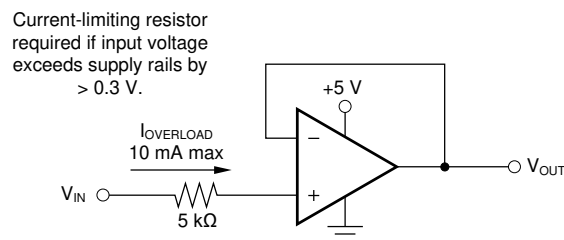


Figure 30. Input Current Protection

7.3.3 Common-Mode Voltage Range

The OPA1671 features true rail-to-rail inputs, allowing full common mode operation from the negative supply voltage to the positive supply voltage. This full common mode operation is achieved with complimentary N-channel and P-channel differential input pairs. The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.25\text{ V}$ to $(V+)$. The P-channel is active for common-mode inputs from $(V-)$ to $(V+) - 1.25\text{ V}$. There is a small transition region, typically from $(V+) - 1.25\text{ V}$ to $(V+) - 1\text{ V}$. In this region, the offset voltage transitions between the P-channel and N-channel offset values. [Figure 5](#) shows the difference between offset in the P and N regions.

Feature Description (continued)

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA1671 operational amplifier incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20 MHz (–3 dB), with a rolloff of 20 dB per decade.

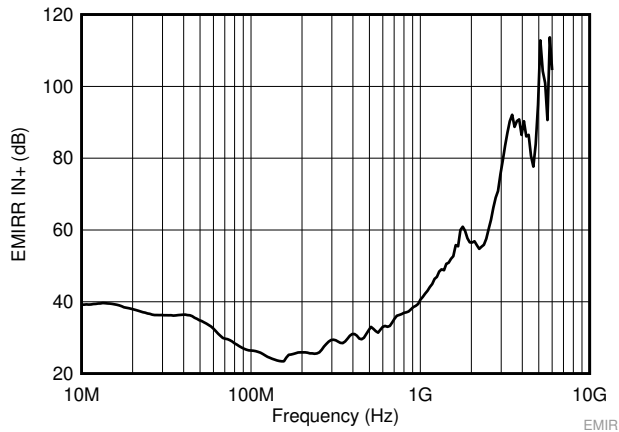


图 31. OPA1671 EMIRR vs Frequency

表 1. OPA1671 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	30 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	38 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	60 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	59 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	90 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	100 dB

7.4 Device Functional Modes

The OPA1671 has a single functional mode and is operational when the power-supply voltage is greater than 1.7 V (± 0.85 V). The maximum specified power-supply voltage for the OPA1671 is 5.5 V (± 2.75 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA1671 is a low-noise, rail-to-rail input and output operational amplifier specifically designed for portable applications. The device operates from 1.7 V to 5.5 V, is unity-gain stable, and suitable for a wide range of audio and general-purpose applications. The class AB output stage is capable of driving $\leq 10\text{-k}\Omega$ loads connected to any point between $V+$ and ground. The input common-mode voltage range includes both rails, and allows the OPA1671 device to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device a great choice for driving sampling analog-to-digital converters (ADCs).

8.1.1 Capacitive Loads

The dynamic characteristics of the OPA1671 amplifiers are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. Add a small resistor (for example, $R_S = 50\ \Omega$) in series with the output to isolate heavier capacitive loads.

8.1.2 Noise Performance

Figure 31 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The op amp itself contributes a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. For a CMOS-input device, the noise resulting from the input current is negligible; therefore, the total noise is dominated by the voltage noise of the OPA1671 at low source resistance, and the resistor noise $> 1\ \text{k}\Omega$.

Figure 31 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- R_S = source impedance
- k = Boltzmann's constant = $1.38 \times 10^{-23}\ \text{J/K}$
- T = temperature in kelvins (K)

For more details on calculating noise, see [Basic Noise Calculations](#).

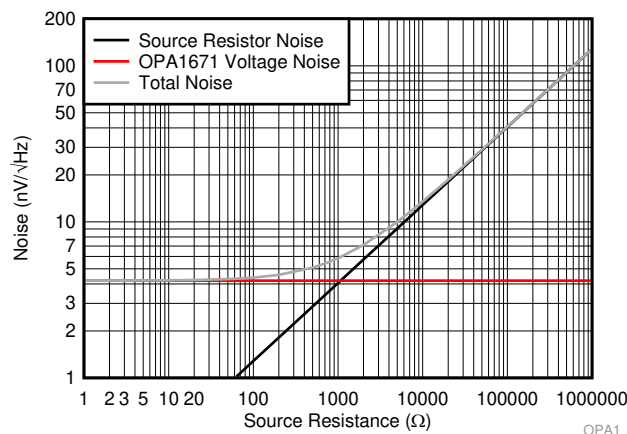


Figure 32. Noise Performance of the OPA1671 in a Unity-Gain Buffer Configuration

Application Information (continued)

8.1.3 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

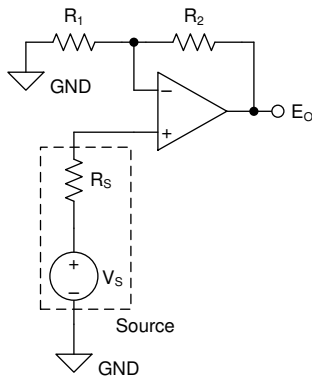
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in [Figure 31](#). The source impedance is typically fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

[Figure 33](#) shows noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components.

The selected feedback resistor values make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

(A) Noise in Noninverting Gain Configuration

Noise at the output is given as E_o , where



$$(1) E_o = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_s)^2 + (e_N)^2 + (e_{R_1 \parallel R_2})^2 + (i_N \cdot R_s)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [V_{RMS}]$$

$$(2) e_s = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_s} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_s$$

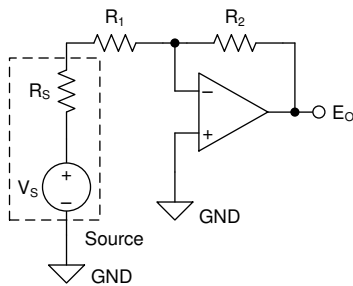
$$(3) e_{R_1 \parallel R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \parallel R_2$$

$$(4) k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5) T(K) = 237.15 + T(^{\circ}C) \quad [K] \quad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration

Noise at the output is given as E_o , where



$$(6) E_o = \left(1 + \frac{R_2}{R_s + R_1}\right) \cdot \sqrt{(e_N)^2 + (e_{R_1 + R_s \parallel R_2})^2 + \left(i_N \cdot \left[\frac{(R_s + R_1) \cdot R_2}{R_s + R_1 + R_2}\right]\right)^2} \quad [V_{RMS}]$$

$$(7) e_{R_1 + R_s \parallel R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_s + R_1) \cdot R_2}{R_s + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_s) \parallel R_2$$

$$(8) k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9) T(K) = 237.15 + T(^{\circ}C) \quad [K] \quad \text{Temperature in kelvins}$$

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- (1) e_N is the voltage noise of the amplifier. For the OPA1671 series of operational amplifiers, $e_N = 4.0 \text{ nV}/\sqrt{\text{Hz}}$ at 10 kHz.
- (2) i_N is the current noise of the amplifier. For the OPA1671 series of operational amplifiers, $i_N = 4.5 \text{ fA}/\sqrt{\text{Hz}}$ at 1 kHz.
- (3) For additional resources on noise calculations, see [TI's Precision Labs Series](#).

[Figure 33](#). Noise Calculation in Gain Configurations

8.2 Typical Application

This design uses an OPA1671 as a preamplifier for an electret microphone. Electret microphone types are common in many audio applications of varying performance levels. The OPA1671 offers very low noise in a tiny package, and is designed for use in electret preamplifier circuits.

Figure 34 shows the solution.

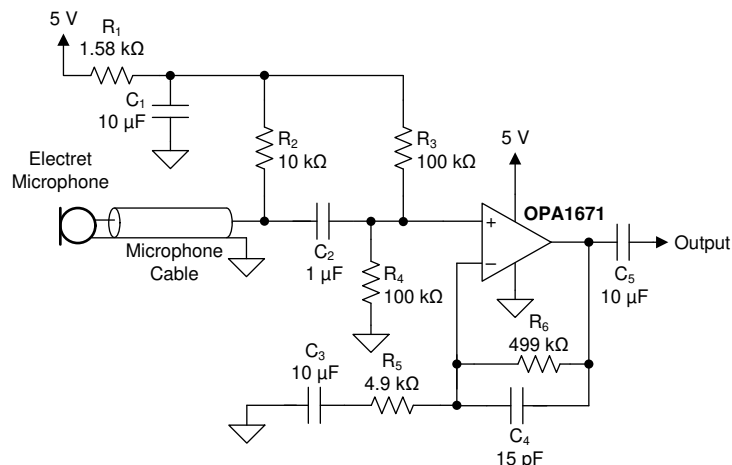


Figure 34. Electret Preamplifier Schematic

8.2.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 5 V
- Gain: 100 V/V
- Frequency response: 3 dB from 20 Hz to 20 kHz
- Output: 2.5 V ±1 V
- Output noise density: < 1 μV/√Hz at 10 kHz

Typical Application (continued)

8.2.2 Detailed Design Procedure

The preamplifier circuit uses a noninverting gain configuration to allow for high input impedance, with independent gain-setting resistor values. DC bypass is accomplished with C_2 and C_3 , with the low frequency poles set by C_2 , R_4 , C_3 and R_5 ; see 式 1 and 式 2.

$$p_{L1} = \frac{1}{2\pi \cdot (R_3 \parallel R_4) \cdot C_2} = 3.18 \text{ Hz} \tag{1}$$

$$p_{L2} = \frac{1}{2\pi \cdot R_5 \cdot C_2} = 3.23 \text{ Hz} \tag{2}$$

The filter cutoff frequency is determined by a higher frequency pole, set by R_5 and C_4 .

$$p_H = \frac{1}{2\pi \cdot R_6 \cdot C_4} = 21.3 \text{ kHz} \tag{3}$$

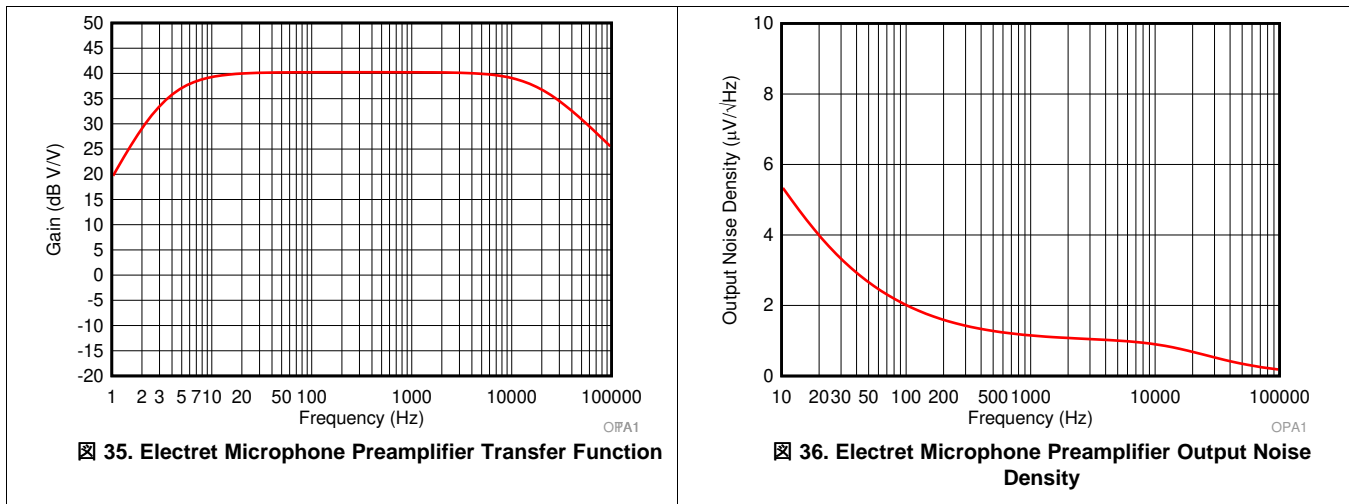
The gain of the circuit in the passband is set by R_5 and R_6 .

$$A(V/V) = \frac{R_6}{R_5} = 100 (40 \text{ dB}) \tag{4}$$

The output noise of the circuit (ignoring the electret microphone intrinsic noise and impedance) is the RSS average noise contribution from R_5 and the input voltage noise of OPA1671. R_5 was selected for minimal noise contribution without requiring a dc blocking cap. (C_3) larger than 10 μF . See 式 5 for the output noise density calculation at 10 kHz.

$$e_{N_OUT} = \text{Input Referred Noise} \cdot \text{Gain} = \sqrt{(4kTR_5)^2 + V_{N_10k}^2} \cdot 100 = 0.96 \mu\text{V}/\sqrt{\text{Hz}} \tag{5}$$

8.2.3 Application Curves



9 Power Supply Recommendations

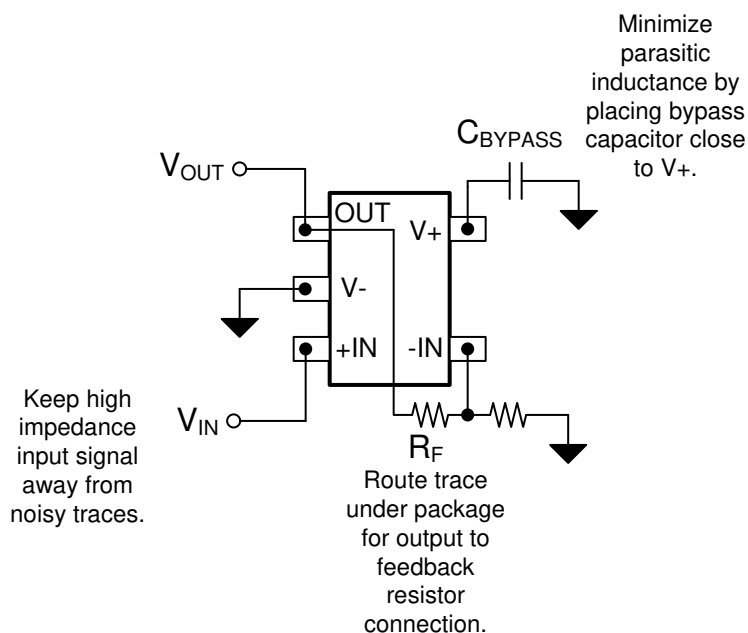
The OPA1671 device is specified for operation from 1.7 V to 5.5 V (± 0.85 V to ± 2.75 V).

10 Layout

10.1 Layout Guidelines

Paying attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1- μ F capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

10.2 Layout Example



☒ 37. OPA1671 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA-TI™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI™は TINA™ソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TI™には従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

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11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、[『回路基板のレイアウト技法』](#)
- テキサス・インスツルメンツ、[『アナログ・エンジニア向け回路クックブック』](#)

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11.4 コミュニティ・リソース

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1671IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	1X6T
OPA1671IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1X6T
OPA1671IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	1X6T
OPA1671IDBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1X6T
OPA1671IDBVTG4.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	1X6T
OPA1671IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	1D3
OPA1671IDCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1D3
OPA1671IDCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	1D3
OPA1671IDCKT.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1D3
OPA1671IDCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1D3
OPA1671IDCKTG4.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1D3

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

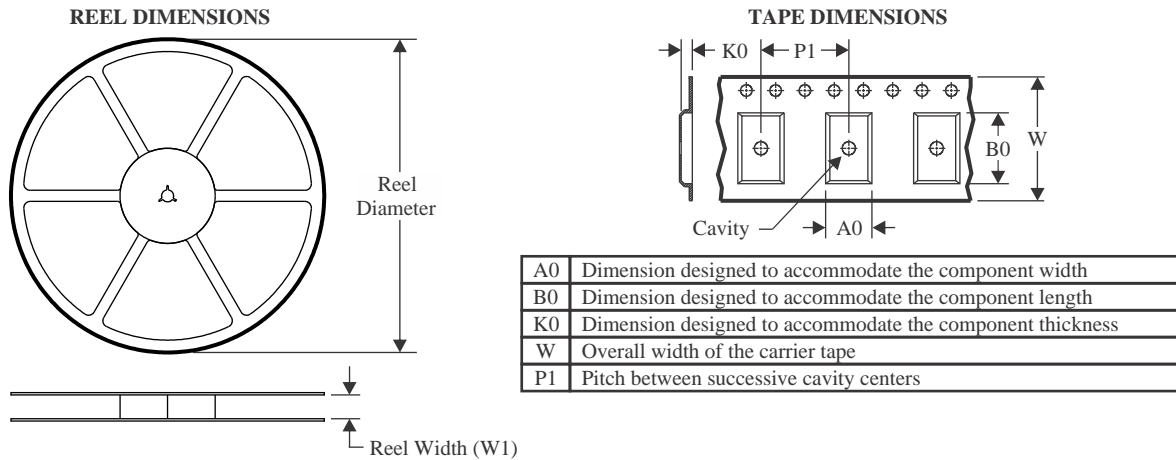
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1671IDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1671IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA1671IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA1671IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
OPA1671IDCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
OPA1671IDCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1671IDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
OPA1671IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA1671IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA1671IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
OPA1671IDCKT	SC70	DCK	5	250	210.0	185.0	35.0
OPA1671IDCKTG4	SC70	DCK	5	250	190.0	190.0	30.0

EXAMPLE BOARD LAYOUT

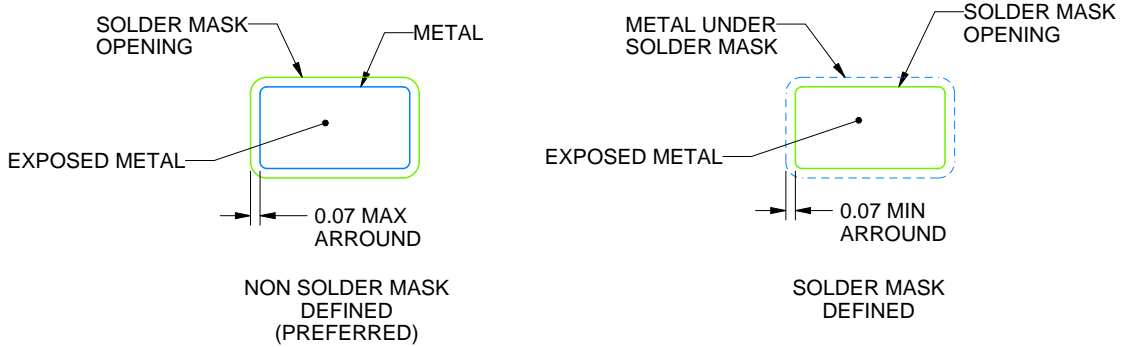
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

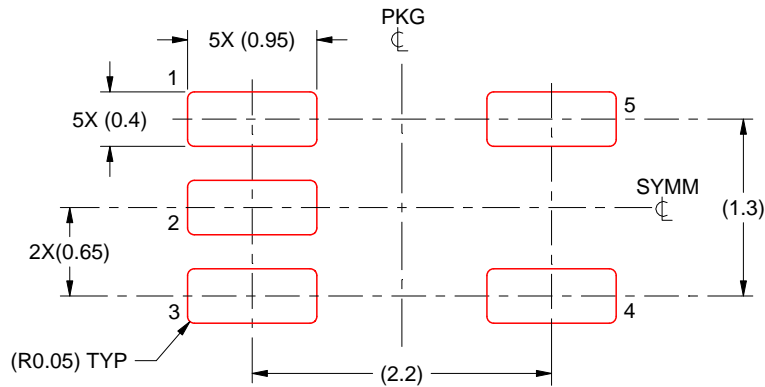
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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