Texas Instruments
OPA2172-Q1, OPA4172-Q1
JAJSCN7A – NOVEMBER 2016 – REVISED JUNE 2017

OPAx172-Q1　36V、単一電源、10MHz、レール・ツー・レール出力、車載用グレード・オペアンプ

1　特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード 1:
    動作時周囲温度範囲-40℃～+125℃
  - デバイスHBM ESD分類レベル3A
  - デバイスCDM ESD分類レベルC6
- 広い電源電圧範囲:
  4.5V～36V、±2.25V～±18V
- 低いオフセット電圧: ±0.2mV
- 低いオフセット・ドリフト: ±0.3µV/℃
- ゲイン帯域幅: 10MHz
- 低い入力バイアス電流: ±8pA
- 低い静止電流: アンプごとに1.6mA
- 低ノイズ: 7nV/√Hz
- EMIおよびRFIフィルタ入力
- 入力範囲は負の電源電圧にも対応
- 入力範囲は正の電源電圧まで動作
- レール・ツー・レール出力
- 高い同相除去: 120dB
- 業界標準のパッケージ
  - VSSOP-8、TSSOP-14

2　アプリケーション

- 車載
- HEVおよびEVパワートレイン
- 先進運転支援システム（ADAS）
- 自動気候制御
- 航空電子工学、着陸装置
- 医療用計測機器
- 電流感知

3　概要

OPA2172-Q1、OPA4172-Q1 (OPAx172-Q1)は36V、単一電源、低ノイズのオペアンプのファミリで、4.5V (±2.25V)～36V (±18V)の範囲の電源で動作できます。

OPAx172-Q1はマイクロパッケージで供給され、低いオフセット、ドリフト係数、静止電流を実現します。広い帯域幅、高速なスルー・レート、高い出力電流駆動能力も、これらのデバイスの特長です。デュアルおよびクワッドの各バージョンは、いずれも同一仕様で、可能な限り柔軟に設計を行えます。

ほとんどのオペアンプでは1つの電源電圧でしか動作が規定されていないのに対して、OPAx172-Q1ファミリは4.5V～36Vでの動作が規定されています。電源レールの範囲外の入力信号が位相反転を起こすことはありません。通常の動作時に、入力は負のレールより100mV下、および上限レールの2V以内で動作できます。これらのデバイスは完全なレール・ツー・レール入力で、上限レールを100mV超えて動作しますが、上限レールから2V以内では性能が低下することに注意してください。

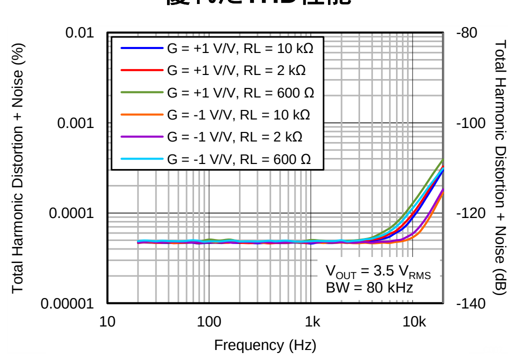
OPAx172-Q1シリーズのオペアンプは、-40℃～+125℃での動作が規定されています。

製品情報(1)

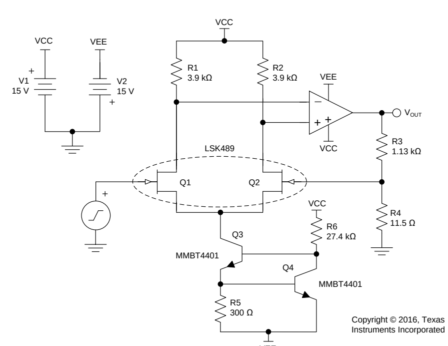
型番	パッケージ	本体サイズ(公称)
OPA2172-Q1	VSSOP (8)	3.00mm×3.00mm
OPA4172-Q1	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

優れたTHD性能



JFET入力の低ノイズ・アンプ



English Data Sheet: SBOS809

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年11月発行のものから更新 **Page**

- データシート全体を通してOPA172-Q1を 削除 1
- Deleted Operating temperature, T_A from *Absolute Maximum Ratings* 4
- Added OPA4172-Q1 in PW package to *ESD Ratings* table 4
- Changed values in the *Thermal Information* table to align with JEDEC standards. 4
- Deleted value: ±14 and temperature range: T_A = –40°C to +125°C from Input bias current and added T_A = 25°C to Input bias current and Input offset current 5
- Changed TYP value from: 2.5 to: 2 for Input voltage noise, E_n 5
- Deleted Specified temperature from *Electrical Characteristics* table 6
- Changed figure: *Operational Amplifier Board Layout for a Noninverting Configuration* with revised content 25

5 Device Comparison Table

Table 1. Device Comparison

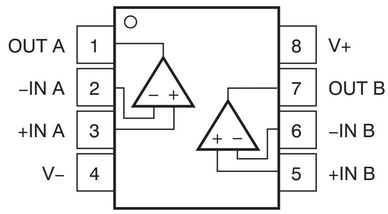
DEVICE	PACKAGE
OPA2172-Q1 (dual)	VSSOP-8
OPA4172-Q1 (quad)	TSSOP-14

Table 2. Device Family Comparison

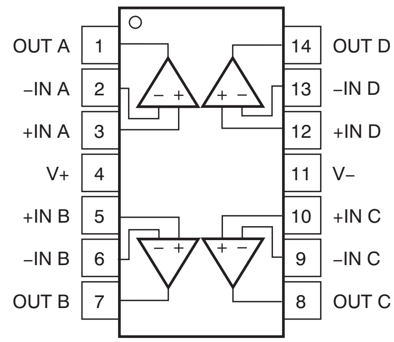
DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH PRODUCT (GBP)	VOLTAGE NOISE DENSITY (e_n)
OPAx172	1600 µA	10 MHz	7 nV/√Hz
OPAx171	475 µA	3.0 MHz	14 nV/√Hz
OPAx170	110 µA	1.2 MHz	19 nV/√Hz

6 Pin Configuration and Functions

OPA2172-Q1 DGK Package
8-Pin VSSOP
Top View



OPA4172-Q1 PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	OPA2172-Q1 DGK (VSSOP)	OPA4172-Q1 PW (TSSOP)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input,,channel C
–IN D	—	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V–	4	11	—	Negative (lowest) power supply
V+	8	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V–		–20	20	V
	Single-supply voltage			40	
	Signal input pins voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	
		Differential(3)	–0.5	0.5	
Current	Signal input pins current		–10	10	mA
	Output short-circuit(4)		Continuous		
Temperature	Junction, T_J			150	°C
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
(3) Refer to the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
OPA2172-Q1 in DGK package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
OPA4172-Q1 in PW package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, (V+) – (V–)	Single-supply	4.5	36	V
	Dual-supply	±2.25	±18	
Specified temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA2172-Q1 DGK (VSSOP) 8 PINS	OPA4172-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	181.4	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.2	32.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	103.3	50.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.6	49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.2	±1	mV
		T_A = –40°C to +125°C				±1.15	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C	OPA4172-Q1		±0.3	±1.5	µV/°C
			OPA2172-Q1			±1.8	
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±1	±3	µV/V
	Channel separation, dc	At dc			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			±8	±15	pA
		T_A = –40°C to +125°C	OPA2172-Q1IDGK			±18	nA
			OPA4172-Q11PW				
I_{OS}	Input offset current	T_A = 25°C			±2	±15	pA
		T_A = –40°C to +125°C	OPA4172-Q1			±1	nA
			OPA2172-Q1			±3	
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			2		$µV_{PP}$
e_n	Input voltage noise density	f = 100 Hz			12		nV/√Hz
		f = 1 kHz			7		
i_n	Input current noise density	f = 1 kHz			1.6		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage (1)			(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		110	120		
INPUT IMPEDANCE							
	Differential				100 || 4		MΩ || pF
	Common-mode				6 || 4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, R_L = 10 kΩ, T_A = –40°C to +125°C	OPA4172-Q1	110	130		dB
			OPA2172-Q1	107	115		
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to +125°C	OPA4172-Q1		116		
			OPA2172-Q1		107		
FREQUENCY RESPONSE							
GBP	Gain bandwidth product				10		MHz
SR	Slew rate	G = 1			10		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = 1, 10-V step			2		µs
		To 0.01% (12 bit), V_S = ±18 V, G = 1, 10-V step			3.2		
	Overload recovery time	V_{IN} × Gain > V_S			200		ns
THD+N	Total harmonic distortion + noise	V_S = 36 V, G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00005%		

(1) The input range can be extended beyond (V+) – 2 V up to (V+) + 0.1 V. See the *Typical Characteristics* and *Application Information* sections for additional information.

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail	V_S = +36 V	R_L = 10 kΩ		70	90	mV
			R_L = 2 kΩ		330	400	
		V_S = +36 V, T_A = –40°C to +125°C	R_L = 10 kΩ		95	120	
			R_L = 2 kΩ		470	530	
		V_S = 4.5 V	R_L = 10 kΩ		10	20	
			R_L = 2 kΩ		40	50	
		V_S = 4.5 V, T_A = –40°C to +125°C	R_L = 10 kΩ		10	25	
			R_L = 2 kΩ		55	70	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive			See the *Typical Characteristics*			pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			60		Ω
POWER SUPPLY							
V_S	Specified voltage			4.5		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A			1.6	1.8	mA
		I_O = 0 A, T_A = –40°C to +125°C				2	

7.6 Typical Characteristics

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

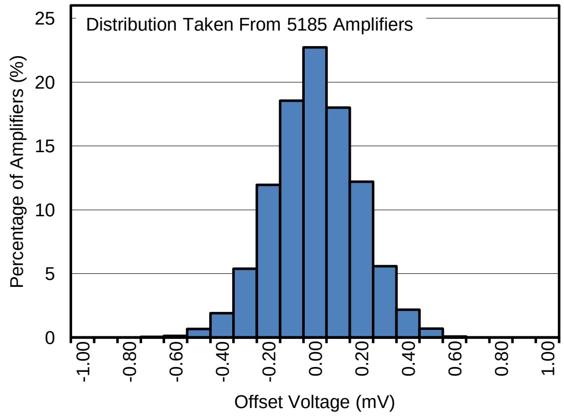


Figure 1. Offset Voltage Production Distribution

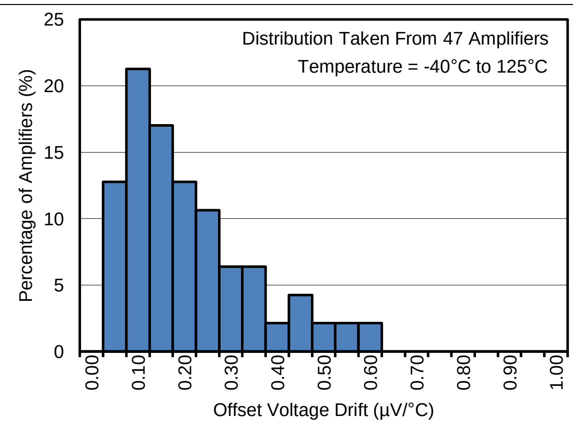


Figure 2. Offset Voltage Drift Production Distribution

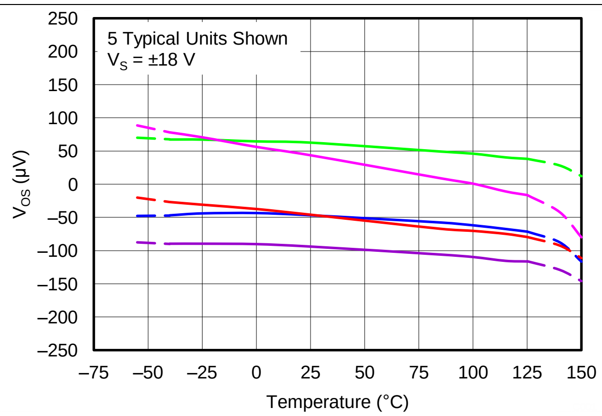


Figure 3. Offset Voltage vs Temperature (V_S = ±18 V)

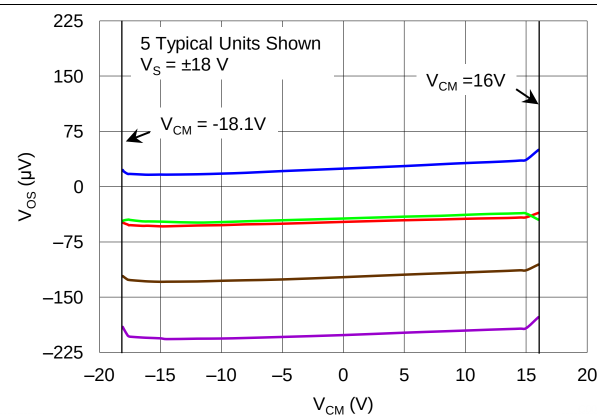


Figure 4. Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)

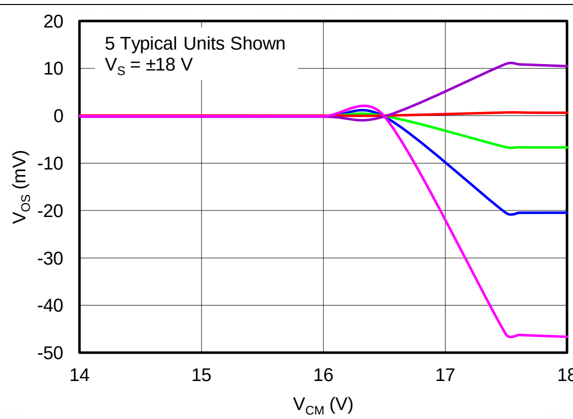


Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

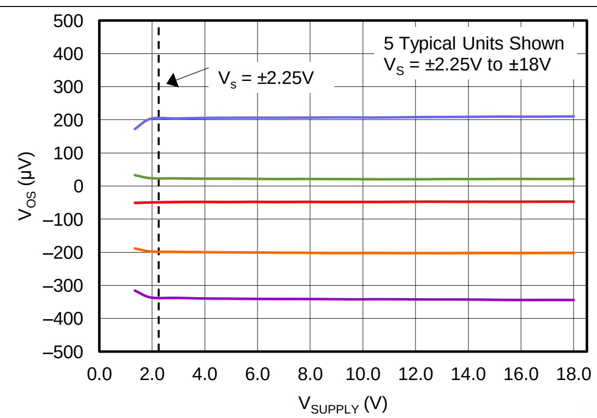


Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

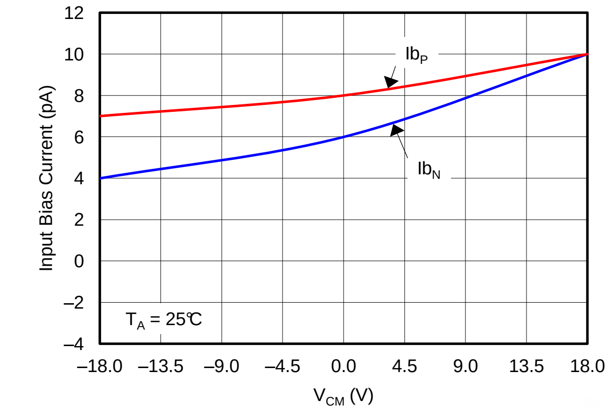


Figure 7. Input Bias Current vs Common-Mode Voltage

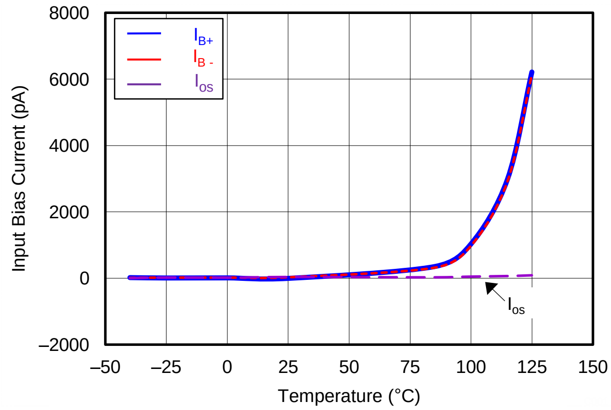


Figure 8. Input Bias Current vs Temperature

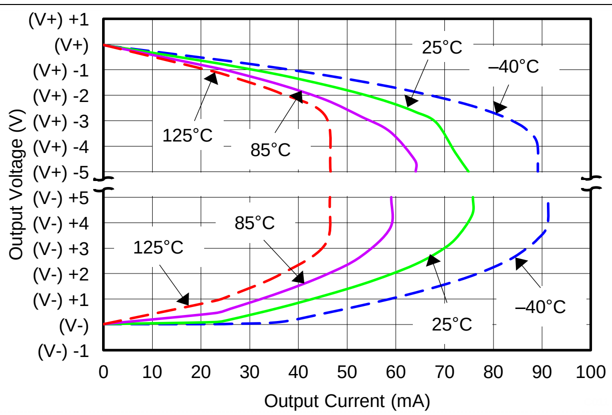


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

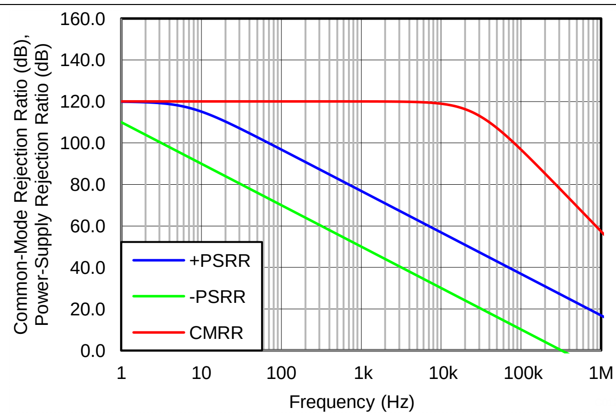


Figure 10. CMRR and PSRR vs Frequency (Referred-to-Input)

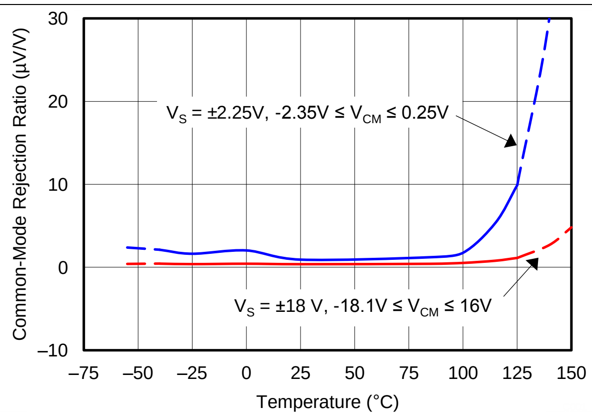


Figure 11. CMRR vs Temperature

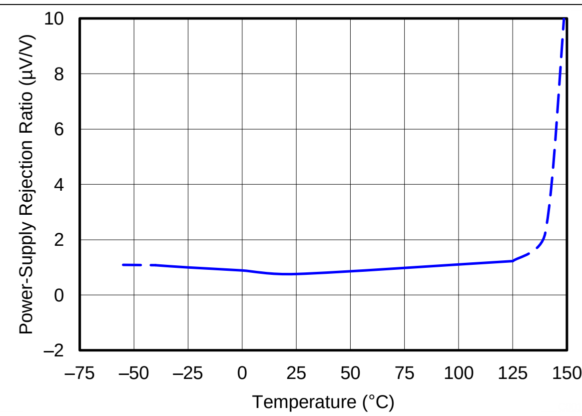


Figure 12. PSRR vs Temperature

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

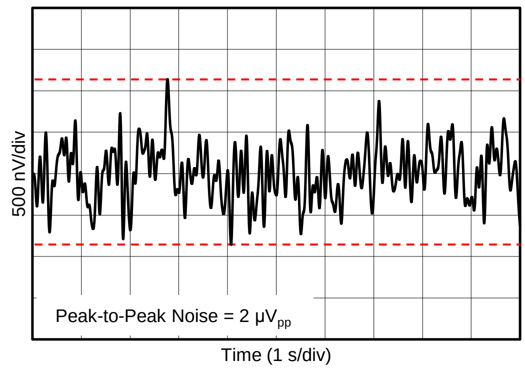


Figure 13. 0.1-Hz to 10-Hz Noise

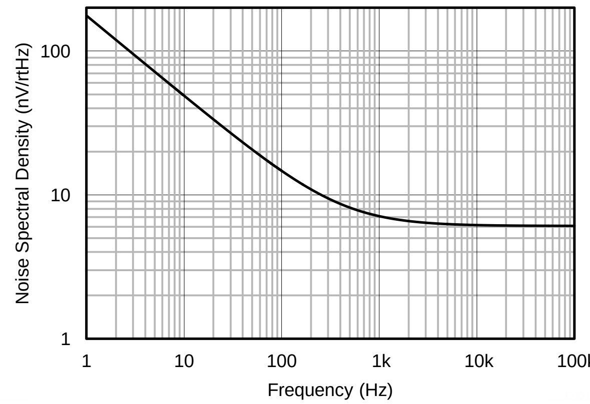


Figure 14. Input Voltage Noise Spectral Density vs Frequency

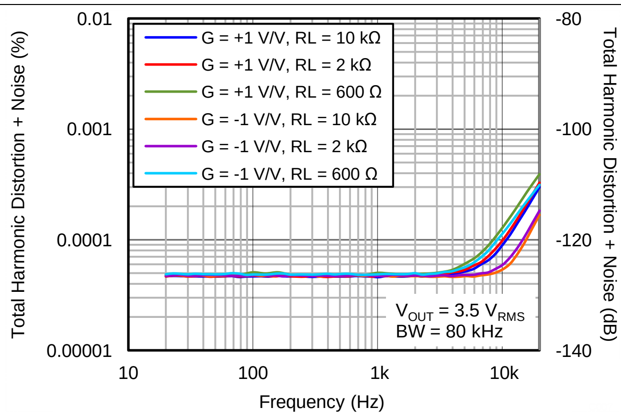


Figure 15. THD+N Ratio vs Frequency

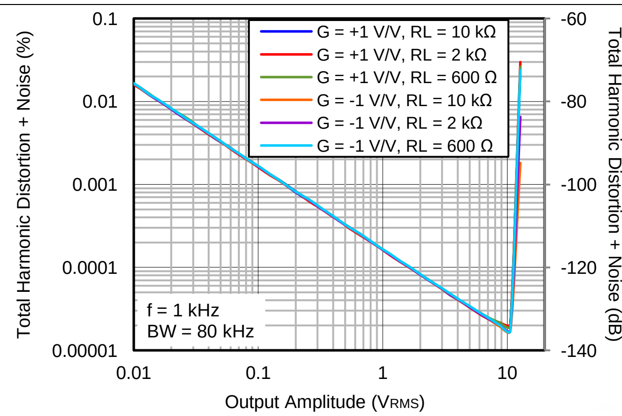


Figure 16. THD+N vs Output Amplitude

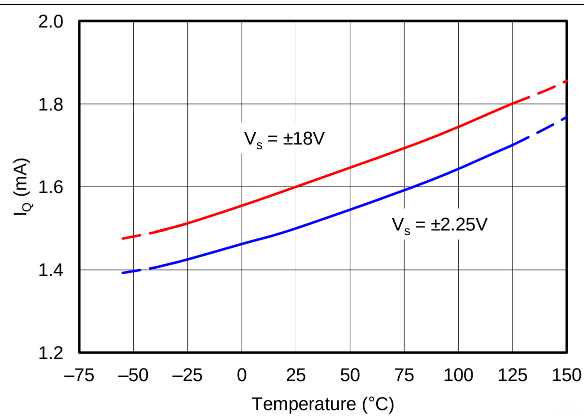


Figure 17. Quiescent Current vs Temperature

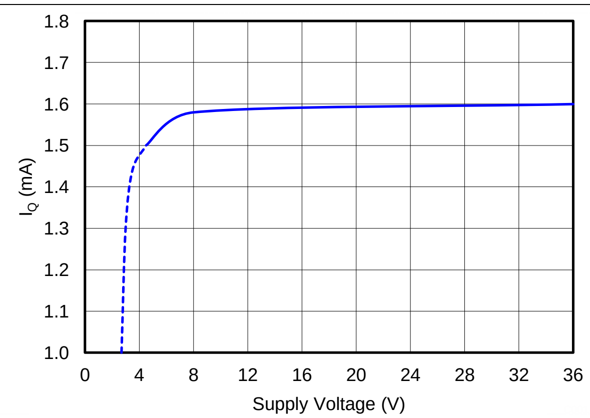


Figure 18. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

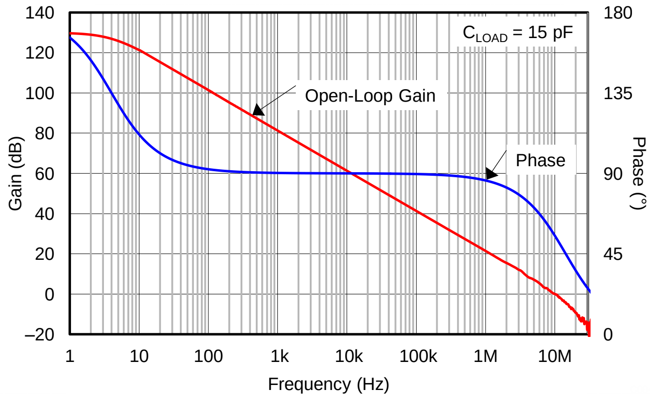


Figure 19. Open-Loop Gain and Phase vs Frequency

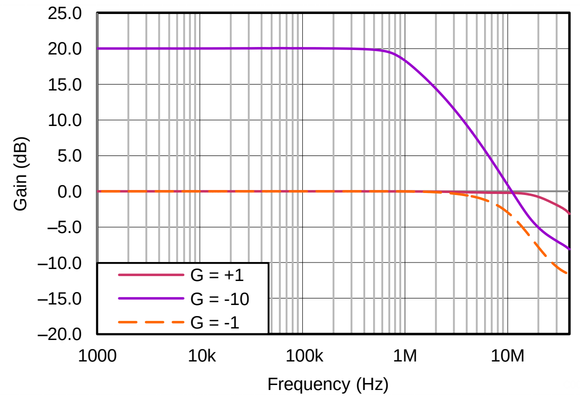


Figure 20. Closed-Loop Gain vs Frequency

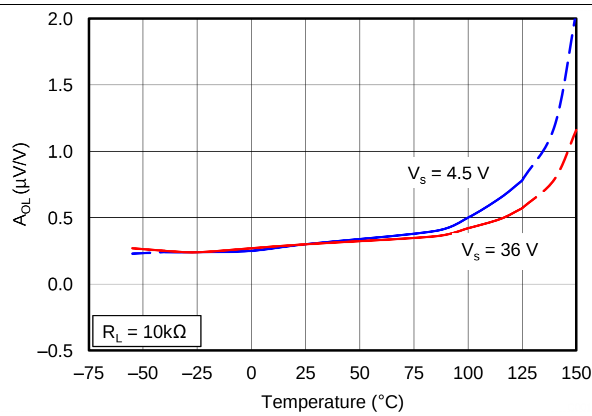


Figure 21. Open-Loop Gain vs Temperature

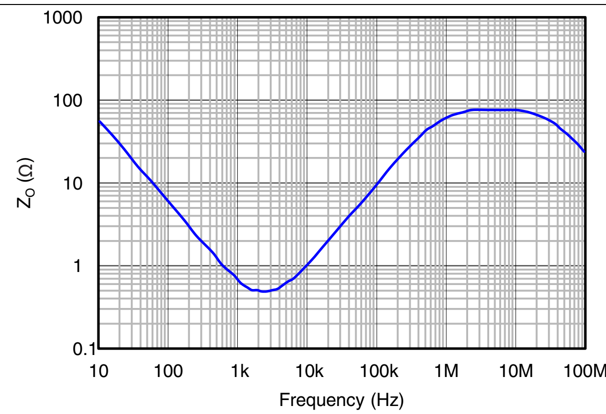


Figure 22. Open-Loop Output Impedance vs Frequency

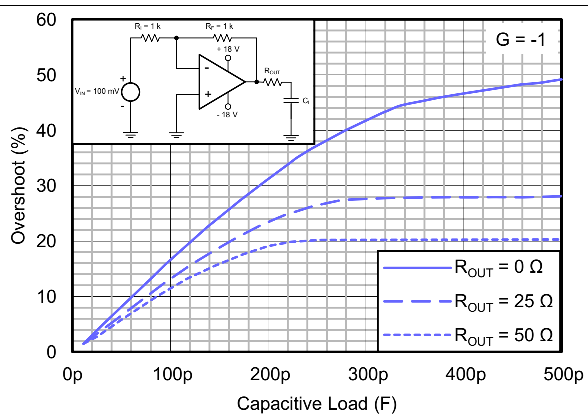


Figure 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

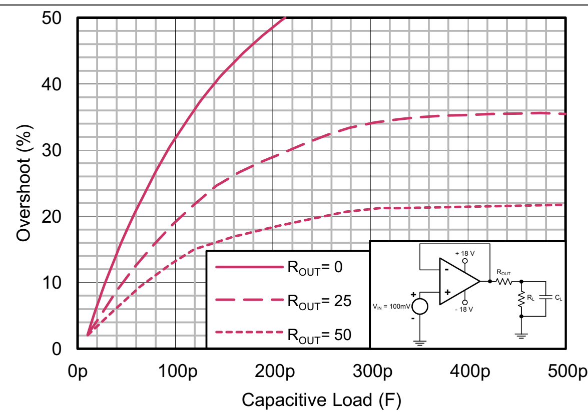


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

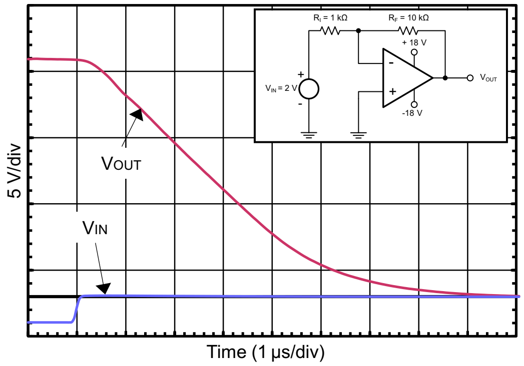


Figure 25. Positive Overload Recovery

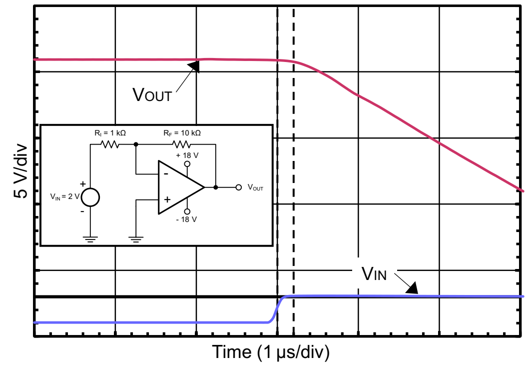


Figure 26. Positive Overload Recovery (Zoomed In)

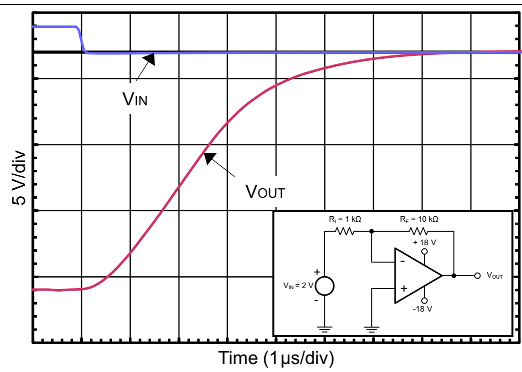


Figure 27. Negative Overload Recovery

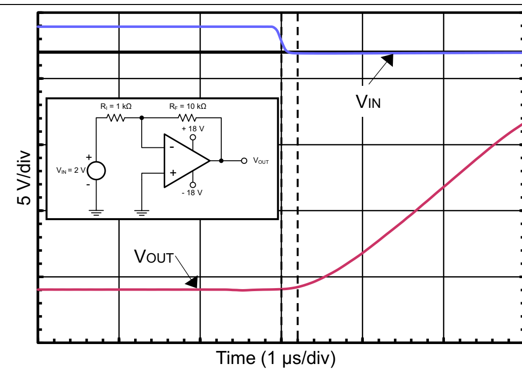


Figure 28. Negative Overload Recovery (Zoomed In)

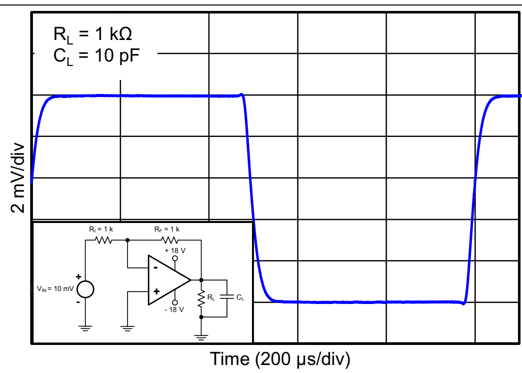


Figure 29. Small-Signal Step Response (10 mV, G = –1)

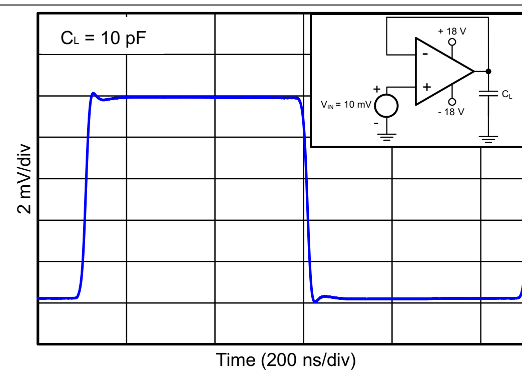


Figure 30. Small-Signal Step Response (10 mV, G = 1)

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

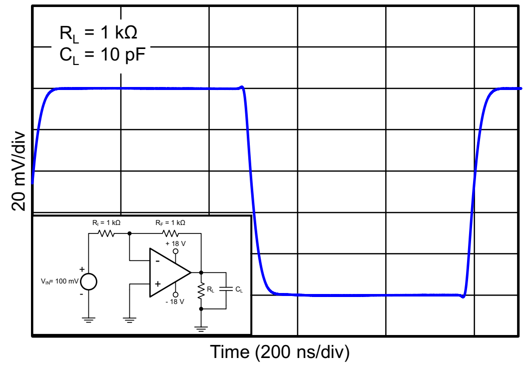


Figure 31. Small-Signal Step Response (100 mV, G = –1)

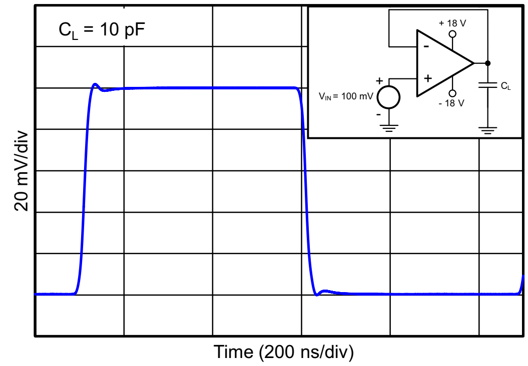


Figure 32. Small-Signal Step Response (100 mV, G = 1)

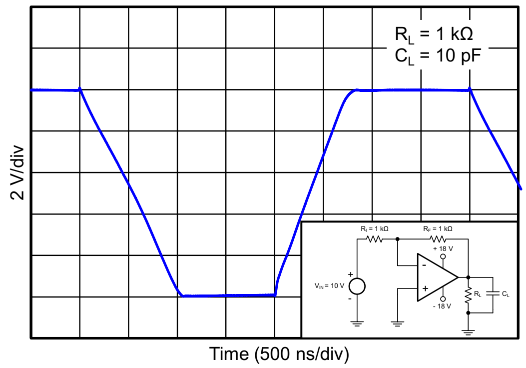


Figure 33. Large-Signal Step Response (10 V, G = –1)

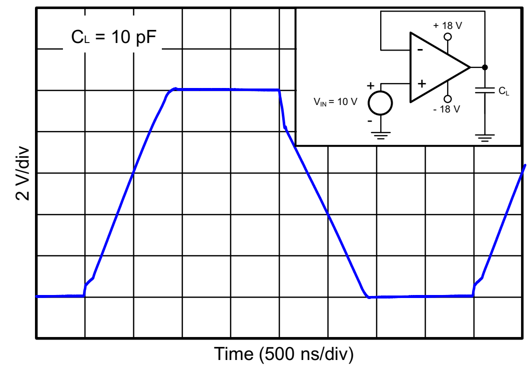


Figure 34. Large-Signal Step Response (10 V, G = 1)

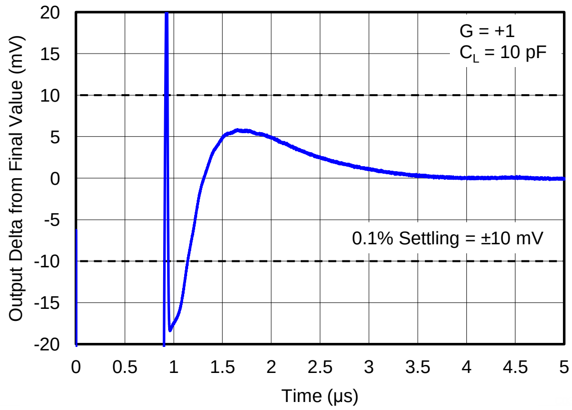


Figure 35. Large-Signal Settling Time (10-V Positive Step)

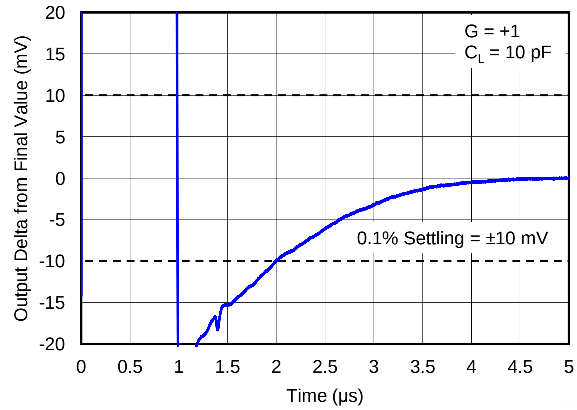


Figure 36. Large-Signal Settling Time (10-V Negative Step)

Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

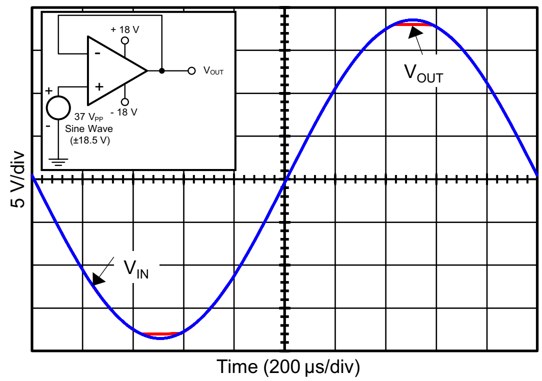


Figure 37. No Phase Reversal

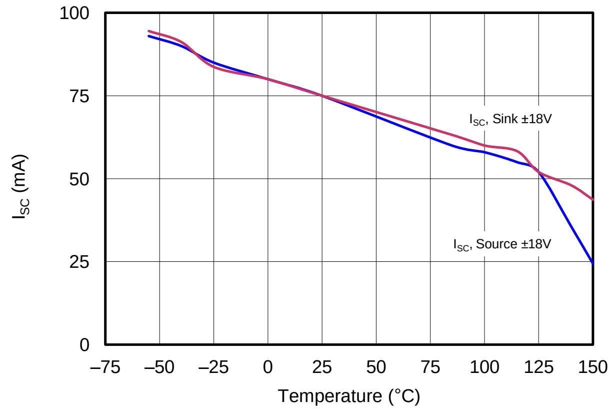


Figure 38. Short-Circuit Current vs Temperature

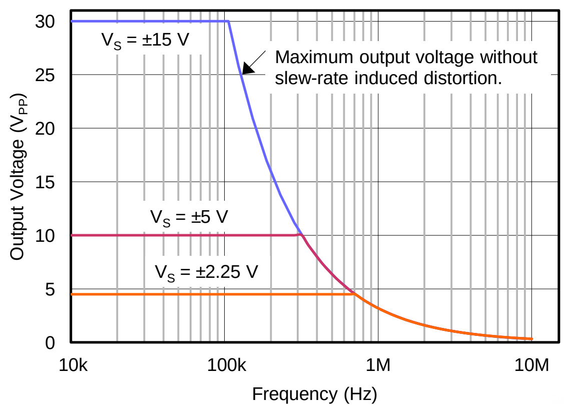


Figure 39. Maximum Output Voltage vs Frequency

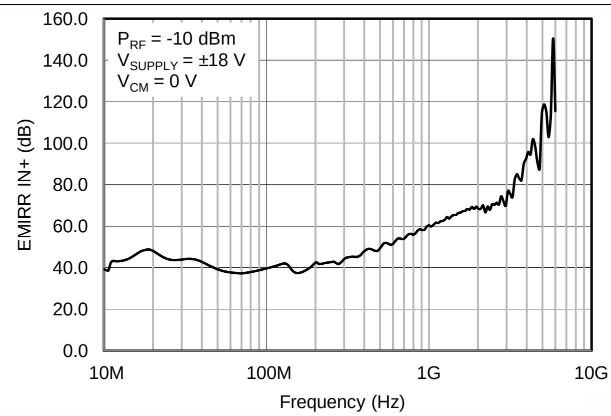


Figure 40. EMIRR vs Frequency

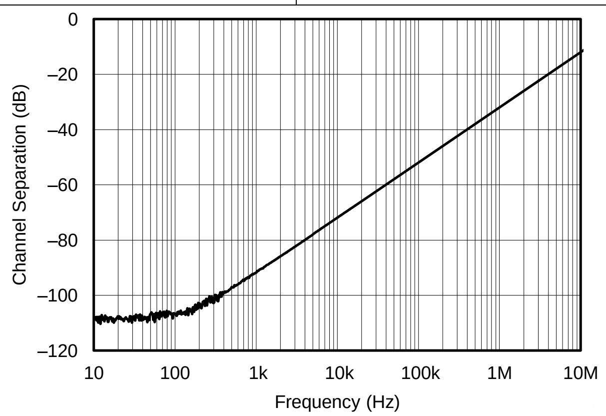


Figure 41. Channel Separation vs Frequency

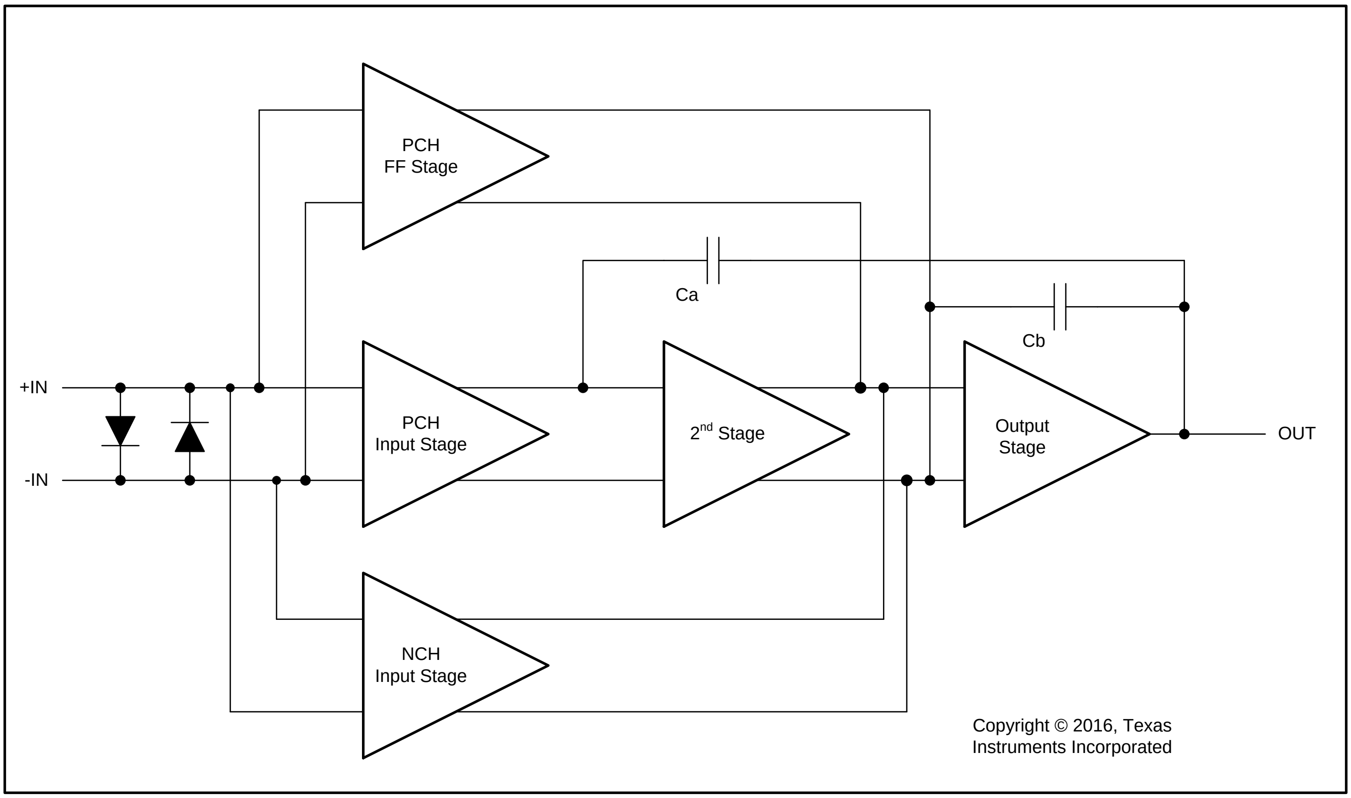
8 Detailed Description

8.1 Overview

The OPAx172-Q1 family of operational amplifiers provide high overall performance, making the devices ideal for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (maximum) provides excellent stability over the entire temperature range. In addition, the family offers very good overall performance with high CMRR, PSRR, A_{OL}, and superior THD.

The *Functional Block Diagram* section shows the simplified diagram of the OPA172-Q1 design. The design topology is a highly-optimized, three-stage amplifier with an active-feedforward gain stage.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 EMI Rejection

The OPAx172-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx172-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 42 shows the results of this testing on the OPAx172-Q1. Table 3 shows the EMIRR IN+ values for the OPAx172-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 3 can be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report (SBOA128), available for download from www.ti.com.

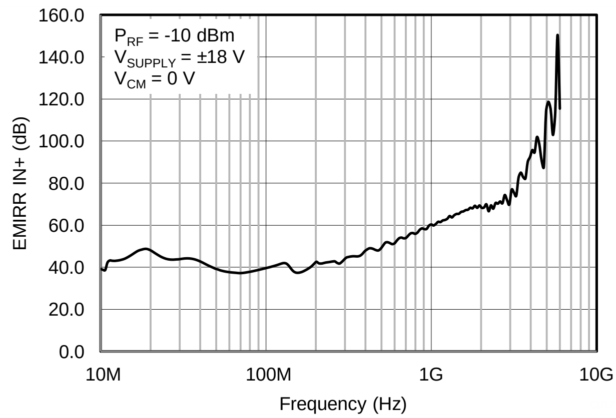


Figure 42. EMIRR Testing

Table 3. OPAx172-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh frequency (UHF) applications	47.6 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	68 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.2 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.9 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	114 dB

8.3.2 Phase-Reversal Protection

The OPAx172-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx172-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in Figure 43.

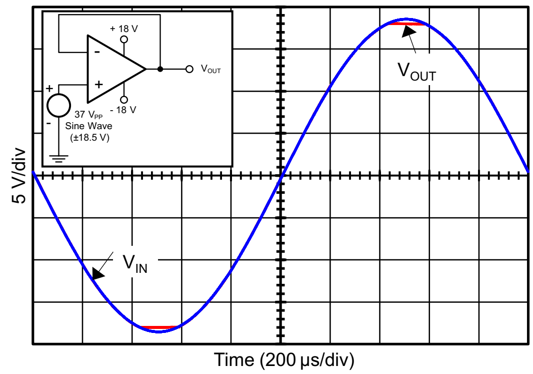


Figure 43. No Phase Reversal

8.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPAx172-Q1 are optimized for commonly-used operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} = 50 Ω) in series with the output. Figure 44 and Figure 45 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. See the *Feedback Plots Define Op Amp AC Performance* application bulletin (SBOA015), available for download from www.ti.com, for details of analysis techniques and application circuits.

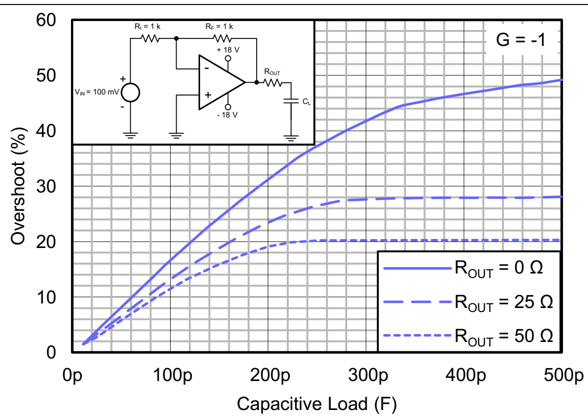


Figure 44. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

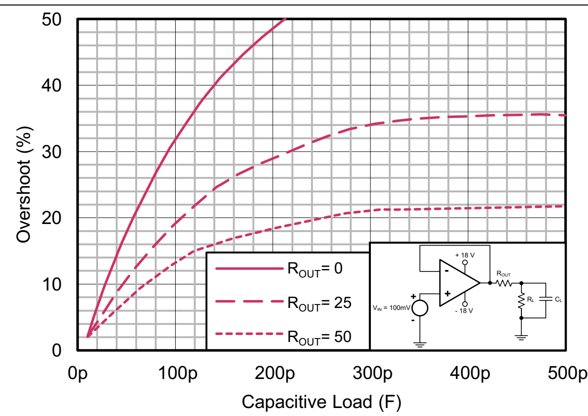


Figure 45. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx172-Q1 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with a full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 4.

Table 4. Typical Performance Range (V_S = ±18 V)

	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		5		mV
Offset voltage vs temperature (T_A = –40°C to +125°C)		10		µV/°C
Common-mode rejection		70		dB
Open-loop gain		60		dB
Gain bandwidth product (GBP)		4		MHz
Slew rate		4		V/µs
Noise at f = 1 kHz		22		nV/√Hz

8.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage terminals or even the output terminal. Each of these different terminal functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the terminal. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 46 illustrates the ESD circuits contained in the OPAx172-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output terminals and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

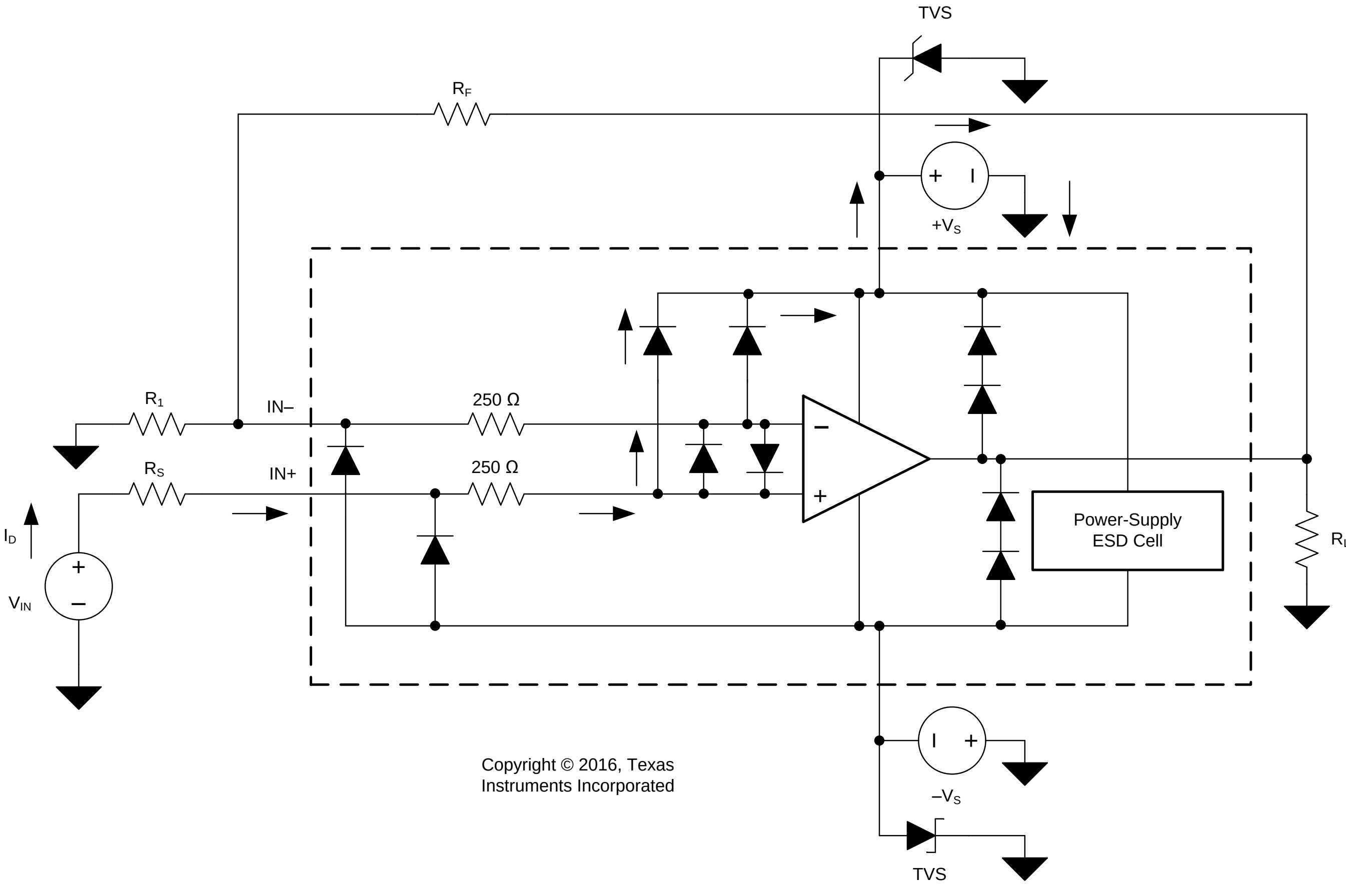


Figure 46. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx172-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 46), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 46 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply terminals; see Figure 46. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The OPAx172-Q1 input terminals are protected from excessive differential voltage with back-to-back diodes; see Figure 46. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx172-Q1. Figure 46 illustrates an example configuration that implements a current-limiting feedback resistor.

8.4.3 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx172-Q1 is approximately 200 ns.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx172-Q1 family of amplifiers is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

9.2 Typical Applications

The following application examples highlight only a few of the circuits where the OPAx172-Q1 can be used.

9.2.1 Capacitive Load Drive Solution Using an Isolation Resistor

The OPA172-Q1 can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin, as shown in Figure 47.

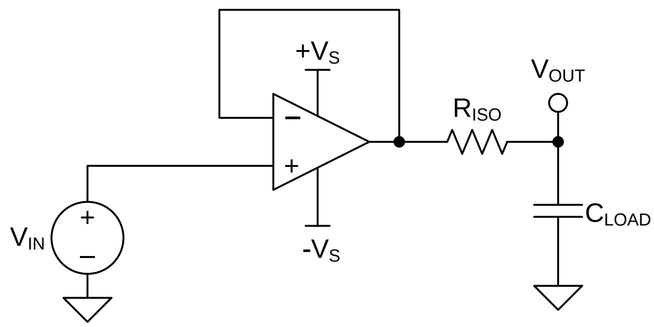


Figure 47. Unity-Gain Buffer with R_{ISO} Stability Compensation

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μF, 0.1 μF, and 1 μF
- Phase margin: 45° and 60°

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Figure 47 depicts a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 47. Not depicted in Figure 47 is the open-loop output resistance of the op amp, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1 / β is 20 dB per decade. Figure 48 shows the concept. Note that the 1 / β curve for a unity-gain buffer is 0 dB.

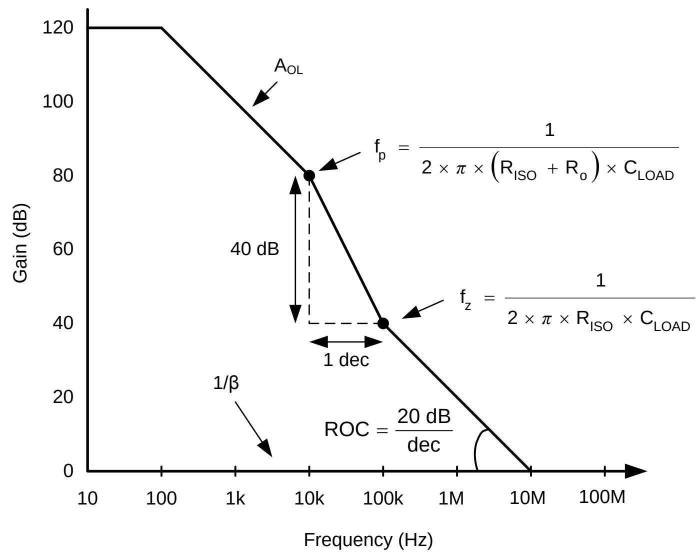


Figure 48. Unity-Gain Amplifier with R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 5 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA172-Q1, see the *Capacitive Load Drive Solution using an Isolation Resistor*precision design (TIPD128).

Table 5. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.1.3 Application Curve

The OPA172-Q1 meets the supply voltage requirements of 30 V. The OPA172-Q1 is tested for various capacitive loads and R_{ISO} is adjusted to get an overshoot corresponding to Table 5. The results of the these tests are summarized in Figure 49.

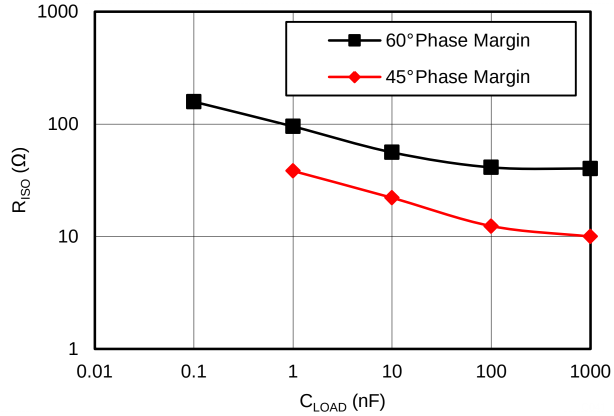


Figure 49. R_{ISO} vs C_{LOAD}

9.2.2 Bidirectional Current Source

The improved Howland current-pump topology shown in Figure 50 provides excellent performance because of the extremely tight tolerances of the on-chip resistors of the INA132. By buffering the output using an OPA172-Q1, the output current the circuit is able to deliver is greatly extended.

The circuit dc transfer function is shown in Equation 2.

$$I_{OUT} = V_{IN} / R1 \quad (2)$$

The OPA172-Q1 can also be used as the feedback amplifier because the low bias current minimizes error voltages produced across R1. However, for improved performance, select a FET-input device with extremely low offset, such as the OPA192, OPA140, or OPA188 as the feedback amplifier.

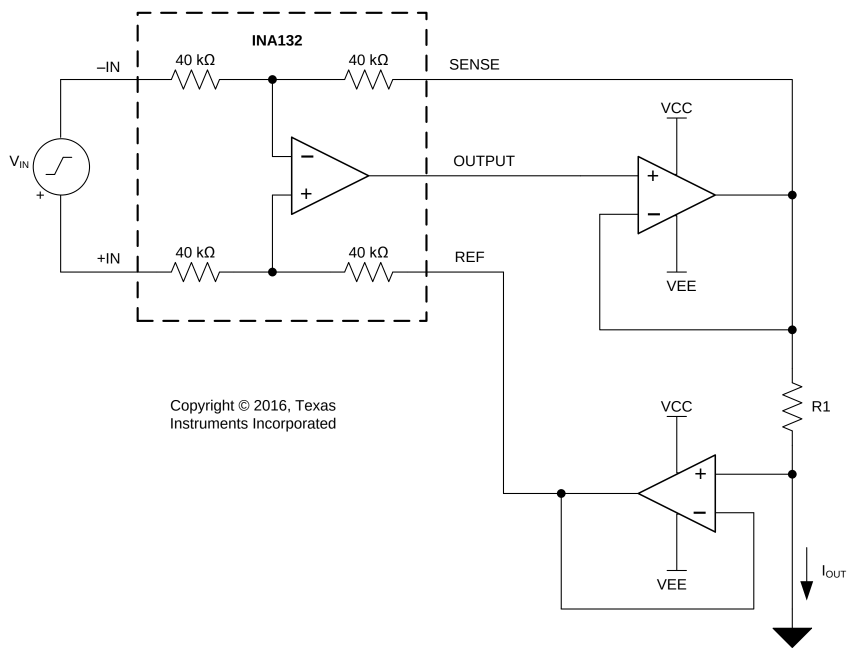


Figure 50. Bidirectional Current Source

9.2.3 JFET-Input Low-Noise Amplifier

Figure 51 shows a low-noise composite amplifier built by adding a low noise JFET pair (Q1 and Q2) as an input preamplifier for the OPA172-Q1. Transistors Q3 and Q4 form a 2-mA current sink that biases each JFET with 1 mA of drain current. Using 3.9-kΩ drain resistors produces a gain of approximately 10 in the input amplifier, making the extremely-low, broadband-noise spectral density of the JFET pair, Q1 and Q2, the dominant noise source of the amplifier. The output impedance of the input differential amplifier is large enough that a FET-input amplifier such as the OPA172-Q1 provides superior noise performance over bipolar-input amplifiers.

The gain of the composite amplifier is given by Equation 3.

$$A_V = (1 + R3 / R4) \quad (3)$$

The resistances shown are standard 1% resistor values that produce a gain of approximately 100 (99.26) with 68° of phase margin. Gains less than 10 may require additional compensation methods to provide stability. Select low resistor values to minimize the resistor thermal noise contribution to the total output noise.

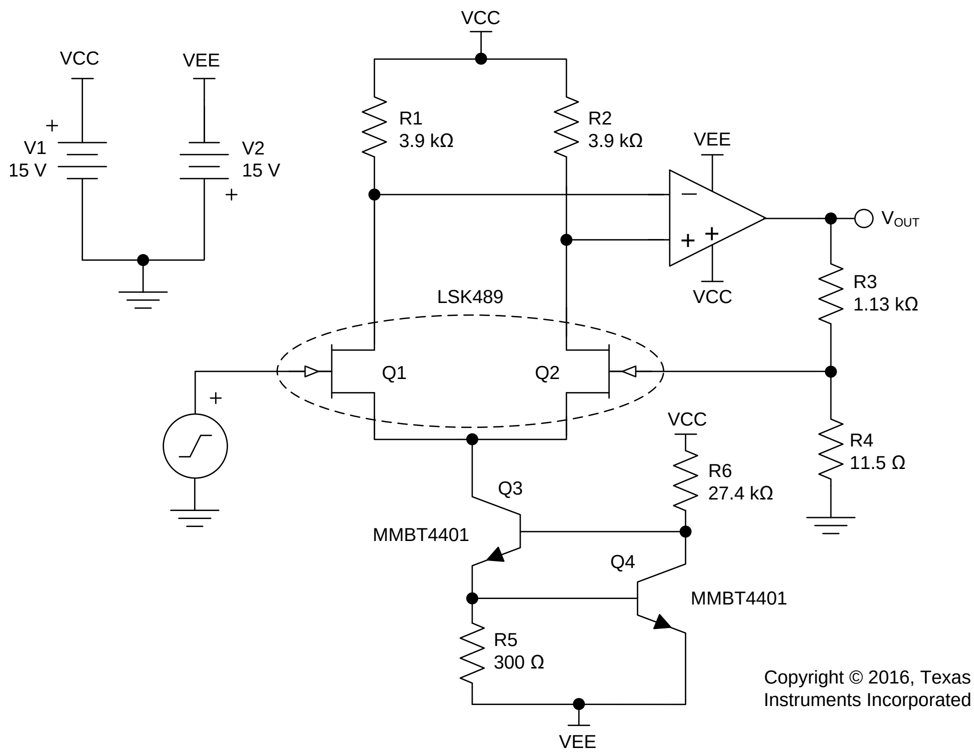


Figure 51. JFET-Input Low-Noise Amplifier

10 Power Supply Recommendations

The OPA172-Q1 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply terminals to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular as opposed to in parallel with the noisy trace is preferable.
- Place the external components as close to the device as possible. As illustrated in Figure 52, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

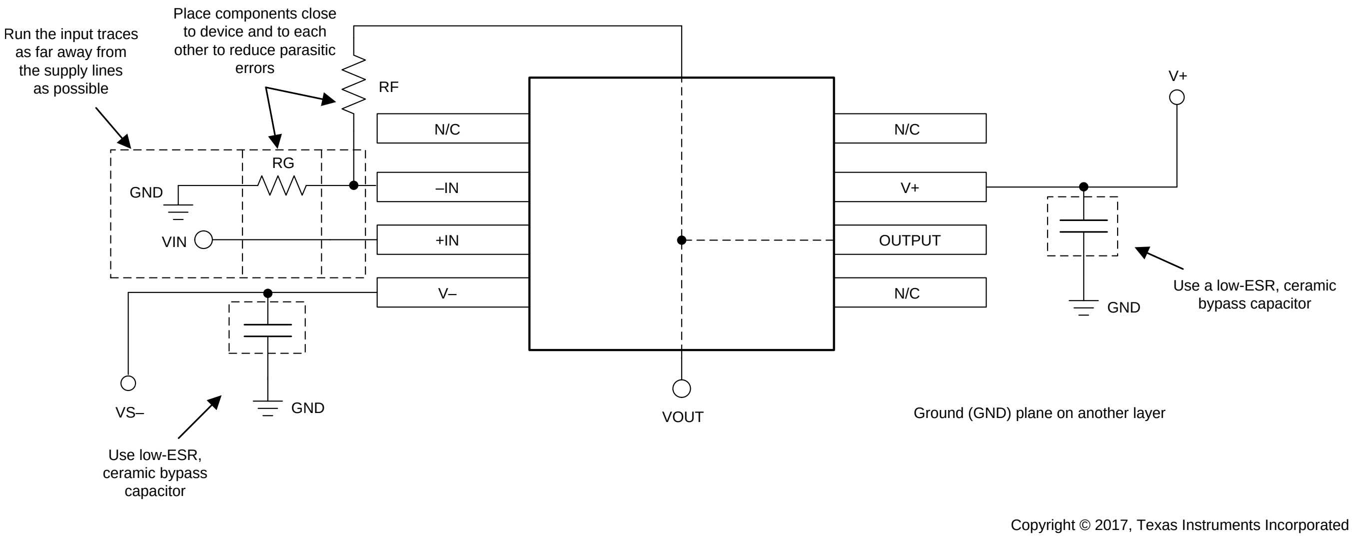


Figure 52. Operational Amplifier Board Layout for a Noninverting Configuration

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA-TI™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI™はTINA-TI™ソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TI™には従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TI™はAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TI™ソフトウェアがインストールされている必要があります。TINA-TI™フォルダから、無料のTINA-TI™ソフトウェアをダウンロードしてください。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください:

- 『フィードバック・プロットによるオペアンプAC性能の定義』(SBOA015)
- 『オペアンプのEMI除去率』(SBOA128)
- 『絶縁抵抗の使用による容量性負荷駆動のソリューション』(TIPD032)
- 『INA132 低消費電力、単一電源の差動アンプ』(SBOS059)
- 『OPAx192 36V、高精度、レール・ツー・レール入力/出力、低オフセット電圧、e-trim™低入力バイアス電流オペアンプ』(SBOS620)
- 『OPA140 高精度、低ノイズ、レール・ツー・レール出力、11MHz JFETオペアンプ』(SBOS498)
- 『OPA188 高精度、低ノイズ、レール・ツー・レール出力、36V、ゼロドリフトのオペアンプ』(SBOS642)

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 6. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA2172-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4172-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.6 商標

TINA-TI, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
DesignSoft is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2172QDGKQ1	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	18W6	Samples
OPA2172QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	18W6	Samples
OPA4172AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4172Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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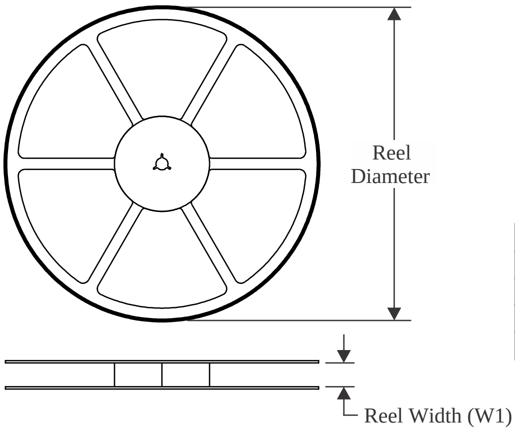
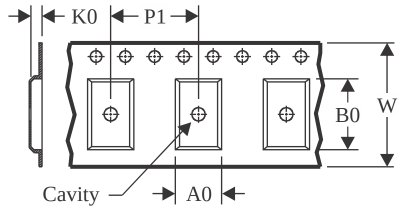
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

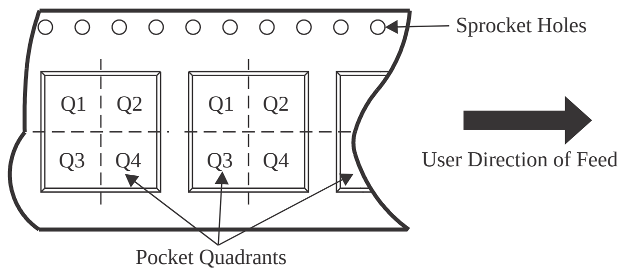


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

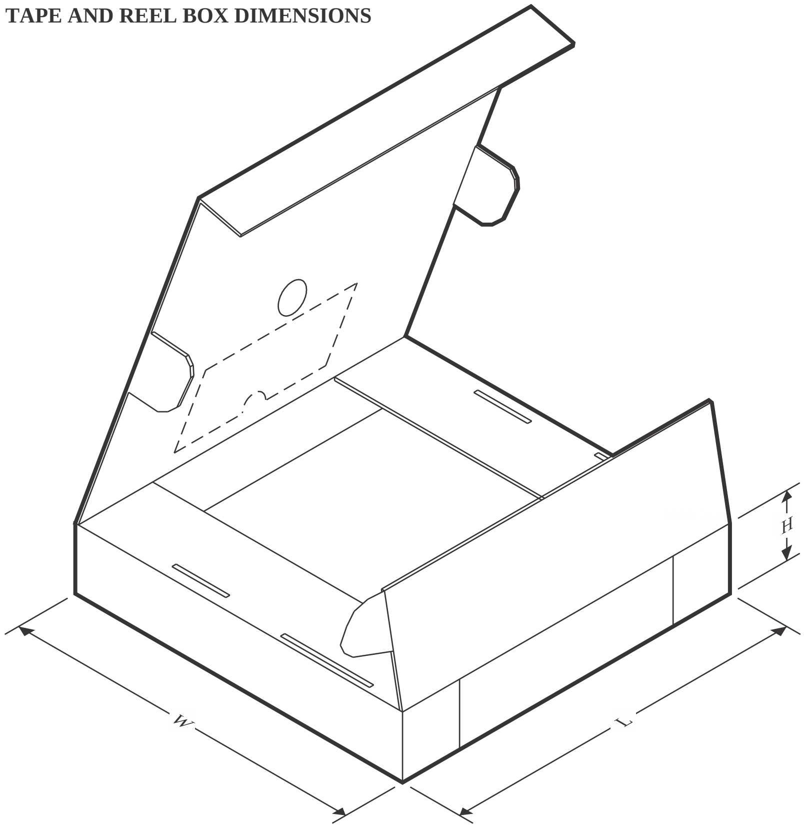
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2172QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA4172AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

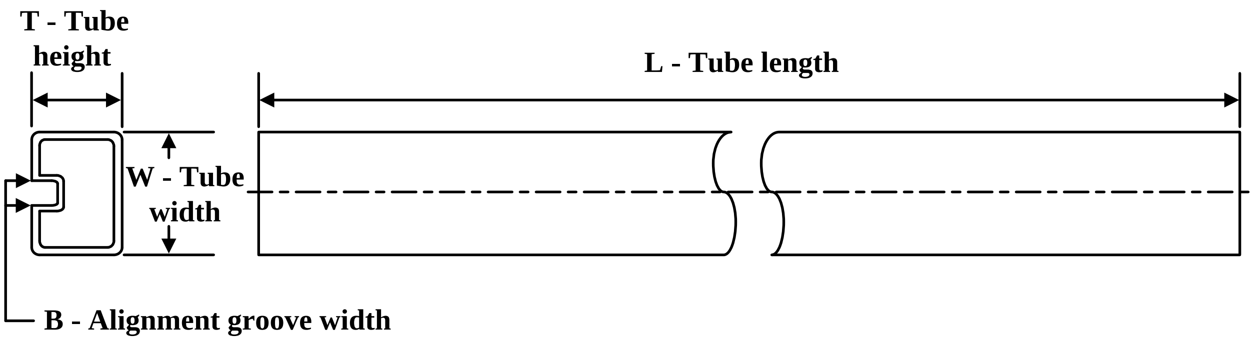
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2172QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA4172AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

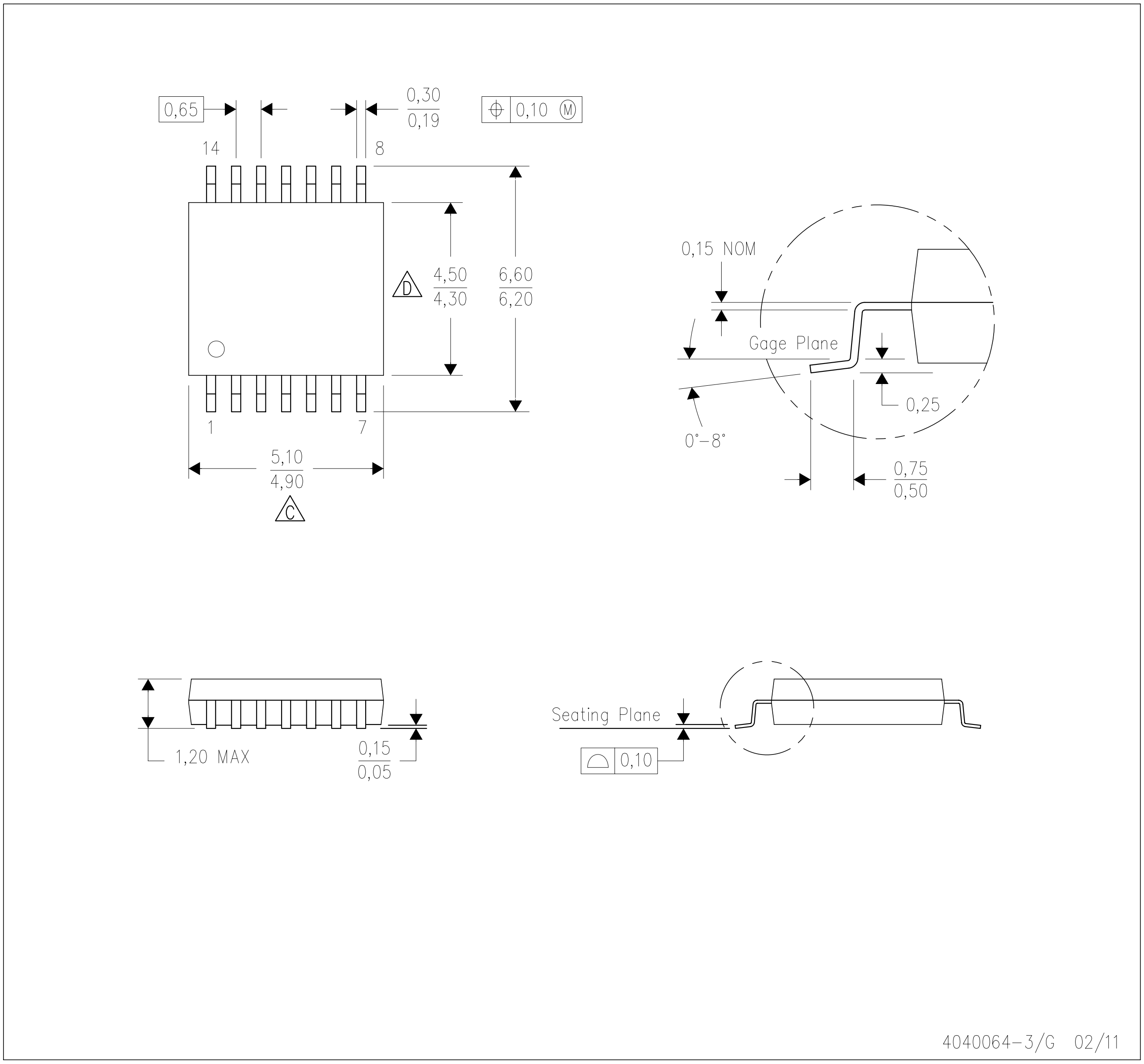
TUBE



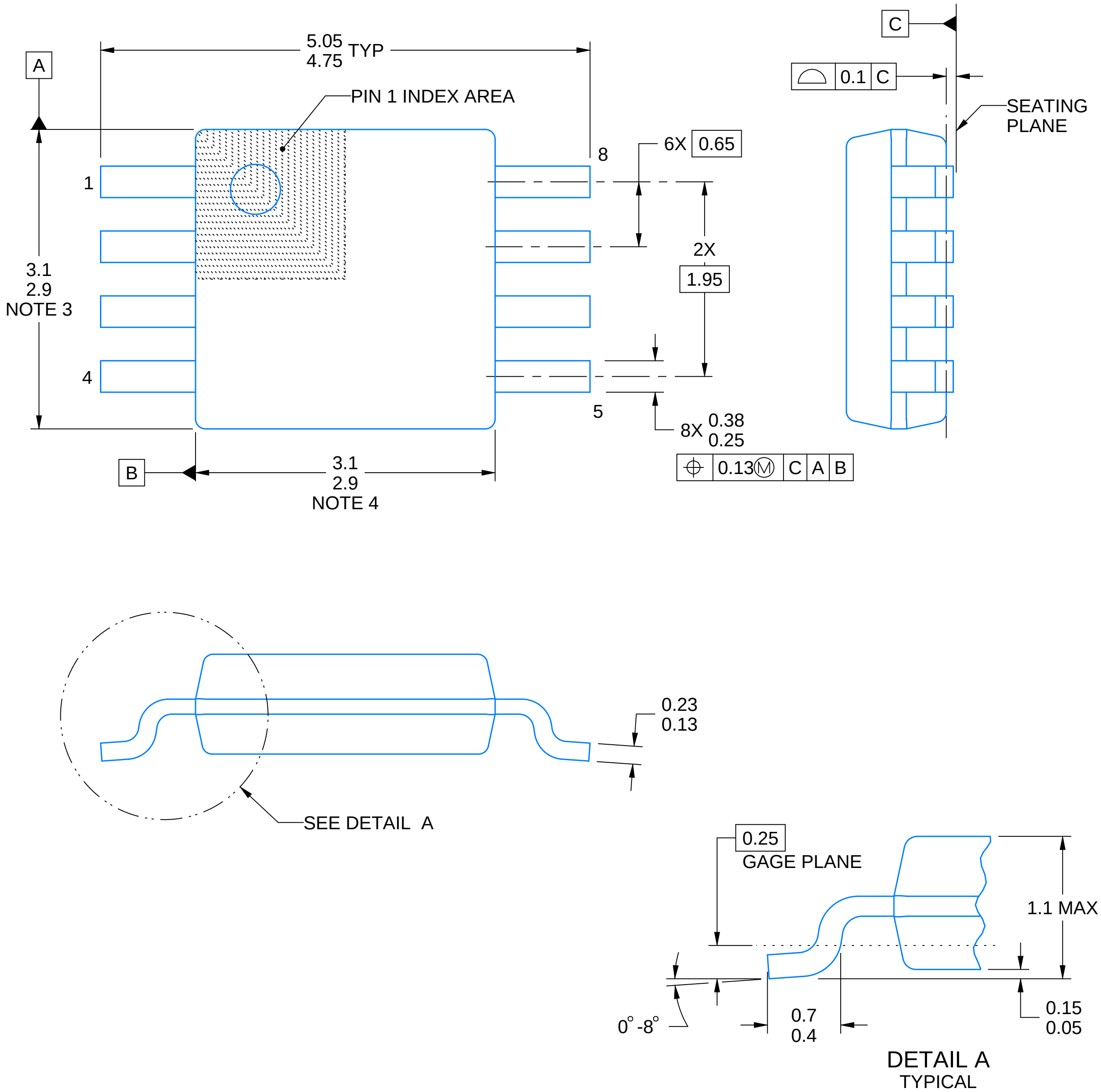
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2172QDGKQ1	DGK	VSSOP	8	80	330	6.55	500	2.88

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153



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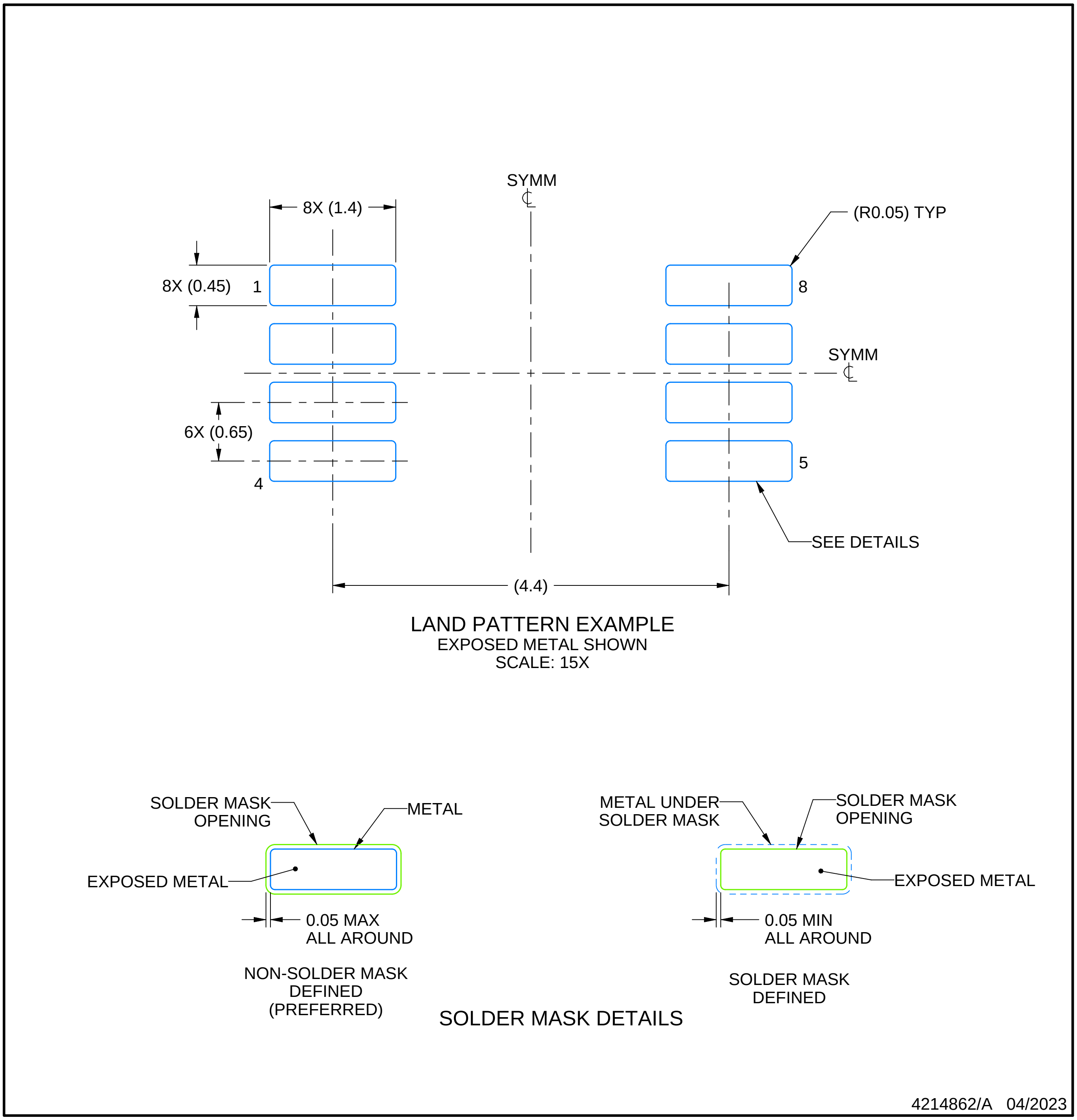
PowerPAD is a trademark of Texas Instruments.

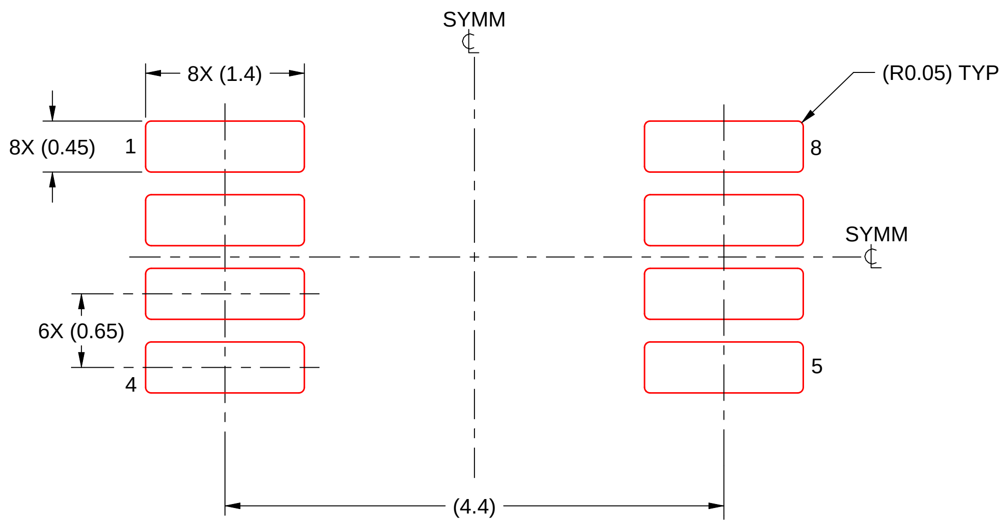
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.