

# OPA2313-Q1 低消費電力、レール・ツー・レール入出力、オフセット標準値500 $\mu$ V、低コスト・システム用1MHzオペアンプ

## 1 特長

- 車載アプリケーション用にAEC-Q100認定済み
  - デバイス温度グレード1
    - 40°C~+125°C, T<sub>A</sub>
- 低コストのシステム用の高精度アンプ
- 低いI<sub>Q</sub>: 50 $\mu$ A/ch
- 広い電源電圧範囲: 1.8V~5.5V
- 低ノイズ: 25nV/ $\sqrt{\text{Hz}}$  (1kHz時)
- ゲイン帯域幅: 1MHz
- レール・ツー・レール入出力
- 低い入力バイアス電流: 0.2pA
- 低いオフセット電圧: 0.5mV
- ユニティ・ゲイン安定
- 内部RFI/EMIフィルタ

## 2 アプリケーション

- インフォテインメント
- エンジン制御ユニット
- 車載照明
- ローサイド・センシング
- バッテリー管理システム
- パッシブ型安全運転支援システム
- 静電容量式センシング
- 燃料ポンプ

## 3 概要

OPA2313-Q1デュアル・チャンネル・オペアンプは、低消費電力と優れた性能を両立した製品です。これによって、インフォテインメント、エンジン制御ユニット、車載用照明など広範な用途に使用できます。OPA2313-Q1はレール・ツー・レール入出力(RRIO)、低い静止電流(標準値50 $\mu$ A)、広い帯域幅(1MHz)、非常に低いノイズ(1kHzにおいて25nV/ $\sqrt{\text{Hz}}$ )が特長で、コストと性能の適切なバランスが必要な各種のアプリケーションに適しています。さらに、入力バイアス電流が小さいため、このデバイスはソース・インピーダンスがメガオーム単位のアプリケーションでも使用できます。

OPA2313-Q1は堅牢に設計されており、150pFまでの容量性負荷に対するユニティ・ゲイン安定性、RFI/EMI除去フィルタの搭載、オーバードライブ状態で位相反転が発生しない、高い静電放電(ESD)保護(4kV HBM)といった特長があるため、回路設計が容易です。

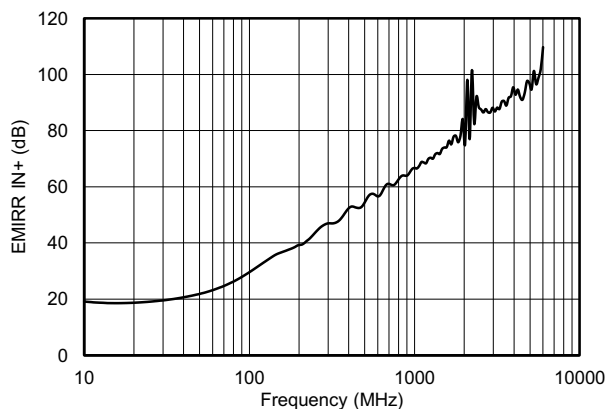
これらのデバイスは、1.8V ( $\pm 0.9$ V)~5.5V ( $\pm 2.75$ V)の電圧で動作するよう最適化され、拡張温度範囲の-40°C ~ +125°Cでの動作が規定されています。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
OPA2313-Q1	SOIC (8)	4.90mmx3.91mm
	VSSOP (8)	3.00mmx3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

### EMIRR IN+と周波数との関係



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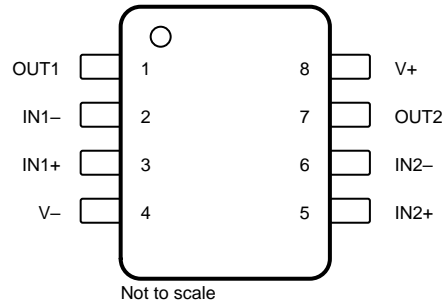
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## 4 改訂履歴

日付	リビジョン	注
2018年12月	*	初版

## 5 Pin Configuration and Functions

**OPA2313-Q1 D, DGK Packages  
8-Pin SOIC, VSSOP  
Top View**



**Pin Functions: OPA2313-Q1**

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1-	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2-	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V-	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply voltage (V+) – (V–)	0	7	V
	Signal input terminals <sup>(2)</sup>	(V–) – (0.5)	(V+) + 0.5	
Current	Signal input terminals <sup>(2)</sup>	–10	10	mA
	Output short circuit <sup>(3)</sup>	Continuous		
Temperature	Operating, T <sub>A</sub>	–40	150	°C
	Junction, T <sub>J</sub>		150	
	Storage, T <sub>stg</sub>	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> HBM ESD Classification Level 3A	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> CDM ESD Classification Level C6	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage (V+) – (V–)	1.8	5.5	V
T <sub>A</sub>	Specified temperature	–40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		OPA2313-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 Pins	8 Pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	138.4	191.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	89.5	61.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	78.6	111.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	29.9	5.1	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	78.1	110.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics: 5.5 V<sup>(1)</sup>

For  $V_S = (V+) - (V-) = 5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage			0.5	2.5	mV
$dV_{OS}/dT$	Input offset voltage vs temperature	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		2		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	74	90		dB
	Channel separation, dc	At dc		10		$\mu\text{V}/\text{V}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	No phase reversal, rail-to-rail input	$(V-) - 0.2$		$(V+) + 0.2$	V
CMRR	Common-mode rejection ratio	$(V-) - 0.2\text{ V} < V_{CM} < (V+) - 1.3\text{ V}$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	70	85	dB
		$V_{CM} = -0.2\text{ V}$ to $5.7\text{ V}$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	64	80	
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current			$\pm 0.2$	$\pm 10$	pA
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ <sup>(2)</sup>		$\pm 50$	
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ <sup>(2)</sup>		$\pm 600$	
$I_{OS}$	Input offset current			$\pm 0.2$	$\pm 10$	pA
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ <sup>(2)</sup>		$\pm 50$	
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ <sup>(2)</sup>		$\pm 600$	
<b>NOISE</b>						
	Input voltage noise (peak-to-peak)	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		6		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$f = 10\text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25		
$i_n$	Input current noise density	$f = 1\text{ kHz}$		5		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT CAPACITANCE</b>						
$C_{IN}$	Differential			1		pF
	Common-mode			5		
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$0.05\text{ V} < V_O < (V+) - 0.05\text{ V}$ , $R_L = 100\text{ k}\Omega$		90	104	dB
		$0.3\text{ V} < V_O < (V+) - 0.3\text{ V}$ , $R_L = 2\text{ k}\Omega$		100	110	
		$0.1\text{ V} < V_O < (V+) - 0.1\text{ V}$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	104	116	
	Phase margin	$V_S = 5\text{ V}$ , $G = +1$		65		$^\circ$
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product	$V_S = 5\text{ V}$ , $C_L = 10\text{ pF}$		1		MHz
SR	Slew rate	$V_S = 5\text{ V}$ , $G = +1$		0.5		$\text{V}/\mu\text{s}$
$t_S$	Settling time	To 0.1%, $V_S = 5\text{ V}$ , 2-V step, $G = +1$		5		$\mu\text{s}$
		To 0.01%, $V_S = 5\text{ V}$ , 2-V step, $G = +1$		6		
	Overload recovery time	$V_S = 5\text{ V}$ , $V_{IN} \times \text{Gain} > V_S$		3		
THD+N	Total harmonic distortion + noise <sup>(3)</sup>	$V_S = 5\text{ V}$ , $V_O = 1\text{ V}_{RMS}$ , $G = +1$ , $f = 1\text{ kHz}$		0.0045%		
<b>OUTPUT</b>						
$V_O$	Voltage output swing from supply rails	$R_L = 100\text{ k}\Omega$ <sup>(2)</sup>		5	20	mV
		$R_L = 100\text{ k}\Omega$ <sup>(2)</sup>	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		30	
		$R_L = 2\text{ k}\Omega$ <sup>(2)</sup>		75	100	
		$R_L = 2\text{ k}\Omega$ <sup>(2)</sup>	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		125	
$I_{SC}$	Short-circuit current			$\pm 15$		mA
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		$\pm 12$	
$R_O$	Open-loop output impedance			2300		$\Omega$

(1) Parameters with minimum or maximum specification limits are 100% production tested at  $25^\circ\text{C}$ , unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.

(2) Specified by design and characterization; not production tested.

(3) Third-order filter; bandwidth = 80 kHz at  $-3\text{ dB}$ .

**Electrical Characteristics: 5.5 V<sup>(1)</sup> (continued)**

For  $V_S = (V+) - (V-) = 5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>							
$V_S$	Specified voltage range			1.8 ( $\pm 0.9$ )		5.5 ( $\pm 2.75$ )	V
$I_Q$	Quiescent current per amplifier	$V_S = 5\text{ V}$ , $I_O = 0\text{ mA}$			50	60	$\mu\text{A}$
		$V_S = 5\text{ V}$ , $I_O = 0\text{ mA}$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$			85	
	Power-on time	$V_S = 0\text{ V}$ to $5\text{ V}$ , to 90% $I_Q$ level			10		$\mu\text{s}$

## 6.6 Electrical Characteristics: 1.8 V<sup>(1)</sup>

For  $V_S = (V+) - (V-) = 1.8\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_{S+} - 1.3\text{ V}$ , and  $V_{OUT} = V_S / 2$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>							
$V_{OS}$	Input offset voltage				0.5	2.5	mV
$dV_{OS}/dT$	Input offset voltage vs temperature		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		2		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	74	90		dB
	Channel separation, dc	At dc			10		$\mu\text{V}/\text{V}$
<b>INPUT VOLTAGE RANGE</b>							
$V_{CM}$	Common-mode voltage range	No phase reversal, rail-to-rail input		$(V-) - 0.2$		$(V+) + 0.2$	V
CMRR	Common-mode rejection ratio	$(V-) - 0.2\text{ V} < V_{CM} < (V+) - 1.3\text{ V}$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	70	85		dB
		$V_S = 1.8\text{ V}$ , $V_{CM} = -0.2\text{ V}$ to $1.8\text{ V}$		58	73		
		$V_{CM} = -0.2\text{ V}$ to $1.6\text{ V}$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	58	70		
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current				$\pm 0.2$	$\pm 10$	pA
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ <sup>(2)</sup>			$\pm 50$	
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ <sup>(2)</sup>			$\pm 600$	
$I_{OS}$	Input offset current				$\pm 0.2$	$\pm 10$	pA
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ <sup>(2)</sup>			$\pm 50$	
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ <sup>(2)</sup>			$\pm 600$	
<b>NOISE</b>							
	Input voltage noise (peak-to-peak)	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$			6		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$f = 10\text{ kHz}$			22		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			25		
$i_n$	Input current noise density	$f = 1\text{ kHz}$			5		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT CAPACITANCE</b>							
$C_{IN}$	Differential				1		pF
	Common-mode				5		
<b>OPEN-LOOP GAIN</b>							
$A_{OL}$	Open-loop voltage gain	$0.05\text{ V} < V_O < (V+) - 0.05\text{ V}$ , $R_L = 100\text{ k}\Omega$		100	110		dB
		$0.1\text{ V} < V_O < (V+) - 0.1\text{ V}$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	90	110		
<b>FREQUENCY RESPONSE</b>							
GBW	Gain-bandwidth product	$C_L = 10\text{ pF}$			0.9		MHz
SR	Slew rate	$G = +1$			0.45		$\text{V}/\mu\text{s}$
$t_s$	Settling time	To 0.1%, $V_S = 5\text{ V}$ , 2-V step, $G = +1$			5		$\mu\text{s}$
		To 0.01%, $V_S = 5\text{ V}$ , 2-V step, $G = +1$			6		
	Overload recovery time	$V_S = 5\text{ V}$ , $V_{IN} \times \text{Gain} > V_S$			3		
THD+N	Total harmonic distortion + noise <sup>(3)</sup>	$V_S = 5\text{ V}$ , $V_O = 1\text{ V}_{RMS}$ , $G = +1$ , $f = 1\text{ kHz}$			0.0045%		
<b>OUTPUT</b>							
$V_O$	Voltage output swing from supply rails	$R_L = 100\text{ k}\Omega$ <sup>(2)</sup>			5	15	mV
		$R_L = 100\text{ k}\Omega$ <sup>(2)</sup>	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$			30	
		$R_L = 2\text{ k}\Omega$ <sup>(2)</sup>			25	50	
		$R_L = 2\text{ k}\Omega$ <sup>(2)</sup>	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$			125	
$I_{SC}$	Short-circuit current				$\pm 6$		mA
$R_O$	Open-loop output impedance				2300		$\Omega$

(1) Parameters with minimum or maximum specification limits are 100% production tested at  $25^\circ\text{C}$ , unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.

(2) Specified by design and characterization; not production tested.

(3) Third-order filter; bandwidth = 80 kHz at  $-3\text{ dB}$ .

**Electrical Characteristics: 1.8 V<sup>(1)</sup> (continued)**

For  $V_S = (V+) - (V-) = 1.8 \text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10 \text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_{S+} - 1.3 \text{ V}$ , and  $V_{OUT} = V_S / 2$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage range		1.8 ( $\pm 0.9$ )		5.5 ( $\pm 2.75$ )	V
$I_Q$	Quiescent current per amplifier	$V_S = 5 \text{ V}$ , $I_O = 0 \text{ mA}$		50	60	$\mu\text{A}$
	Power-on time	$V_S = 0 \text{ V}$ to $5 \text{ V}$ , to 90% $I_Q$ level		10		$\mu\text{s}$



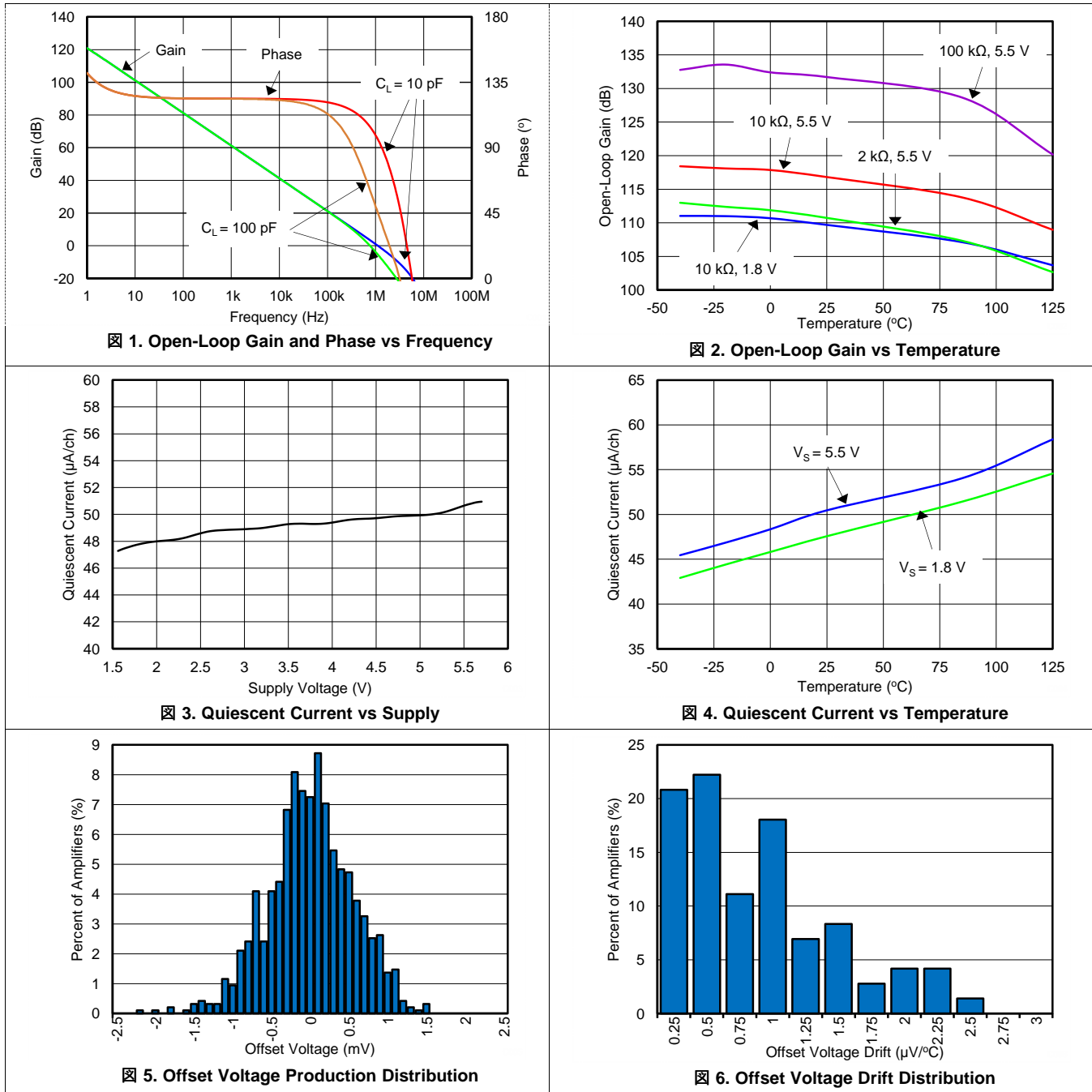
## 6.7 Typical Characteristics: Tables of Graphs

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THD+N vs Amplitude ( $G = +1, 2\text{ k}\Omega, 10\text{ k}\Omega$ )	<a href="#">图 30</a>
THD+N vs Amplitude ( $G = -1, 2\text{ k}\Omega, 10\text{ k}\Omega$ )	<a href="#">图 31</a>
THD+N vs Frequency (0.5 $V_{\text{RMS}}$ , $G = +1, 2\text{ k}\Omega, 10\text{ k}\Omega$ )	<a href="#">图 32</a>
EMIRR IN+ vs Frequency	<a href="#">图 33</a>

### 6.8 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , unless otherwise noted.



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , unless otherwise noted.

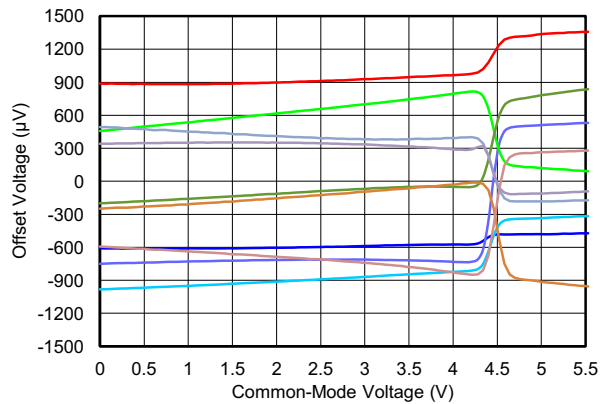


Fig 7. Offset Voltage vs Common-Mode Voltage

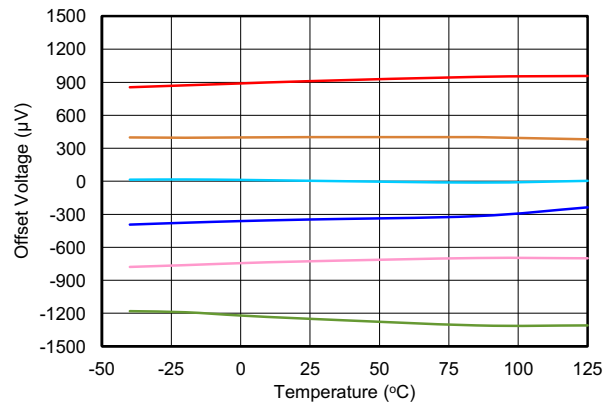


Fig 8. Offset Voltage vs Temperature

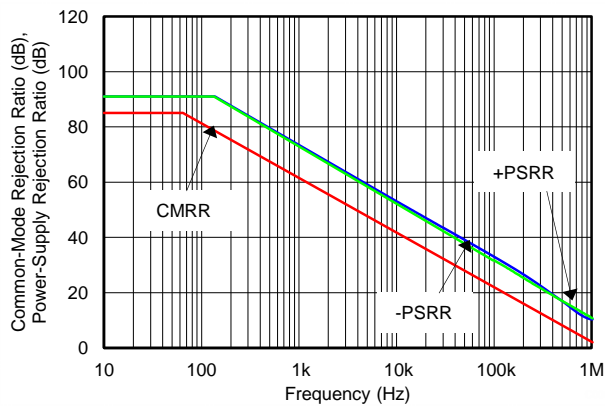


Fig 9. CMRR and PSRR vs Frequency (Referred-to-Input)

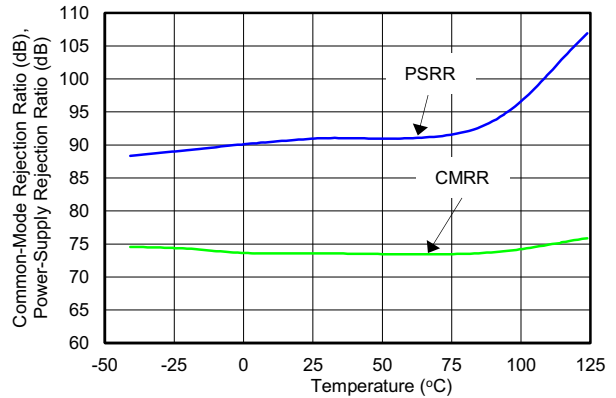


Fig 10. CMRR and PSRR vs Temperature

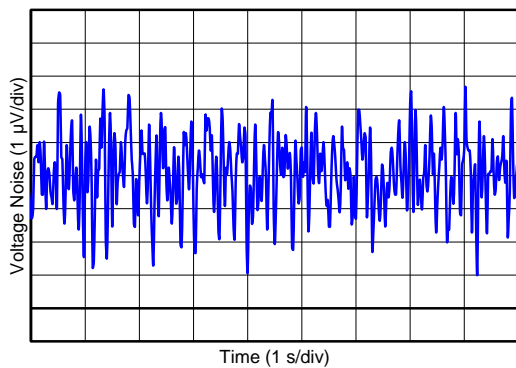


Fig 11. 0.1-Hz to 10-Hz Input Voltage Noise

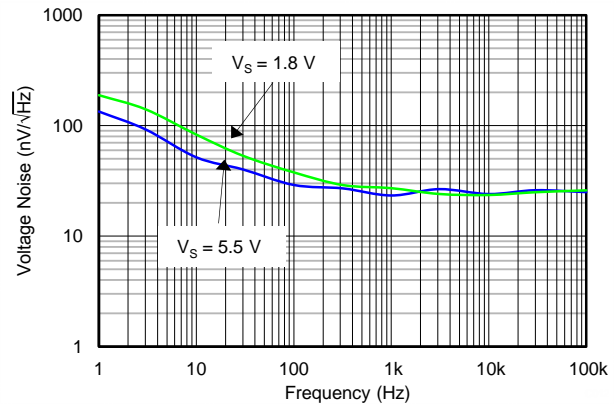
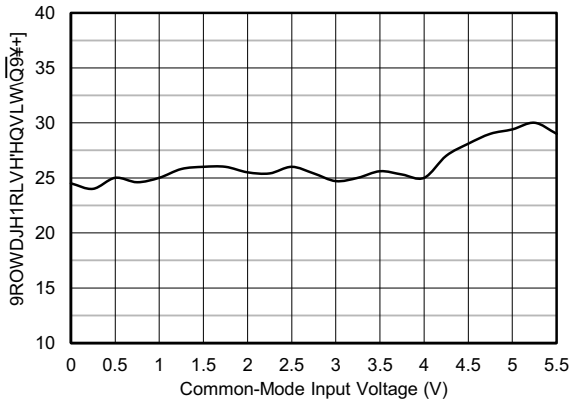


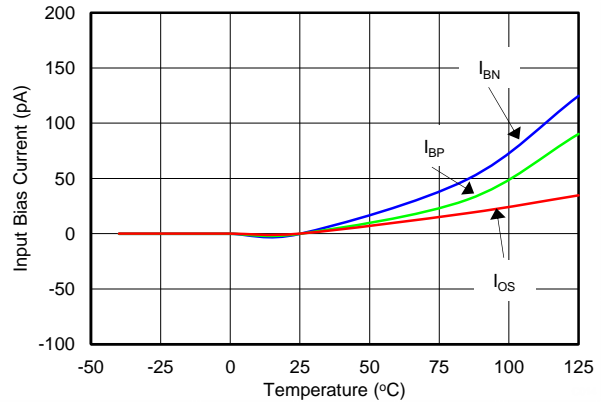
Fig 12. Input Voltage Noise Spectral Density vs Frequency

**Typical Characteristics (continued)**

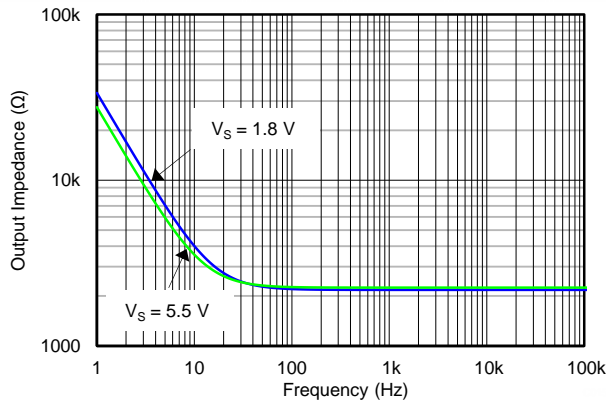
At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , unless otherwise noted.



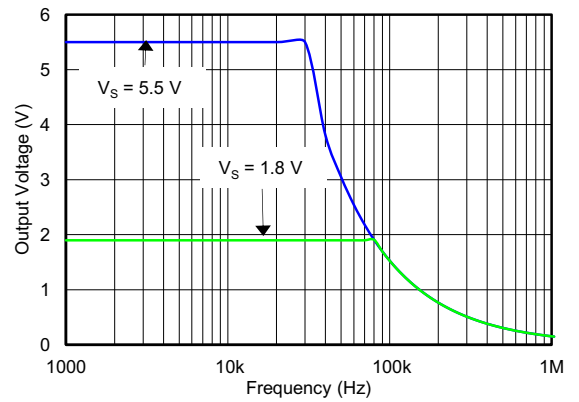
**13. Voltage Noise vs Common-Mode Voltage**



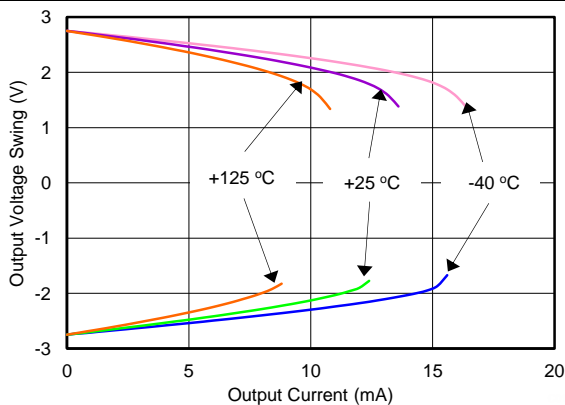
**14. Input Bias and Offset Current vs Temperature**



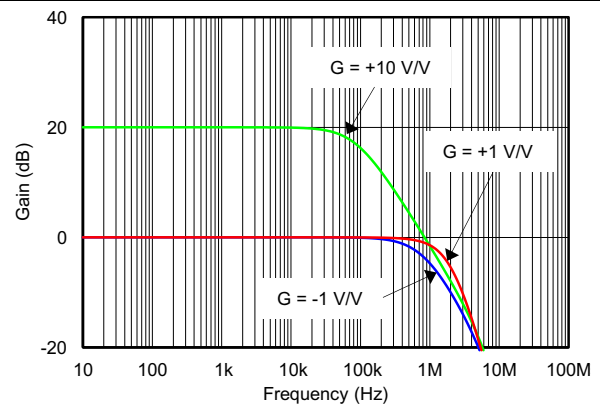
**15. Open-Loop Output Impedance vs Frequency**



**16. Maximum Output Voltage vs Frequency and Supply Voltage**



**17. Output Voltage Swing vs Output Current (Over Temperature)**



**18. Closed-Loop Gain vs Frequency (Minimum Supply)**

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , unless otherwise noted.

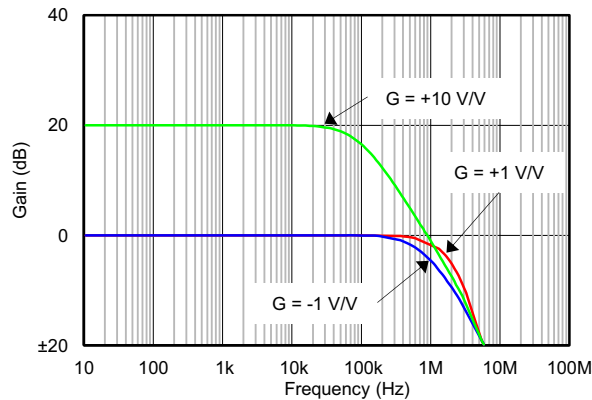


Figure 19. Closed-Loop Gain vs Frequency (Maximum Supply)

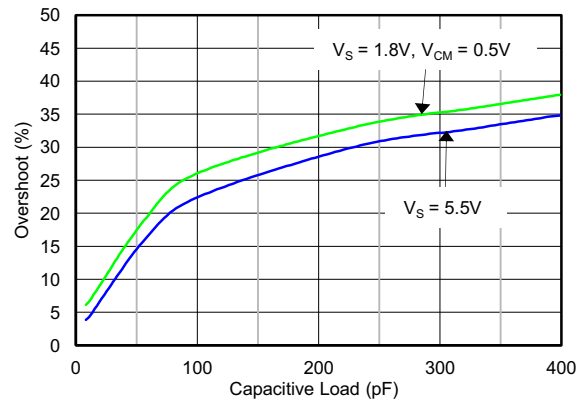


Figure 20. Small-Signal Overshoot vs Load Capacitance

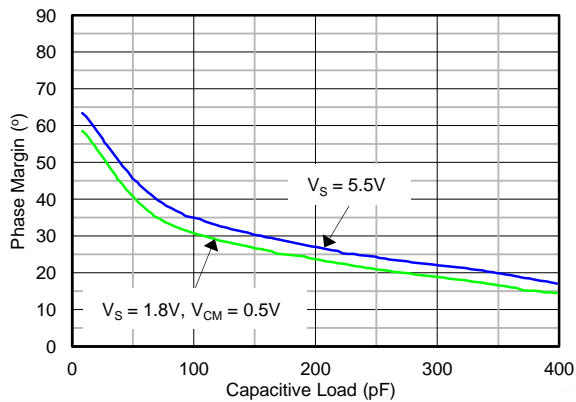


Figure 21. Phase Margin vs Capacitive Load

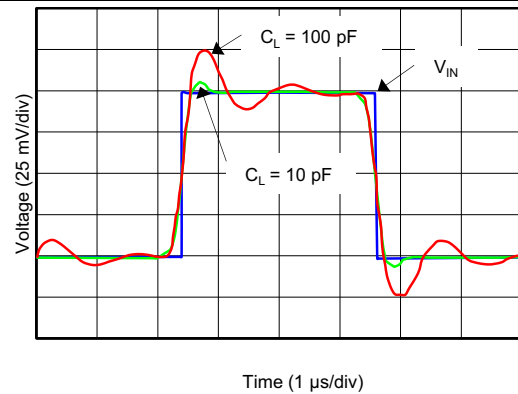


Figure 22. Small-Signal Pulse Response (Minimum Supply)

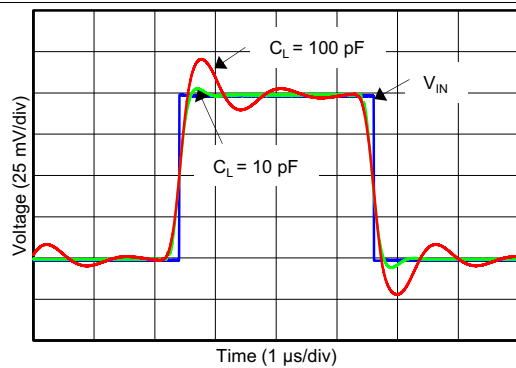


Figure 23. Small-Signal Pulse Response (Maximum Supply)

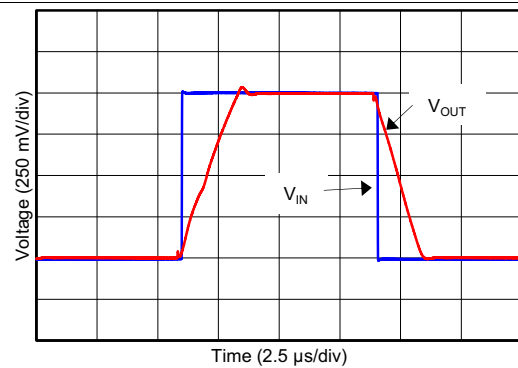
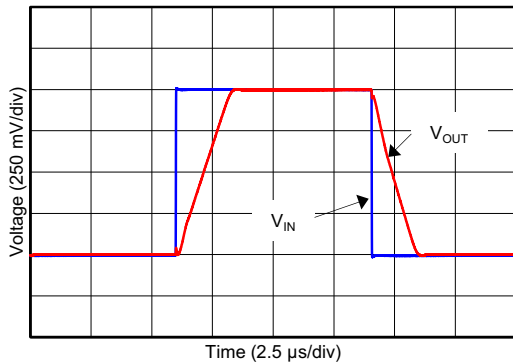


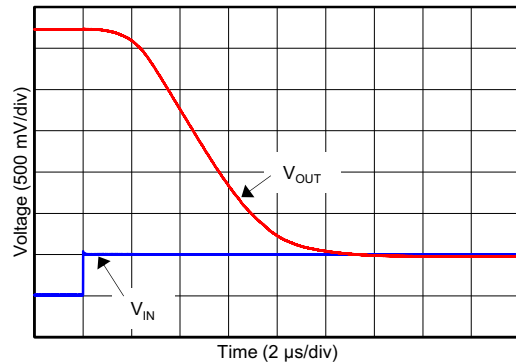
Figure 24. Large-Signal Pulse Response (Minimum Supply)

**Typical Characteristics (continued)**

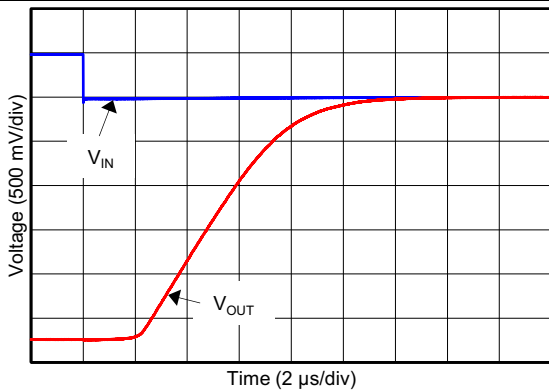
At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , unless otherwise noted.



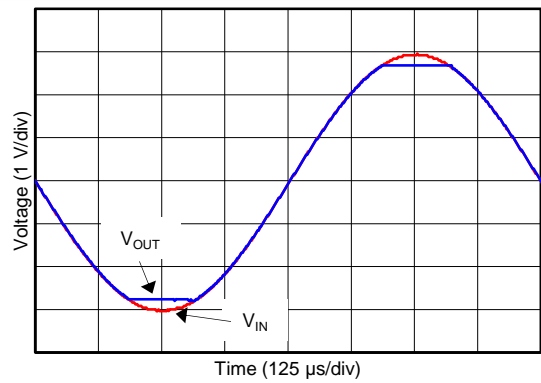
**Figure 25. Large-Signal Pulse Response (Maximum Supply)**



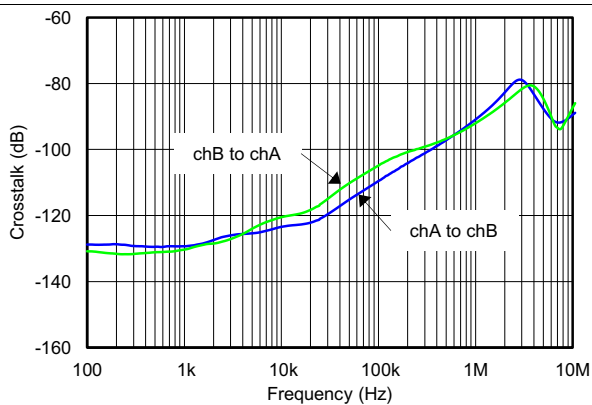
**Figure 26. Positive Overload Recovery**



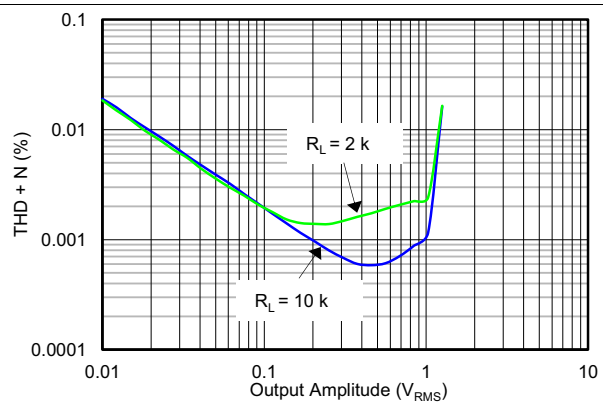
**Figure 27. Negative Overload Recovery**



**Figure 28. No Phase Reversal**



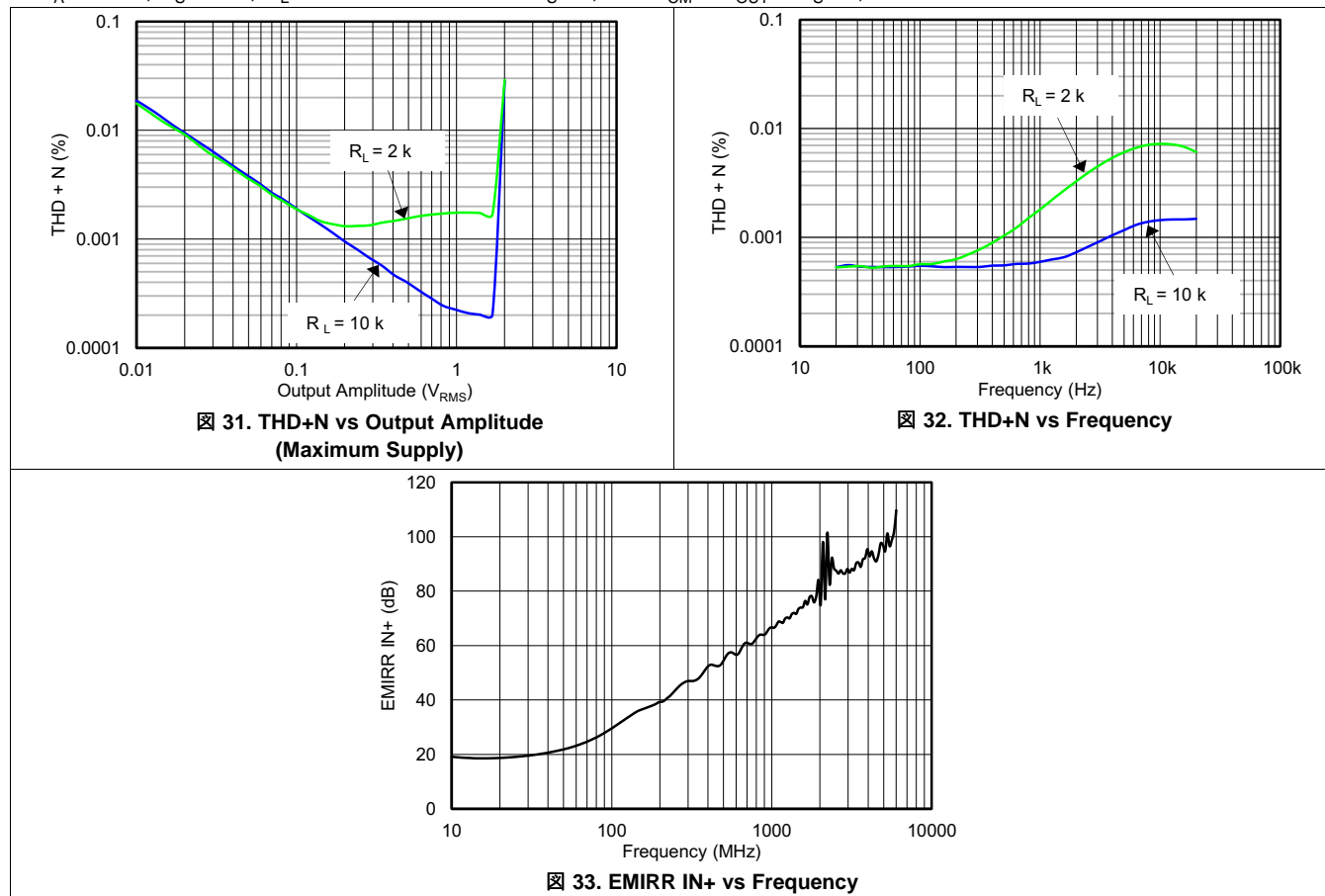
**Figure 29. Channel Separation vs Frequency**



**Figure 30. THD+N vs Output Amplitude (Minimum Supply)**

**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{CM} = V_{OUT} = V_S / 2$ , unless otherwise noted.



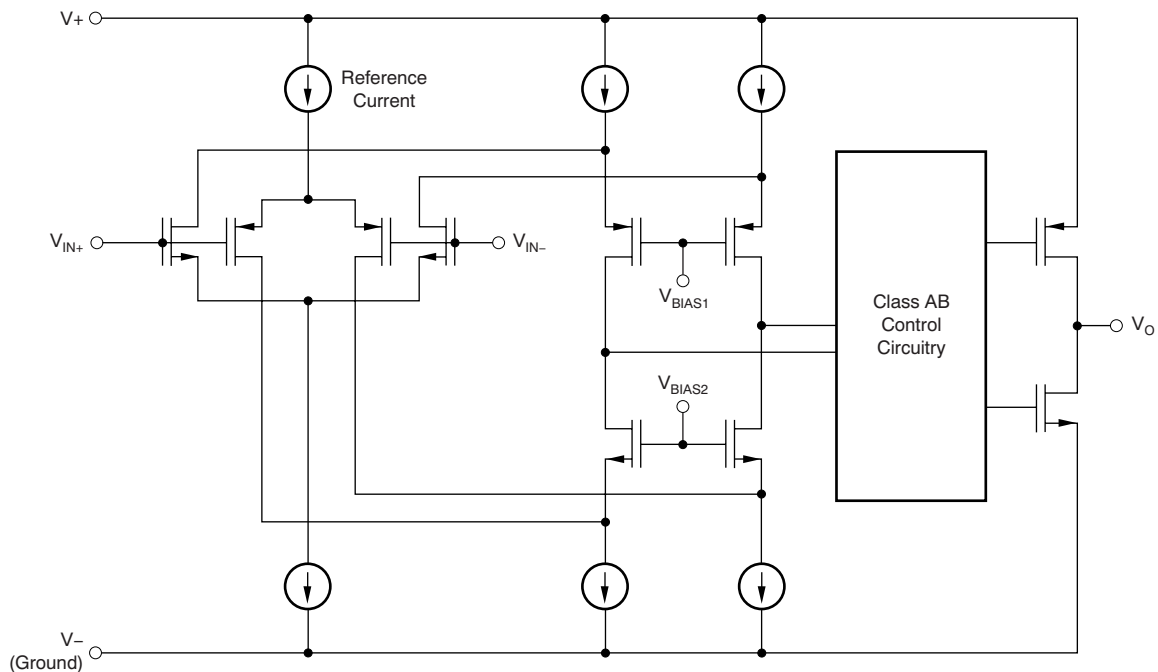
## 7 Detailed Description

### 7.1 Overview

The OPA2313-Q1 is a low-power, rail-to-rail input and output operational amplifier designed for cost-constrained applications. This device operates from 1.8 V to 5.5 V, is unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving loads greater than 10-k $\Omega$  connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2313-Q1 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes this device ideal for driving sampling analog-to-digital converters (ADCs).

The OPA2313-Q1 features 1-MHz bandwidth and 0.5-V/ $\mu$ s slew rate with only 50- $\mu$ A supply current per channel, providing good ac performance at very low power consumption. Low frequency (dc) applications are also well served with a low input noise voltage of 25 nV/ $\sqrt{\text{Hz}}$  at 1 kHz, low input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical). The typical offset voltage drift is 2  $\mu$ V/ $^{\circ}\text{C}$ ; over the full temperature range the input offset voltage changes only 200  $\mu$ V (0.5 mV to 0.7 mV).

### 7.2 Functional Block Diagram





## 7.3 Feature Description

### 7.3.1 Operating Voltage

The OPA2313-Q1 device is fully specified and tested from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V). Parameters that vary with supply voltage are illustrated in the [Typical Characteristics](#) section.

### 7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPA2313-Q1 device extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#) section. The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.3$  V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately  $(V+) - 1.3$  V. There is a small transition region, typically  $(V+) - 1.4$  V to  $(V+) - 1.2$  V, in which both pairs are on. This 200-mV transition region may vary up to 300 mV with process variation. Thus, the transition region (both stages on) may range from  $(V+) - 1.7$  V to  $(V+) - 1.5$  V on the low end, up to  $(V+) - 1.1$  V to  $(V+) - 0.9$  V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

### 7.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPA2313-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 k $\Omega$ , the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails, as shown in [Figure 17](#).

### 7.3.4 Common-Mode Rejection Ratio (CMRR)

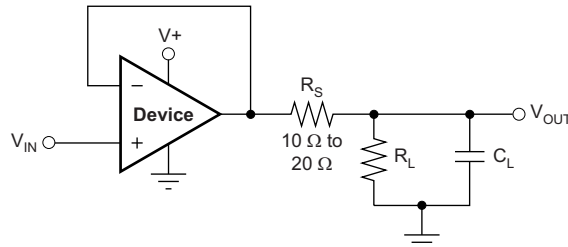
CMRR for the OPA2313-Q1 device is specified in several ways so the best match for a given application may be used; see the [Electrical Characteristics](#). First, the CMRR of the device in the common-mode range below the transition region ( $V_{CM} < (V+) - 1.3$  V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at ( $V_{CM} = -0.2$  V to 5.7 V). This last value includes the variations seen through the transition region, as shown in [Figure 7](#).

### 7.3.5 Capacitive Load and Stability

The OPA2313-Q1 device is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA2313-Q1 device may become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in the unity-gain ( $+1$ -V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA2313-Q1 device remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some capacitors ( $C_L$  greater than 1  $\mu$ F) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graph, [Figure 20](#).

## Feature Description (continued)

One technique for increasing the capacitive load drive capability of the amplifier when it operates in a unity-gain configuration is to insert a small resistor, typically  $10\ \Omega$  to  $20\ \Omega$ , in series with the output, as shown in [Figure 34](#). This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.



**Figure 34. Improving Capacitive Load Drive**

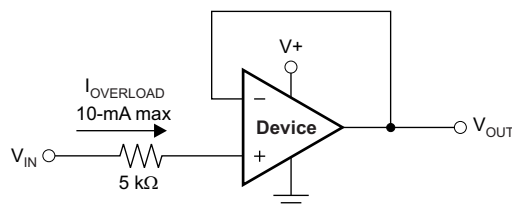
### 7.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions may be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA2313-Q1 device incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a common-mode cutoff frequency of approximately 35 MHz ( $-3\ \text{dB}$ ), with a rolloff of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. [Figure 33](#) illustrates the results of this testing on the OPA2313-Q1 device. Detailed information may be found in [EMI Rejection Ratio of Operational Amplifiers](#), available for download from [www.ti.com](http://www.ti.com).

### 7.3.7 Input and ESD Protection

The OPA2313-Q1 device incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. The ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#). [Figure 35](#) shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.



**Figure 35. Input Current Protection**

## 7.4 Device Functional Modes

The OPA2313-Q1 device has a single functional mode. The device is powered on as long as the power-supply voltage is between 1.8 V ( $\pm 0.9\ \text{V}$ ) and 5.5 V ( $\pm 2.75\ \text{V}$ ).

## 8 Application and Implementation

### 注

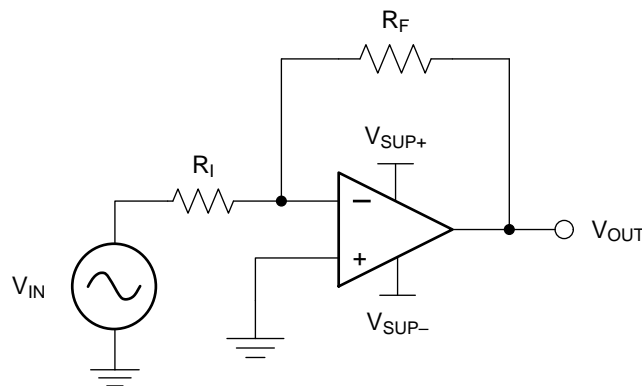
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The OPA2313-Q1 device is a low-power, rail-to-rail input and output operational amplifier. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is designed for a wide range of general-purpose applications. The class AB output stage is capable of driving loads greater than 10 kΩ connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2313-Q1 to be used in virtually any single-supply application.

### 8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in [Figure 36](#). An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification may be added by selecting the input resistor (R<sub>I</sub>) and the feedback resistor (R<sub>F</sub>).



**Figure 36. Inverting Amplifier Application**

#### 8.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V<sub>CM</sub>) and the output voltage swing to the rails (V<sub>O</sub>) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

#### 8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

### Typical Application (continued)

When the desired gain is determined, choose a value for  $R_1$  or  $R_F$ . Choosing a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of kilohms) draw the smallest current but generate the highest noise. Small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 k $\Omega$  for  $R_1$ , resulting in a 36-k $\Omega$  resistor being used for  $R_F$ . The values are determined by 式 3:

$$A_V = -\frac{R_F}{R_1} \tag{3}$$

### 8.2.3 Application Curve

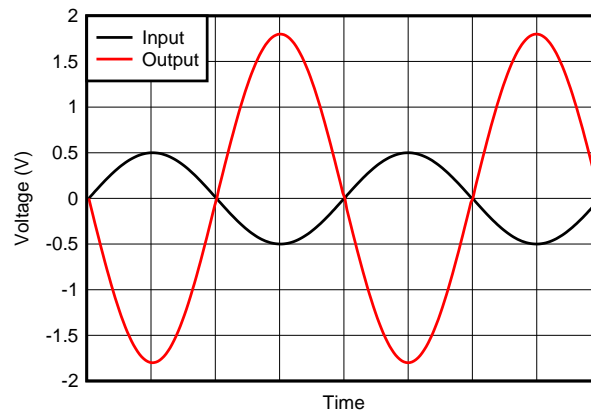
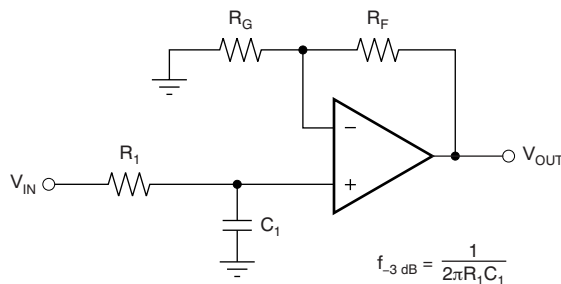


图 37. Inverting Amplifier Input and Output

### 8.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in 图 38.

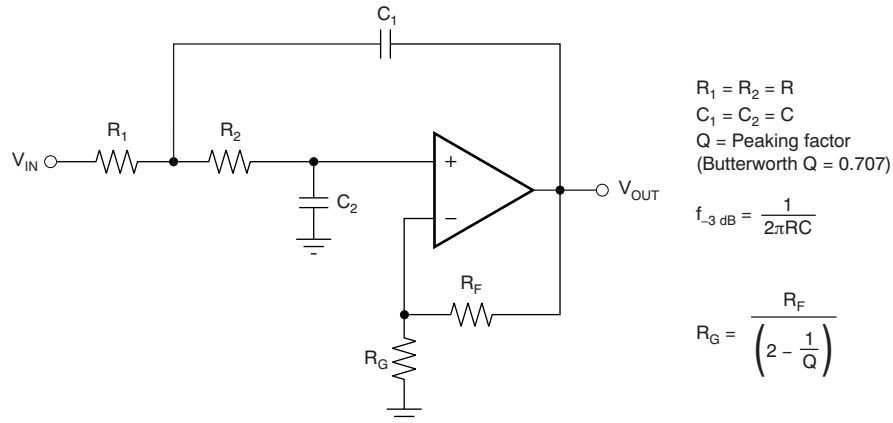


$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

图 38. Single-Pole Low-Pass Filter

## System Examples (continued)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter may be used for this task, as shown in [Figure 39](#). For best results, the amplifier must have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to follow this guideline may result in phase shift of the amplifier.



**Figure 39. Two-Pole, Low-Pass, Sallen-Key Filter**

## 9 Power Supply Recommendations

The OPA2313-Q1 device is specified for operation from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V); many specifications apply from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . The [Typical Characteristics](#) section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

### 注意

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#) table).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#) section.

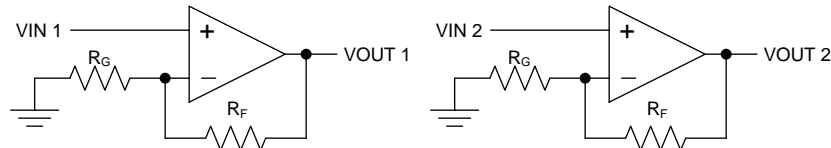
## 10 Layout

### 10.1 Layout Guidelines

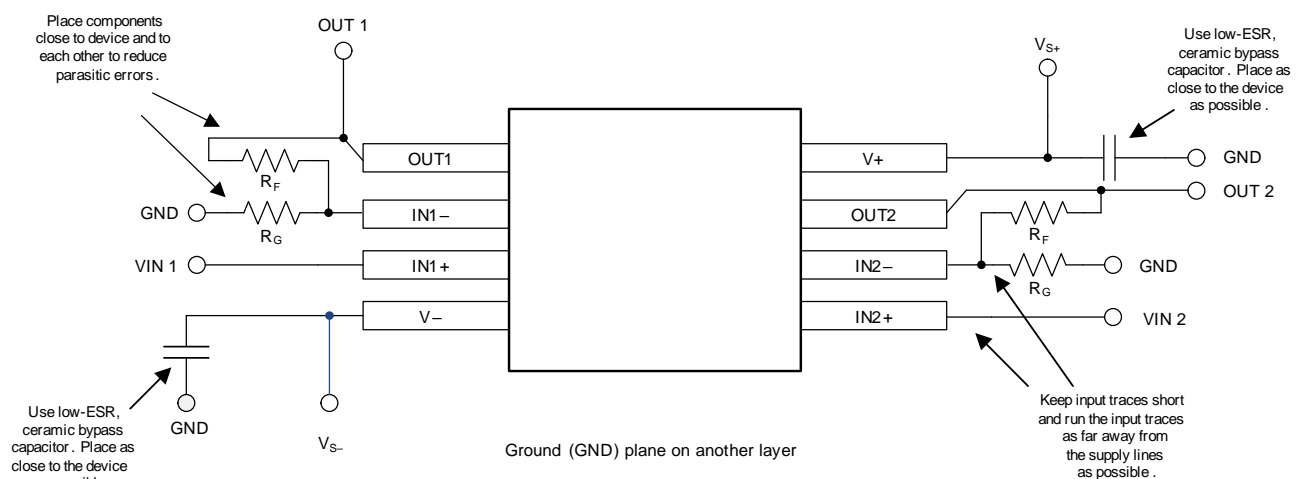
For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise may propagate into analog circuitry through the power pins of the circuit and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If the traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep  $R_F$  and  $R_G$  close to the inverting input to minimize parasitic capacitance, as shown in [40](#).
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.

### 10.2 Layout Example



**40. Schematic Representation for 41**



**41. Layout Example**

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントのサポート

#### 11.1.1 関連資料

関連資料については、以下を参照してください。

- 『オペアンプのEMI除去率』
- 『基板のレイアウト技法』

### 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.3 コミュニティ・リソース

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### 11.4 商標

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### 11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2313QDGKRQ1</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	23131
OPA2313QDGKRQ1.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	23131
<a href="#">OPA2313QDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2313Q
OPA2313QDRQ1.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2313Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF OPA2313-Q1 :**



- Catalog : [OPA2313](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2313QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2313QDRQ1	SOIC	D	8	2500	340.5	336.1	25.0

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

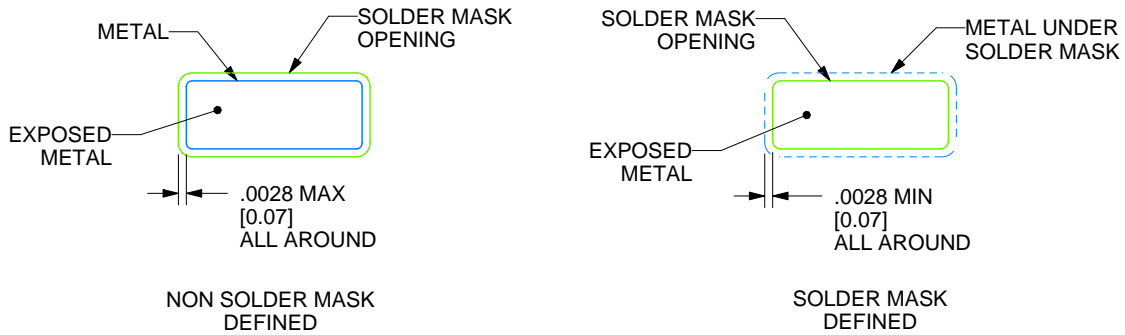
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月