OPA2830 デュアル、低消費電力、単一電源、広帯域オペアンプ

1 特長

- 広い帯域幅:
  - 230MHz (ゲイン = +1)
  - 100MHz (ゲイン = +2)
- 低い消費電流: 8.8mA (V_S = 5V)
- フレキシブルな電源電圧範囲:
  - デュアル電源:±1.5V～±5.5V
  - シングル電源:3V～11V
- シングル電源の場合、入力範囲はグランドまで対応
- 出力スイング:5V 電源で 4.82V
- 高いスルーレート:500V/µs
- 小さい入力電圧ノイズ:9.2nV/√Hz
- パッケージ:VSSOP-8

2 アプリケーション

- 単一電源 A/D コンバータ (ADC) の入力バッファ
- 単一電源 ビデオ ライン ドライバ
- CCD イメージング チャネル
- 低消費電力超音波
- PLL 積分器
- 携帯型消費者向け電子機器

3 概要

OPA2830 は、デュアル、低消費電力、単一電源、広帯域、電圧帰還型アンプであり、3V または 5V の単一電源で動作するよう設計されています。このデバイスは、±5V または +10V 電源での動作もサポートしています。入力範囲は、負の電源よりも下から始まり、正の電源の 1.8V 内側までとなっています。相補的共通エミッタ出力を使用することにより、150Ω を駆動して、どちらの電源からも 25mV 以内の出力スイングが得られます。また、大きい出力駆動電流 (±75mA) と、小さい差動ゲインおよび位相誤差により、このデバイスは単一電源の消費者向けビデオ製品に最適です。

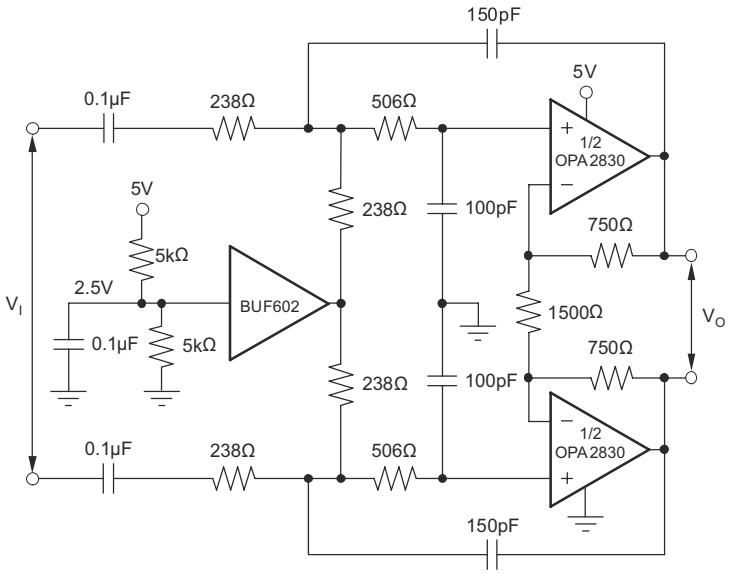
大きいゲイン帯域幅積 (100MHz) とスルーレート (500V/µs) により低歪み動作を実現しているため、OPA2830 は 3V および 5V CMOS ADC への優れた入力バッファ段となります。他の低消費電力、単電源のアンプとは異なり、信号振幅が小さくなるにつれて歪み性能は向上します。入力電圧ノイズが 9.2nV/√Hz と低いため、広いダイナミック レンジでの動作に対応できます。

OPA2830 は業界標準の SO-8 パッケージで供給されます。OPA2830 は 小型の VSSOP-8 パッケージでも供給されます。固定ゲインおよびライン ドライバ アプリケーションについては、OPA2832 をご検討ください。

パッケージ情報

部品番号 (1)	パッケージ (2)	パッケージ サイズ (3)
OPA2830	D (SOIC、8)	4.9mm × 6mm
	DGK (VSSOP、8)	3mm × 3mm

(1) セクション 4 を参照してください。
(2) 詳細については、セクション 11 を参照してください。
(3) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



DC 結合、3V ADC ドライバ

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4 Device Comparison Table

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-rail	—	OPA2830	—	OPA4830
Rail-to-rail fixed gain	OPA832	OPA2832	OPA3832	—
General-purpose (1800V/µs slew rate)	OPA690	OPA2690	OPA3690	—
Low-noise, high dc precision	OPA820	OPA2822	—	OPA4820

5 Pin Configurations and Functions

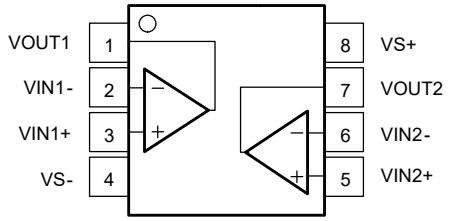


図 5-1. D Package, 8-Pin SOIC and DGK Package (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VIN1–	2	Input	Negative (inverting) input signal, channel 1
VIN1+	3	Input	Positive (noninverting) input signal, channel 1
VIN2–	6	Input	Negative (inverting) input signal, channel 2
VIN2+	5	Input	Positive (noninverting) input signal, channel 2
VOUT1	1	Output	Output, channel 1
VOUT2	7	Output	Output, channel 2
VS–	4	—	Negative (lowest) power supply
VS+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Power supply		±6.5	V_{DC}
	Internal power dissipation	See *Thermal Information Table*		
V_{ID}	Differential input voltage		±2.5	V
V_I	Input voltage	($V_{S–}$) – 0.5V	(V_{S+}) + 0.3V	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* causes permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	3	10	11	V
T_A	Operating temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2830		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	122.6	144.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	62.2	56.2	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	70.1	77.6	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	11.9	3.9	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	69.2	76.4	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics V_S = ±5V

at T_A = 25°C(1), G = +2, R_F = 750Ω, R_L = 150Ω to GND, and R_{SRC} = 375Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +1, V_O ≤ 0.2V_{PP}		290		MHz
	G = +2, V_O ≤ 0.2V_{PP}	66	100		
	G = +5, V_O ≤ 0.2V_{PP}	16	30		
	G = +10, V_O ≤ 0.2V_{PP}	8	13		
Gain bandwidth product	G ≥ +10	80	130		MHz
Peaking at a gain of +1	V_O ≤ 0.2V_{PP}		4		dB
Slew rate	G = +2, 2V step, 20% to 80%	275	560		V/µs
Rise time	0.5V step, 20% to 80%		3.4	5.9	ns
Fall time	0.5V step, 20% to 80%		3.6	6.0	ns
Settling time to 0.1%	G = +2, 1V step		43	64	ns
Harmonic distortion	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω	–55	–62		dBc
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω	–58	–66		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω	–50	–59		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω	–65	–77		
Input voltage noise	f > 1MHz		5.6	10.6	nV/√Hz
	f > 1MHz, T_A = –40°C to +85°C			11.6	
Input current noise	f > 1MHz		3.7	5.4	pA/√Hz
	f > 1MHz, T_A = –40°C to +85°C			6.4	
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±1V	66	74		dB
	V_O = ±1V, T_A = –40°C to +85°C	64			
Input offset voltage			±1.5	±7.5	mV
	T_A = –40°C to +85°C			±9.3	
Average offset voltage drift	T_A = –40°C to +85°C			±27	µV/°C
Input bias current	V_{CM} = 2V		5	18	µA
	V_{CM} = 2V, T_A = –40°C to +85°C			19	
Input bias current drift	V_{CM} = 0V, T_A = –40°C to +85°C			±46	nA/°C
Input offset current	V_{CM} = 2V		±0.2	±1.1	µA
	V_{CM} = 2V, T_A = –40°C to +85°C			±1.5	
Input offset current drift	V_{CM} = 0V, T_A = –40°C to +85°C			±6	nA/°C
INPUT					
Negative input voltage	0.4V step		–5.5	–5.4	V
	0.4V step, T_A = –40°C to +85°C			–5.2	
Positive input voltage	0.4V step	3.1	3.2		V
	0.4V step, T_A = –40°C to +85°C	2.9			
Common-mode rejection ratio (CMRR)	Input-referred	76	80		dB
	Input-referred, T_A = –40°C to +85°C	71			
Input impedance	Differential mode		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		

6.5 Electrical Characteristics V_S = ±5V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, R_L = 150Ω to GND, and R_{SRC} = 375Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT					
Output voltage swing	R_L = 1kΩ to GND	±4.86	±4.88		V
	R_L = 1kΩ to GND, T_A = –40°C to +85°C	±4.84			
	R_L = 150Ω to GND	±4.60	±4.64		
	R_L = 150Ω to GND, T_A = –40°C to +85°C	±4.56			
Current output, sinking and sourcing	V_O = ±2.75V, V_{OS} = 20mV	±63	±82		mA
	V_O = ±2.75V, V_{OS} = 20mV, T_A = –40°C to +85°C	±53			
Short-circuit current	Output shorted to ground		120		mA
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.03		Ω
POWER SUPPLY					
Quiescent current		7.6	9	10.6	mA
	T_A = –40°C to +85°C	6.2		12.2	
Power-supply rejection ratio (–PSRR)	Input-referred, 1V step	61	66		dB
	Input-referred, T_A = –40°C to +85°C	59			

(1) Junction temperature = ambient for 25°C specifications.

6.6 Electrical Characteristics V_S = 5V

at T_A = 25°C[(1)], G = +2, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +1, V_O ≤ 0.2V_{PP}		230		MHz
	G = +2, V_O ≤ 0.2V_{PP}	70	100		
	G = +5, V_O ≤ 0.2V_{PP}	15	21		
	G = +10, V_O ≤ 0.2V_{PP}	7	10		
Gain bandwidth product	G ≥ +10	75	100		MHz
Peaking at a gain of +1	V_O ≤ 0.2V_{PP}		4		dB
Slew rate	G = +2, 2V step, 20% to 80%	270	500		V/µs
Rise time	0.5V step, 20% to 80%		3.4	5.8	ns
Fall time	0.5V step, 20% to 80%		3.4	5.8	ns
Settling time to 0.1%	G = +2, 1V step		44	65	ns
Harmonic distortion	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω	–52	–58		dBc
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω	–56	–62		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω	–50	–58		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω	–65	–84		
Input voltage noise	f > 1MHz		5.8	10.3	nV/√Hz
	f > 1MHz, T_A = –40°C to +85°C			11.3	
Input current noise	f > 1MHz		4	5.4	pA/√Hz
	f > 1MHz, T_A = –40°C to +85°C			6.4	
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±1V	66	72		dB
	V_O = ±1V, T_A = –40°C to +85°C	64			
Input offset voltage			±0.5	±5.5	mV
	T_A = –40°C to +85°C			±7.0	
Average offset voltage drift	T_A = –40°C to +85°C			±22	µV/°C
Input bias current	V_{CM} = 2.5V		+5	+18	µA
	V_{CM} = 2.5V, T_A = –40°C to +85°C			+18	
Input bias current drift	V_{CM} = 2.5V, T_A = –40°C to +85°C			±46	nA/°C
Input offset current	V_{CM} = 2.5V		±0.2	±0.9	µA
	V_{CM} = 2.5V, T_A = –40°C to +85°C			±1.3	
Input offset current drift	V_{CM} = 2.5V, T_A = –40°C to +85°C			±6	nA/°C
INPUT					
Negative input voltage	0.4V step		–0.5	–0.4	V
	0.4V step, T_A = –40°C to +85°C			–0.2	
Positive input voltage	0.4V step	3.1	3.2		V
	0.4V step, T_A = –40°C to +85°C	2.9			
Common-mode rejection ratio (CMRR)	Input-referred	76	80		dB
	Input-referred, T_A = –40°C to +85°C	71			
Input impedance	Differential mode		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		

6.6 Electrical Characteristics V_S = 5V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT					
Output voltage swing low	G = +5, R_L = 1kΩ to 2.5V			0.09	V
	G = +5, R_L = 1kΩ to 2.5V, T_A = –40°C to +85°C			0.13	
	G = +5, R_L = 150Ω to 2.5V			0.21	
	G = +5, R_L = 150Ω to 2.5V, T_A = –40°C to +85°C			0.26	
Output voltage swing high	G = +5, R_L = 1kΩ to 2.5V	4.91			V
	G = +5, R_L = 1kΩ to 2.5V, T_A = –40°C to +85°C	4.87			
	G = +5, R_L = 150Ω to 2.5V	4.78			
	G = +5, R_L = 150Ω to 2.5V, T_A = –40°C to +85°C	4.72			
Current output, sinking and sourcing	V_O = ±0.88V, V_{OS} = 20mV	±58	±75		mA
	V_O = ±0.88V, V_{OS} = 20mV, T_A = –40°C to +85°C	±50			
Short-circuit current	Output shorted to either supply		125		mA
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.06		Ω
POWER SUPPLY					
Quiescent current		7.4	8.8	10	mA
	T_A = –40°C to +85°C	6.2		11.4	
Power-supply rejection ratio (PSRR)	Input-referred, 0.5V step	61	66		dB
	Input-referred, T_A = –40°C to +85°C	59			

(1) Junction temperature = ambient for +25°C specifications.

6.7 Electrical Characteristics V_S = 3V

at T_A = 25°C[(1)], G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/3 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +2, V_O ≤ 0.2V_{PP}	70	90		MHz
	G = +5, V_O ≤ 0.2V_{PP}	15	20		
	G = +10, V_O ≤ 0.2V_{PP}	7.5	9		
Gain bandwidth product	G ≥ +10	75	90		MHz
Slew rate	G = +2, 1V step, 20% to 80%	135	220		V/µs
Rise time	0.5V step, 20% to 80%		3.4	5.6	ns
Fall time	0.5V step, 20% to 80%		3.4	5.6	ns
Settling time to 0.1%	G = +2, 1V step		46	73	ns
Harmonic distortion	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω	–56	–60		dBc
	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω	–59	–64		
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω	–59	–68		
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω	–65	–72		
Input voltage noise	f > 1MHz		5.8	10.3	nV/√Hz
	f > 1MHz, T_A = 0°C to 70°C			10.8	
Input current noise	f > 1MHz		4	5.4	pA/√Hz
	f > 1MHz, T_A = 0°C to 70°C			6.2	
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±0.5V	66	72		dB
	V_O = ±0.5V, T_A = 0°C to 70°C	65			
Input offset voltage			±1.5	±7.5	mV
	T_A = 0°C to 70°C			±8.7	
Average offset voltage drift	T_A = 0°C to 70°C			±27	µV/°C
Input bias current	V_{CM} = 1.0V		+5	+18	µA
	V_{CM} = 1.0V, T_A = 0°C to 70°C			±18	
Input bias current drift	V_{CM} = 1.0V, T_A = 0°C to 70°C			±44	nA/°C
Input offset current	V_{CM} = 1.0V		±0.2	±1.1	µA
	V_{CM} = 1.0V, T_A = 0°C to 70°C			±1.3	
Input offset current drift	V_{CM} = 1.0V, T_A = 0°C to 70°C			±5	nA/°C
INPUT					
Negative input voltage	0.4V step		–0.45	–0.4	V
	T_A = 0°C to +70°C, 0.4V step			–0.27	
Positive input voltage	0.4V step	1.1	1.2		V
	T_A = 0°C to +70°C, 0.4V step	1			
Common-mode rejection ratio (CMRR)	Input-referred	74	80		dB
	Input-referred, T_A = 0°C to 70°C	72			dB
Input impedance	Differential mode		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		
OUTPUT					
Current output, sinking and sourcing	V_O = ±0.125V, V_{OS} = 20mV	±20	±30		mA
	V_O = ±0.125V, V_{OS} = 20mV, T_A = 0°C to 70°C	±18			
Short-circuit current	Output shorted to either supply		120		mA
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.06		Ω

6.7 Electrical Characteristics V_S = 3V (続き)

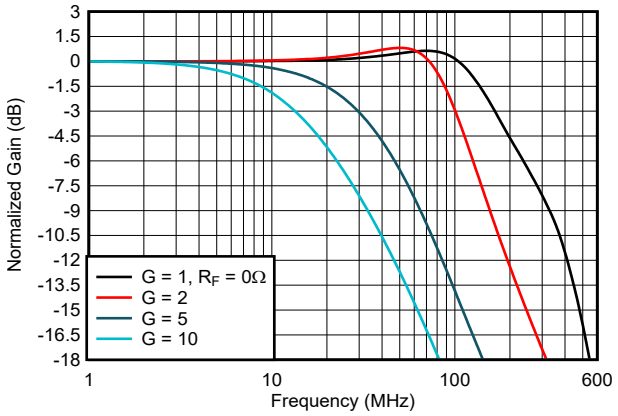
at T_A = 25°C(1), G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/3 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Quiescent current		6.6	8.6	9.8	mA
	T_A = 0°C to +70°C	6.2		11	
Power-supply rejection ratio (PSRR)	Input-referred, 0.3V step	60	64		dB
	Input-referred, T_A = 0°C to 70°C	58			

(1) Junction temperature = ambient for +25°C specifications.

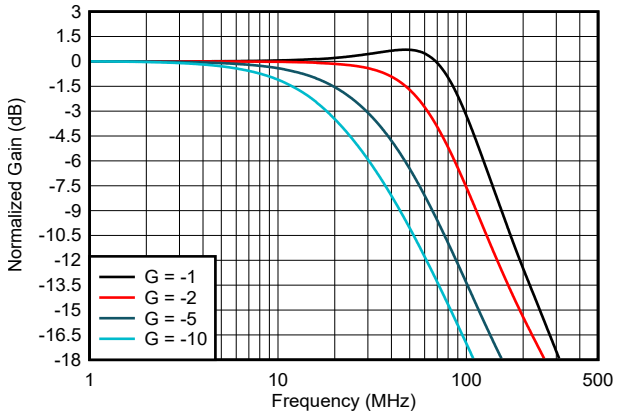
6.8 Typical Characteristics: V_S = ±5V

at T_A = 25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted); see 図 8-3



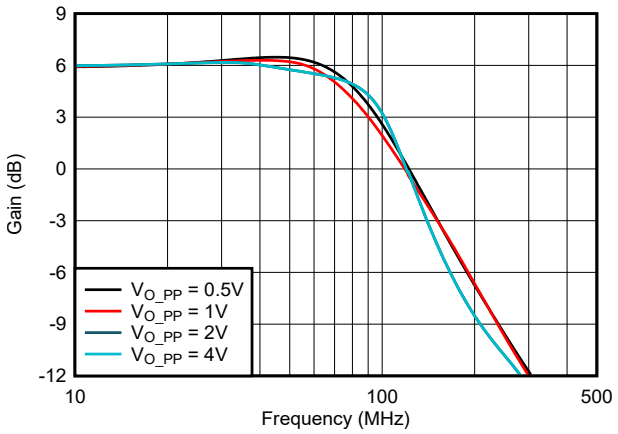
R_L = 150Ω V_O = 0.2V_{PP}

図 6-1. Noninverting Small-Signal Frequency Response



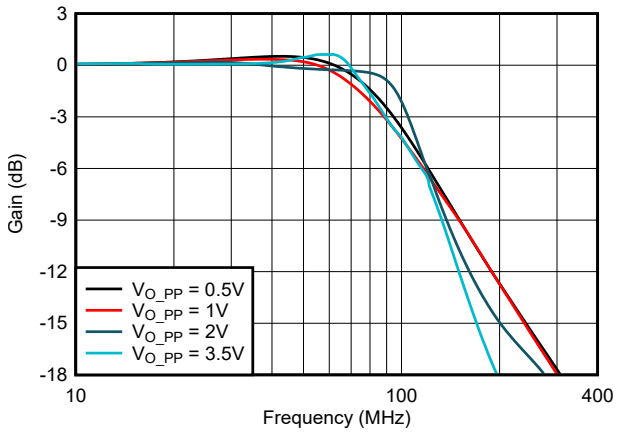
R_L = 150Ω V_O = 0.2V_{PP}

図 6-2. Inverting Small-Signal Frequency Response



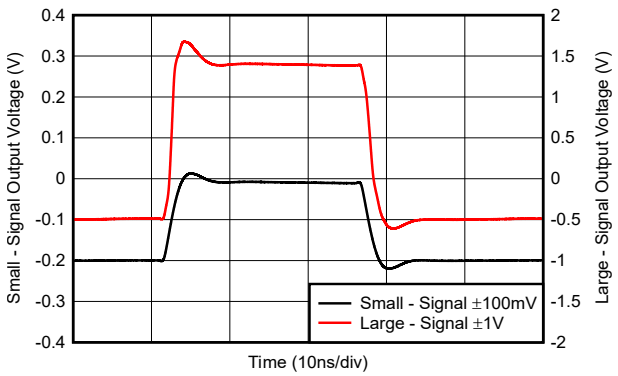
R_L = 150Ω G = +2V/V

図 6-3. Noninverting Large-Signal Frequency Response



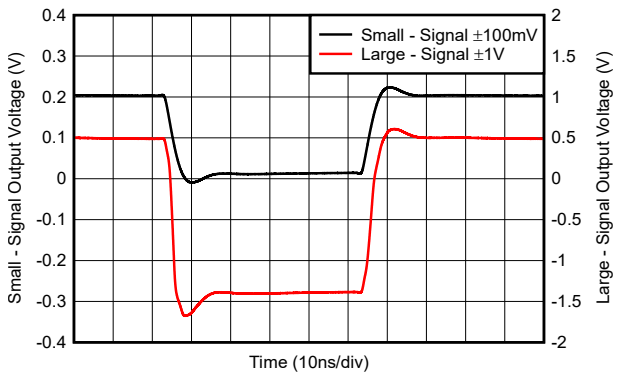
R_L = 150Ω G = –1V/V

図 6-4. Inverting Large-Signal Frequency Response



G = +2V/V

図 6-5. Noninverting Pulse Response

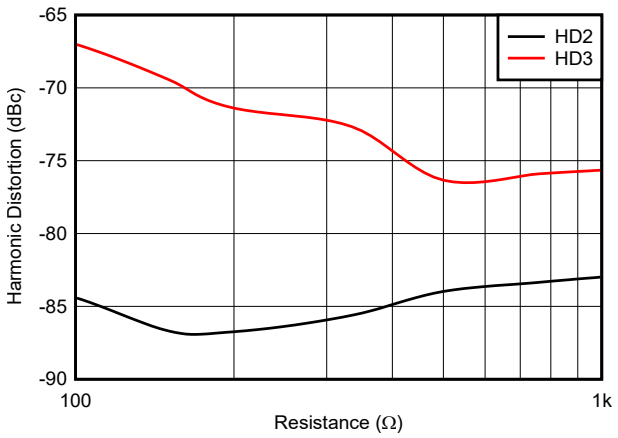


G = –1V/V

図 6-6. Inverting Pulse Response

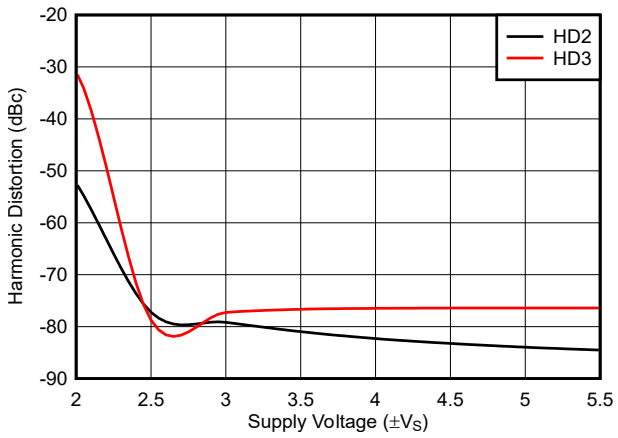
6.8 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted); see 図 8-3



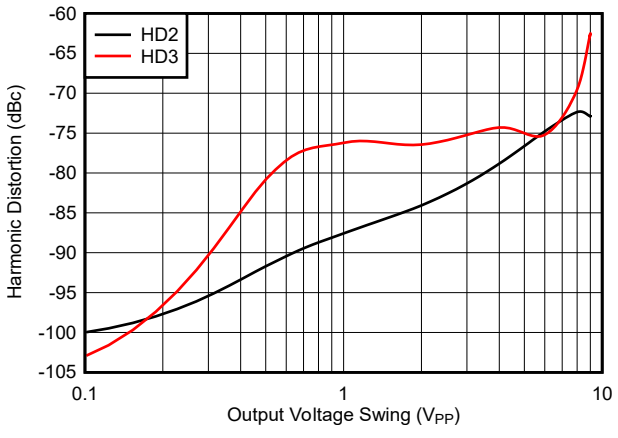
f = 5MHz V_O = 2V_{PP} G = +2V/V

図 6-7. Harmonic Distortion vs Load Resistance



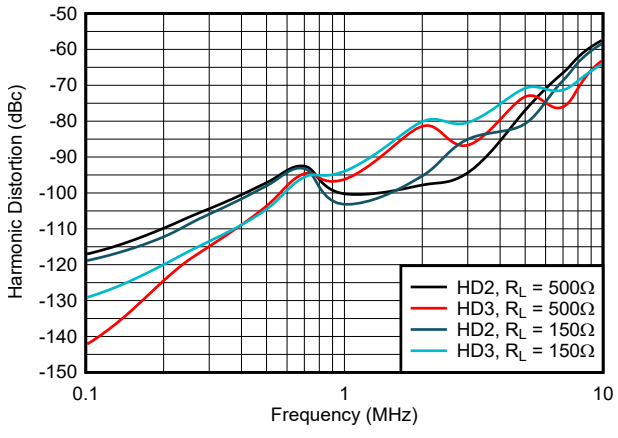
R_L = 500Ω V_O = 2V_{PP} G = +2V/V

図 6-8. 5MHz Harmonic Distortion vs Supply Voltage



f = 5MHz R_L = 500Ω G = +2V/V

図 6-9. Harmonic Distortion vs Output Voltage



V_O = 2V_{PP} G = +2V/V

図 6-10. Harmonic Distortion vs Frequency

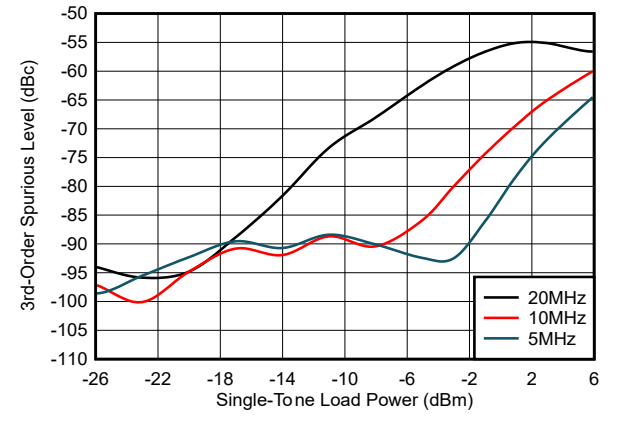


図 6-11. Two-Tone, 3rd-Order Intermodulation Spurious

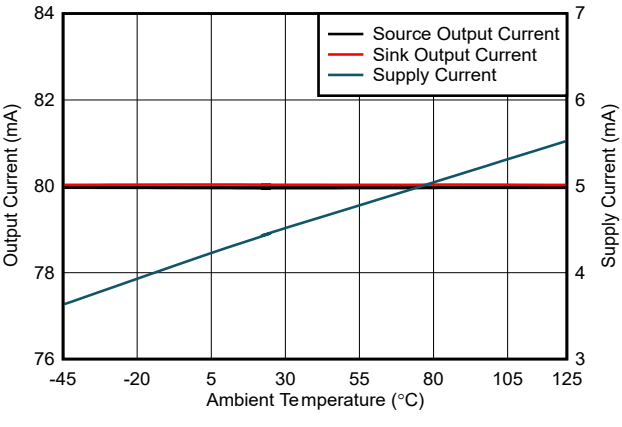


図 6-12. Supply and Output Current vs Temperature

6.8 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted); see 図 8-3

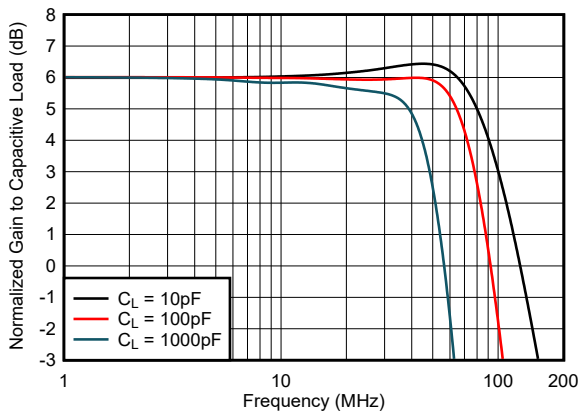


図 6-13. Frequency Response vs Capacitive Load

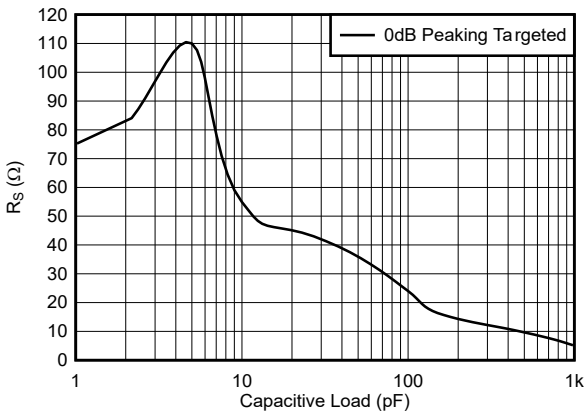


図 6-14. Recommended R_S vs Capacitive Load

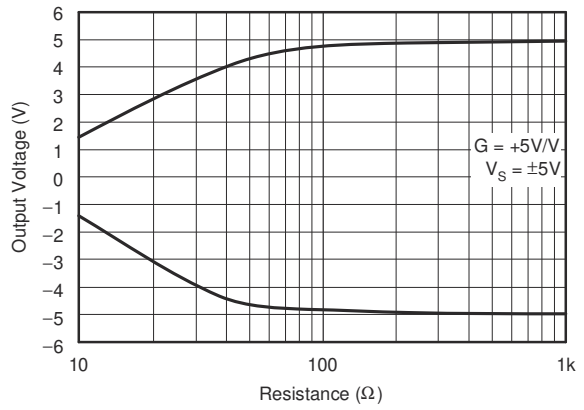


図 6-15. Output Swing vs Load Resistance

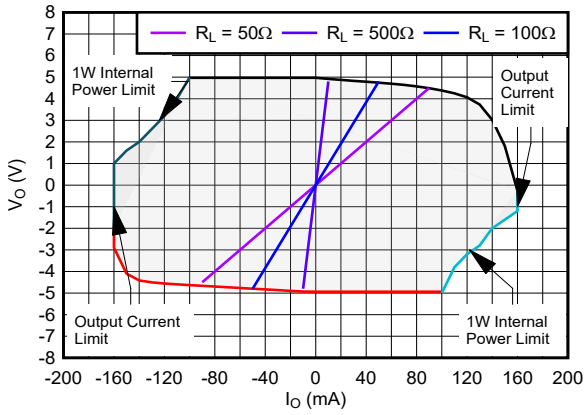


図 6-16. Output Voltage and Current Limitations

6.9 Typical Characteristics: V_S = ±5V, Differential Configuration

At T_A = 25°C, R_F = 604Ω (see 図 7-1), and R_L = 500Ω (unless otherwise noted)

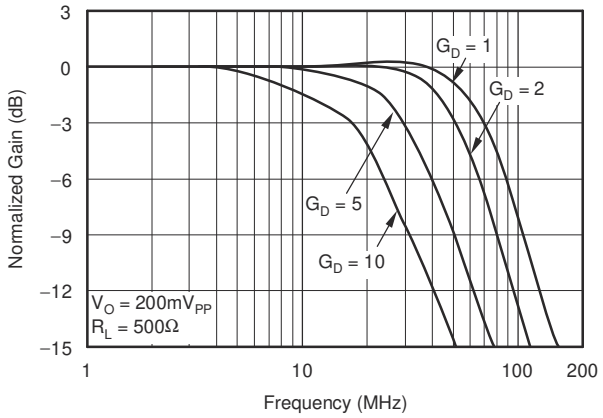


図 6-17. Differential Small-Signal Frequency Response

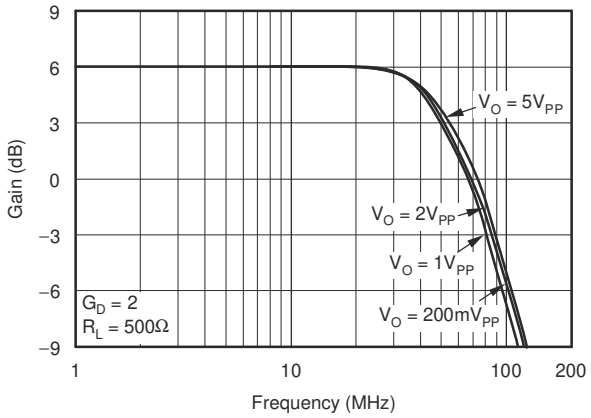


図 6-18. Differential Large-Signal Frequency Response

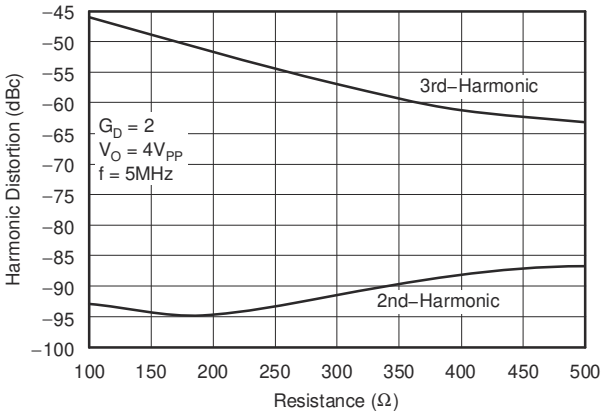


図 6-19. Differential Distortion vs Load Resistance

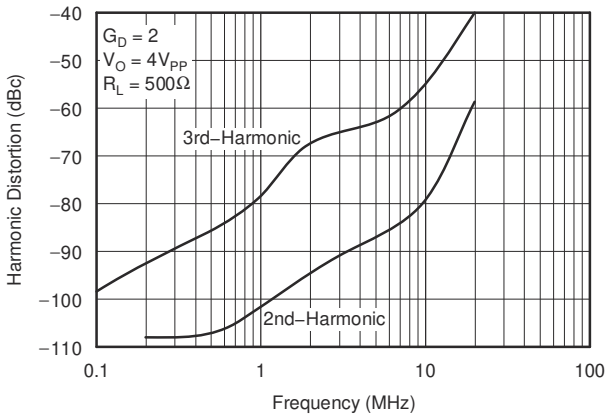


図 6-20. Differential Distortion vs Frequency

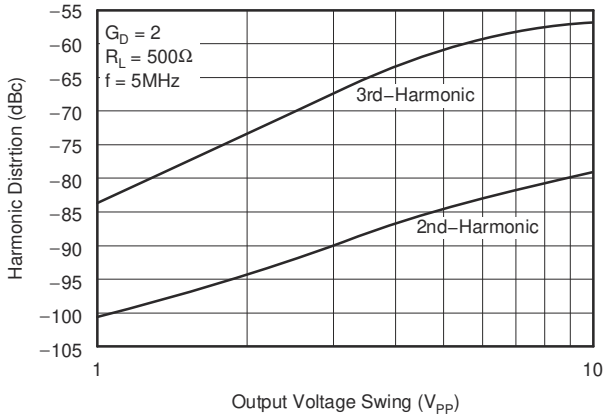
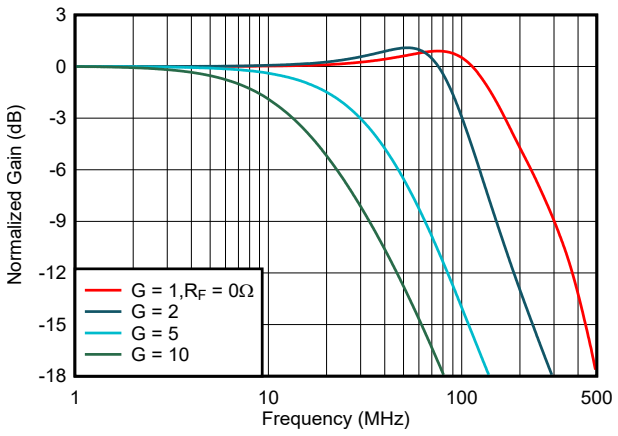


図 6-21. Differential Distortion vs Output Voltage

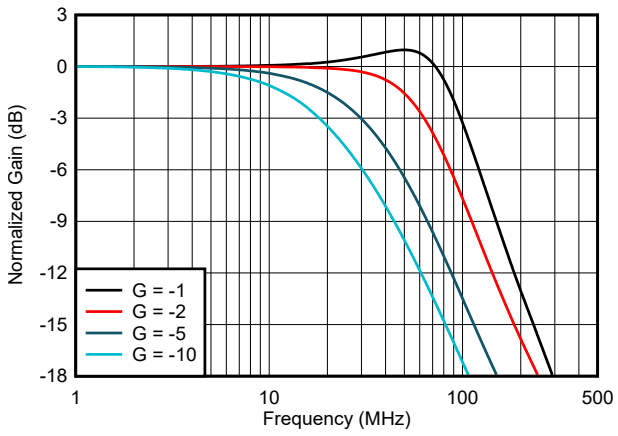
6.10 Typical Characteristics: V_S = 5V

at T_A = 25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see 図 8-1



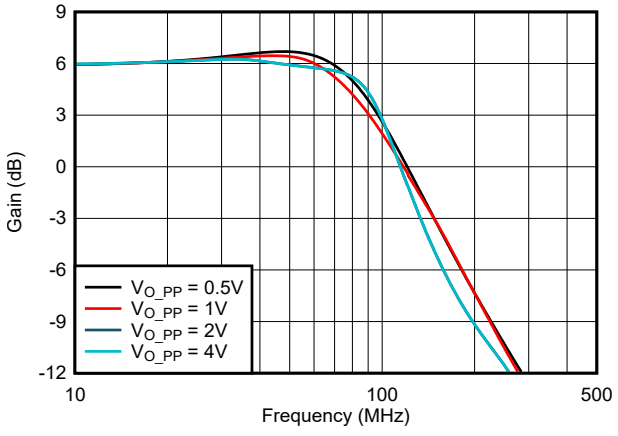
R_L = 150Ω V_O = 0.2V_{PP}

図 6-22. Noninverting Small-Signal Frequency Response



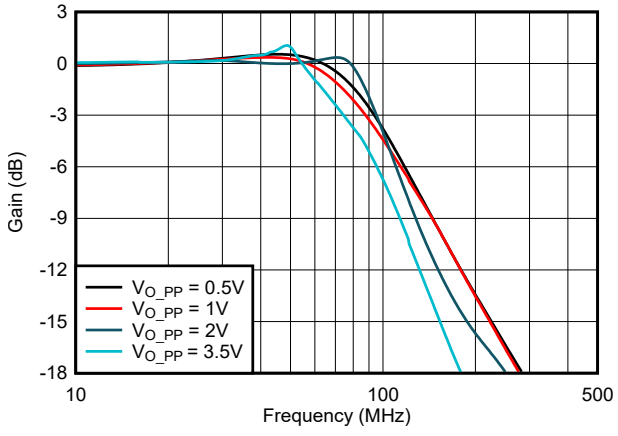
R_L = 150Ω V_O = 0.2V_{PP}

図 6-23. Inverting Small-Signal Frequency Response



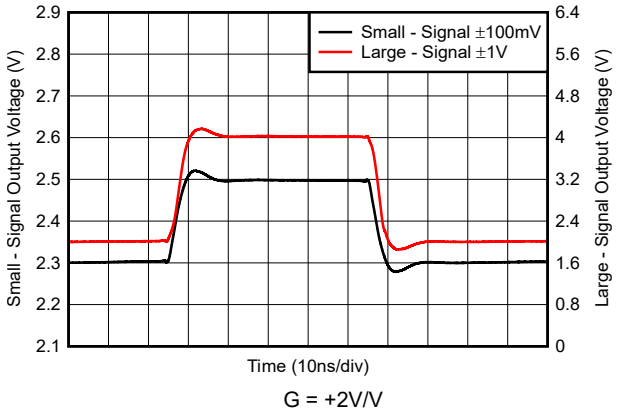
R_L = 150Ω G = +2V/V

図 6-24. Noninverting Large-Signal Frequency Response



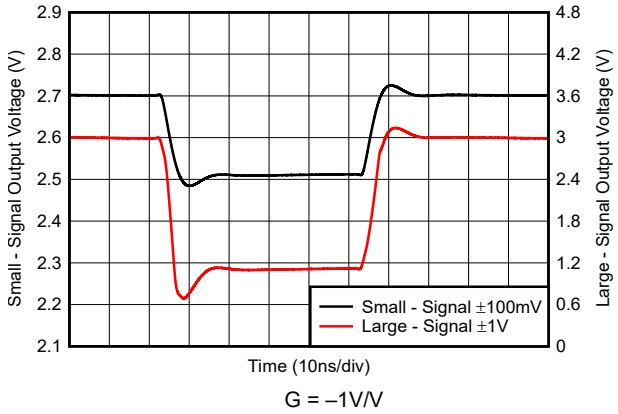
R_L = 150Ω G = –1V/V

図 6-25. Inverting Large-Signal Frequency Response



G = +2V/V

図 6-26. Noninverting Pulse Response



G = –1V/V

図 6-27. Inverting Pulse Response

6.10 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see 図 8-1

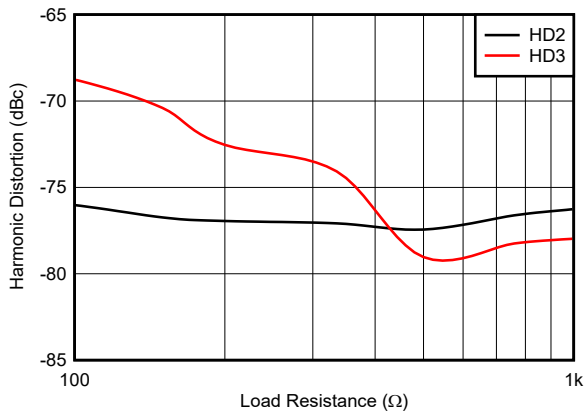


図 6-28. Harmonic Distortion vs Load Resistance

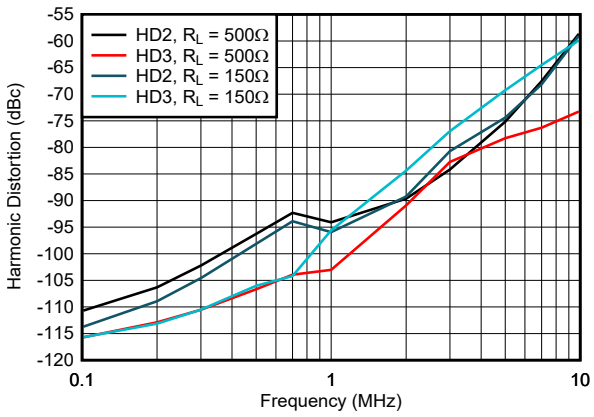


図 6-29. Harmonic Distortion vs Frequency

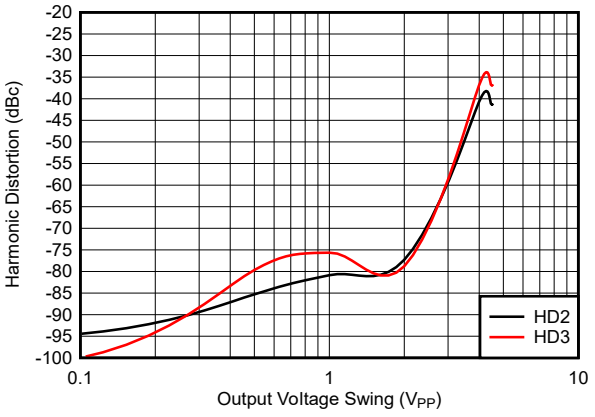


図 6-30. Harmonic Distortion vs Output Voltage

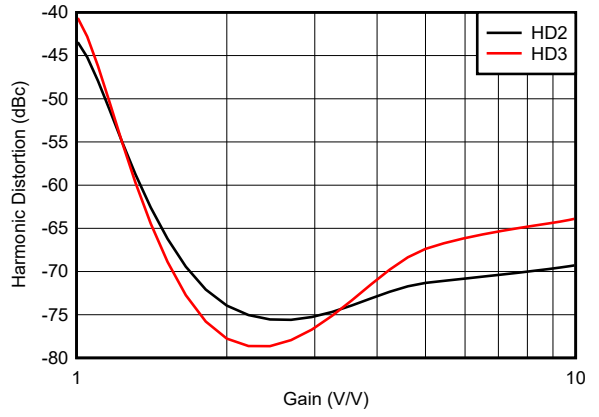


図 6-31. Harmonic Distortion vs Noninverting Gain

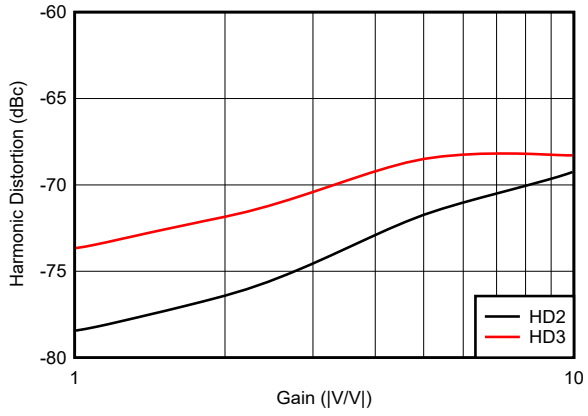


図 6-32. Harmonic Distortion vs Inverting Gain

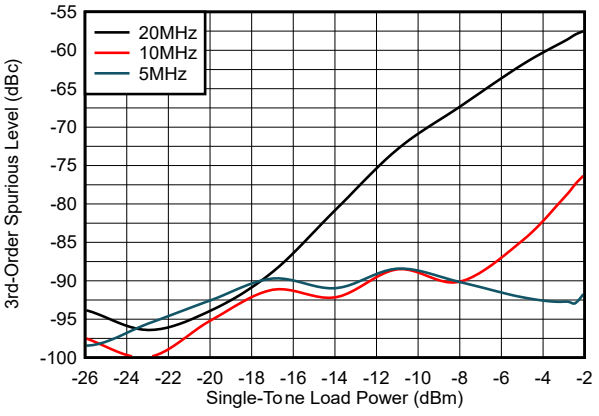


図 6-33. Two-Tone, 3rd-Order Intermodulation Spurious

6.10 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see 図 8-1

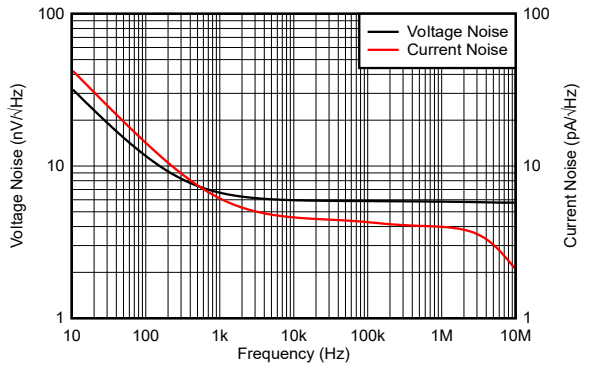


図 6-34. Input Voltage and Current Noise Density

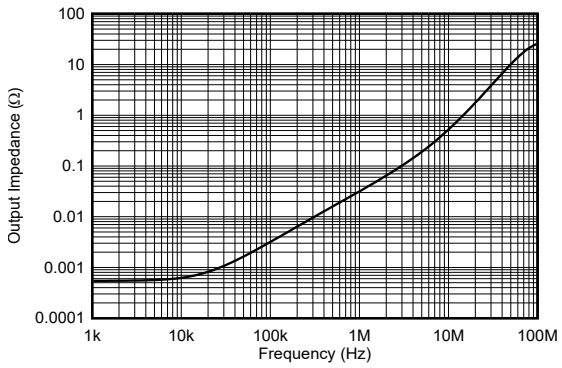


図 6-35. Closed-Loop Output Impedance vs Frequency

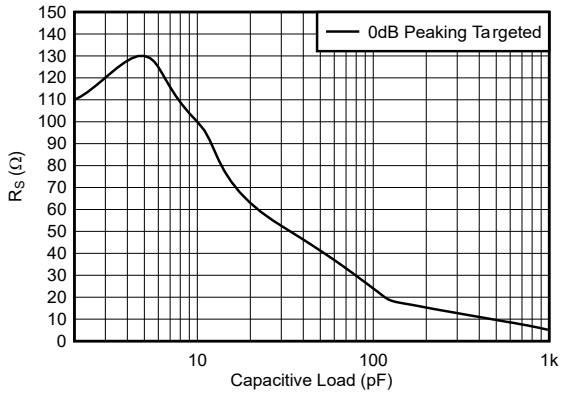


図 6-36. Recommended R_S vs Capacitive Load

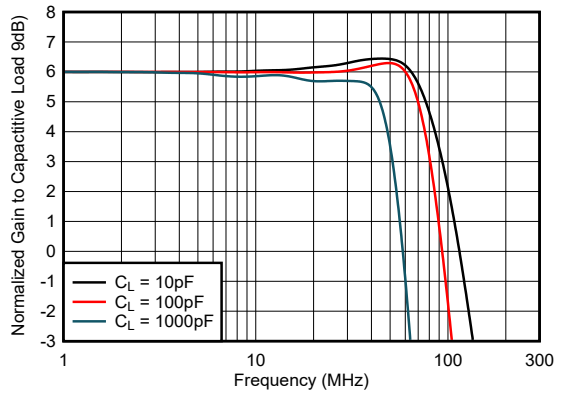


図 6-37. Frequency Response vs Capacitive Load

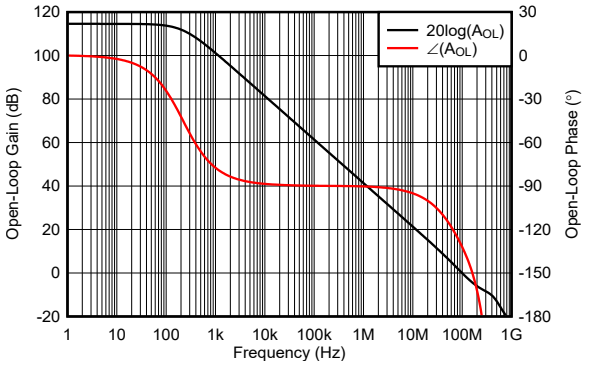


図 6-38. Open-Loop Gain and Phase

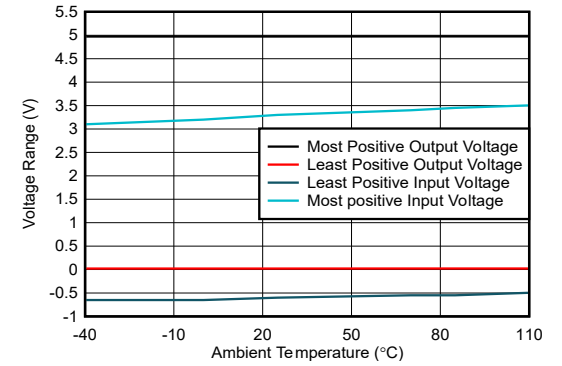


図 6-39. Voltage Ranges vs Temperature

6.10 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see 図 8-1

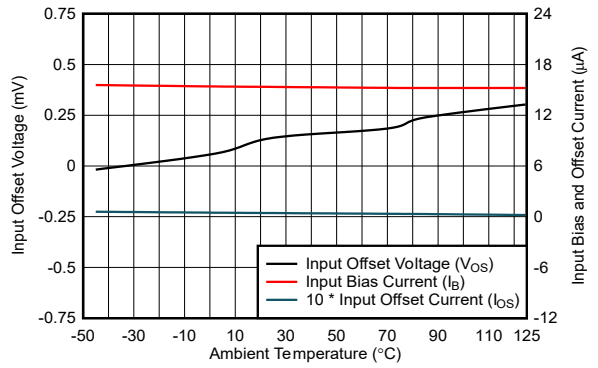


図 6-40. Typical DC Drift Over Temperature

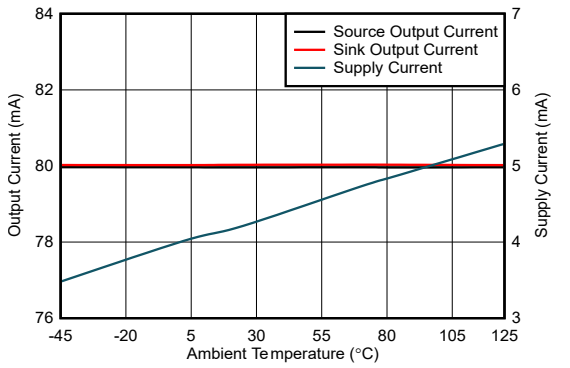


図 6-41. Supply and Output Current vs Temperature

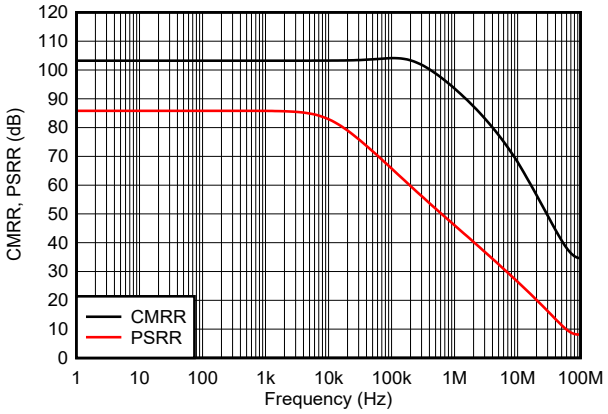


図 6-42. CMRR and PSRR vs Frequency

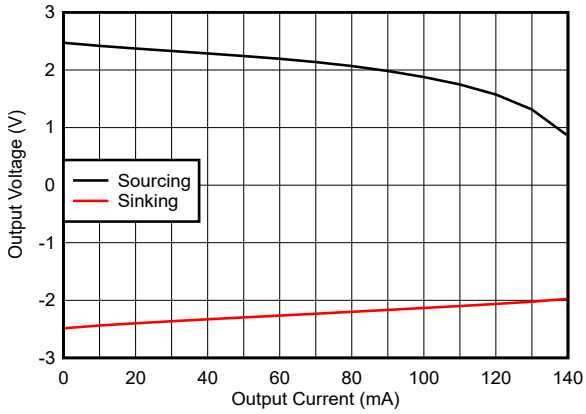


図 6-43. Output Voltage Swing vs Output Current

6.11 Typical Characteristics: V_S = 5V, Differential Configuration

at T_A = 25°C, R_F = 604Ω, and R_L = 500Ω differential; see 図 7-2 (unless otherwise noted)

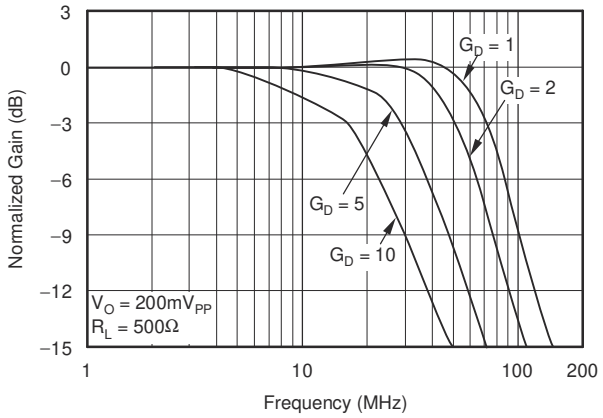


図 6-44. Differential Small-Signal Frequency Response

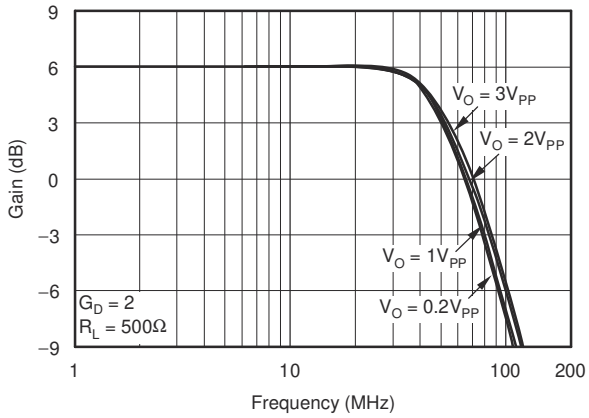


図 6-45. Differential Large-Signal Frequency Response

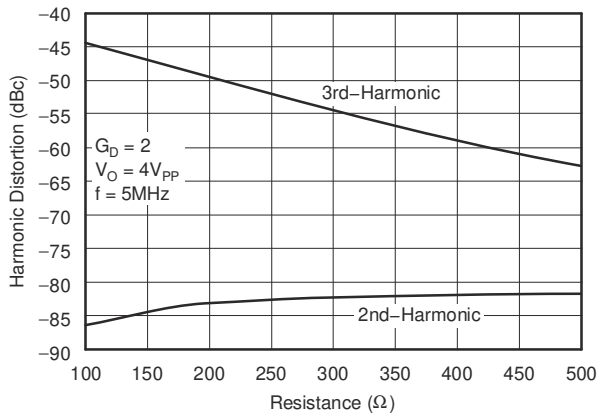


図 6-46. Differential Distortion vs Load Resistance

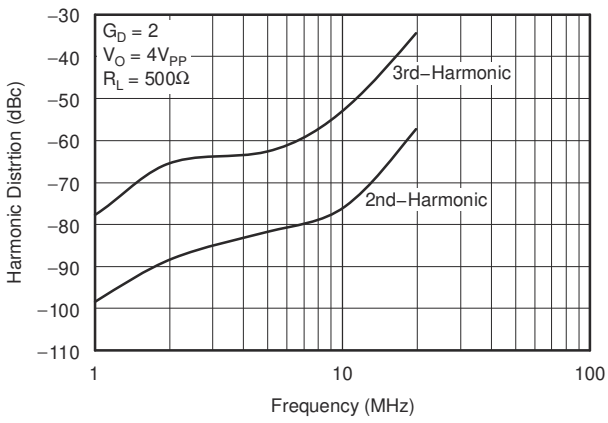


図 6-47. Differential Distortion vs Frequency

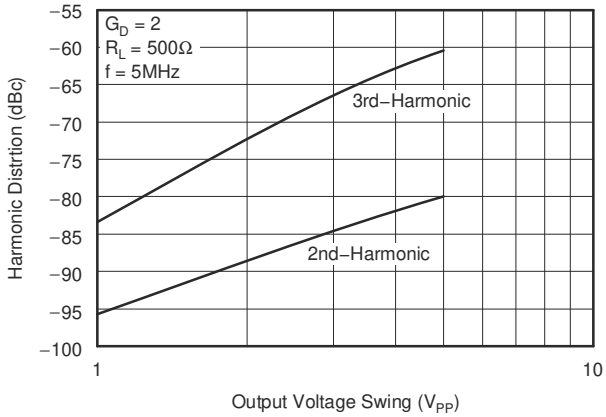
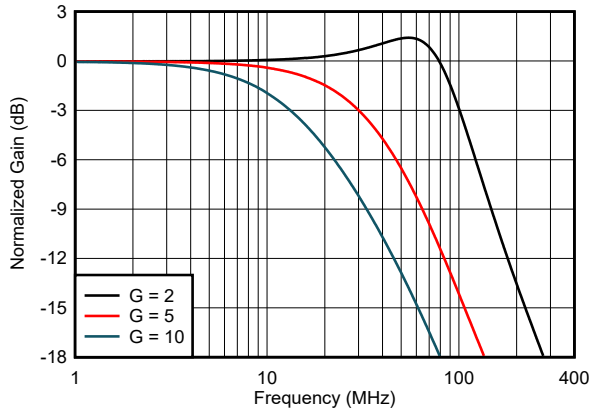


図 6-48. Differential Distortion vs Output Voltage

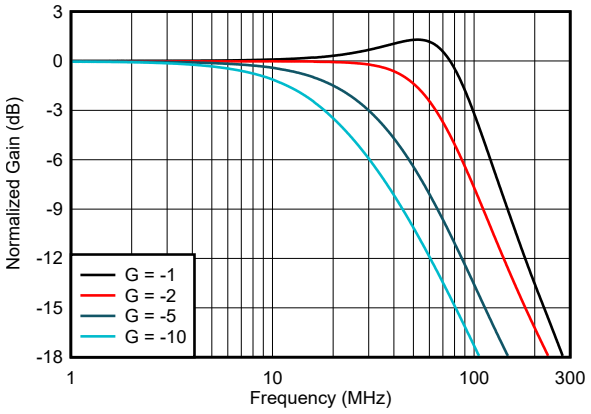
6.12 Typical Characteristics: V_S = 3V

at T_A = 25°C, G = +2V/V, and R_L = 150Ω to V_S/3 (unless otherwise noted); see also 図 8-2



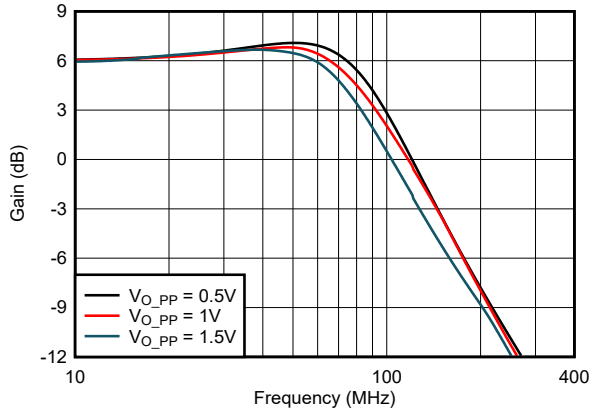
R_L = 150Ω V_O = 0.2V_{PP}

図 6-49. Noninverting Small-Signal Frequency Response



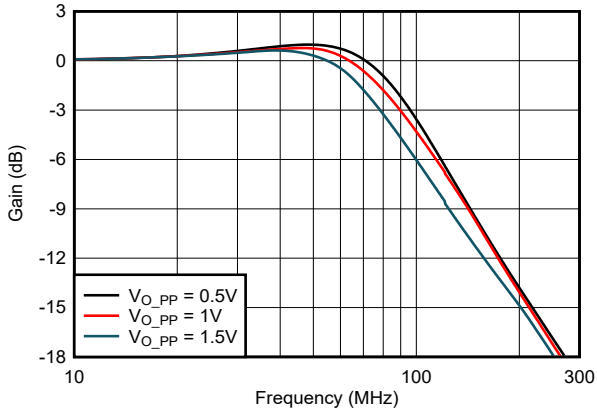
R_L = 150Ω V_O = 0.2V_{PP}

図 6-50. Inverting Small-Signal Frequency Response



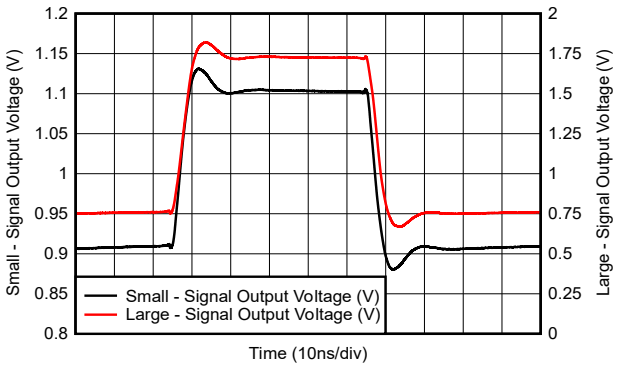
R_L = 150Ω G = +2V/V

図 6-51. Noninverting Large-Signal Frequency Response



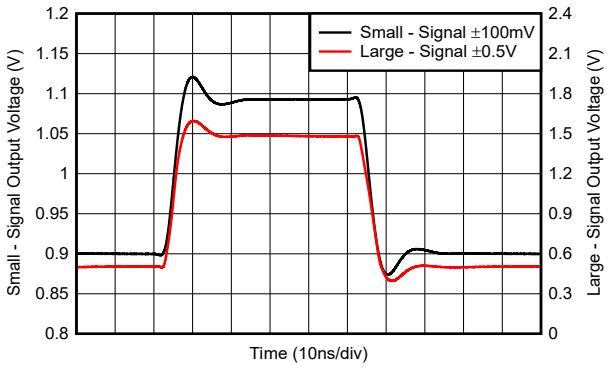
R_L = 150Ω G = –1V/V

図 6-52. Inverting Large-Signal Frequency Response



G = +2V/V

図 6-53. Noninverting Pulse Response

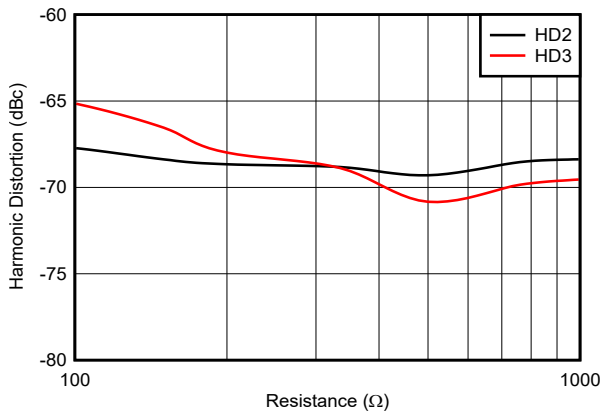


G = –1V/V

図 6-54. Inverting Pulse Response

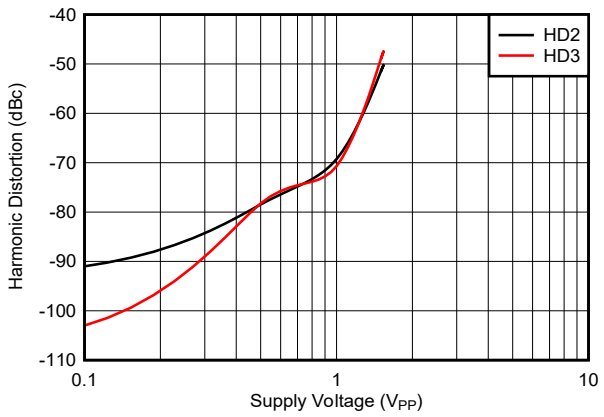
6.12 Typical Characteristics: V_S = 3V (continued)

at T_A = 25°C, G = +2V/V, and R_L = 150Ω to V_S/3 (unless otherwise noted); see also 図 8-2



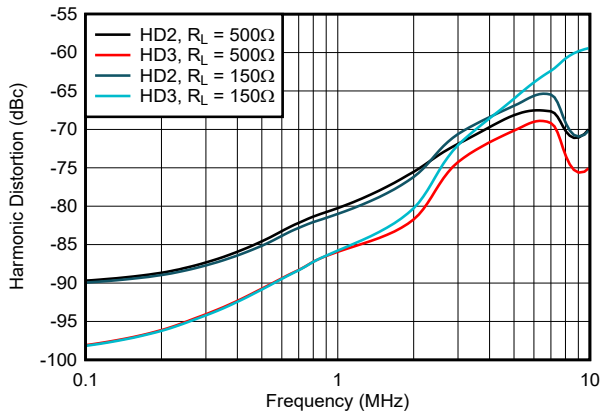
f = 5MHz $V_O = 1_{VPP}$ G = +2V/V

図 6-55. Harmonic Distortion vs Load Resistance



f = 5MHz R_L = 500Ω G = +2V/V

図 6-56. Harmonic Distortion vs Output Voltage



$V_O = 1V_{pp}$ G = +2V/V

図 6-57. Harmonic Distortion vs Frequency

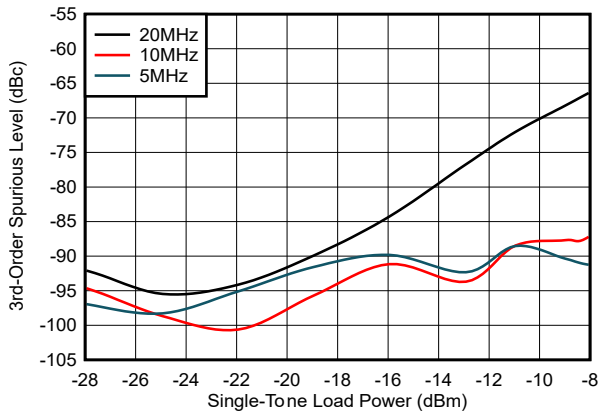


図 6-58. Two-Tone, 3rd-Order Intermodulation Spurious

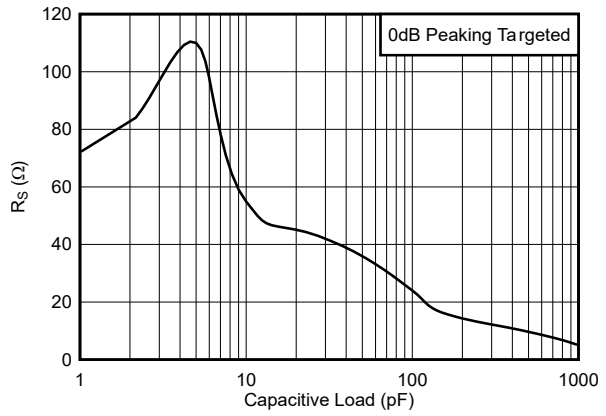


図 6-59. Recommended R_S vs Capacitive Load

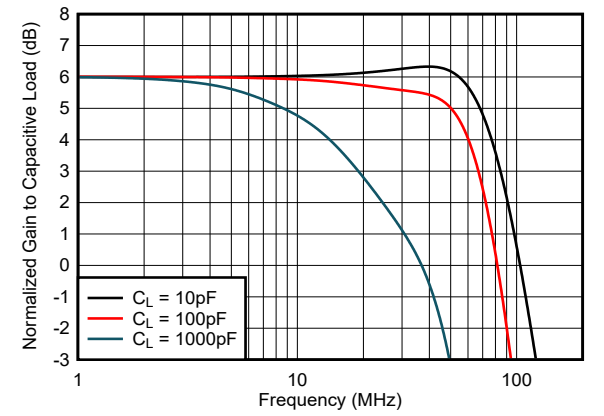


図 6-60. Frequency Response vs Capacitive Load

6.12 Typical Characteristics: V_S = 3V (continued)

at T_A = 25°C, G = +2V/V, and R_L = 150Ω to V_S/3 (unless otherwise noted); see also 図 8-2

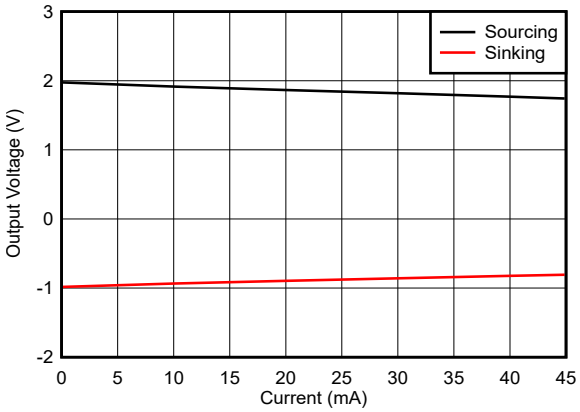


図 6-61. Output Swing vs Load Resistance

6.13 Typical Characteristics: V_S = 3V, Differential Configuration

at T_A = 25°C, R_F = 604Ω, and R_L = 500Ω differential; see 図 7-3 (unless otherwise noted)

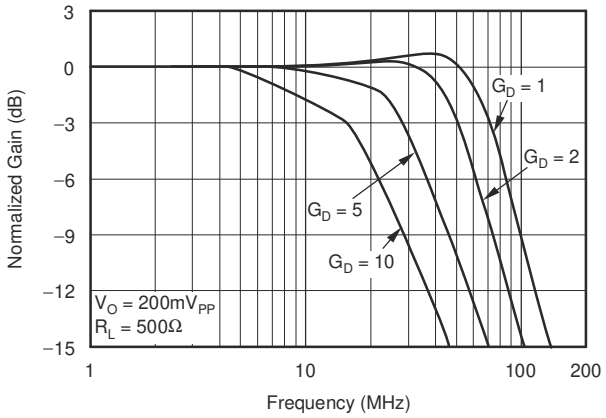


図 6-62. Differential Small-Signal Frequency Response

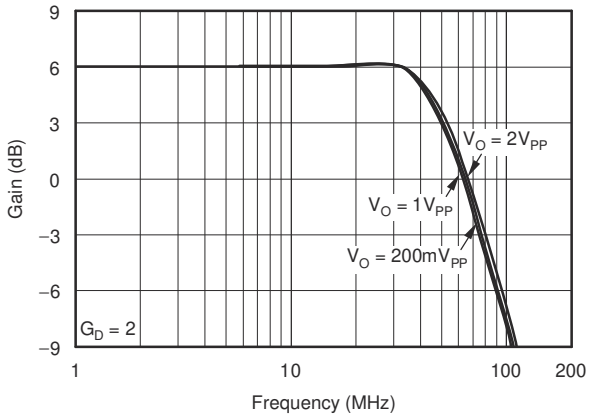


図 6-63. Differential Large-Signal Frequency Response

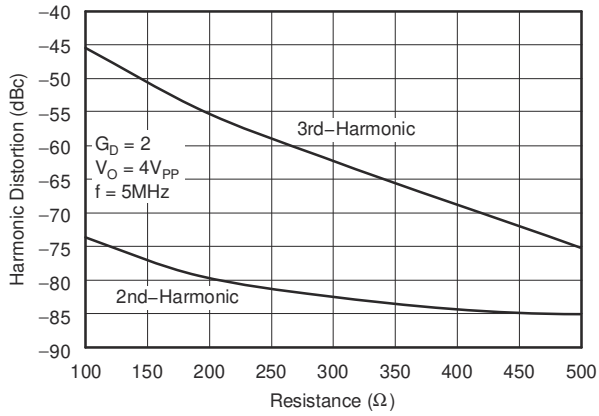


図 6-64. Differential Distortion vs Load Resistance

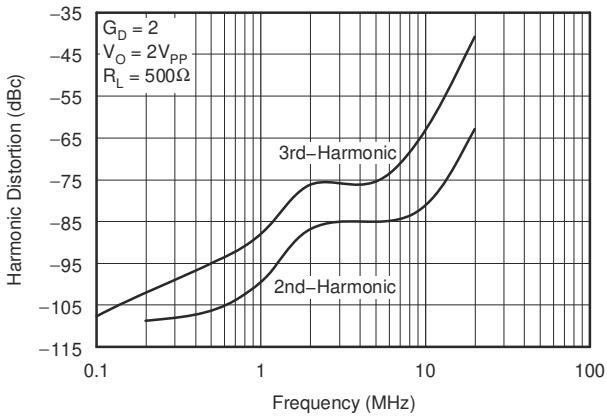


図 6-65. Differential Distortion vs Frequency

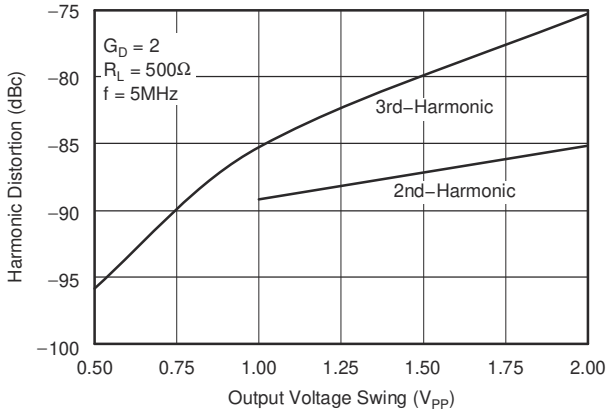


図 6-66. Differential Distortion vs Output Voltage

7 Parameter Measurement Information

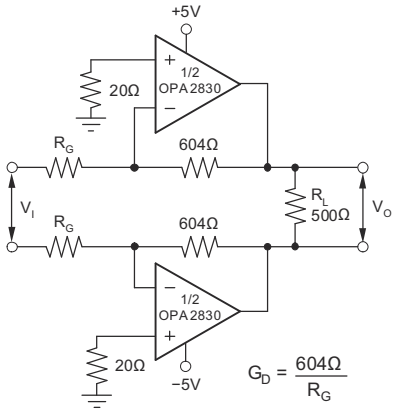


図 7-1. 10V Differential Configuration Test Circuit

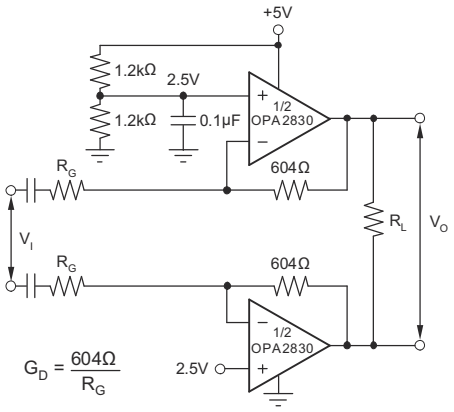


図 7-2. 5V Differential Configuration Test Circuit

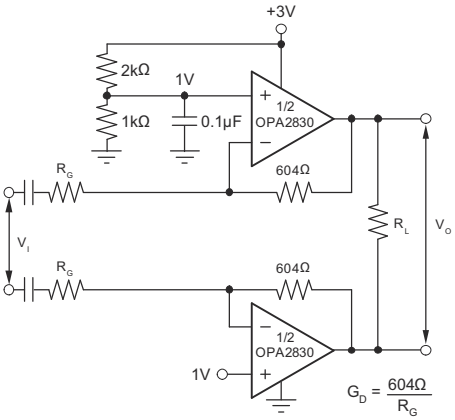


図 7-3. 3V Differential Configuration Test Circuit

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Wideband Voltage-Feedback Operation

The OPA2830 is a unity-gain stable, very high-speed voltage-feedback op amp designed for single-supply operation (3V to 10V). The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of ground and the positive supply. The OPA2830 is compensated to provide stable operation with a wide range of resistive loads.

図 8-1 shows the ac-coupled, gain of +2 configuration used for the 5V *Specifications* and *Typical Characteristics*. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the *Electrical Characteristics* are taken directly at the input and output pins. For the circuit of 図 8-1, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.5kΩ resistors at the noninverting input provide the common-mode bias voltage. The parallel combination equals the dc resistance at the inverting input (R_F), reducing the dc output offset due to input bias current.

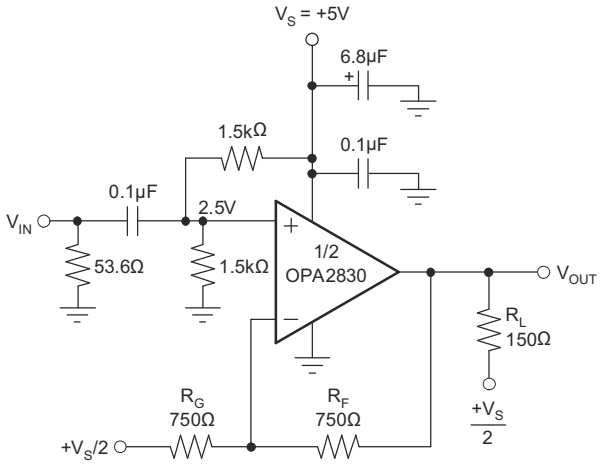


図 8-1. AC-Coupled, G = +2, 5V Single-Supply Specification and Test Circuit

図 8-2 shows the ac-coupled, gain of +2 configuration used for the 3V *Specifications* and *Typical Characteristics*. Voltage swings reported in the *Electrical Characteristics* are taken directly at the input and output pins. For the circuit of 図 8-2, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.13kΩ and 2.26kΩ resistors at the noninverting input provide the common-mode bias voltage. The parallel combination equals the dc resistance at the inverting input (R_F), reducing the dc output offset due to input bias current.

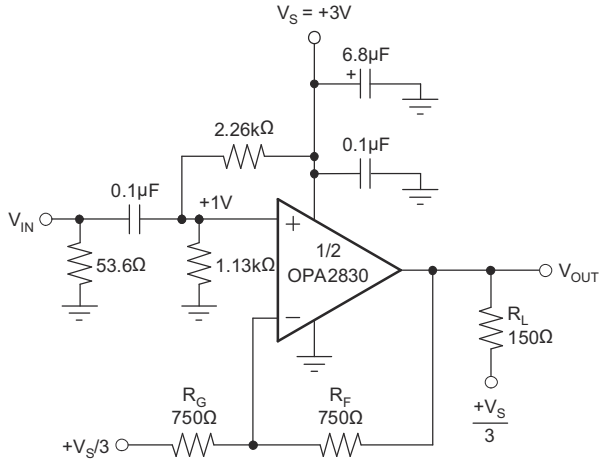


図 8-2. AC-Coupled, G = +2, 3V Single-Supply Specification and Test Circuit

図 8-3 shows the dc-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the *±5V Electrical Characteristics* and *Typical Characteristics*. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of 図 8-3, the total effective load is 150Ω || 1.5kΩ. Two optional components are included in 図 8-3. An additional resistor (348Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this configuration gives an input bias current canceling resistance that matches the 375Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

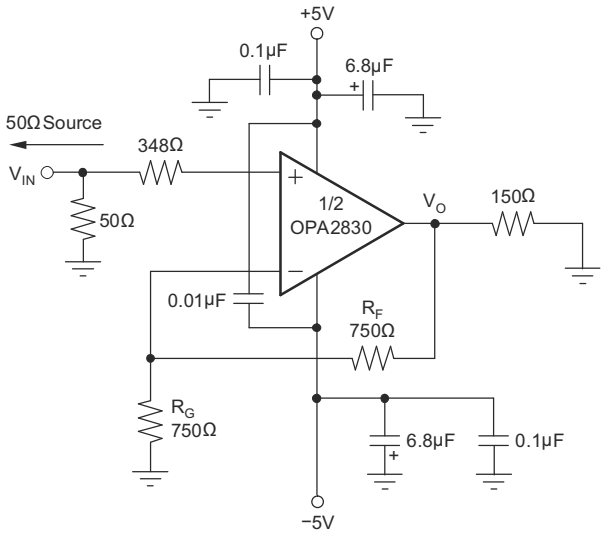


図 8-3. DC-Coupled, G = +2, Bipolar Supply Specification and Test Circuit

8.1.2 Single-Supply ADC Interface

The ADC interface of 図 8-4 shows a dc-coupled, single-supply ADC driver circuit. Many systems are now requiring 3V to 5V supply capability of both the ADC and ADC driver. The OPA2830 provides excellent performance in this demanding application. The large input and output voltage ranges and low distortion support converters, such as the ADS5203 in the figure on page 1. The input level-shifting circuitry is designed so that V_{IN} can be between 0V and 0.5V, while delivering an output voltage of 1V to 2V for the ADS5203.

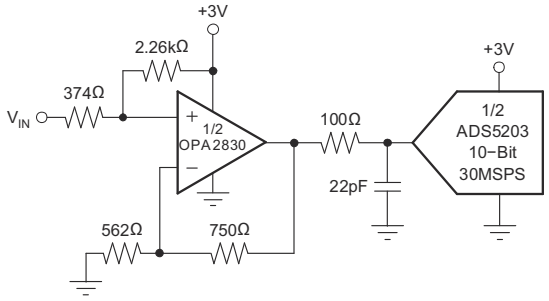


図 8-4. DC-Coupled, 3V ADC Driver

8.1.3 DC Level-Shifting

図 8-5 shows the general form of 図 8-4 as a dc-coupled noninverting amplifier that level-shifts the input up to accommodate the desired output voltage range. Given the desired signal gain (G), and the amount V_{OUT} must be shifted up (ΔV_{OUT}) when V_{IN} is at the center of the range, the following equations give the resistor values that produce the desired performance. Assume that R_4 is between 200Ω and 1.5kΩ.

- $NG = G + V_{OUT} / V_S$
- $R_1 = R_4 / G$
- $R_2 = R_4 / (NG – G)$
- $R_3 = R_4 / (NG – 1)$

where:

- $NG = 1 + R_4 / R_3$
- $V_{OUT} = (G)V_{IN} + (NG – G)V_S$

Ensure that V_{IN} and V_{OUT} stay within the specified input and output voltage ranges.

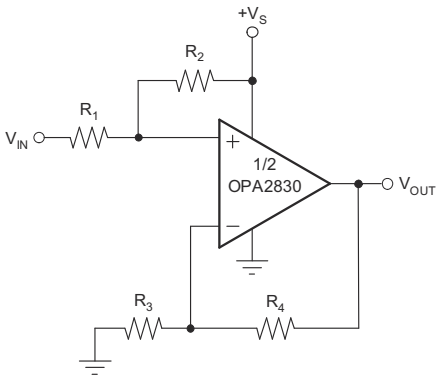


図 8-5. DC Level Shifting

The circuit of 図 8-4 is a good example of this type of application. The circuit designed to take V_{IN} between 0V and 0.5V and produce V_{OUT} between 1V and 2V when using a 3V supply. This means G = 2.00, and ΔV_{OUT} = 1.50V – G × 0.25V = 1.00V. Plugging these values into the previous equations (with R_4 = 750Ω) gives: NG =

2.33, R_1 = 375Ω, R_2 = 2.25kΩ, and R_3 = 563Ω. The resistors were changed to the nearest standard values for the circuit of 図 8-4.

8.1.4 AC-Coupled Output Video Line Driver

Low-power and low-cost video line drivers often buffer digital-to-analog converter (DAC) outputs with a gain of 2 into a doubly-terminated line. Those interfaces typically require a dc blocking capacitor. For a simple design, that interface often has used a very large value blocking capacitor (220µF) to limit tilt, or SAG, across the frames. 図 8-7 shows one approach to create a very low high-pass pole location using much lower capacitor values. This circuit gives a voltage gain of 2 at the output pin with a high-pass pole at 8Hz. Given the 150Ω load, a simple blocking capacitor approach requires a 133µF value. The two much-lower-valued capacitors give this same low-pass pole using this simple *SAG correction* circuit of 図 8-7.

The input is shifted slightly positive in 図 8-7 using the voltage divider from the positive supply. This shift gives about a 200mV input dc offset that shows up at the output pin as a 400mV dc offset when the DAC output is at zero current during the sync tip portion of the video signal. This offset acts to hold the output in the linear operating region. This configuration passes on any power-supply noise to the output with a gain of approximately –20dB; therefore, good supply decoupling is recommended on the power-supply pin. 図 8-6 shows the frequency response for the circuit of 図 8-7. This plot shows the 8Hz low-frequency high-pass pole and a high-end cutoff at approximately 100MHz.

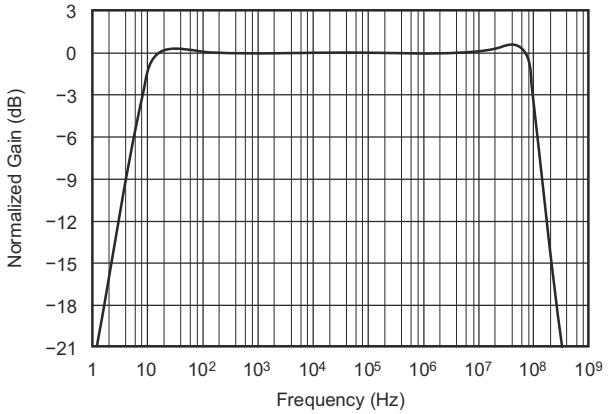


図 8-6. Video-Line-Driver Response to Matched Load

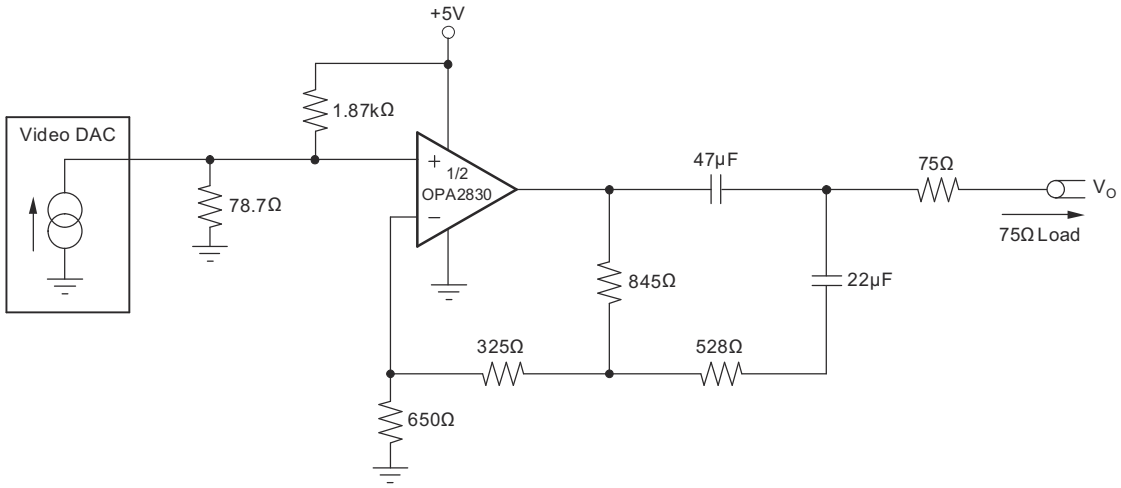


図 8-7. Video Line Driver With SAG Correction

8.1.5 Noninverting Amplifier With Reduced Peaking

図 8-8 shows a noninverting amplifier that reduces peaking at low gains. The resistor R_C compensates the OPA2830 to have higher Noise Gain (NG), which reduces the ac response peaking (typically 4dB at G = +1 without R_C) without changing the dc gain. V_{IN} needs to be a low impedance source, such as an op amp.

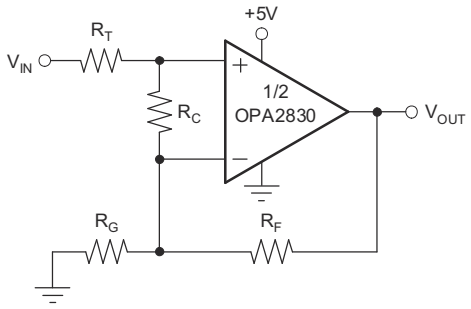


図 8-8. Compensated Noninverting Amplifier

The Noise Gain can be calculated as follows:

$$G_1 = 1 + \frac{R_F}{R_G} \quad (1)$$

$$G_2 = 1 + \frac{R_T + \frac{R_F}{G_1}}{R_C} \quad (2)$$

$$NG = G_1 \times G_2 \quad (3)$$

A unity-gain buffer can be designed by selecting $R_T = R_F = 20.0\Omega$ and $R_C = 40.2\Omega$ (do not use R_G). This gives a noise gain of 2, so the response is similar to the Characteristics Plots with G = +2 giving less peaking.

8.1.6 Single-Supply Active Filter

The OPA2830 operating on a single 3V or 5V supply lends well to high-frequency active filter designs. The key additional requirement is to establish the dc operating point of the signal near the supply midpoint for highest dynamic range. 図 8-9 shows an example design of a 1MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are ac-coupled using 0.1µF blocking capacitors (actually giving band-pass response with the low-frequency pole set to 32kHz for the component values shown). This configuration allows the midpoint bias formed by the two 1.87kΩ resistors to appear at both the input and output pins. The midband signal gain is set to +4 (12dB) in this case. The capacitor to ground on the noninverting input is intentionally designed at a greater value to dominate input parasitic terms. At a gain of +4, the OPA2830 on a single supply shows 30MHz of small- and large-signal bandwidth. The filter resistor values are slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 1MHz, –3dB point with a maximally flat pass band (above the 32kHz ac-coupling corner), and a maximum stop-band attenuation of 36dB at the amplifier –3dB bandwidth of 30MHz.

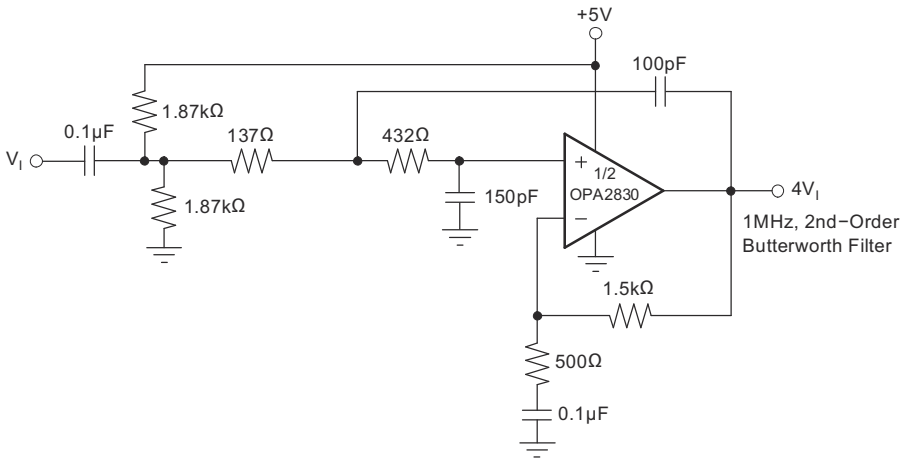


図 8-9. Single-Supply, High-Frequency Active Filter

8.1.7 Differential Low-Pass Active Filters

The dual OPA2830 offers an easy way to implement low-power differential active filters. On a single supply, 図 8-10 shows one way to implement a 2nd-order, low-pass filter. This circuit provides a net differential gain of 1 with a precise 5MHz Butterworth response. The signal is ac-coupled (giving a high-pass pole at low frequencies) with the dc operating point for the circuit set by the unity-gain buffer—the BUF602. This buffer gives a very low output impedance to high frequencies to maintain accurate filter characteristics. If the source is a dc coupled signal already biased into the operating range of the OPA2830 input CMR, these capacitors and the midpoint bias can be removed. To get the desired 5MHz cutoff, the input resistors to the filter is actually 119Ω. This is implemented in 図 8-10 as the parallel combination of the two 238Ω resistors on each half of the differential input as part of the dc biasing network. If the BUF602 is removed, these resistors must be collapsed back to a single 119Ω input resistor.

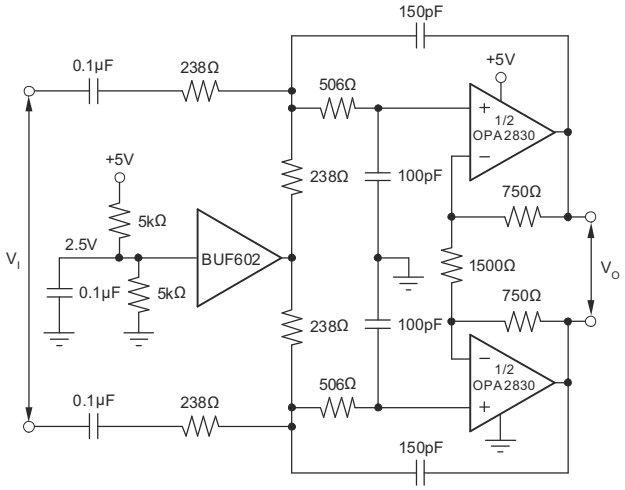


図 8-10. Single-Supply, 2nd-Order, Low-Pass Sallen-Key Filter

Implementing the dc bias in this way also attenuates the differential signal by half. This attenuation is recovered by setting the amplifier gain at 2V/V to get a net unity-gain filter characteristic from input to output. The filter design shown here has also adjusted the resistor values slightly from an calculated value to account for the 100MHz bandwidth in the amplifier stages. The filter capacitors at the noninverting inputs are shown as two separate capacitors to ground. While that is certainly correct to collapse these two capacitors into a single capacitor across the two inputs (which is 50pF for this circuit) to get the same differential filtering characteristic, tests have shown two separate capacitors to a low impedance point act to attenuate the common-mode feedback present in this circuit giving more stable operation in actual implementation. 図 8-11 shows the frequency response for the filter of 図 8-10.

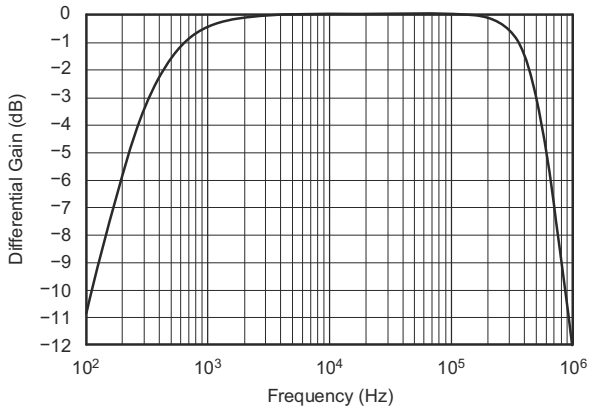


図 8-11. 5MHz, 2nd-Order, Butterworth Low-Pass Filter

8.1.8 High-Pass Filters

図 8-12 shows another approach to mid-supply biasing. This method uses a bypassed divider network in place of the buffer used in 図 8-10. The impedance is set by the parallel combination of the resistors forming the divider network, but as frequency increases impedance looks more and more like a short due to the capacitor. Generally, the capacitor value must be two to three orders of magnitude greater than the filter capacitors shown for the circuit to properly work.

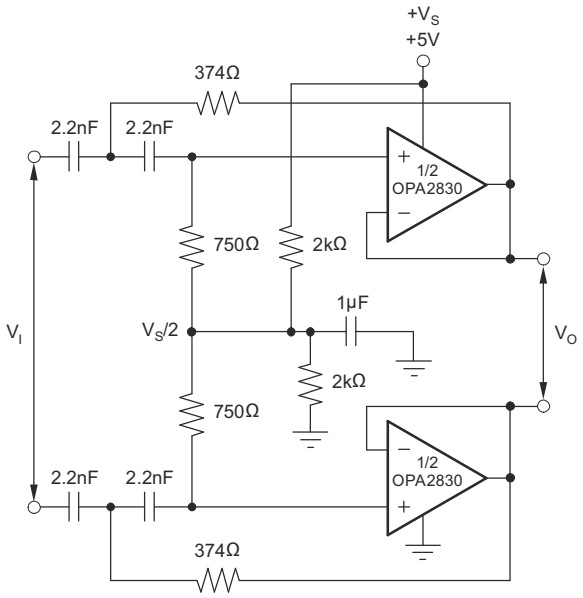


図 8-12. 138kHz, 2nd-Order, High-Pass Filter

Results showing the frequency response for the circuit of 図 8-12 is shown in 図 8-13.

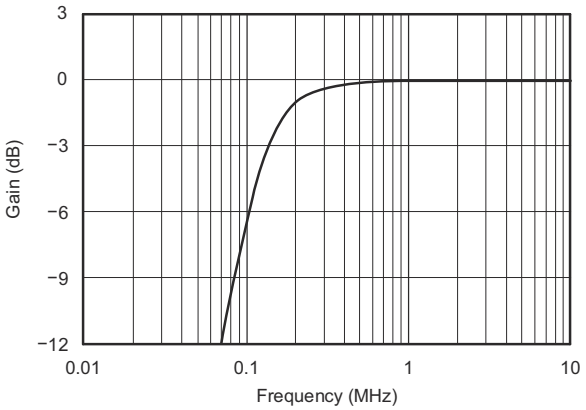


図 8-13. Frequency Response for the Filter of 図 8-12

8.1.9 High-Performance DAC Transimpedance Amplifier

High-frequency video digital-to-analog converters (DACs) sometimes benefit from a low distortion output amplifier to retain the SFDR performance into real-world loads. 図 8-14 shows a differential output drive implementation. The diagram shows one or more of the signal output currents connected into one or more of the virtual ground summing junctions of the OPA2830, which is set up as a transimpedance stage or *I-V converter*. If the DAC outputs require to terminate to a compliance voltage other than ground for operation, the appropriate voltage level can be applied to the noninverting input of the OPA2830. The dc gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D in 図 8-14) produces a zero in the noise gain for the OPA2830 that can cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network can be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \tag{4}$$

which gives a cutoff frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \tag{5}$$

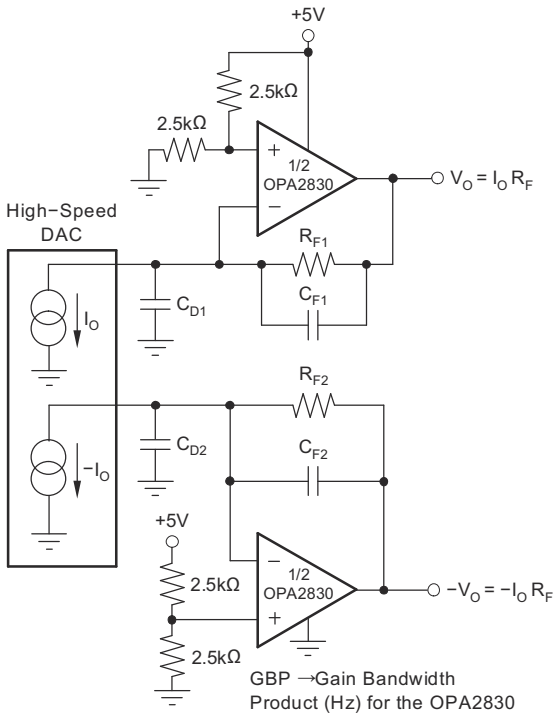


図 8-14. High-Speed DAC—Differential Transimpedance Amplifier

8.1.10 Operating Suggestions Optimizing Resistor Values

The OPA2830 is a unity-gain stable, voltage-feedback op amp; therefore, a wide range of resistor values can be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection can be made with a direct short.

Less than 200Ω, the feedback network presents additional output loading that can degrade the harmonic distortion performance of the OPA2830. Greater than 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor can cause unintentional band limiting in the amplifier response.

Recommended to target the parallel combination of R_F and R_G (see 図 8-3) to be less than about 400Ω. The combined impedance R_F || R_G interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding R_F || R_G < 400Ω keeps the pole above 200MHz. This constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G can be set equal to the required termination value. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) requires a 100Ω feedback resistor, which contributes to output loading in parallel with the external load. In such a case, preferably to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see 図 8-15). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

8.1.11 Bandwidth vs Gain: Noninverting Operation

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the gain bandwidth product (GBP) shown in the *Specifications*. This is designed for dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as in high-gain configurations. At low gains (increased feedback factors), most amplifier exhibits a more complex response with lower phase margin. The OPA2830 is compensated to give a slightly peaked response in a noninverting gain of 2 (see 図 8-3). This compensation results in a typical gain of +2 bandwidth of 105MHz, far exceeding that predicted by dividing the 105MHz GBP by 2. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 10MHz bandwidth shown in the *Electrical Characteristics* agrees with that predicted using the simple formula and the typical GBP of 105MHz.

Frequency response in a gain of +2 can be modified to achieve exceptional flatness simply by increasing the noise gain to 3. One method, without affecting the +2 signal gain, is to add an 2.55kΩ resistor across the two inputs (see 図 8-8). A similar technique can be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 750Ω feedback resistor along with a 750Ω resistor across the two op amp inputs, the voltage follower response is similar to the gain of +2 response of 図 8-2. Further reducing the value of the resistor across the op amp inputs, further dampen the frequency response due to increased noise gain. The OPA2830 exhibits minimal bandwidth reduction going to single-supply (5V) operation as compared with ±5V. This minimal reduction is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

8.1.12 Inverting Amplifier Operation

All of the familiar op amp application circuits are available to the designer with the OPA2830. 図 8-15 shows a typical inverting configuration where the I/O impedance and signal gain from 図 8-1 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. Inverting operation also allows the input to be biased at $V_S/2$ without any headroom issues. The output voltage can be independently moved to be within the output voltage range with coupling capacitors or bias adjustment resistors.

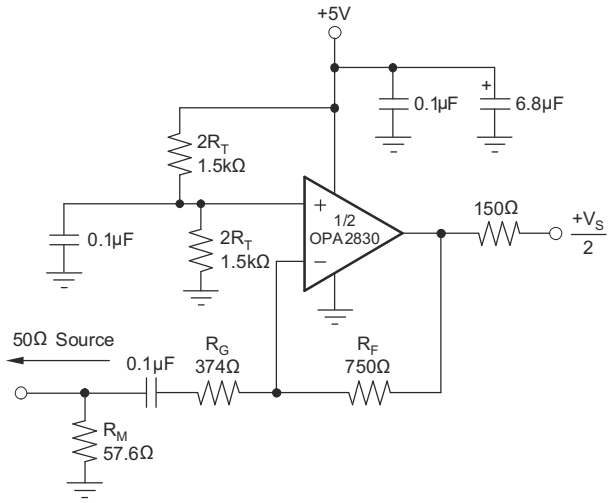


図 8-15. AC-Coupled, G = –2 Example Circuit

In the inverting configuration, consider three key design considerations. The first consideration is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace, or other transmission line conductor), R_G can be set equal to the required termination value and R_F adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance.

However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This configuration has the interesting advantage of the noise gain becoming equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered previously. The amplifier output now has the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor is limited to the 200Ω to 1.5kΩ range. In this case, preferably increase both the R_F and R_G values (see 図 8-15), and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For the example in 図 8-15, the R_M value combines in parallel with the external 50Ω source impedance (at high frequencies), yielding an effective driving impedance of 50Ω || 57.6Ω = 26.8Ω. This impedance is added in series with R_G for calculating the noise gain. The resulting noise gain is 2.87 for 図 8-15, as opposed to only 2 if R_M can be eliminated as discussed above. The bandwidth can therefore be lower for the gain of –2 circuit of 図 8-15 (NG = +2.87) than for the gain of +2 circuit of 図 8-1.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistors on the noninverting input (a parallel combination of R_T = 750Ω). If this resistor is set equal to the total dc resistance looking out of the inverting node, the output dc error, due to the input bias currents, can be reduced to (input offset current) times R_F. With the dc blocking capacitor in series with R_G, the dc source impedance looking out of

the inverting mode is simply R_F = 750Ω for 図 8-15. To reduce the additional high-frequency noise introduced by this resistor and power-supply feed-through, R_T is bypassed with a capacitor.

8.1.13 Output Current and Voltages

The OPA2830 provides outstanding output voltage capability. For the 5V supply, under no-load conditions at 25°C, the output voltage typically swings closer than 90mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the extreme cold temperature. Only at cold start up the output current and voltage decrease to the numbers shown in the tables. As the output transistors deliver power, the junction temperature increases, decreasing the V_{BE}s (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the overtemperature specifications because the output stage junction temperature is higher than the minimum specified operating ambient.

8.1.14 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which is recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2830 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective way is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristic curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2830. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see the *Board Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain also reduces the peaking (see 図 8-8).

8.1.15 Distortion Performance

The OPA2830 provides good distortion performance into a 150Ω load. Relative to alternatives, this device provides exceptional performance into lighter loads operating on a single 3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see 図 8-3) this is sum of R_F + R_G, while in the inverting configuration, only R_F must be included in parallel with the actual load. Running differentially suppresses the 2nd-harmonic; see also the differential *Typical Characteristics*.

8.1.16 Noise Performance

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve a high slew rate at the expense of a higher input noise voltage. However, the 9.2nV/√Hz input voltage noise for the OPA2830 is much less than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.8pA/√Hz) combine to give low output noise under a wide variety of operating conditions. 図 8-16 shows the op-amp noise-analysis model with all the noise terms included. In this model, all noise terms are taken to be noise-voltage or current-density terms in either nV/√Hz or pA/√Hz.

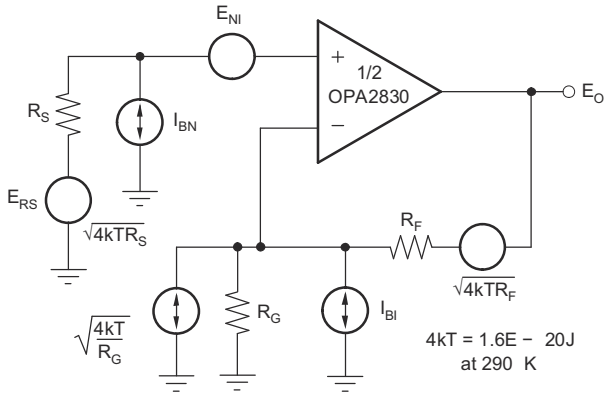


図 8-16. Noise Analysis Model

The total output spot noise voltage is computed as the square root of the sum of all squared output noise voltage contributors. 式 6 shows the general form for the output noise voltage using the terms shown in 図 8-16:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (6)$$

Dividing this expression by the noise gain
(NG = (1 + R_F / R_G)) gives the equivalent input-referred spot-noise voltage at the noninverting input shown in 式 7:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (7)$$

Evaluating these two equations for the circuit and component values shown in 図 8-1 gives a total-output spot-noise voltage of 19.3nV/√Hz and a total-equivalent-input spot-noise voltage of 9.65nV/√Hz. This result includes the noise added by the resistors. This total input-referred spot noise voltage is not much greater than the 9.2nV/√Hz specification for the op-amp voltage noise alone.

8.1.17 DC Accuracy and Offset Control

The balanced input stage of a wide-band voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. The power-supply current trim for the OPA2830 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5µA out of each input terminal), the close matching between them can be used to reduce the output dc error caused by this current. This is done by matching the dc source resistances appearing at the two inputs. Evaluating the configuration of 図 8-3 (which has matched dc input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

- (NG = noninverting signal gain at dc)
- $\pm(NG \times V_{OS(MAX)}) + (R_F \times I_{OS(MAX)})$
- $= \pm(2 \times 7.5mV) \times (375\Omega \times 1.1\mu A)$
- $= \pm 15.41mV$

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques are based on adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input can be considered. Bring the dc offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

8.2 Power Supply Recommendations

8.2.1 Thermal Analysis

The maximum desired junction temperature sets the maximum allowed internal power dissipation. Do not exceed the maximum junction temperature of 150°C.

The operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the device. P_{DL} depends on the required output signal and load; however, for resistive loads connected to mid-supply ($V_S/2$), P_{DL} is at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2 / (16 \times R_L)$, where R_L includes feedback network loading.

The power in the output stage, and not into the load, determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2830 (VSSOP-8 package) in the circuit of 図 8-3 operating at the maximum specified ambient temperature of 85°C and driving a 150Ω load at $2.5V_{DC}$ on both outputs.

$P_D = 10V \times 11.9mA + 2 \times [5^2 / (16 \times (150\Omega \parallel 1500\Omega))] = 142mW$

Maximum $T_J = +85°C + (0.142W \times 122.6°C/W) = 102.5°C$.

Although this result is still much less than the specified maximum junction temperature, system reliability considerations require lower junction temperatures. The highest possible internal dissipation occurs if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This configuration forces a high current through a large internal voltage drop in the output transistors.

8.3 Layout

8.3.1 Board Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA2830 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, capacitance can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins can be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes can be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout can not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Each power-supply connection is always be decoupled with one of these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, can also be used on the main supply pins. These can be placed somewhat farther from the device and shared among several devices in the same area of the PC board.

c) Carefully select and place external components to preserve high-frequency performance. Resistors must be a very low reactant type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keeping the leads and PCB traces as short as possible. Never use wire-wound type resistors in a high-frequency application. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, can also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can

degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the Typical Characteristics is a good starting point for design.

d) Connections to other wide-band devices on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) can be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) do not need an R_S since the OPA2830 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using micro-strip or strip-line techniques (consult an ECL design handbook for micro-strip and strip-line layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment improves the distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2830 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance can be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve *Recommended R_S vs Capacitive Load*. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Do not socket a high-speed part. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2830 onto the board.

8.3.1.1 Input and ESD Protection

The OPA2830 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in 図 8-17.

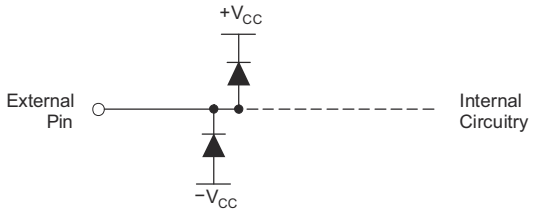


図 8-17. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages greater than the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA2830), current-limiting series resistors added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Design-In Tools

9.1.1.1 Demonstration Fixtures

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2830 with two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in 表 9-1.

表 9-1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2830ID	SOIC-8	DEM-OPA-SO-2A	SBOU003
OPA2830IDGK	VSSOP-8	DEM-OPA-MSOP-2A	SBOU004

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2830 product folder.

9.1.1.2 Macro-model and Applications Support

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA2830 circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA2830 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in small-signal AC performance.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (August 2008) to Revision E (December 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「パッケージ情報」表、「ピンの機能」表、「ESD 定格」、「熱に関する情報」、「推奨動作条件」、「詳細説明」セクションを追加	1
• Updated electrical characteristics to match device performance	4
• Updated plots in *Typical Characteristics*	10
• Updated thermal analysis with new θ_{JA}	38

Changes from Revision C (March 2006) to Revision D (August 2008)	Page
• Changed rating of storage temperature range in Absolute Maximum Ratings table from –40°C to +125°C to–65°C to +125°C	3

Changes from Revision B (February 2006) to Revision C (August 2008)	Page
• Changed differential input voltage to ±2.5V from ±1.2V	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2830ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 2830
OPA2830IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 85	A59
OPA2830IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	A59
OPA2830IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	A59
OPA2830IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(2830, OPA)
OPA2830IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(2830, OPA)
OPA2830IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(2830, OPA)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

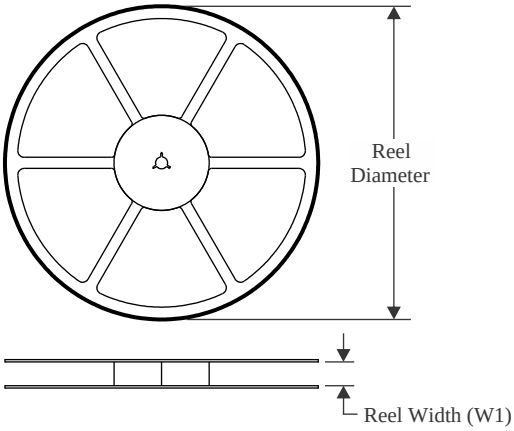
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

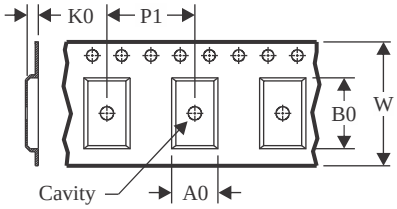
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

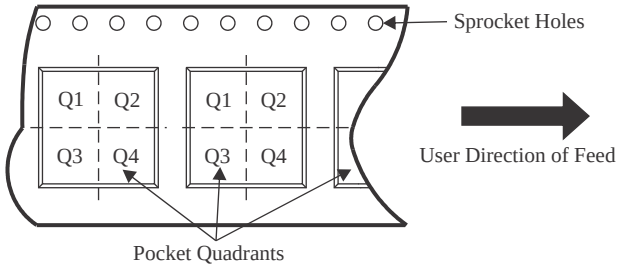


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

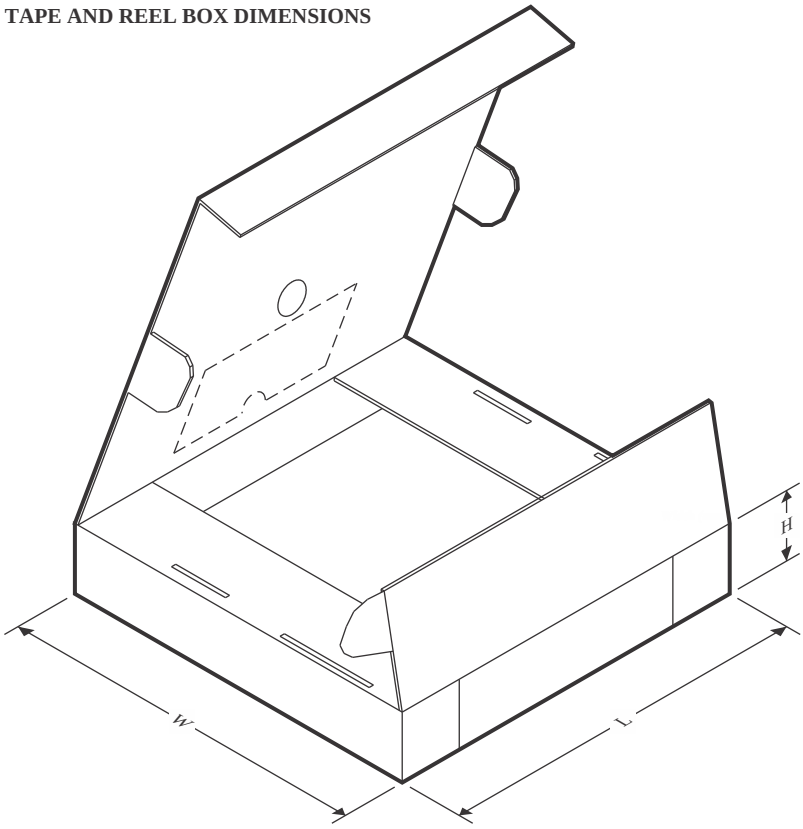
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

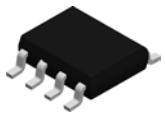
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2830IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2830IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2830IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2830IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2830IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2830IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2830IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2830IDR	SOIC	D	8	2500	353.0	353.0	32.0

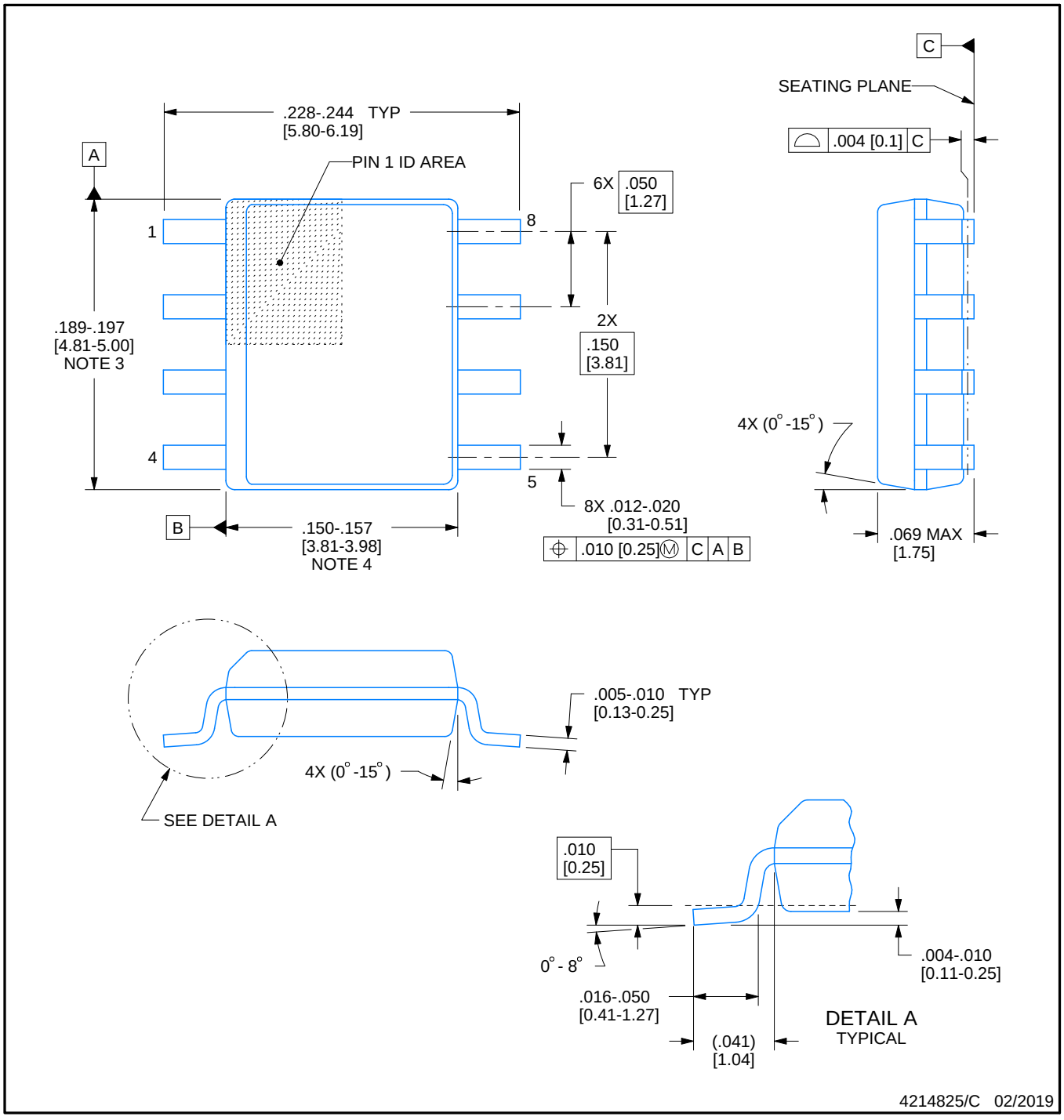


PACKAGE OUTLINE

D0008A

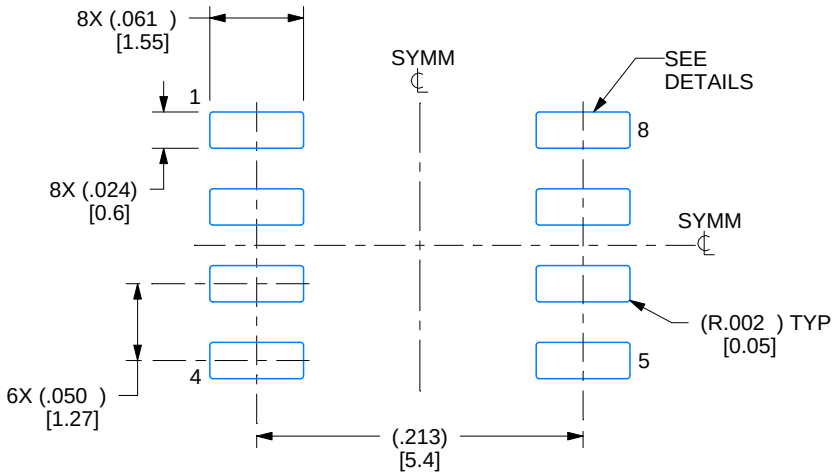
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

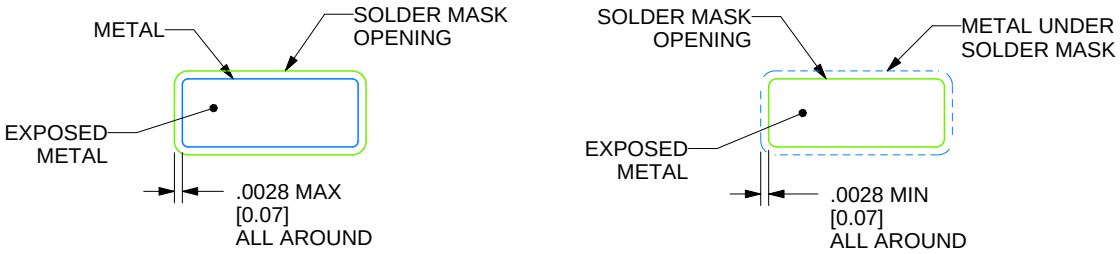


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

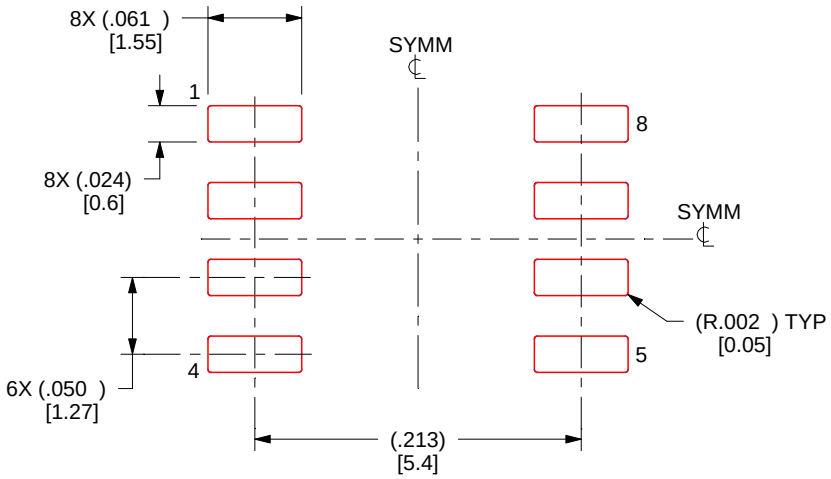
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

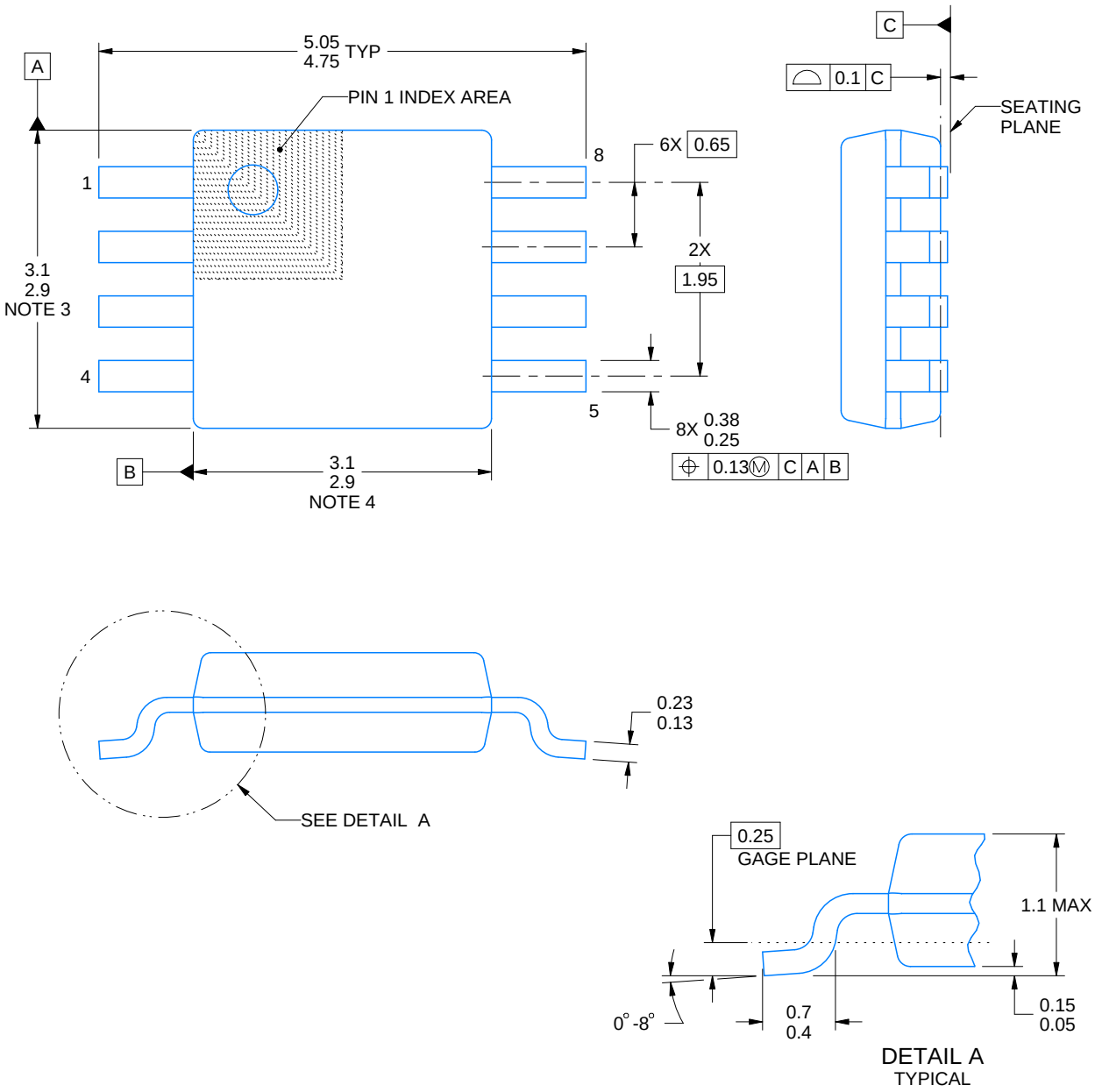
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

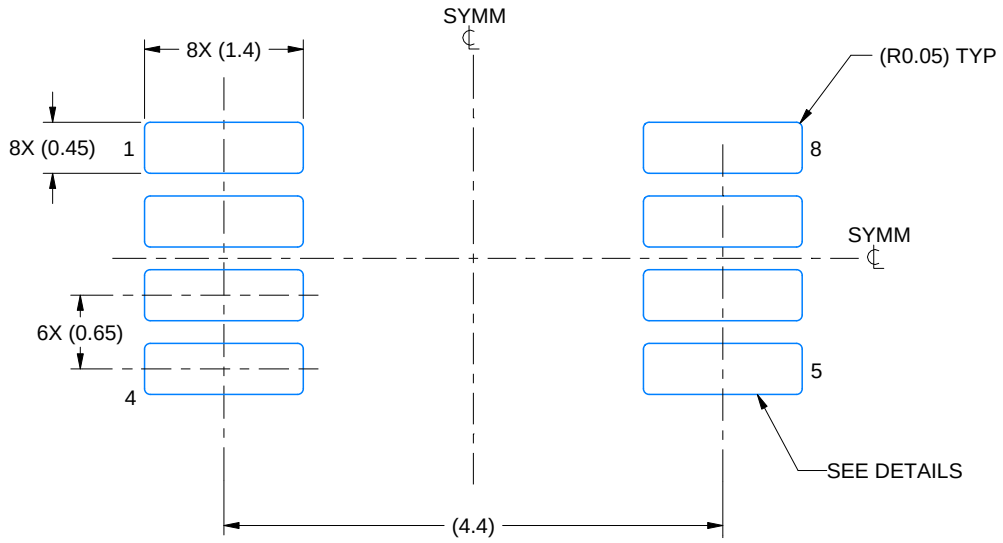
SMALL OUTLINE PACKAGE



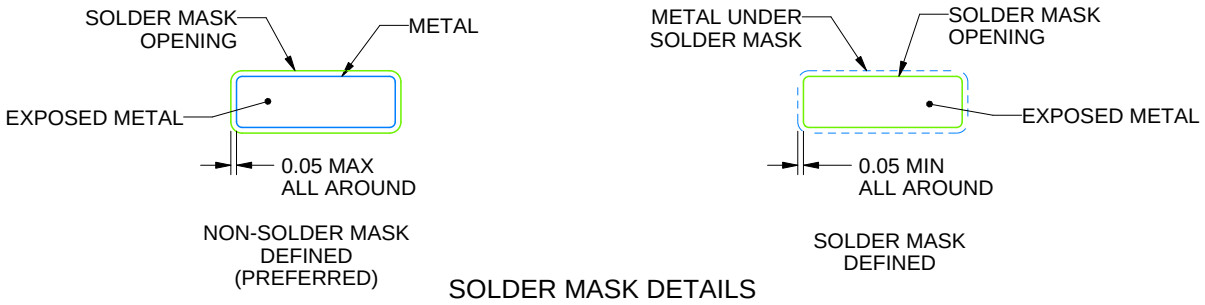
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

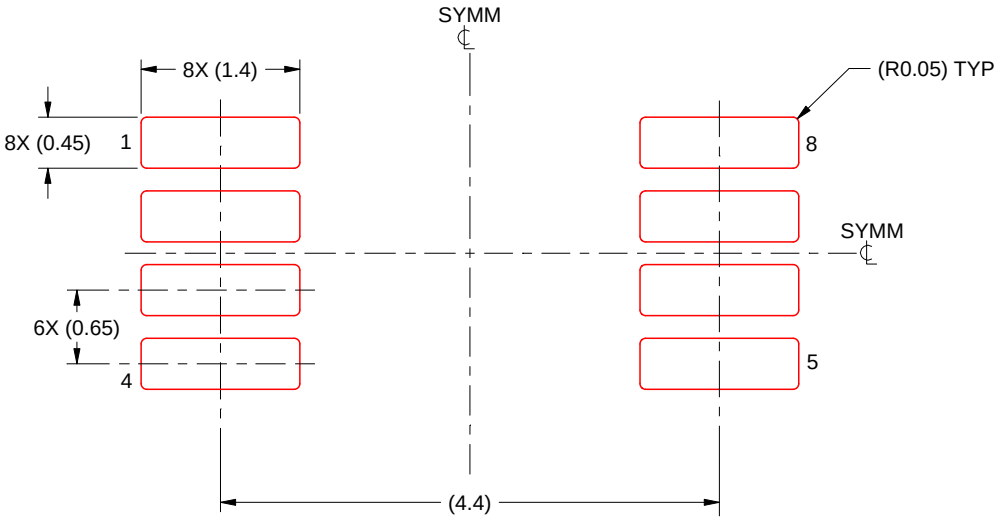


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月