OPAx354 250MHz、レール・ツー・レールI/O、CMOSオペアンプ

1 特長

- **ユニティ・ゲイン帯域幅**: 250MHz
- **広い帯域幅**: 100MHz GBW
- **高いスルー・レート**: 150V/µs
- **低ノイズ**: 6.5nV/√Hz
- **レール・ツー・レールI/O**
- **高い出力電流**: 100mA超
- **非常に優れたビデオ性能**
  - 差動ゲイン: 0.02%、差動位相: 0.09°
  - 0.1dBのゲイン・フラットネス(40MHz)
- **低い入力バイアス電流**: 3pA
- **静止電流**: 4.9mA
- **サーマル・シャットダウン**
- **電源電圧範囲**: 2.5V～5.5V
- *Micro*SIZEおよび PowerPAD™搭載のパッケージ

2 アプリケーション

- ビデオ処理
- 超音波
- 光ネットワーク、調節可能なレーザー
- フォトダイオード・トランスインピーダンス・アンプ
- アクティブ・フィルタ
- 高速積分器
- A/Dコンバータ入力バッファ
- D/Aコンバータ出力アンプ
- バーコード・スキャナ
- 通信

3 概要

OPAx354シリーズの高速、電圧帰還型CMOSオペアンプは、広い帯域幅を必要とするビデオおよびその他のアプリケーション用に設計されています。これらはユニティ・ゲイン安定で、大きな出力電流を駆動できます。差動ゲインは0.02%、差動位相は0.09°です。静止電流はチャネルごとにわずか4.9mAです。

OPAx354シリーズのオペアンプは、最低2.5V (±1.25V)、最高5.5V (±2.75V)のシングルまたはデュアル電源で動作するよう最適化されています。同相入力範囲は電源の範囲よりも拡大されています。出力スイングはレールから100mV以内で、広いダイナミック・レンジに対応しています。

100mAの連続出力電流のすべてを必要とするアプリケーションでは、シングルおよびデュアルの8ピンHSOP PowerPADバージョンを使用できます。

シングル・バージョン(OPA354)は、小型の5ピンSOT-23および8ピンHSOP PowerPADパッケージで供給されます。デュアル・バージョン(OPA2354)は、小型の8ピンVSSOPおよび8ピンHSOP PowerPADパッケージで供給されます。クワッド・バージョン(OPA4354)は14ピンTSSOPと14ピンSOICパッケージで供給されます。

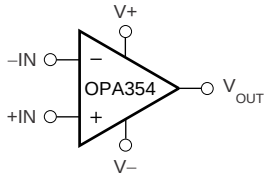
マルチチャネル・バージョンは、完全に独立した回路により、クロストークを最小化し、干渉の発生を防止しています。すべての仕様は、拡張温度範囲の-40℃～+125℃で規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA354	HSOP (8)	4.89mm×3.90mm
	SOT-23 (5)	2.90mm×1.60mm
OPA2354	VSSOP (8)	3.00mm×3.00mm
	HSOP (8)	4.89mm×3.90mm
OPA4354	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

Revision F (June 2016) から **Revision G** に変更 **Page**

- Deleted table note about input pins and input signals from *Absolute Maximum Ratings* table ... 6

Revision E (March 2002) から **Revision F** に変更 **Page**

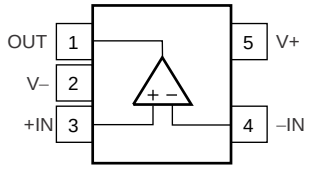
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- データシートの末尾にあるPOAを参照し、「*パッケージ/注文情報*」表を 削除 ... 1
- Renamed *OPAx354 Related Products* table to *Device Comparison Table* ... 3

5 Device Comparison Table

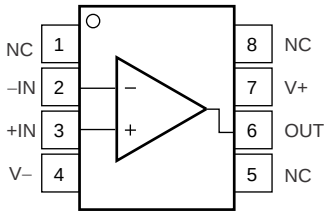
FEATURES	PRODUCT
Shutdown Version of OPAx354 Family	OPAx357
200-MHz GBW, Rail-to-Rail Output, CMOS, Shutdown	OPAx355
200-MHz GBW, Rail-to-Rail Output, CMOS	OPAx356
38-MHz GBW, Rail-to-Rail Input/Output, CMOS	OPAx350/OPAx353
75-MHz BW G = 2, Rail-to-Rail Output	OPA2631
150-MHz BW G = 2, Rail-to-Rail Output	OPA2634
100-MHz BW, Differential Input/Output, 3.3-V Supply	THS412x

6 Pin Configuration and Functions

OPA354 DBV Package
5-Pin SOT-23
Top View



OPA354 DDA Package
8-Pin HSOP
Top View



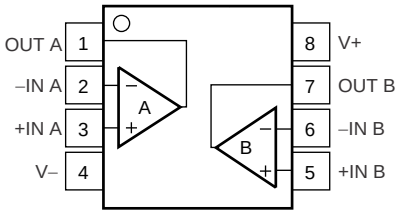
NC – no internal connection

PowerPAD must be connected to V− or left floating.

Pin Functions: OPA354

PIN			I/O	DESCRIPTION
NAME	SOT-23	HSOP		
–IN	4	2	I	Inverting input
+IN	3	3	I	Noninverting input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) supply
V+	5	7	—	Positive (highest) supply

OPA2354 DGK and DDA Packages
8-Pin VSSOP, HSOP
Top View

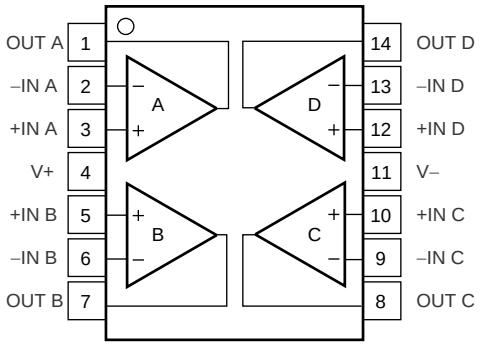


(1) PowerPAD must be connected to V− or left floating.

Pin Functions: OPA2354

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply
V+	8	—	Positive (highest) supply

OPA4354 D and PW Packages
14-Pin SOIC, TSSOP
Top View



Pin Functions: OPA4354

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply
V+	4	—	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V−		7.5	V
	Signal input terminals	(V−) − (0.5)	(V+) + 0.5	
Current	Signal input terminals	–10	10	mA
	Output short circuit(2)	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.5	5.5	V
	Specified temperature	–40	125	°C

7.4 Thermal Information: OPA354

THERMAL METRIC(1)		OPA354		UNIT
		DBV (SOT-23)	DDA (HSOP)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.3	42.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.3	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	26.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.3	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2354

THERMAL METRIC(1)		OPA2354		UNIT
		DDA (HSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	175.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4354

THERMAL METRIC(1)		OPA4354		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics: V_S = 2.7 V to 5.5 V (Single-Supply)

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V T_A = 25°C		±2	±8	mV
		V_S = 5 V, T_A = −40°C to +125°C			±10	
dV_{OS}/dT	Input offset voltage vs temperature	V_S = 5 V T_A = −40°C to +125°C		±4		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 5.5 V V_{CM} = (V_S / 2) − 0.55 V		±200	±800	µV/V
		V_S = 2.7 V to 5.5 V V_{CM} = (V_S / 2) − 0.55 V at T_A = −40°C to +125°C			±900	
INPUT BIAS CURRENT						
I_B	Input bias current			3	±50	pA
I_{OS}	Input offset current			±1	±50	pA
NOISE						
e_n	Input voltage noise density	f = 1 MHz		6.5		nV/√Hz
i_n	Current noise density	f = 1 MHz		50		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V –0.1 V < V_{CM} < 3.5 V T_A = 25°C	66	80		dB
		V_S = 5.5 V –0.1 V < V_{CM} < 3.5 V T_A = −40°C to +125°C	64			
		V_S = 5.5 V –0.1 V < V_{CM} < 5.6 V T_A = 25°C	56	68		
		V_S = 5.5 V –0.1 V < V_{CM} < 5.6 V T_A = −40°C to +125°C	55			
INPUT IMPEDANCE						
	Differential			10^{13} || 2		Ω || pF
	Common-mode			10^{13} || 2		Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop gain	V_S = 5.5 V 0.3 V < V_O < 4.7 V T_A = 25°C	94	110		dB
		V_S = 5 V 0.4 V < V_O < 4.6 V T_A = −40°C to +125°C	90			
FREQUENCY RESPONSE						
f_{-3dB}	Small-signal bandwidth	At G = +1 V_O = 100 mV_{PP} R_F = 25 Ω		250		MHz
		At G = +2 V_O = 100 mV_{PP}		90		
GBW	Gain-bandwidth product	G = +10		100		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness	At G = +2 V_O = 100 mV_{PP}		40		MHz

Electrical Characteristics: V_S = 2.7 V to 5.5 V (Single-Supply) (continued)

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	V_S = 5 V, G = +1, 4-V step		150		V/µs
		V_S = 5 V, G = +1, 2-V step		130		
		V_S = 3 V, G = +1, 2-V step		110		
	Rise-and-fall time	At G = +1 V_O = 200 mV_{PP} 10% to 90%		2		ns
		At G = +1, V_O = 2 V_{PP}, 10% to 90%		11		
	Settling time	0.1%, V_S = 5 V, G = +1 2-V output step		30		ns
		0.01%, V_S = 5 V, G = +1 2-V output step		60		
	Overload recovery time	V_{IN} × Gain = V_S		5		ns

Electrical Characteristics: V_S = 2.7 V to 5.5 V (Single-Supply) (continued)

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE (CONTINUED)							
	Harmonic distortion	Second harmonic	At G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–75		dBc
		Third harmonic	At G = +1, f = 1 MHz V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–83		
	Differential gain error		NTSC, R_L = 150 Ω		0.02%		
	Differential phase error		NTSC, R_L = 150 Ω		0.09		°
	Channel-to-channel crosstalk	OPA2354	f = 5 MHz		–100		dB
		OPA4354			–84		
OUTPUT							
	Voltage output swing from rail		V_S = 5 V, R_L = 1 kΩ, A_{OL} > 94 dB T_A = 25°C		0.1	0.3	V
			V_S = 5 V, R_L = 1 kΩ, A_{OL} > 90 dB T_A = −40°C to +125°C			0.4	
I_O	Output current, single, dual, quad(1)(2)		V_S = 5 V	100			mA
			V_S = 3 V		50		mA
	Closed-loop output impedance		f < 100 kHz		0.05		Ω
R_O	Open-loop output resistance				35		Ω
POWER SUPPLY							
V_S	Specified voltage			2.7		5	V
	Operating voltage			2.5		5.5	
I_Q	Quiescent current (per amplifier)		T_A = 25°C, V_S = 5 V (enabled) I_O = 0		4.9	6	mA
			T_A = –40°C to +125°C			7.5	
THERMAL SHUTDOWN: JUNCTION TEMPERATURE							
	Shutdown				160		°C
	Reset from shutdown				140		°C
THERMAL RANGE							
	Specified			–40		125	°C
	Operating			–55		150	°C
	Storage			–65		150	°C

(1) See typical characteristic curves, *Output Voltage Swing vs Output Current* (図 20 and 図 22).
(2) Specified by design.

7.8 Typical Characteristics

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

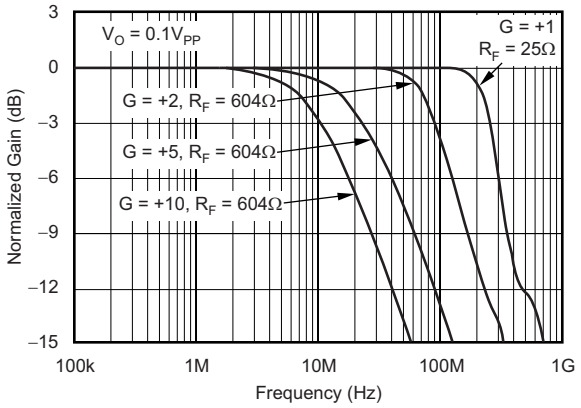


図 1. Noninverting Small-Signal Frequency Response

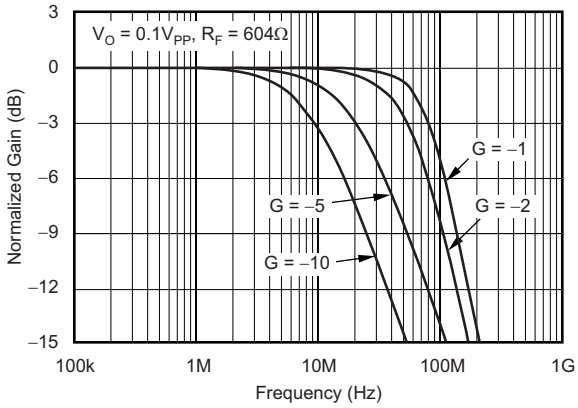


図 2. Inverting Small-Signal Frequency Response

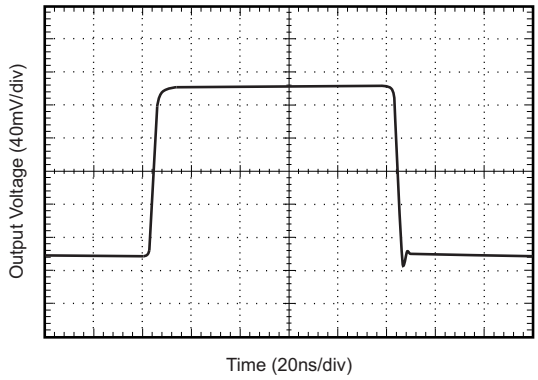


図 3. Noninverting Small-Signal Step Response

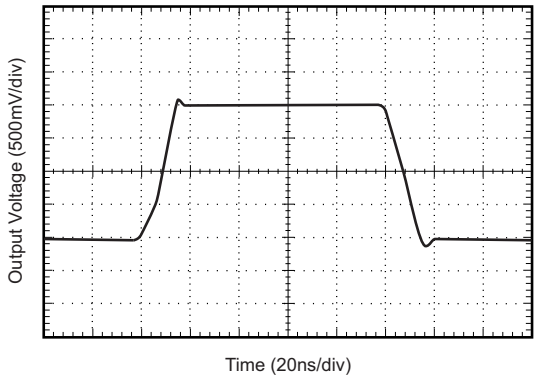


図 4. Noninverting Large-Signal Step Response

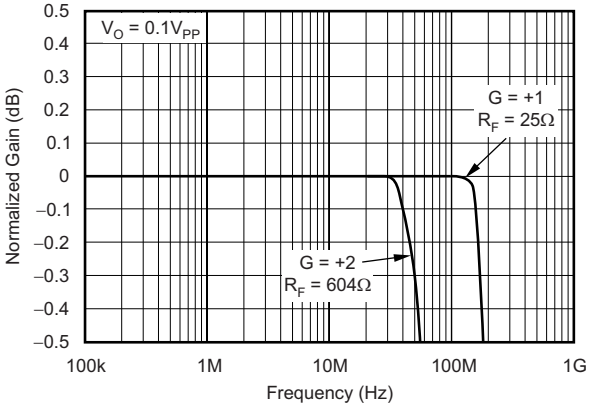


図 5. 0.1-dB Gain Flatness

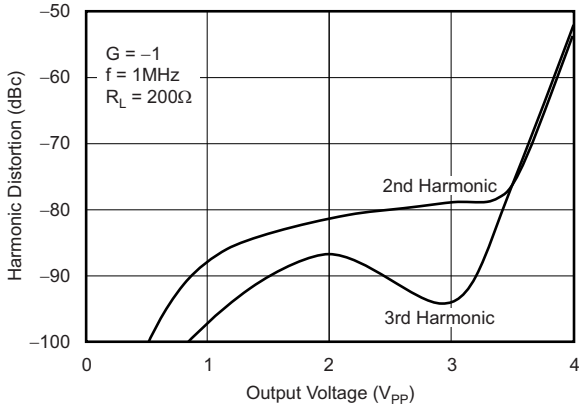


図 6. Harmonic Distortion vs Output Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

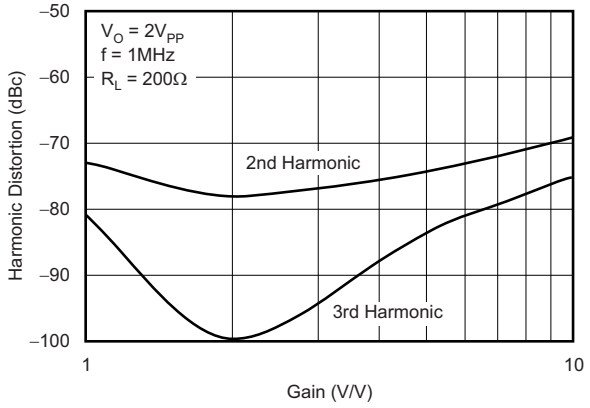


図 7. Harmonic Distortion vs Noninverting Gain

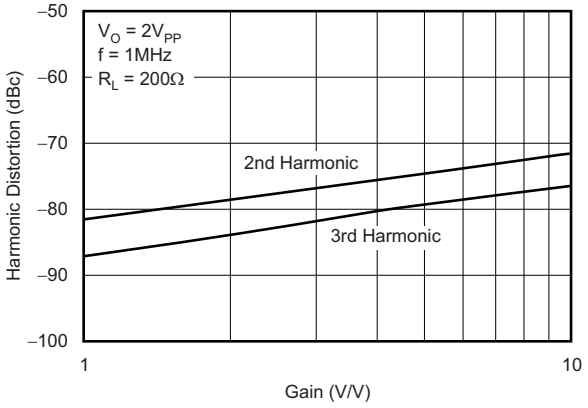


図 8. Harmonic Distortion vs Inverting Gain

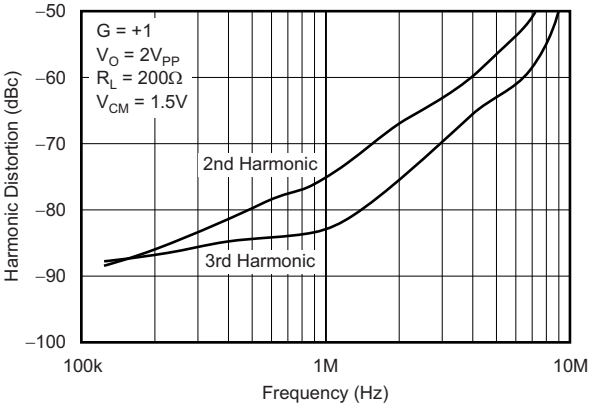


図 9. Harmonic Distortion vs Frequency

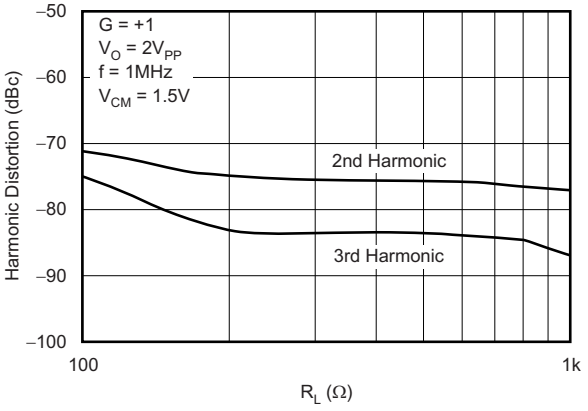


図 10. Harmonic Distortion vs Load Resistance

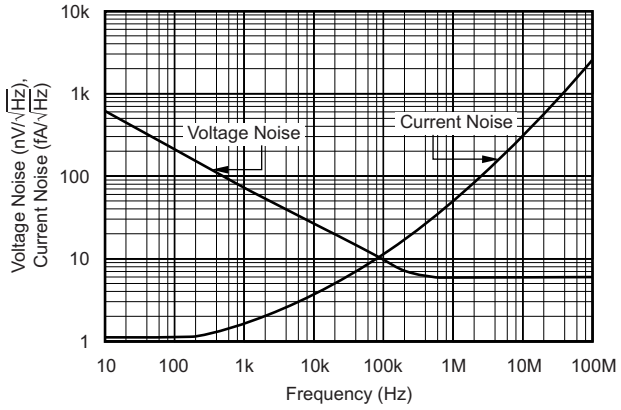


図 11. Input Voltage and Current Noise Spectral Density vs Frequency

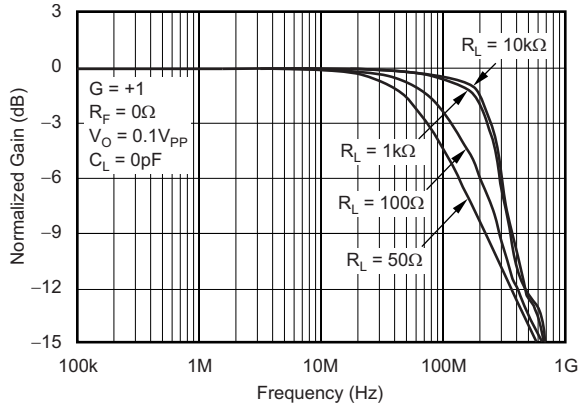


図 12. Frequency Response for Various R_L Values

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

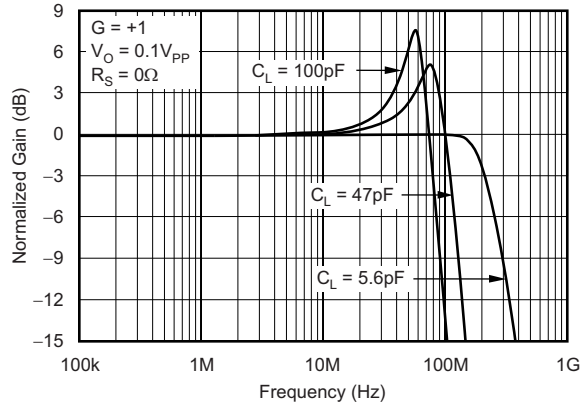


図 13. Frequency Response for Various C_L Values

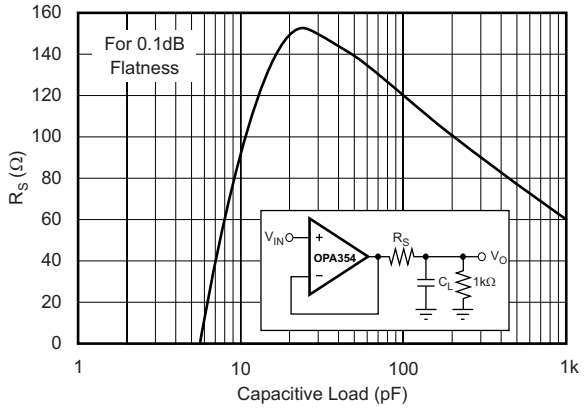


図 14. Recommended R_S vs Capacitive Load

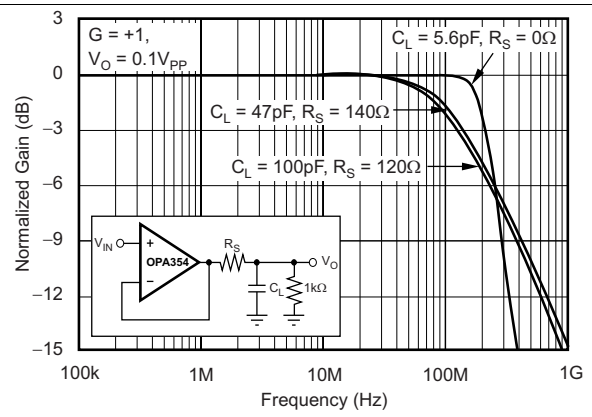


図 15. Frequency Response vs Capacitive Load

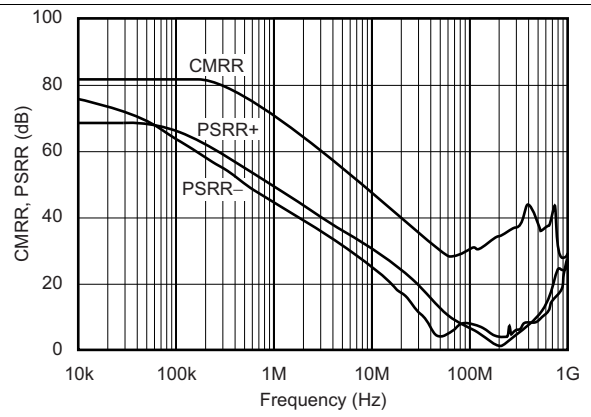


図 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

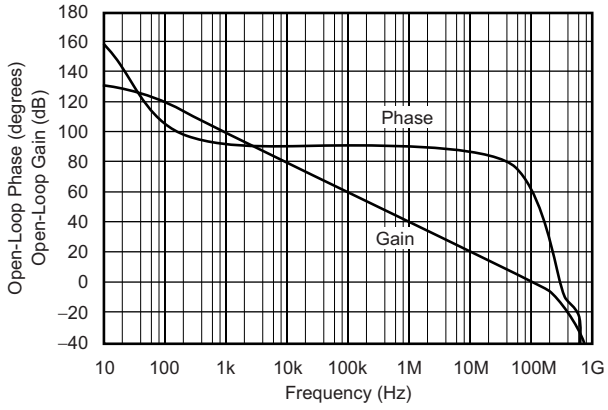


図 17. Open-Loop Gain and Phase

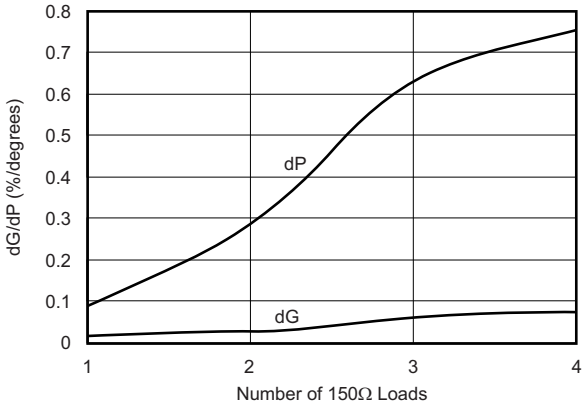


図 18. Composite Video Differential Gain and Phase

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

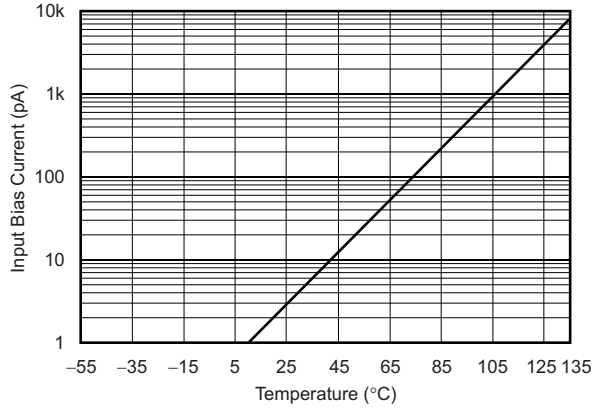


図 19. Input Bias Current vs Temperature

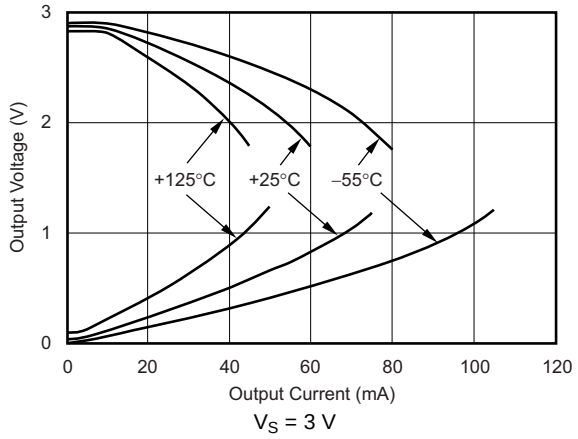


図 20. Output Voltage Swing vs Output Current

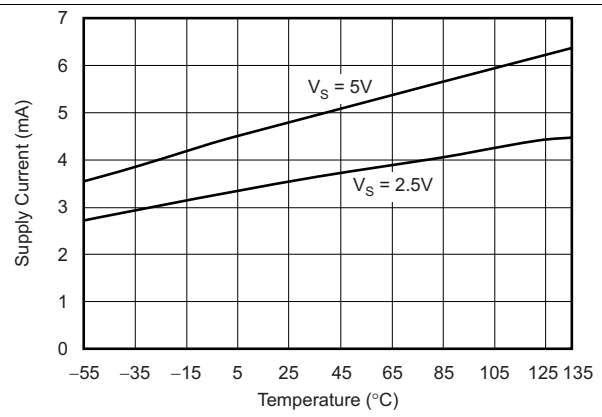


図 21. Supply Current vs Temperature

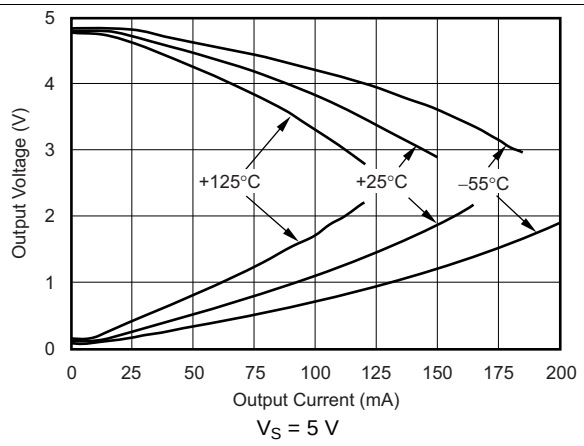


図 22. Output Voltage Swing vs Output Current

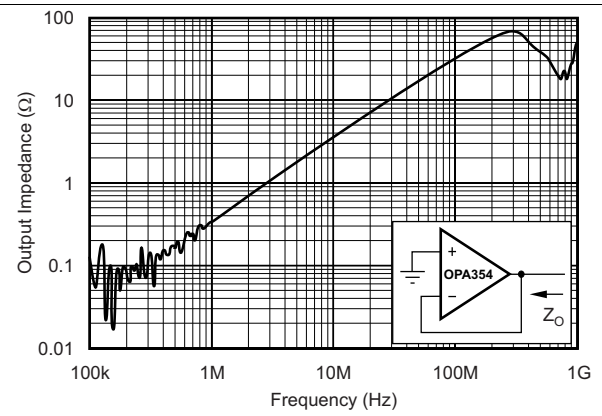


図 23. Closed-Loop Output Impedance vs Frequency

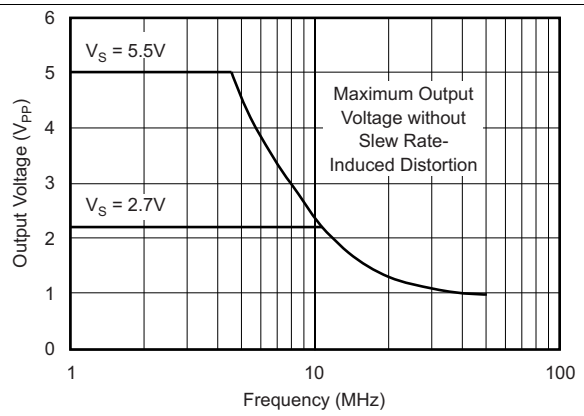


図 24. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

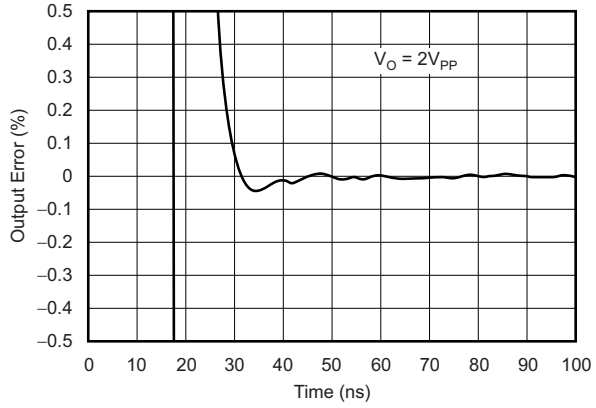


図 25. Output Settling Time to 0.1%

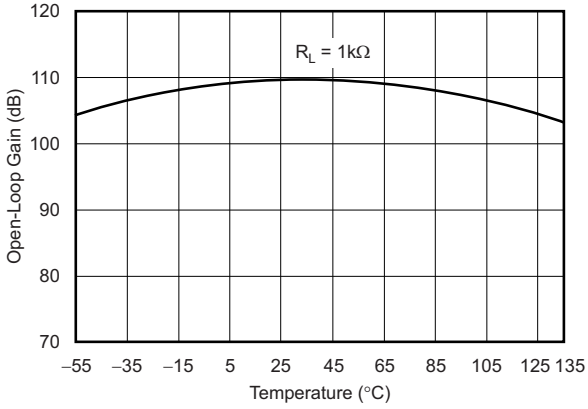


図 26. Open-Loop Gain vs Temperature

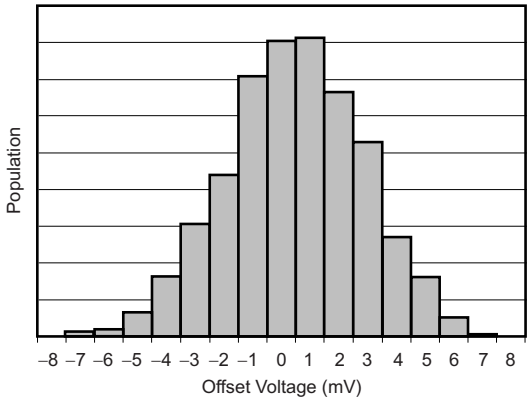


図 27. Offset Voltage Production Distribution

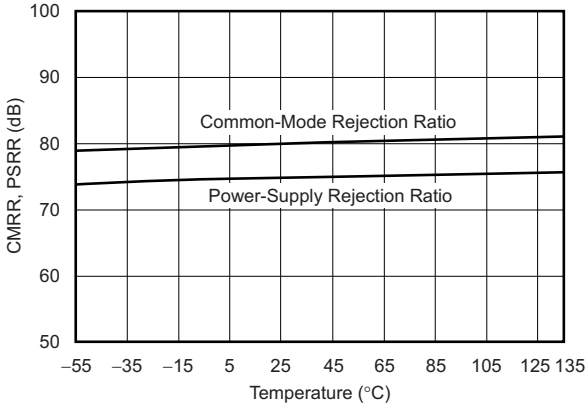


図 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

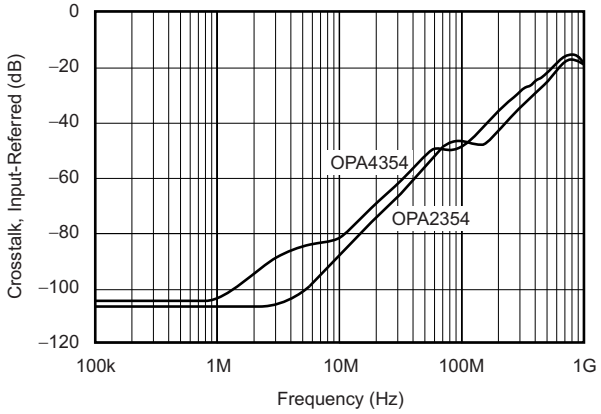


図 29. Channel-to-Channel Crosstalk

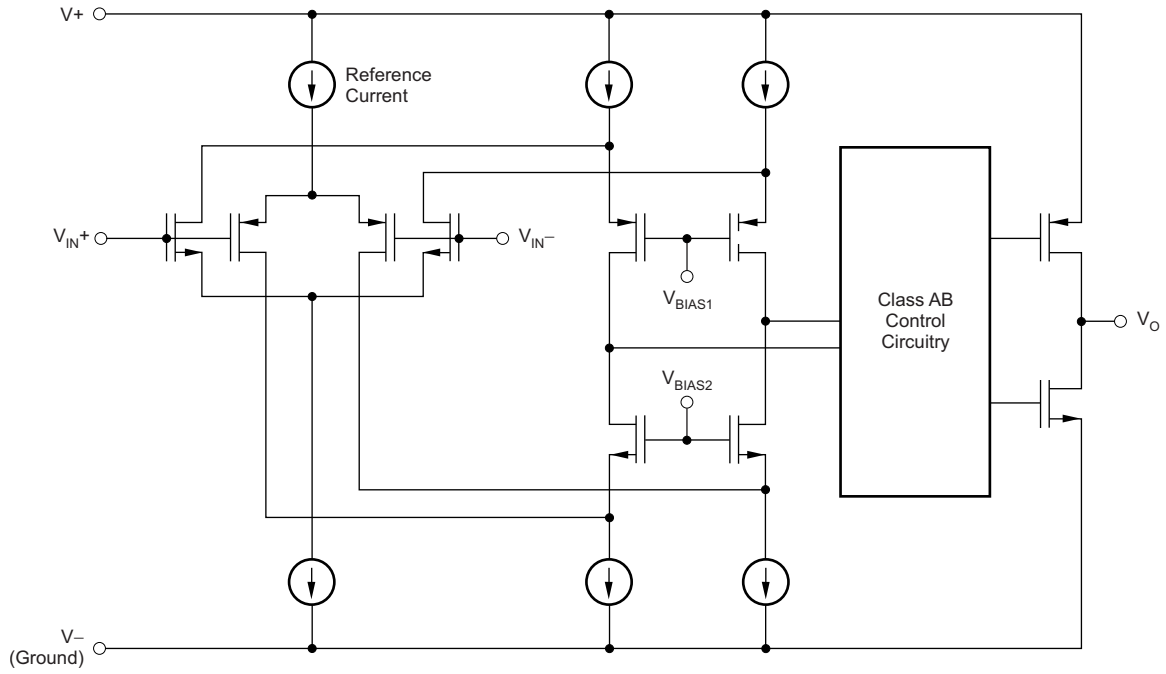
8 Detailed Description

8.1 Overview

The OPAx354 is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. It is available as a single, dual, or quad op amp.

The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but the amplifier is unity-gain stable and can operate as a 1-V/V voltage follower.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPAx354 is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics section of this data sheet.*

8.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the OPAx354 extends 100 mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2 V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) − 1.2 V. There is a small transition region, typically (V+) − 1.5 V to (V+) − 0.9 V, in which both pairs are on. This 600-mV transition region vary ±500 mV with process variation. Therefore, the transition region (both input stages on) range from (V+) − 2 V to (V+) − 1.5 V on the low end, up to (V+) − 0.9 V to (V+) − 0.4 V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

8.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors achieves rail-to-rail output. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a useful output swing is achieved while maintaining high open-loop gain. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (図 20 and 図 22).

8.3.4 Output Drive

The OPAx354 output stage supplies a continuous output current of ±100 mA and yet provide approximately 2.7 V of output swing on a 5-V supply, as shown in 図 30. For maximum reliability, TI does not recommend running a continuous DC current in excess of ±100 mA. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (図 20 and 図 22). For supplying continuous output currents greater than ±100 mA, the OPAx354 may be operated in parallel, as shown in 図 31.

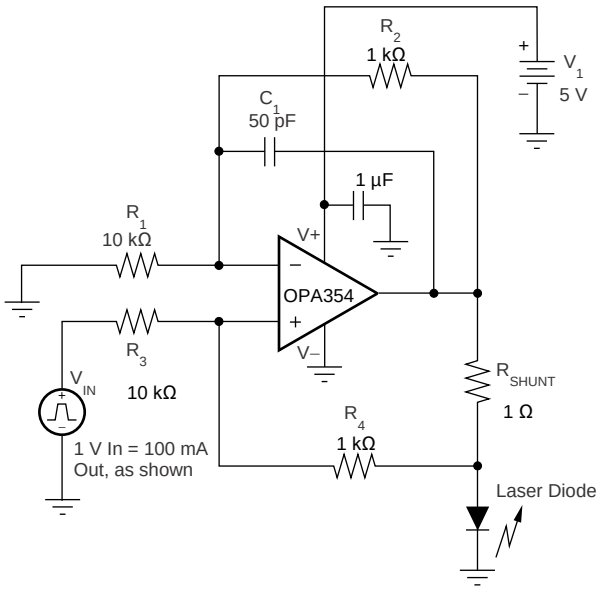


図 30. Laser Diode Driver

Feature Description (continued)

The OPAx354 provides peak currents up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPAx354 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

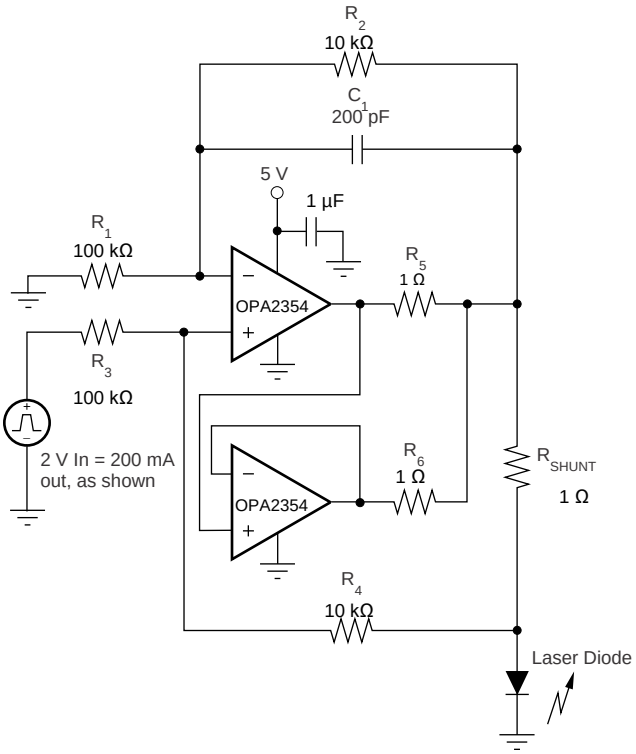


図 31. Parallel Operation

8.3.5 Video

The OPAx354 output stage is capable of driving standard back-terminated 75-Ω video cables, as shown in 図 32. By back-terminating a transmission line, the output stage does not exhibit a capacitive load to the driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the cable presents a 150-Ω resistive load to the OPAx354 output.

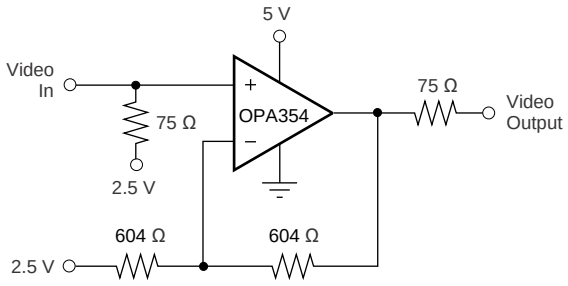
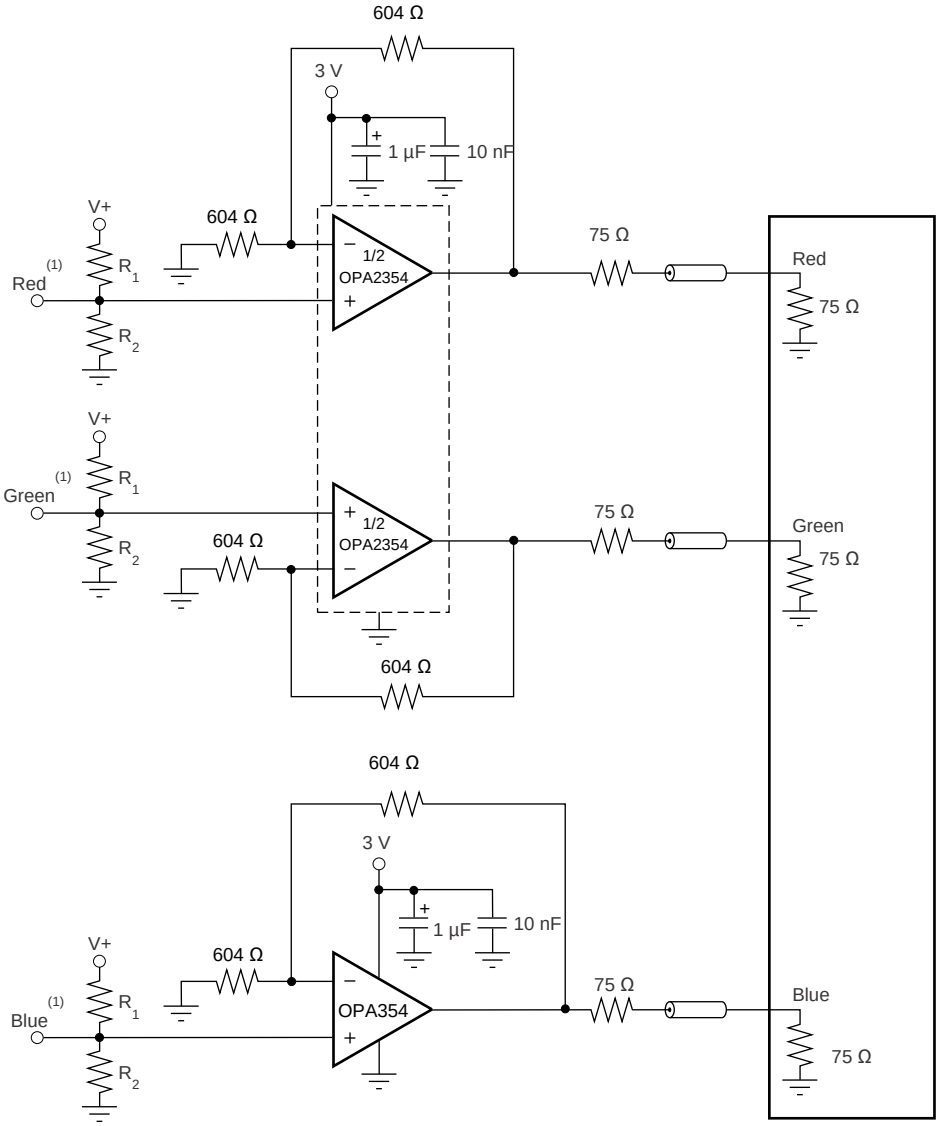


図 32. Single-Supply Video Line Driver

The OPAx354 is used as an amplifier for RGB graphic signals, which feature a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See 図 33.

Feature Description (continued)



(1) Source video signal offset 300 mV above ground to accommodate op amp swing−to−ground capability.

図 33. RGB Cable Driver

Feature Description (continued)

8.3.6 Driving Analog-to-Digital converters

The OPAx354 series op amps offer 60 ns of settling time to 0.01%, making the series a good choice for driving high- and medium-speed sampling A/D converters and reference circuits. The OPAx354 series provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, the OPA350 series is recommended.

図 34 shows the OPAx354 driving an A/D converter. With the OPAx354 in an inverting configuration, a capacitor across the feedback resistor is used to filter high-frequency noise in the signal.

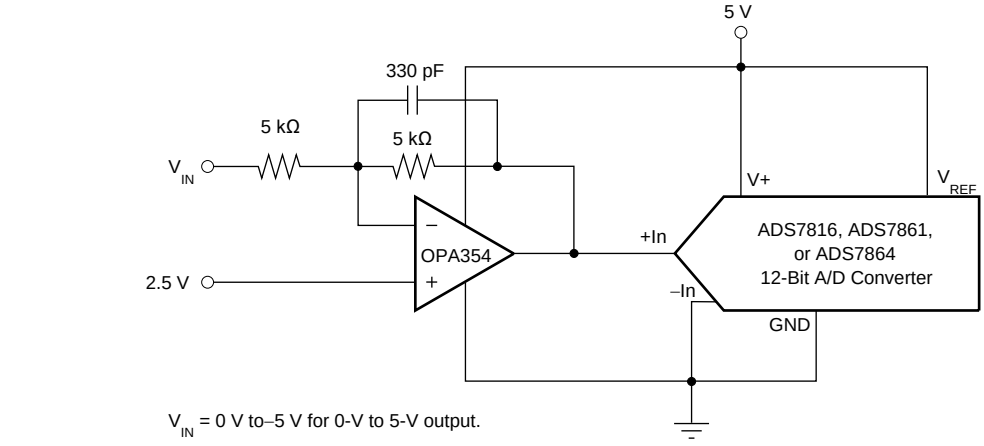


図 34. The OPAx354 in Inverting Configuration Driving the ADS7816

8.3.7 Capacitive Load and Stability

The OPAx354 series op amps drives a wide range of capacitive loads. However, all op amps may become unstable under certain conditions. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. See the *Frequency Response for Various C_L* typical characteristic curve (図 13) for details.

The OPAx354 topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. See the *Recommended R_S vs Capacitive Load* (図 14) and *Frequency Response vs Capacitive Load* (図 15) typical characteristic curves for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in 図 35. This configuration significantly reduces ringing with large capacitive loads; see the *Frequency Response vs Capacitive Load* typical characteristic curve (図 15). However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is an error of approximately 0.2% at the output.

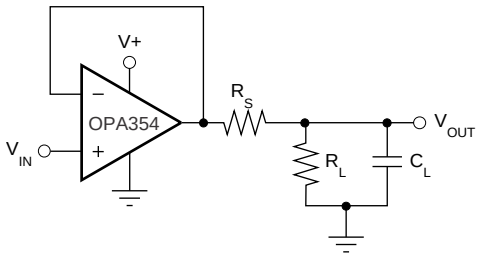


図 35. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

Feature Description (continued)

8.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 a preferred wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design (as shown in 図 36) are the expected diode capacitance [including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the OPAx354], the desired transimpedance gain (R_F), and the gain-bandwidth product (GBW) for the OPAx354 (100 MHz, typical). With these three variables set, the feedback capacitor value (C_F) may be set to control the frequency response.

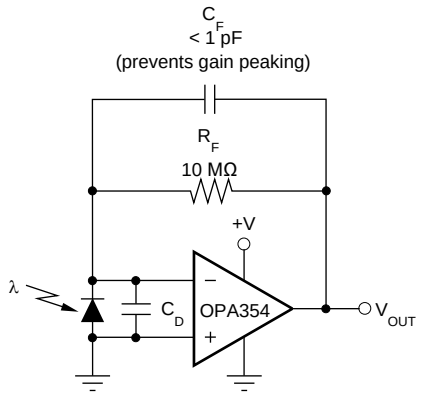


図 36. Transimpedance Amplifier

To achieve a maximally flat, second-order, Butterworth frequency response, the feedback pole must be set as shown in 式 1:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by 式 2:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200-MHz GBW) or the OPA655 (400-MHz GBW) may be used.

8.4 Device Functional Modes

The OPAx354 family of devices is powered on when the supply is connected. The devices can operate as single-supply operational amplifiers or dual-supply amplifiers depending on the application. The devices are used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (example: V– set to –3.5 V and V+ set to 1.5 V).

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx354 family of devices is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The OPAx354 family of devices is available as a single, dual, or quad op amp. The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but it is unity-gain stable and operates as a 1-V/V voltage follower.

9.2 Typical Application

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 family of devices an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency. The key elements to a transimpedance design, as shown in 図 37, are the expected diode capacitance, (which include the parasitic input common-mode and differential-mode input capacitance) the desired transimpedance gain, and the gain-bandwidth (GBW) for the OPAx354 family of devices (20 MHz). With these three variables set, the feedback capacitor value is set to control the frequency response. Feedback capacitance includes the stray capacitance , which is 0.2 pF for a typical surface-mount resistor.

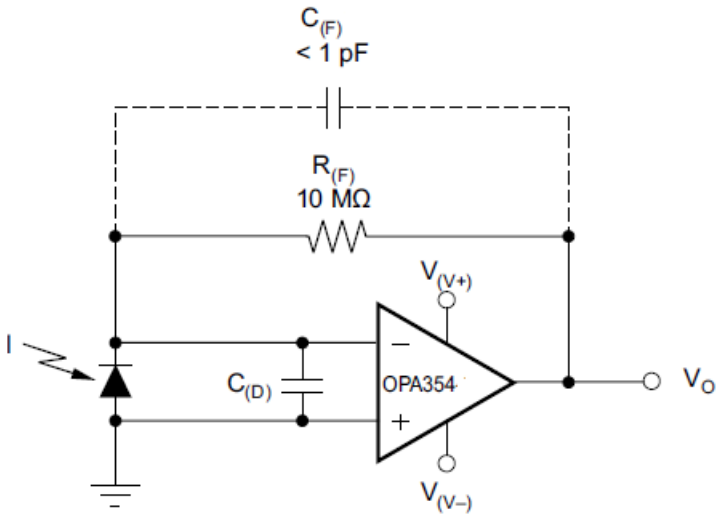


図 37. Dual-Supply Transimpedance Amplifier

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the input parameters.

表 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage, $V_{(V+)}$	2.5 V
Supply voltage, $V_{(V-)}$	–2.5 V

$C_{(F)}$ is optional to prevent gain peaking. $C_{(F)}$ includes the stray capacitance of $R_{(F)}$.

9.2.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole using 式 3.

$$\frac{1}{2 \times \pi \times R_{(F)} \times C_{(F)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (3)$$

Calculate the bandwidth using 式 4.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (4)$$

9.2.2.1 Optimizing the Transimpedance Circuit

To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select $R_{(F)}$ to create the total required gain. Using a lower value for $R_{(F)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(F)}$ increases with the square-root of $R_{(F)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.

2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only the required bandwidth. Use a capacitor across the $R_{(F)}$ to limit bandwidth, even if a capacitor not required for stability.

4. Circuit board leakage degrades the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage helps control leakage.

9.2.3 Application Curve

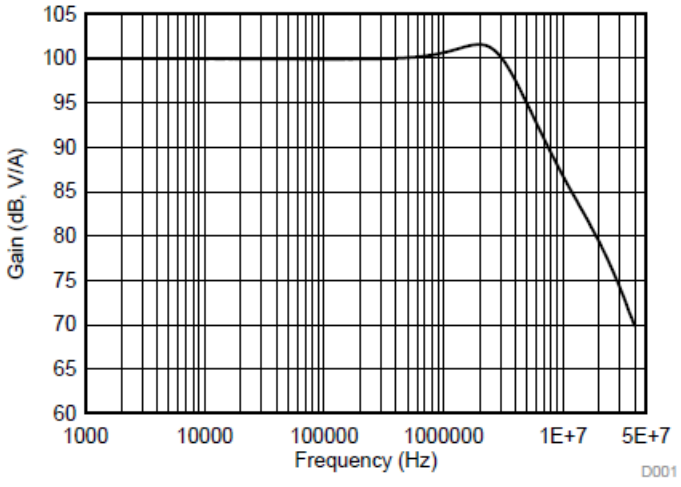


図 38. AC Transfer Function

10 Power Supply Recommendations

The OPAx354 family of devices is specified for operation from 2.5 V to 5.5 V (±1.25 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that exhibit significant variance with regard to operating voltage or temperature are shown *Typical Characteristics*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section..

11 Layout

11.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be employed for the OPAx354. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin ensure clean, stable operation. Large areas of copper provides a means of dissipating heat that is generated in normal operation.

TI does not recommend using sockets with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel is beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving low harmonic and intermodulation distortion.

11.2 Layout Example

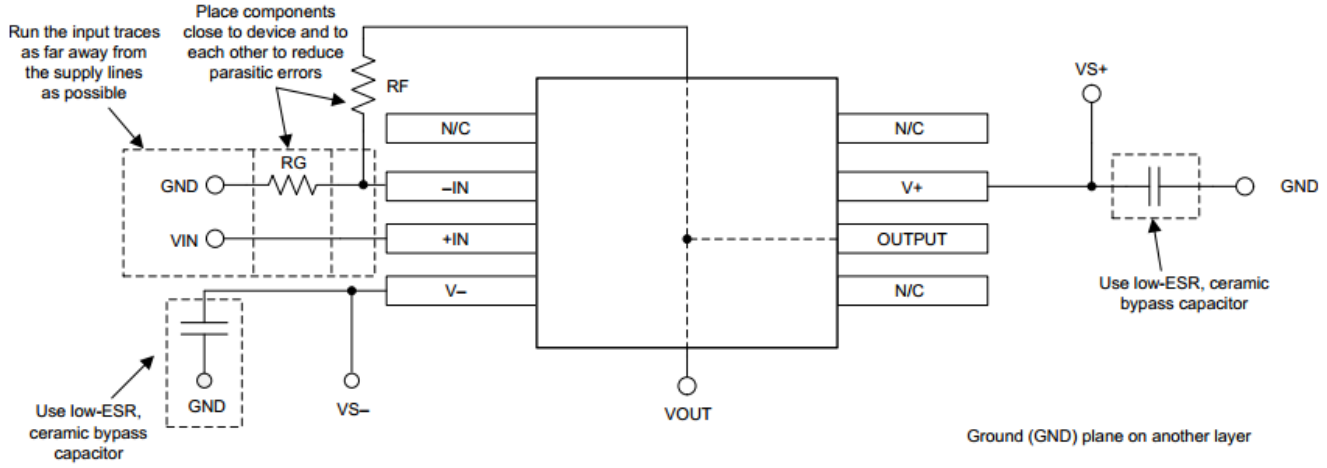


図 39. Operational Amplifier Board Layout for Noninverting Configuration

11.3 Power Dissipation

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S - V_O$. Power dissipation is minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. AB-039 *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads See www.ti.com for more details.

Power Dissipation (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 150°C (maximum.) To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

11.4 PowerPAD Thermally-Enhanced Package

In addition to the regular 5-pin SOT-23 and 9-pin VSSOP packages, the single and dual versions of the OPAx354 also come in an 8-pin SOIC PowerPAD package. The 98-pin SO with PowerPAD is a standard size 8-pin SOIC package where the exposed leadframe on the bottom of the package is soldered directly to the PCB to create a low thermal resistance. This direct attachment enhances the OPAx354 power dissipation capability significantly, and eliminates the use of bulky heat sinks and slugs that are traditionally used in thermal packages. This package is easily mounted using standard PCB assembly techniques.

注

Because the 8-pin HSOP PowerPAD is pin-compatible with standard 8-pin SOIC packages, the OPA354 and OPA2354 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. This configuration provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the device, as shown in 図 40. This exposed die provides an extremely low thermal resistance ($R_{\theta JC}$) path between the die and the exterior of the package. The thermal pad on the bottom of the device can then be soldered directly to the PCB, using the PCB as a heat sink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

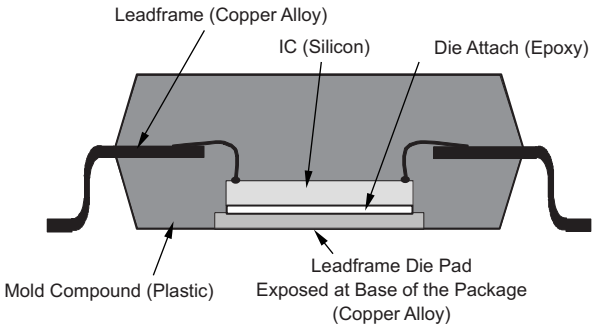


図 40. Section View of a PowerPAD Package

11.5 PowerPAD Assembly Process

The PowerPAD must be connected to the most negative supply voltage for the device, which is ground in single-supply applications and V− in split-supply applications.

Prepare the PCB with a top-side etch pattern, as shown in 図 41. The exact land design may vary based on the specific assembly process requirements. There must be etch for the leads and etch for the thermal land.

Place the recommended number of plated-through holes (or thermal vias) in the area of the thermal pad. These holes must be 13 mils (.013 in) in diameter. The holes are small so that solder wicking through the holes is not a problem during reflow. TI recommends a minimum of five holes for the 8-pin HSOP PowerPAD package, as shown in 図 41.

PowerPAD Assembly Process (continued)

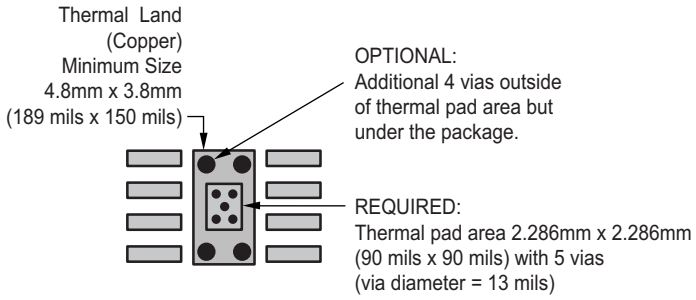


図 41. 8-Pin PowerPAD PCB Etch and Via Pattern

TI recommends, but does not require, placing a small number of additional holes under the package and outside the thermal pad area. These holes provide additional heat paths between the copper thermal land and the ground plane. The holes may be larger because the holes are not in the area to be soldered, so wicking is not a problem. This technique is shown in 図 41.

Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane for single-supply applications, and to V− for split-supply applications.

When laying out these holes, do not use the typical web or spoke via connection methodology, as shown in 図 42. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This feature makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package must make connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

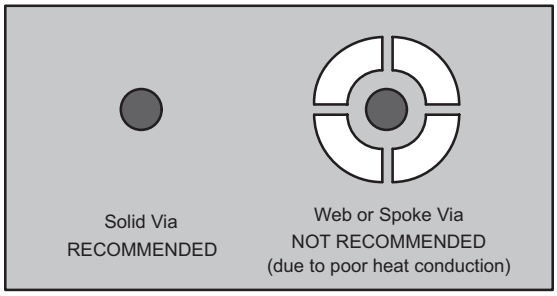


図 42. Via Connection

The top-side solder mask must leave the pad connections and the thermal pad area exposed. The thermal pad area must leave the 13-mil holes exposed. The larger holes outside the thermal pad area may be covered with a solder mask.

Apply solder paste to the exposed thermal pad area and all of the package pins.

With these preparatory steps in place, the PowerPAD device is placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation and processing results in a part that is properly installed.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see *PowerPAD Thermally Enhanced Package* on www.ti.com.

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『ADS8326 16ビット、高速、2.7V～5.5V microPowerサンプリングのアナログ/デジタル・コンバータ』*
- テキサス・インスツルメンツ、*『回路基板のレイアウト技法』*
- テキサス・インスツルメンツ、*『トランスインピーダンス・アンプの直感的な補償』*
- テキサス・インスツルメンツ、*『FilterPro™ユーザー・ガイド』*
- テキサス・インスツルメンツ、*『高速オペアンプのノイズ解析』*
- テキサス・インスツルメンツ、*『OPA380およびOPA2380 高精度、高速トランスインピーダンス・アンプ』*
- テキサス・インスツルメンツ、*『OPA355、OPA2355、OPA3355 シャットダウン機能付き200MHz、CMOSオペアンプ』*
- テキサス・インスツルメンツ、*『OPA656 広帯域、ユニティ・ゲイン安定、FET入力オペアンプ』*
- テキサス・インスツルメンツ、*『パワー・アンプのストレスと電力処理の制限』*
- テキサス・インスツルメンツ、*『放熱特性に優れたPowerPADパッケージ』*

12.2 関連リンク

表 2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA354	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2354	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4354	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** **エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.5 商標

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2354AIDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAG3	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDDARG3	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A
OPA2354AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKTG4	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA2354AIDGKTG4.B	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI
OPA354AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI
OPA354AIDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA354AIDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDA.B	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAG3	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA354AIDDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A
OPA4354AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDRG4	Last Time Buy	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIDRG4.B	Last Time Buy	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A
OPA4354AIPWR	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWR.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWR.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWRG4	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A
OPA4354AIPWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA4354 :

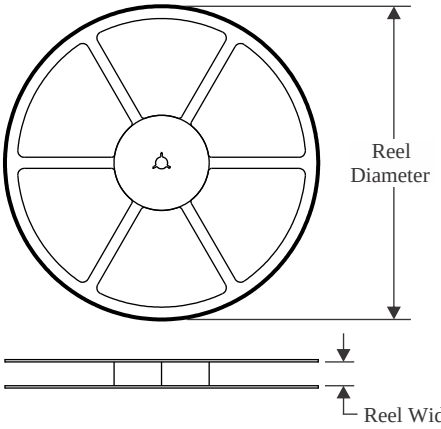
- Automotive : OPA4354-Q1

NOTE: Qualified Version Definitions:

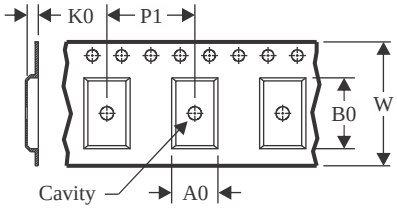
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

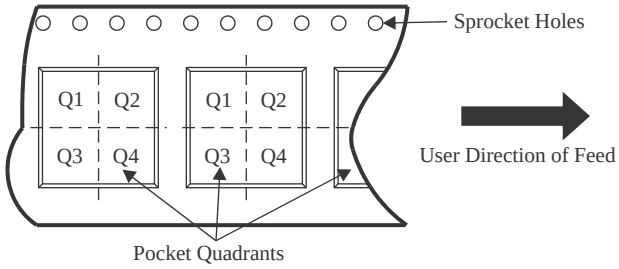


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

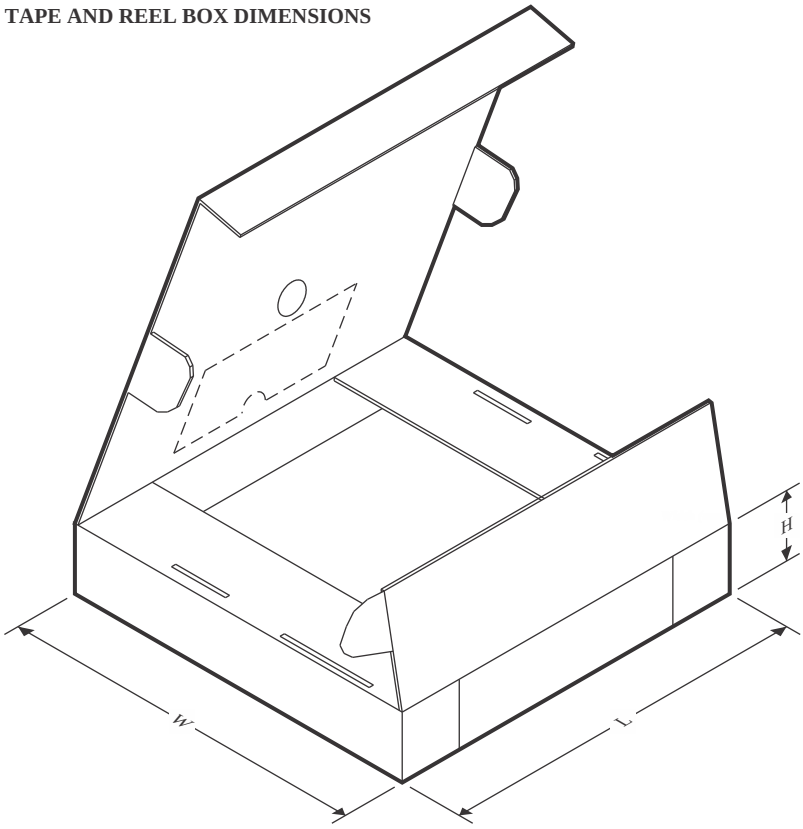
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2354AIDDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2354AIDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA354AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA354AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA354AIDDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4354AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4354AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4354AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4354AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

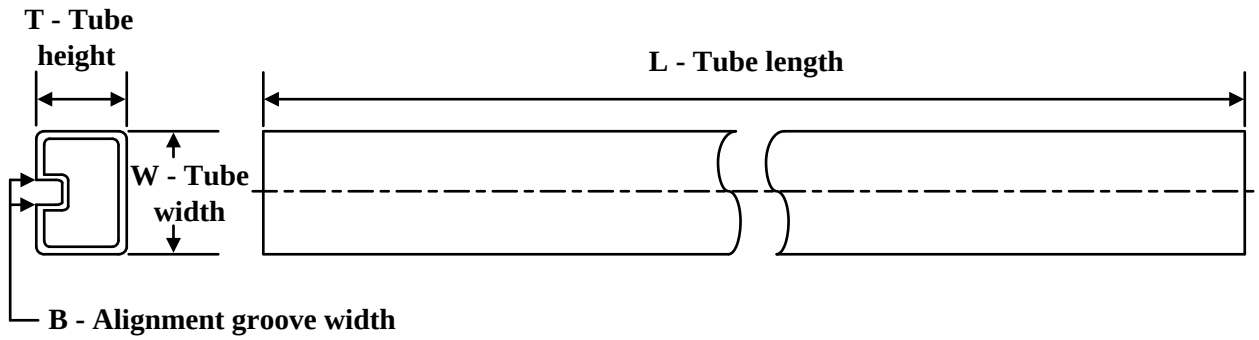
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

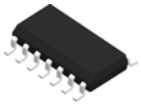
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2354AIDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2354AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2354AIDGKTG4	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA354AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA354AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA354AIDDAR	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
OPA4354AIDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4354AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
OPA4354AIPWR	TSSOP	PW	14	2500	353.0	353.0	32.0
OPA4354AIPWT	TSSOP	PW	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2354AIDDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA2354AIDDA.B	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA2354AIDDAG3	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA354AIDDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA354AIDDA.B	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA354AIDDAG3	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA4354AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4354AID.B	D	SOIC	14	50	506.6	8	3940	4.32

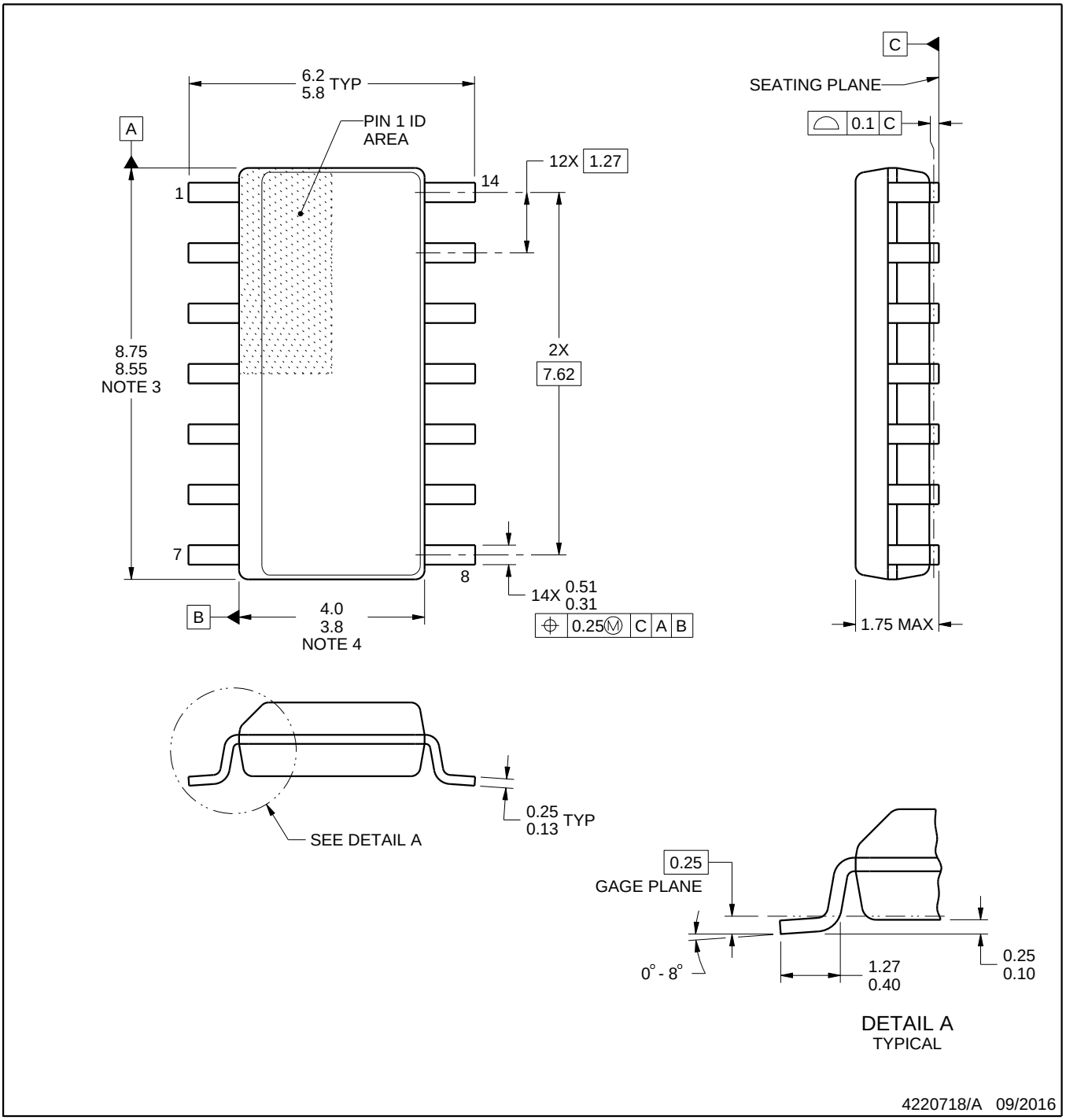


PACKAGE OUTLINE

D0014A

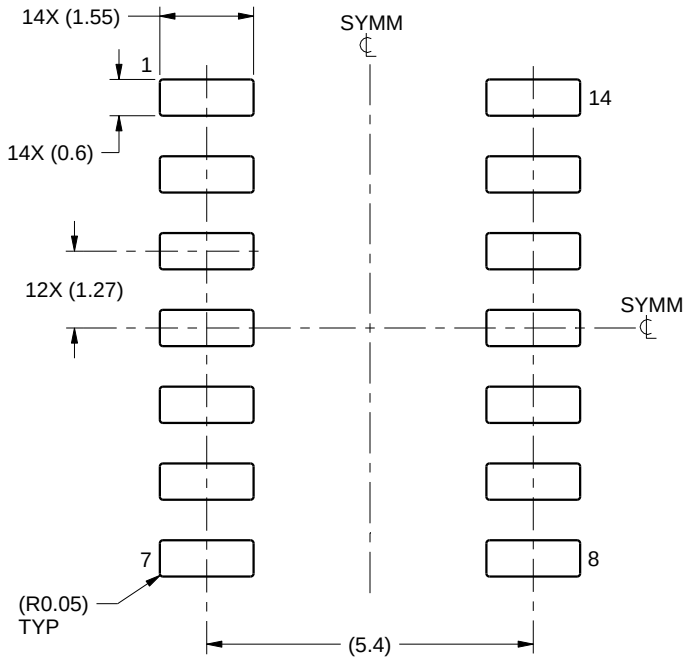
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

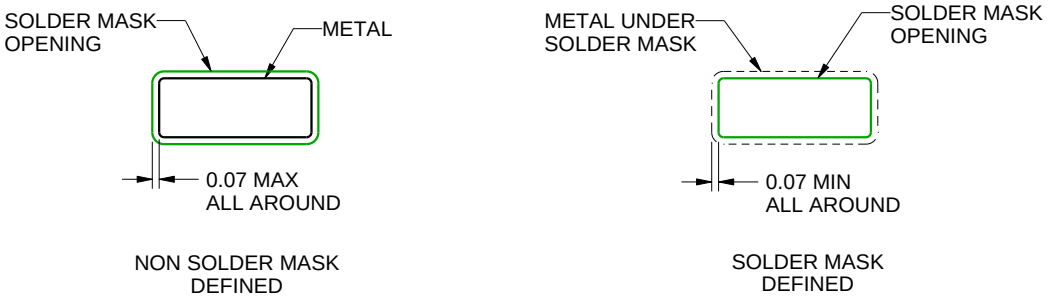


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

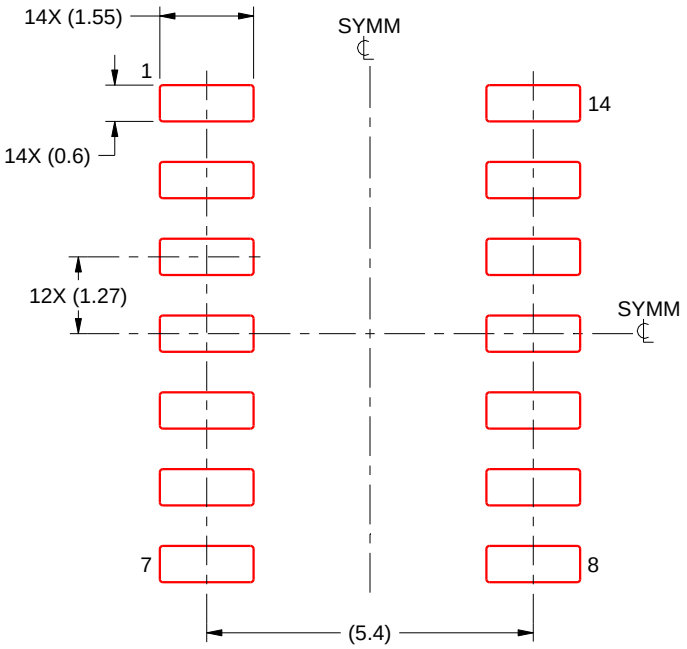
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

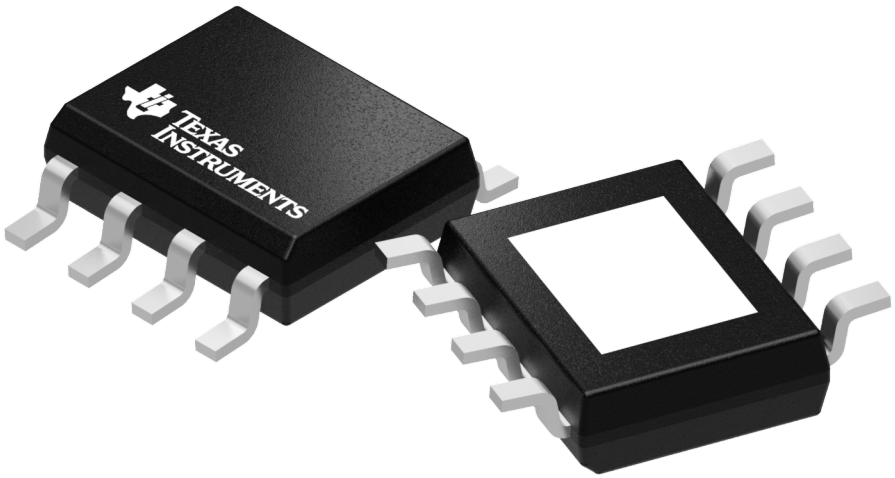
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



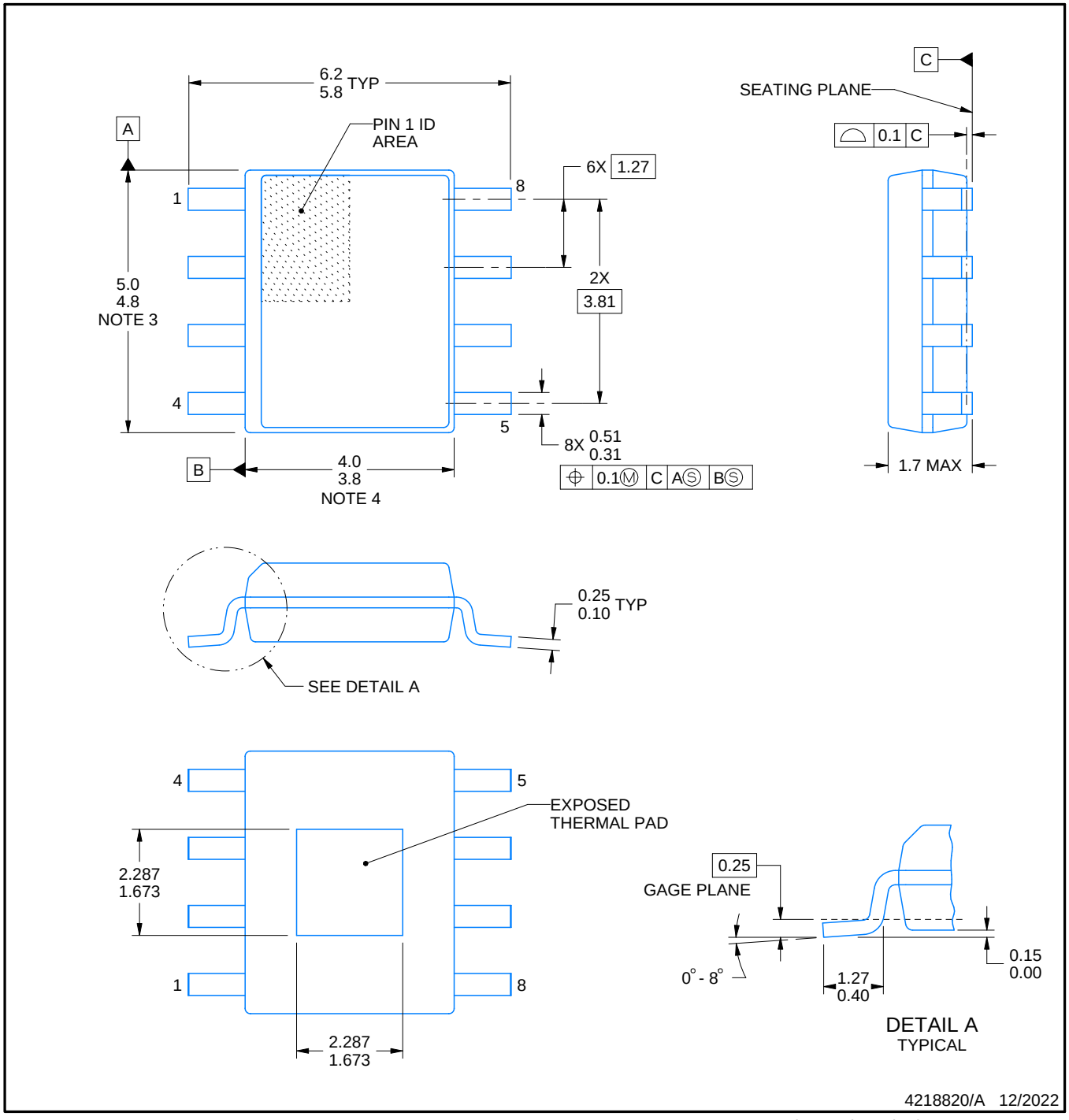
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008D

PowerPAD™ SOIC - 1.7 mm max height

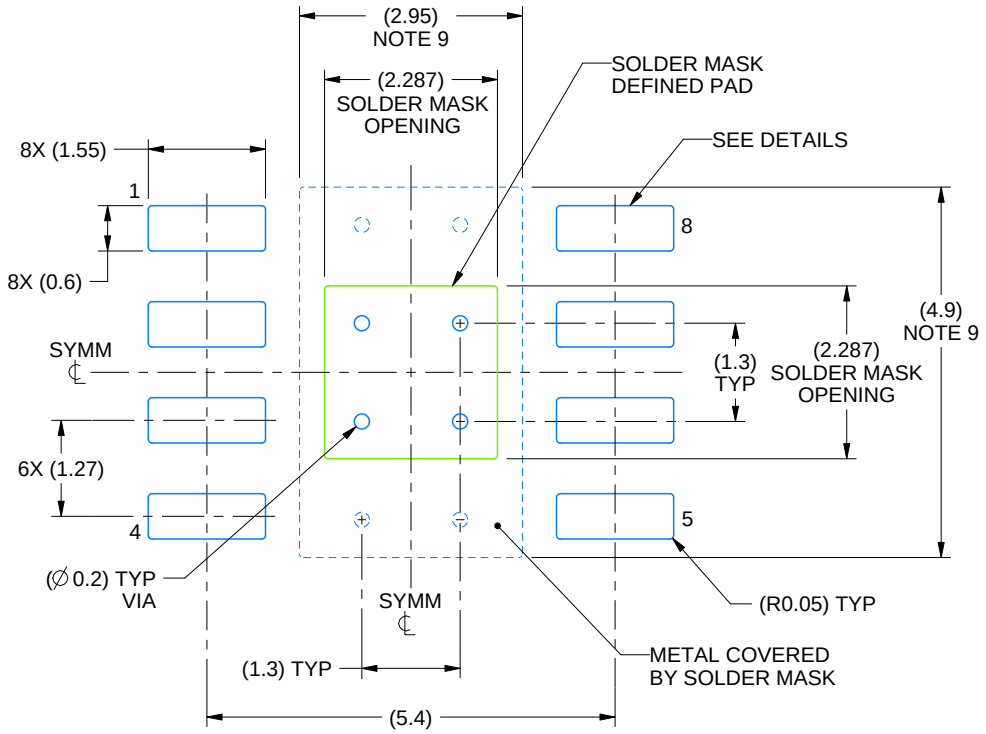
PLASTIC SMALL OUTLINE



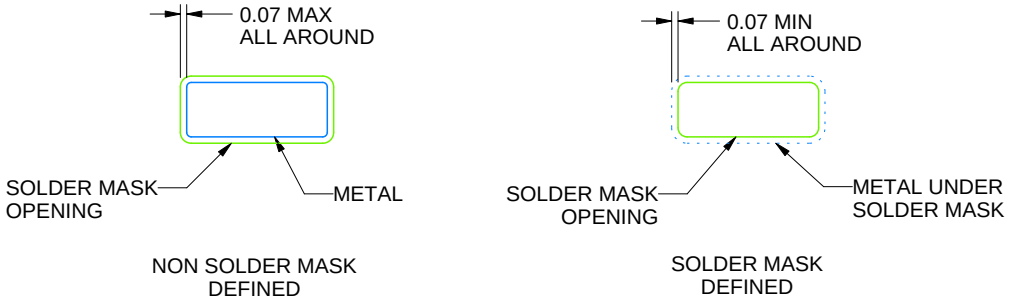
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

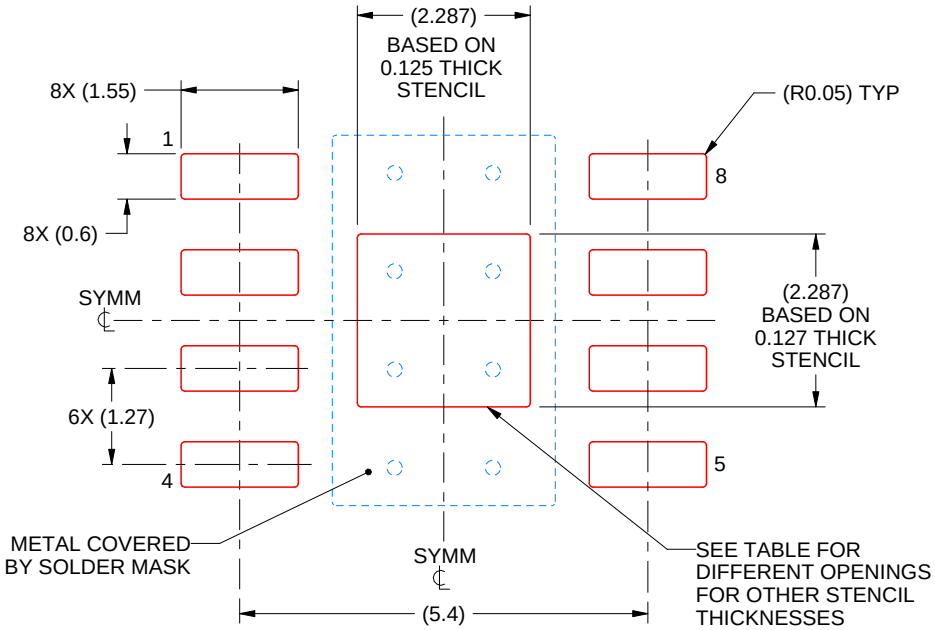


SOLDER MASK DETAILS

4218820/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.557 X 2.557
0.125	2.287 X 2.287 (SHOWN)
0.150	2.088 X 2.088
0.175	1.933 X 1.933

4218820/A 12/2022

NOTES: (continued)

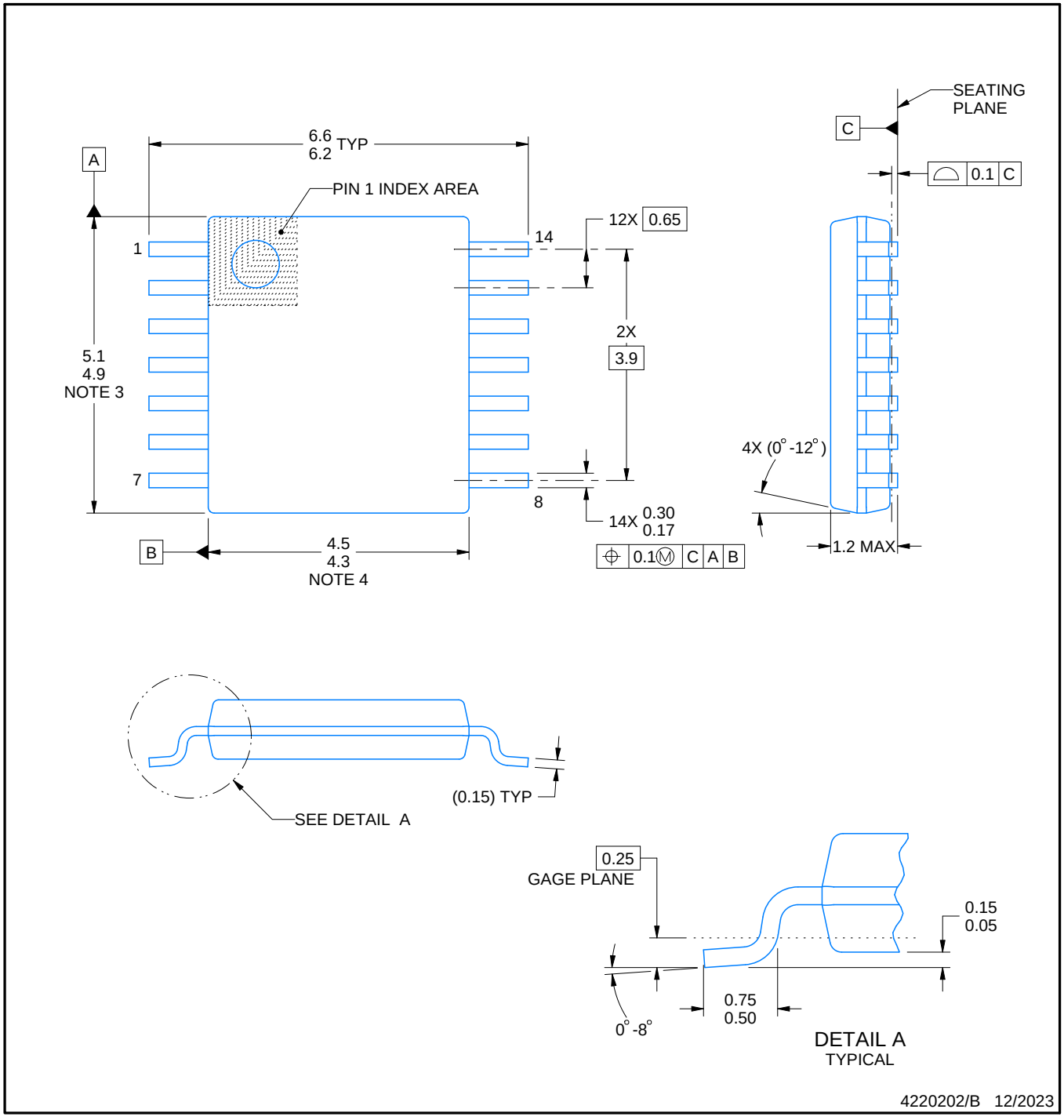
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

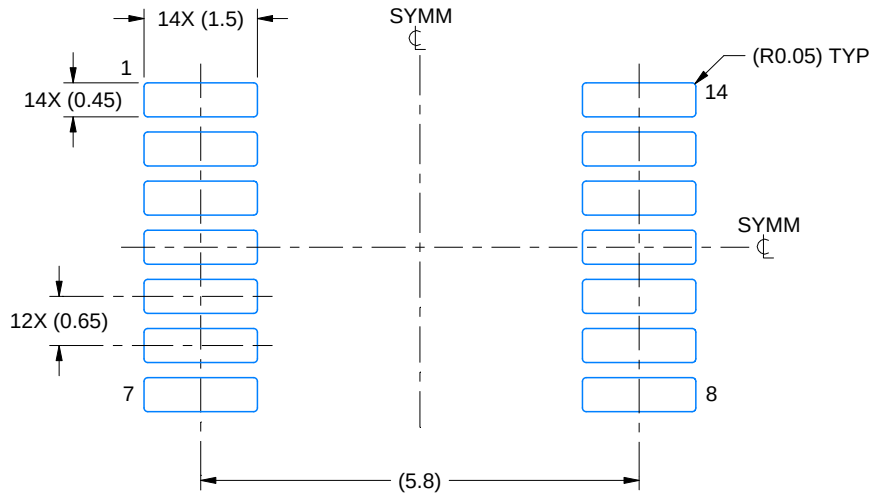
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

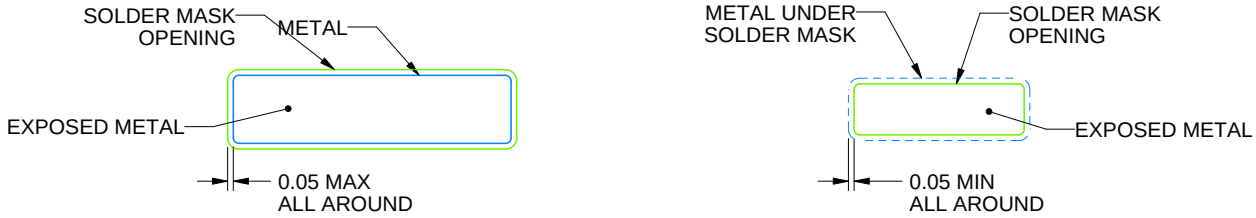


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

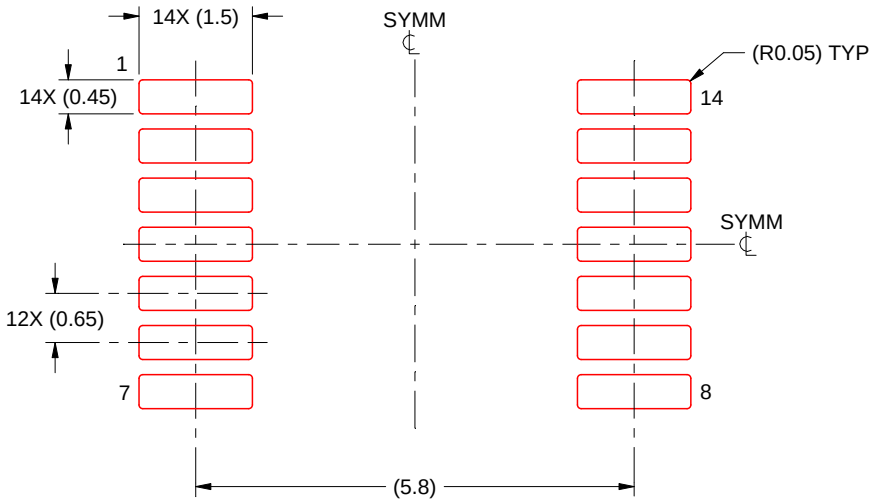


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

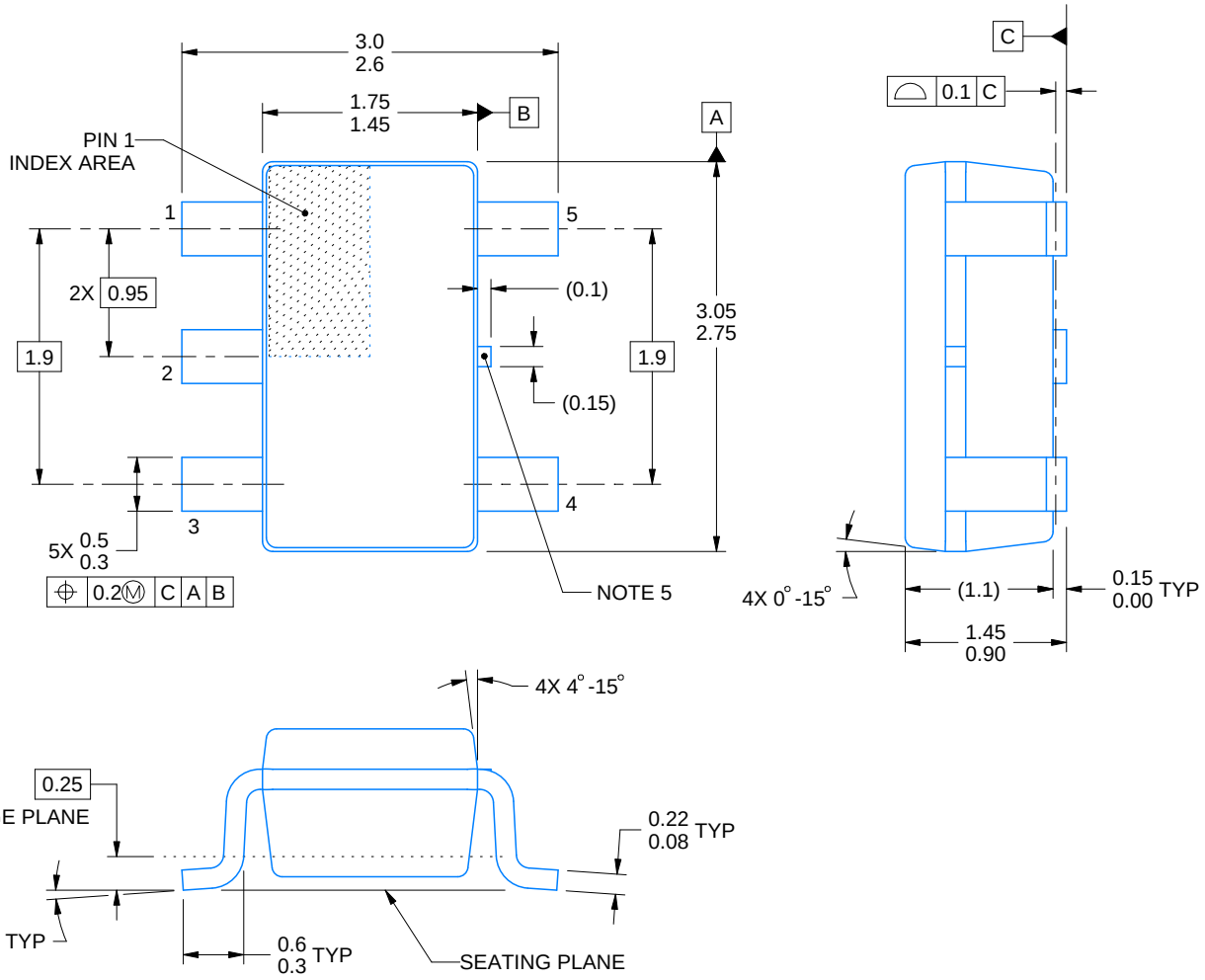
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

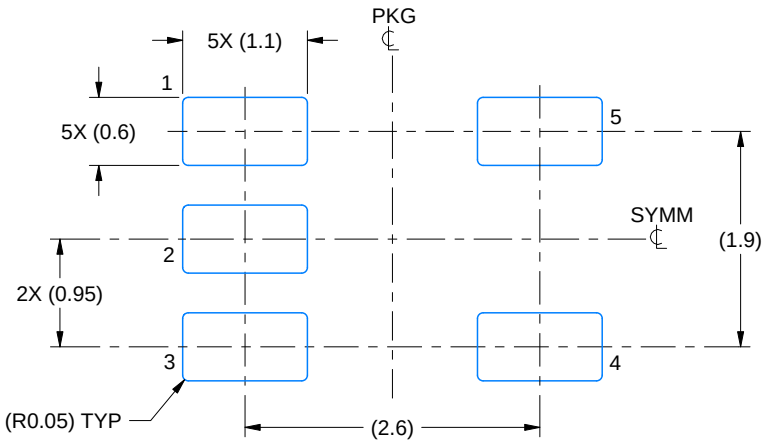
SMALL OUTLINE TRANSISTOR



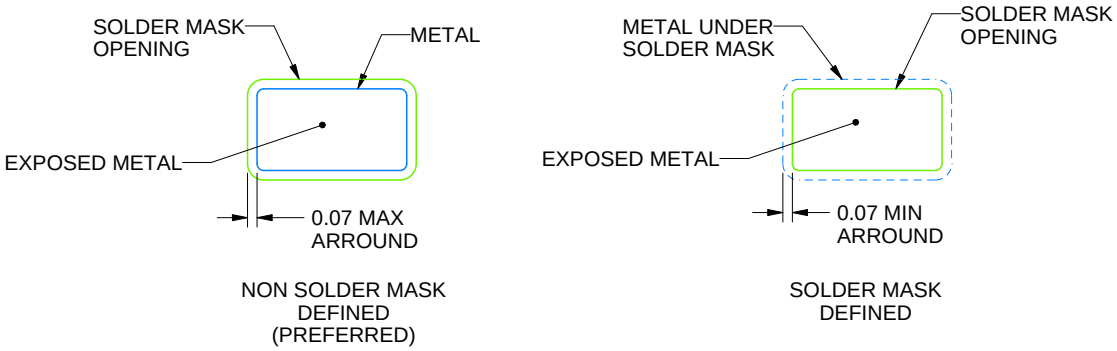
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

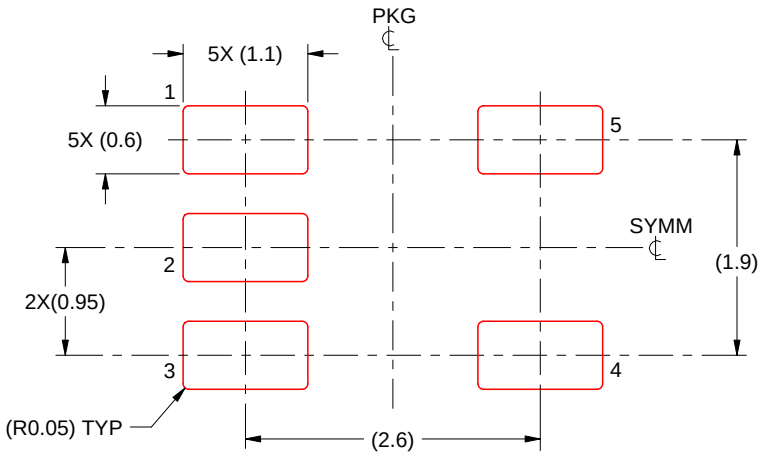


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

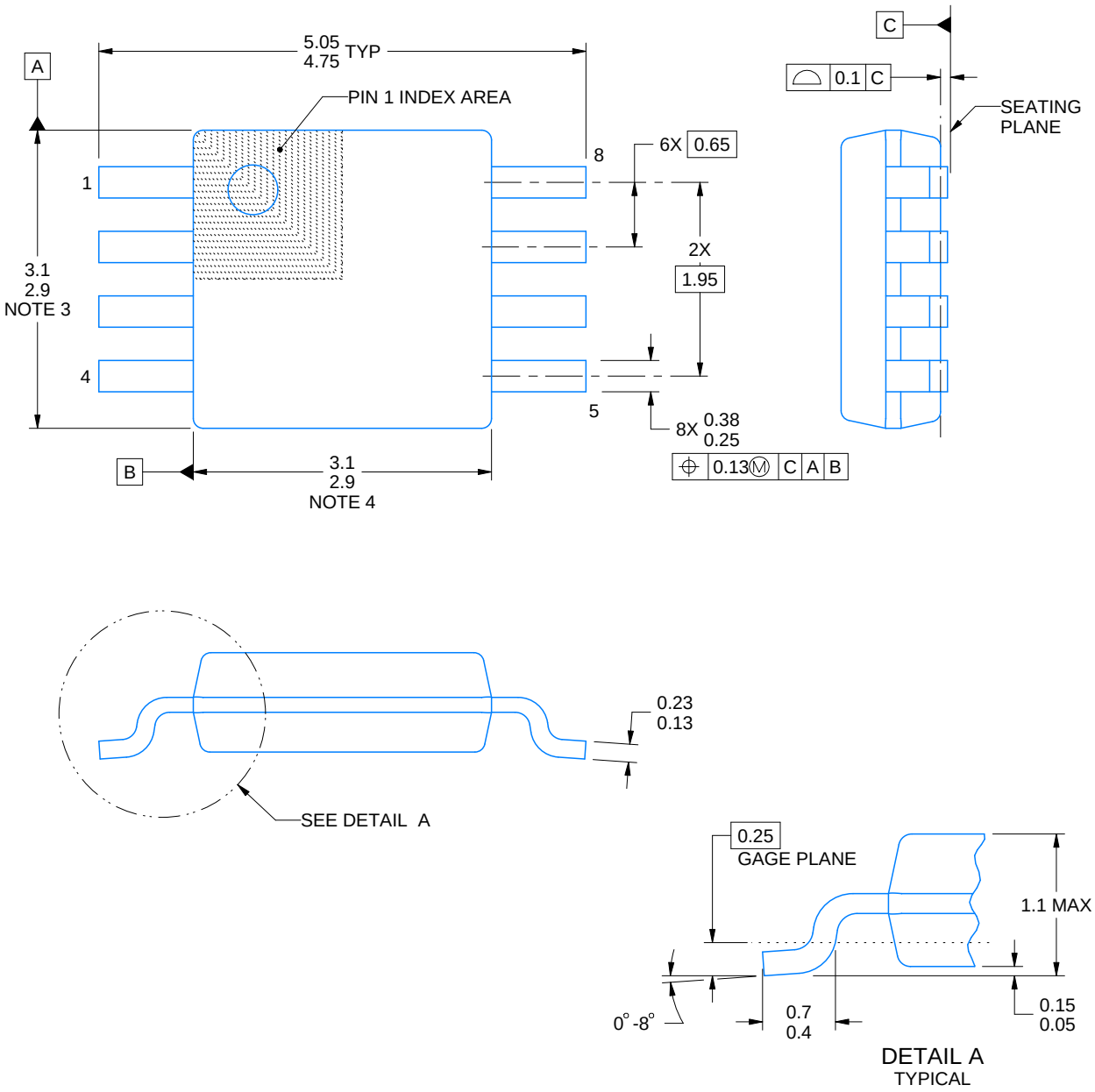
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

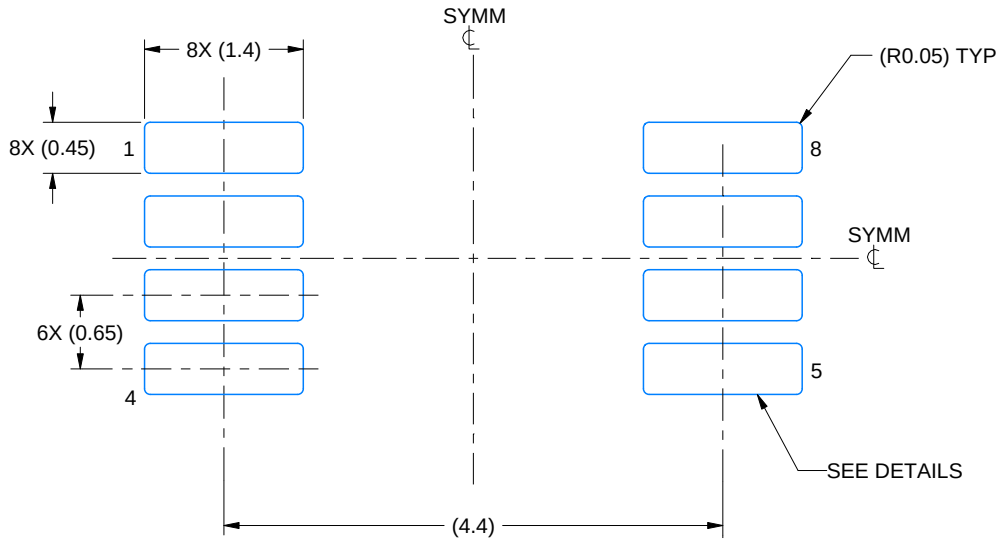
SMALL OUTLINE PACKAGE



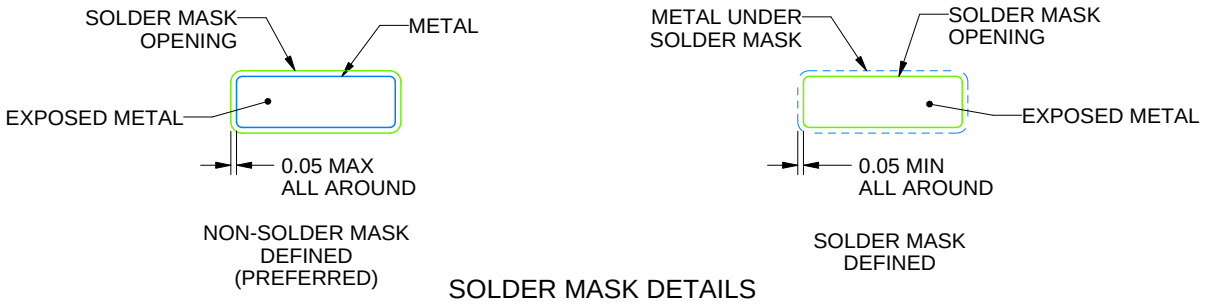
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

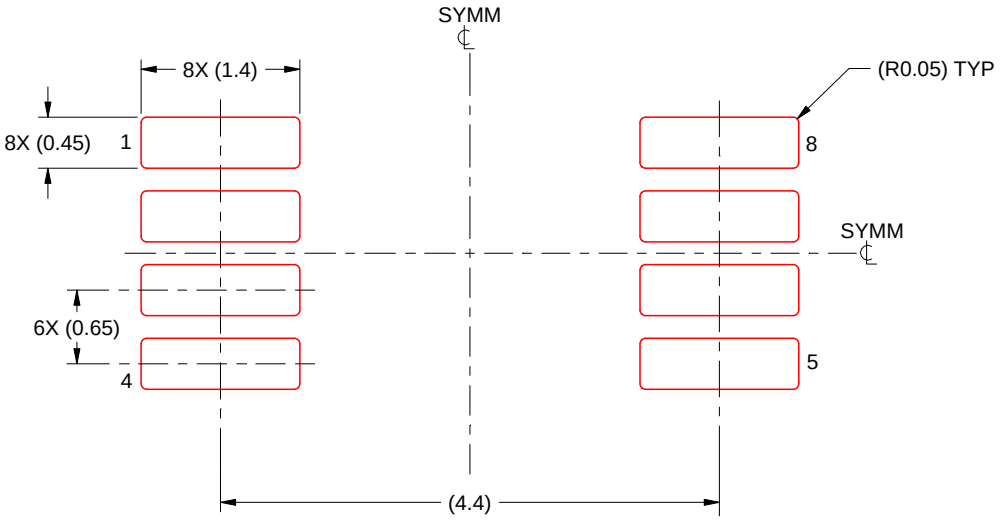


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月