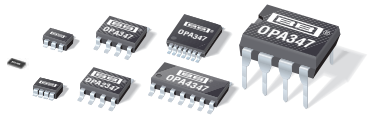
OPA347
OPA2347
OPA4347



SBOS167D – NOVEMBER 2000– REVISED JULY 2007

*micro*Power, Rail-to-Rail Operational Amplifiers

FEATURES

- **LOW I_Q: 20μA**
- ***micro*SIZE PACKAGES: WCSP-8, SC70-5 SOT23-5, SOT23-8, and TSSOP-14**
- **HIGH SPEED/POWER RATIO WITH BANDWIDTH: 350kHz**
- **RAIL-TO-RAIL INPUT AND OUTPUT**
- **SINGLE SUPPLY: 2.3V to 5.5V**

APPLICATIONS

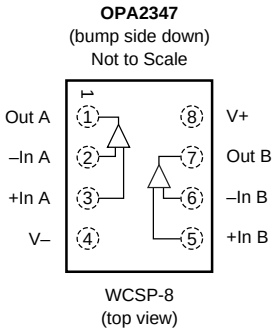
- **PORTABLE EQUIPMENT**
- **BATTERY-POWERED EQUIPMENT**
- **2-WIRE TRANSMITTERS**
- **SMOKE DETECTORS**
- **CO DETECTORS**

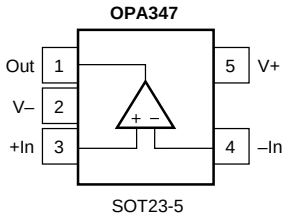
DESCRIPTION

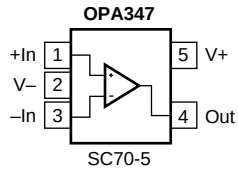
The OPA347 is a *micro*Power, low-cost operational amplifier available in *micro*packages. The OPA347 (single version) is available in the SC-70 and SOT23-5 packages. The OPA2347 (dual version) is available in the SOT23-8 and WCSP-8 packages. Both are also available in the SO-8. The OPA347 is also available in the DIP-8. The OPA4347 (quad) is available in the SO-14 and the TSSOP-14.

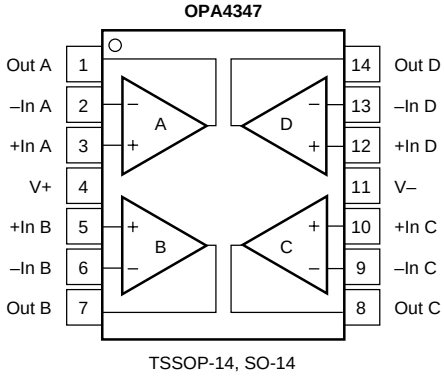
The small size and low power consumption (34μA per channel maximum) of the OPA347 make it ideal for portable and battery-powered applications. The input range of the OPA347 extends 200mV beyond the rails, and the output range is within 5mV of the rails. The OPA347 also features an excellent speed/power ratio with a bandwidth of 350kHz.

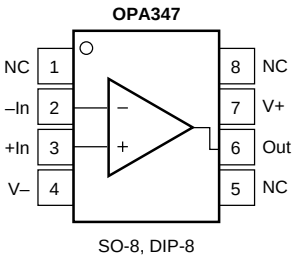
The OPA347 can be operated with a single or dual power supply from 2.3V to 5.5V. All models are specified for operation from –55°C to +125°C.

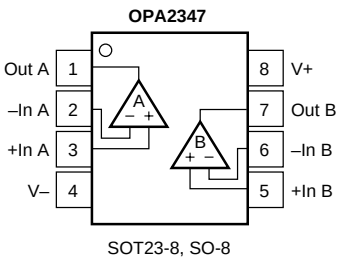












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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	7.5V
Signal Input Terminals, Voltage[2]	(V–) – 0.5V to (V+) + 0.5V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–65°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE/LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA347NA	SOT23-5	DBV	A47
"	"	"	"
OPA347PA	DIP-8	P	OPA347PA
OPA347UA	SO-8	D	OPA347UA
"	"	"	"
OPA347SA	SC-70	DCK	S47
"	"	"	"
OPA2347EA	SOT23-8	DCN	B47
"	"	"	"
OPA2347UA	SO-8	D	OPA2347UA
"	"	"	"
OPA2347YED	WCSP-8	YED	YMD CCS
"	"	"	"
OPA2347YZDR	Lead-Free WCSP-8	YZD	A9
OPA4347EA	TSSOP-14	PW	OPA4347EA
"	"	"	"
OPA4347UA	SO-14	D	OPA4347UA
"	"	"	"

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS: V_S = 2.5V to 5.5V

Boldface limits apply over the specified temperature range, **T_A = –55°C to +125°C.**

At T_A = +25°C, R_L = 100kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

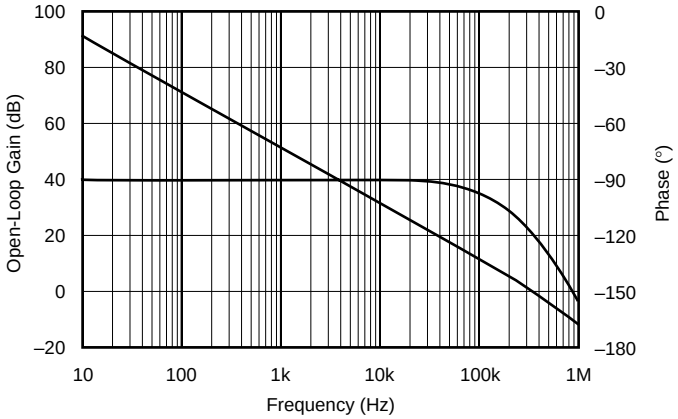
PARAMETER		CONDITION	OPA347NA, UA, PA, SA OPA2347EA, UA, YED OPA4347EA, UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5.5V, V_{CM} = (V–) + 0.8V		2	6	mV
over Temperature				**2**	**7**	**mV**
Drift	**dV_{OS}/dT**			**3**		**µV/°C**
vs Power Supply	PSRR	V_S = 2.5V to 5.5V, V_{CM} < (V+) – 1.7V		60	175	µV/V
over Temperature		**V_S = 2.5V to 5.5V, V_{CM} < (V+) – 1.7V**			**300**	**µV/V**
Channel Separation, DC				0.3		µV/V
		f = 1kHz		128		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.2		(V+) + 0.2	V
Common-Mode Rejection Ratio	CMRR	V_S = 5.5V, (V–) – 0.2V < V_{CM} < (V+) – 1.7V	70	80		dB
over Temperature		**V_S = 5.5V, V– < V_{CM} < (V+) – 1.7V**	**66**			**dB**
		Vs = 5.5V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V	54	70		dB
over Temperature		**Vs = 5.5V, V– < V_{CM} < V+**	**48**			**dB**
INPUT BIAS CURRENT(1)						
Input Bias Current	I_b			±0.5	±10	pA
Input Offset Current	I_{OS}			±0.5	±10	pA
INPUT IMPEDANCE						
Differential				10^{13} || 3		Ω || pF
Common-Mode				10^{13} || 6		Ω || pF
NOISE		V_{CM} < (V+) – 1.7V				
Input Voltage Noise, f = 0.1Hz to 10Hz				12		μV_{PP}
Input Voltage Noise Density, f = 1kHz	e_n			60		$nV/\sqrt{Hz}$
Input Current Noise Density, f = 1kHz	i_n			0.7		$fA/\sqrt{Hz}$
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_S = 5.5V, R_L = 100kΩ, 0.015V < V_O < 5.485V	100	115		dB
over Temperature		**V_S = 5.5V, R_L = 100kΩ, 0.015V < V_O < 5.485V**	**88**			**dB**
		V_S = 5.5V, R_L = 5kΩ, 0.125V < V_O < 5.375V	100	115		dB
over Temperature		**V_S = 5.5V, R_L = 5kΩ, 0.125V < V_O < 5.375V**	**88**			**dB**
A_{OL} (SC-70 only)		V_S = 5.5V, R_L = 5kΩ 0.125V < V_O < 5.375V	96	115		dB
OUTPUT						
Voltage Output Swing from Rail		R_L = 100kΩ, A_{OL} > 100dB		5	15	mV
over Temperature		**R_L = 100kΩ, A_{OL} > 88dB**			**15**	**mV**
		R_L = 5kΩ, A_{OL} > 100dB		90	125	mV
over Temperature		**R_L = 5kΩ, A_{OL} > 88dB**			**125**	**mV**
Short-Circuit Current	I_{SC}			±17		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW			350		kHz
Slew Rate	SR	G = +1		0.17		V/µs
Settling Time, 0.1%	t_S	V_S = 5V, 2V Step, G = +1		21		µs
0.01%		V_S = 5V, 2V Step, G = +1		27		µs
Overload Recovery Time		V_{IN} × Gain = V_S		23		µs
POWER SUPPLY						
Specified Voltage Range	V_S		2.5		5.5	V
Minimum Operating Voltage				2.3		V
Minimum Operating Voltage (OPA347SA)				2.4		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		20	34	µA
over Temperature					**38**	**µA**
TEMPERATURE RANGE						
Specified Range			–55		125	°C
Operating Range			–65		150	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
SOT23-5 Surface-Mount				200		°C/W
SOT23-8 Surface-Mount				150		°C/W
SO-8 Surface-Mount				150		°C/W
SO-14 Surface-Mount				100		°C/W
TSSOP-14 Surface-Mount				100		°C/W
DIP-8				100		°C/W
SC70-5 Surface-Mount				250		°C/W
WCSP				250		°C/W

NOTE: (1) Input bias current for the OPA2347YED package is specified in the absence of light. See the Photosensitivity section for further detail.

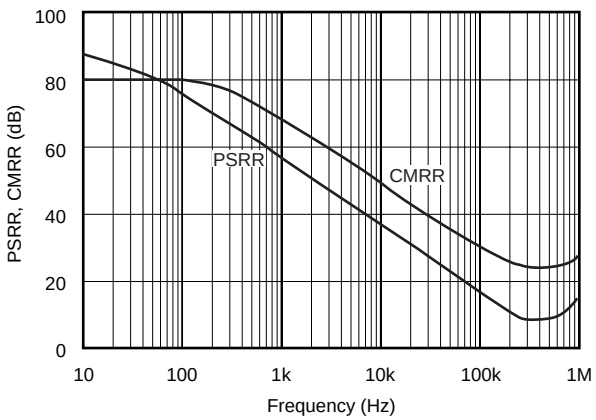
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and R_L = 100kΩ connected to V_S/2, unless otherwise noted.

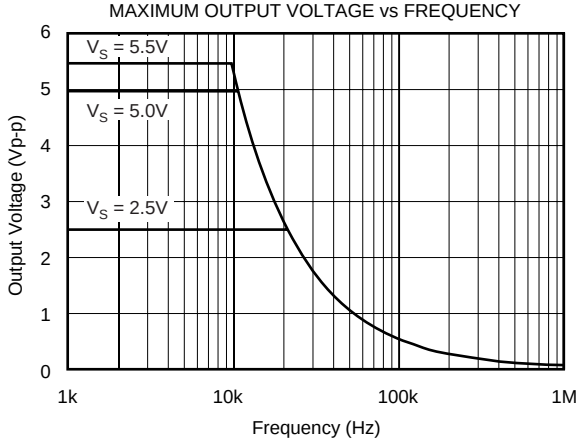
OPEN-LOOP GAIN/PHASE vs FREQUENCY



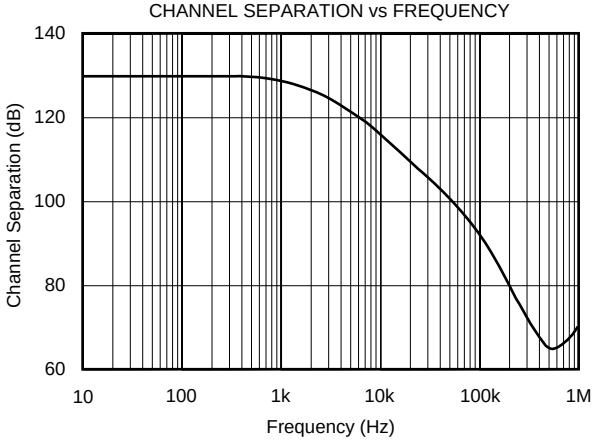
POWER-SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



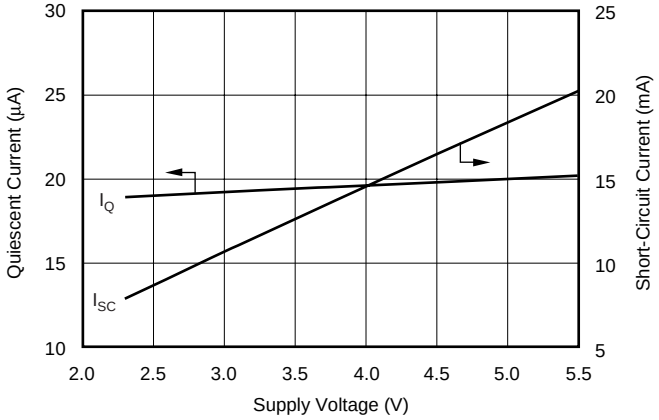
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



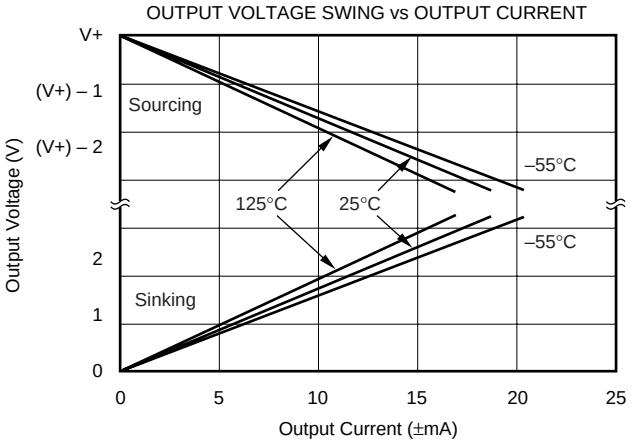
CHANNEL SEPARATION vs FREQUENCY



QUIESCENT AND SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



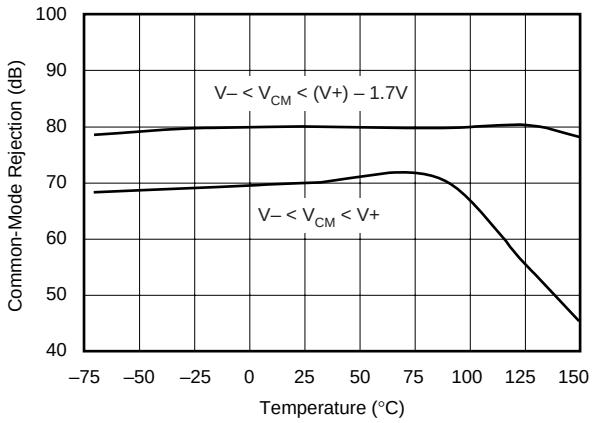
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



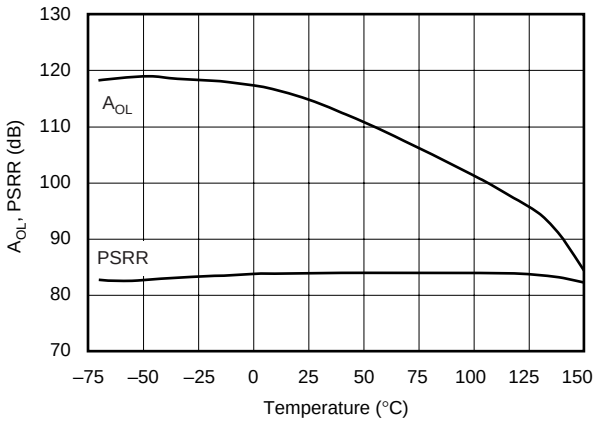
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 100kΩ connected to V_S/2, unless otherwise noted.

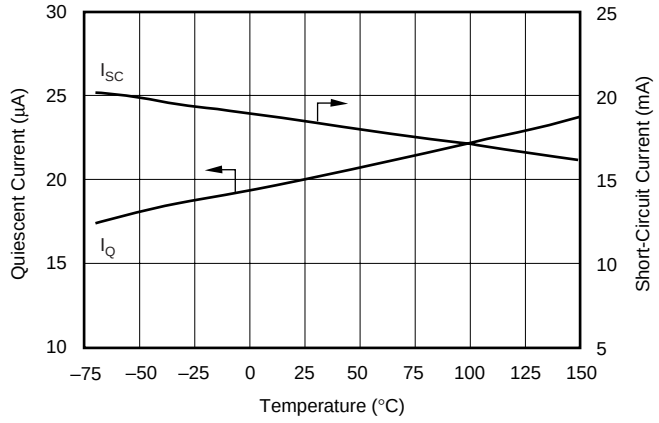
COMMON-MODE REJECTION vs TEMPERATURE



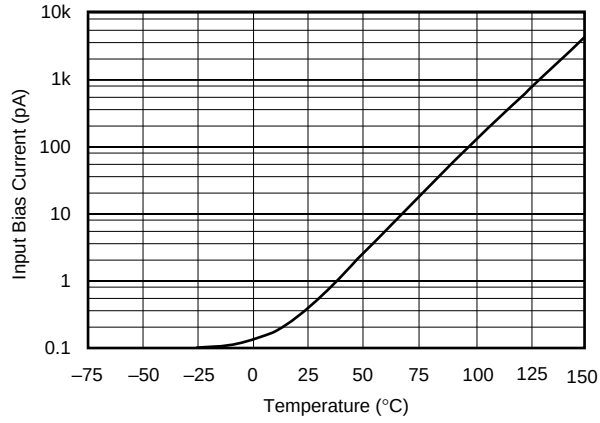
OPEN-LOOP GAIN AND POWER-SUPPLY REJECTION vs TEMPERATURE



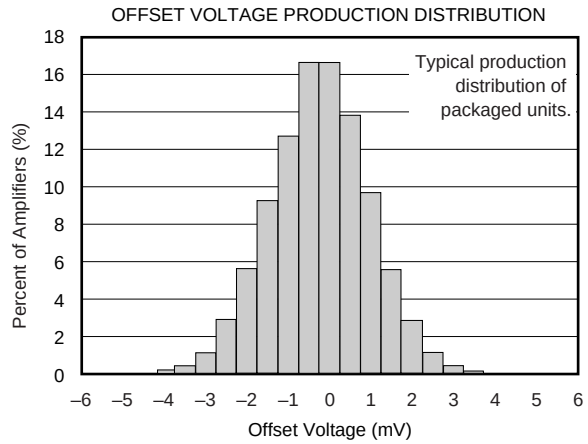
QUIESCENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



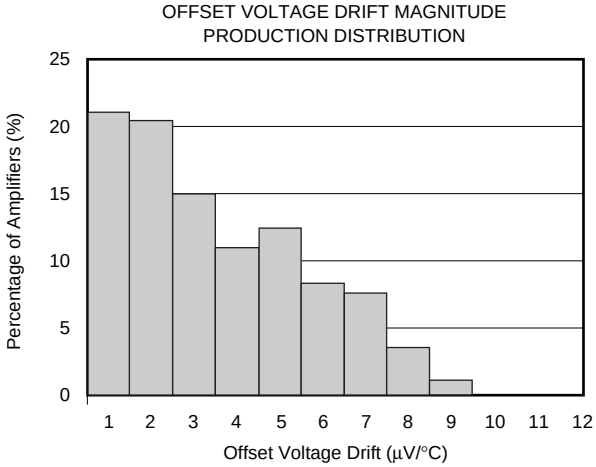
INPUT BIAS CURRENT vs TEMPERATURE



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



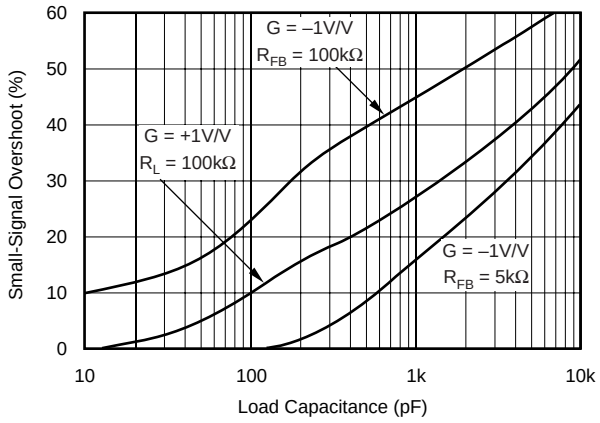
OFFSET VOLTAGE DRIFT MAGNITUDE PRODUCTION DISTRIBUTION



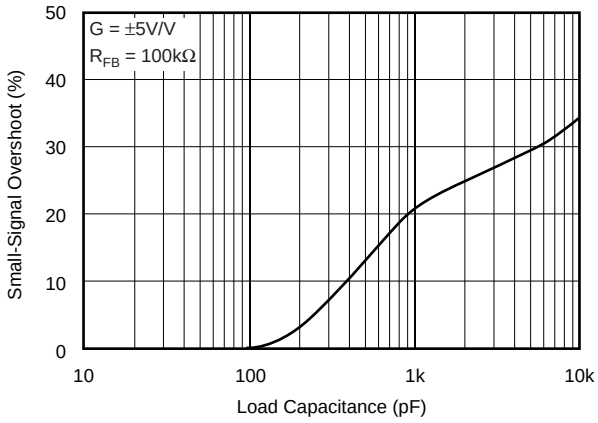
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, and R_L = 100kΩ connected to V_S/2, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

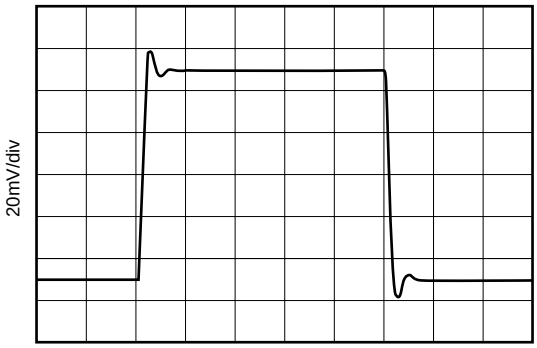


SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



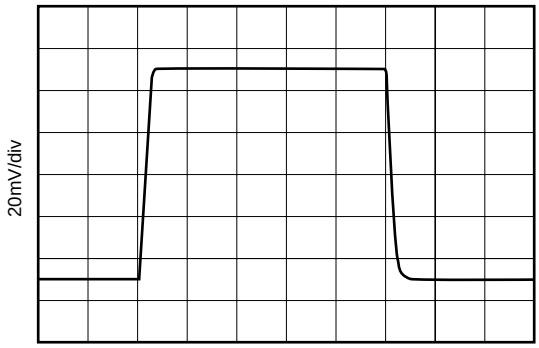
SMALL-SIGNAL STEP RESPONSE

G = +1V/V, R_L = 100kΩ, C_L = 100pF



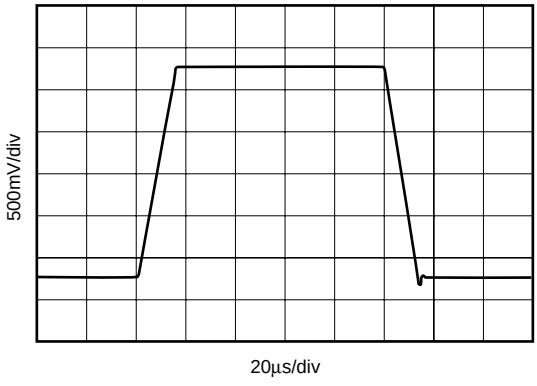
SMALL-SIGNAL STEP RESPONSE

G = +1V/V, R_L = 5kΩ, C_L = 100pF

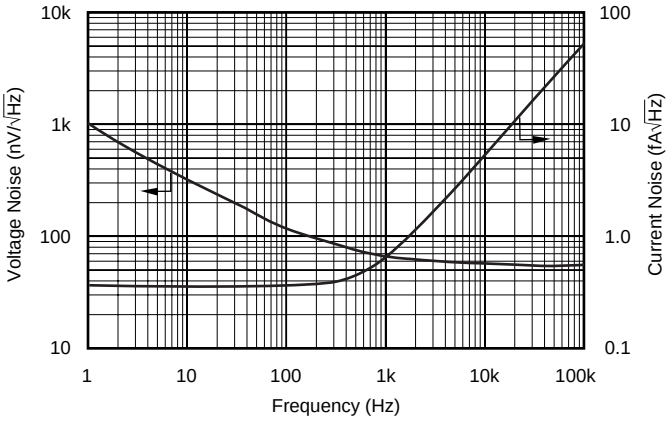


LARGE-SIGNAL STEP RESPONSE

G = +1V/V, R_L = 100kΩ, C_L = 100pF



INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



APPLICATIONS INFORMATION

The OPA347 series op amps are unity-gain stable and can operate on a single supply, making them highly versatile and easy to use.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA347 in unity-gain configuration. Operation is from V_S = +5V with a 100kΩ load connected to $V_S/2$. The input is a $5V_{PP}$ sinusoid. Output voltage is approximately $4.995V_{PP}$.

Power-supply pins should be bypassed with 0.01µF ceramic capacitors.

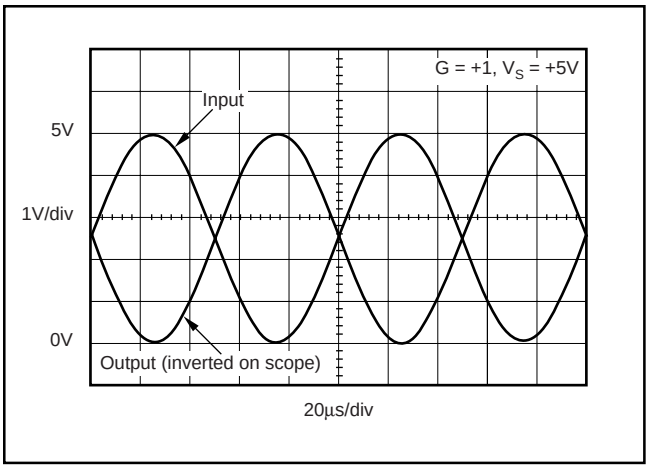


FIGURE 1. Rail-to-Rail Input and Output.

OPERATING VOLTAGE

The OPA347 series op amps are fully specified and ensured from 2.5V to 5.5V. In addition, many specifications apply from –55°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA347 series extends 200mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 2. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3V to 200mV above the positive supply, while the P-channel pair is on for inputs from 200mV below the negative supply to approximately (V+) – 1.3V. There is a small transition region, typically (V+) – 1.5V to (V+) – 1.1V, in which both pairs are on. This 400mV transition region can vary 300mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.65V to (V+) – 1.25V on the low end, up to (V+) – 1.35V to (V+) – 0.95V on the high end. Within the 400mV transition region PSRR, CMRR, offset voltage, and offset drift may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3, *Design Optimization with Rail-to-Rail Input Op Amps*.

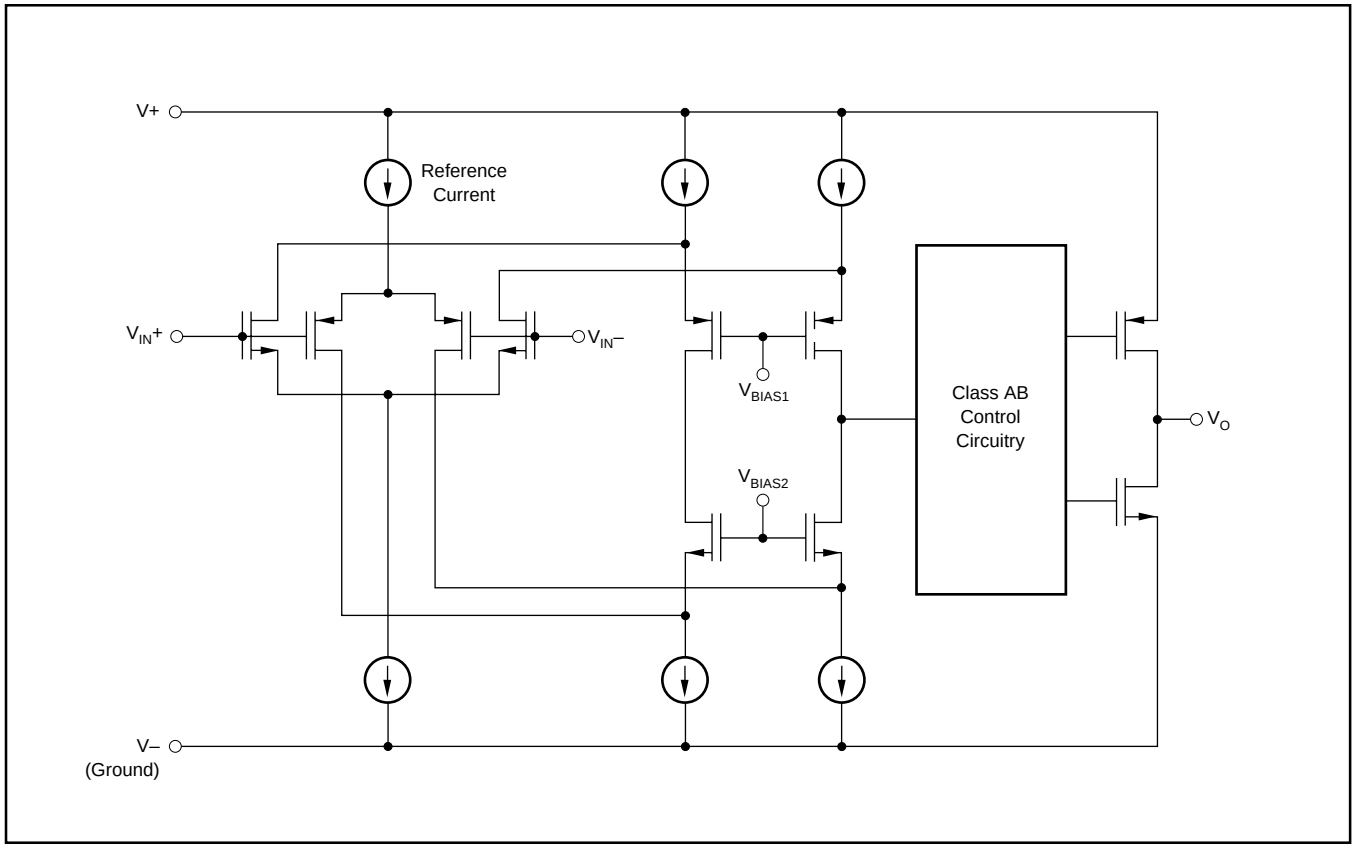


FIGURE 2. Simplified Schematic.

DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

Rail-to-rail op amps can be used in virtually any op amp configuration. To achieve optimum performance, however, applications using these special double-input-stage op amps may benefit from consideration of their special behavior.

In many applications, operation remains within the common-mode range of only one differential input pair. However, some applications exercise the amplifier through the transition region of both differential input stages. A small discontinuity may occur in this transition. Careful selection of the circuit configuration, signal levels, and biasing can often avoid this transition region.

With a unity-gain buffer, for example, signals will traverse this transition at approximately 1.3V below the V+ supply and may exhibit a small discontinuity at this point.

The common-mode voltage of the noninverting amplifier is equal to the input voltage. If the input signal always remains less than the transition voltage, no discontinuity will be created. The closed-loop gain of this configuration can still produce a rail-to-rail output.

Inverting amplifiers have a constant common-mode voltage equal to V_B. If this bias voltage is constant, no discontinuity will be created. The bias voltage can generally be chosen to avoid the transition region.

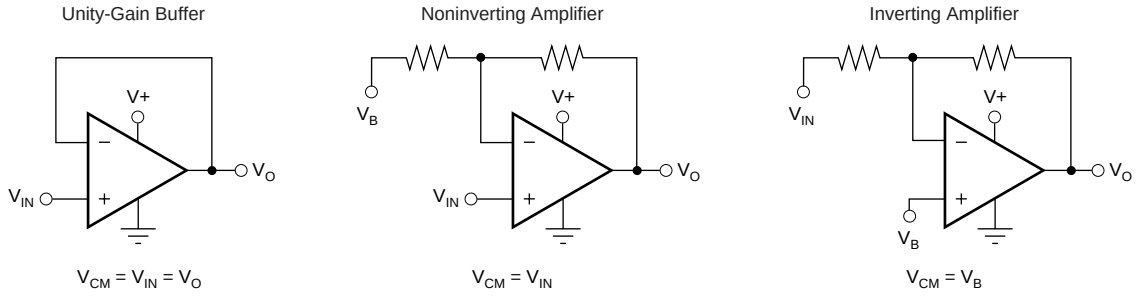


FIGURE 3. Design Optimization with Rail-to-Rail Input Op Amps.

COMMON-MODE REJECTION

The CMRR for the OPA347 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 1.7V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at V_S = 5.5V over the entire common-mode range is specified.

INPUT VOLTAGE

The input common-mode range extends from (V–) – 0.2V to (V+) + 0.2V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, if input current is limited the inputs may go beyond the power supplies without phase inversion, as shown in Figure 4, unlike some other op amps.

Normally, input currents are 0.4pA. However, large inputs (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. This is easily accomplished with an input resistor, as shown in Figure 5.

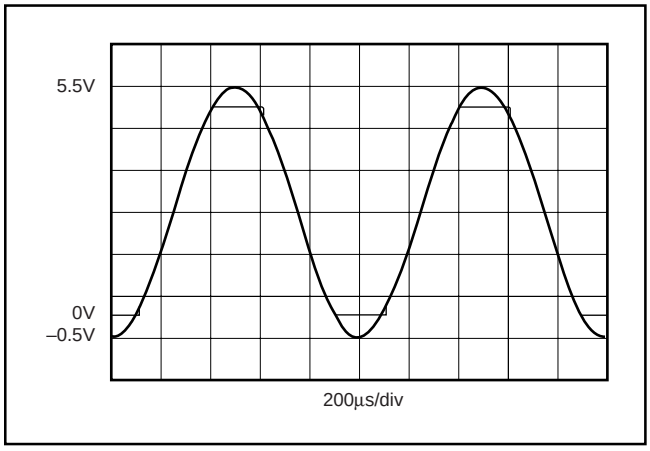


FIGURE 4. OPA347—No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

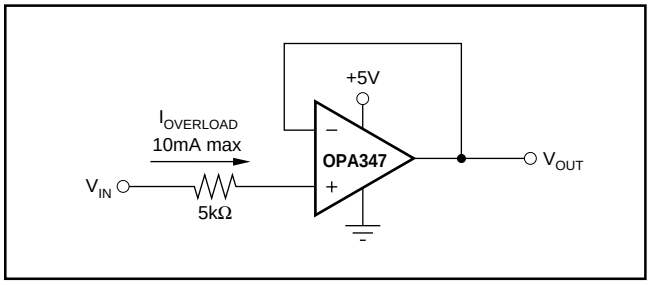


FIGURE 5. Input Current Protection for Voltages Exceeding the Supply Voltage.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 5kΩ loads connected to any potential between V+ and ground. For light resistive loads (> 100kΩ), the output voltage can typically swing to within 5mV from supply rail. With moderate resistive loads (10kΩ to 50kΩ), the output can swing to within a few tens of millivolts from the supply rails while maintaining high open-loop gain (see the typical characteristic Output Voltage Swing vs Output Current).

CAPACITIVE LOAD AND STABILITY

The OPA347 in a unity-gain configuration can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads (see the characteristic curve Small-Signal Overshoot vs Capacitive Load). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor, R_S, in series with the output, as shown in Figure 6. This significantly reduces ringing while maintaining Direct Current (DC) performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a DC error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L, and is generally negligible.

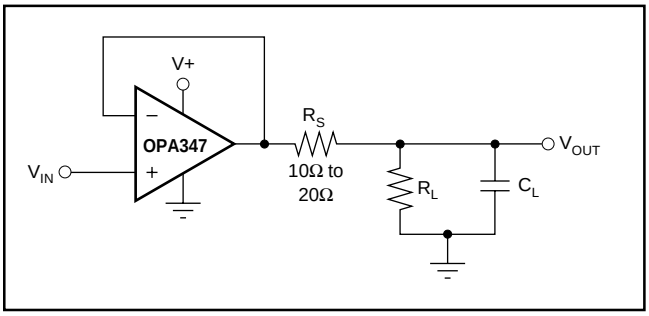


FIGURE 6. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive.

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input, and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small valued resistors. For example, when driving a 500pF load, reducing the resistor values from 100kΩ to 5kΩ decreases overshoot from 40% to 8% (see the characteristic curve Small-Signal Overshoot vs Load Capacitance). However, when large-valued resistors can not be avoided, a small (4pF to 6pF) capacitor, C_{FB}, can be inserted in the feedback, as shown in Figure 7. This significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the amplifier input capacitance and PC board parasitic capacitance.

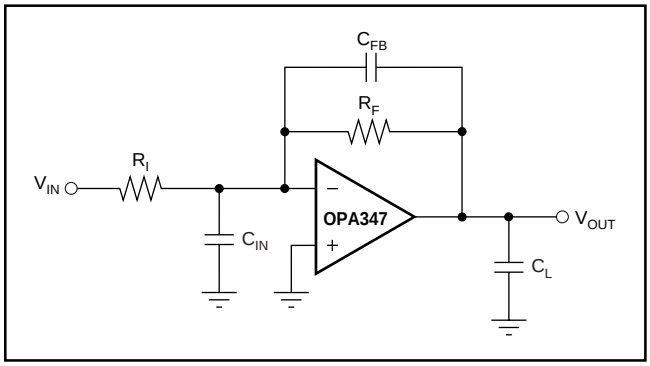


FIGURE 7. Adding a Feedback Capacitor In the Unity-Gain Inverter Configuration Improves Capacitative Load.

DRIVING ADCs

The OPA347 series op amps are optimized for driving medium-speed sampling Analog-to-Digital Converters (ADCs). The OPA347 op amps buffer the ADC's input capacitance and resulting charge injection while providing signal gain.

See Figure 8 for the OPA347 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, *micro*Power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA347, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide for anti-aliasing filter and charge injection current.

See Figure 9 for the OPA2347 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with V_S = 2.7V to 5V with less than 250µA typical quiescent current.

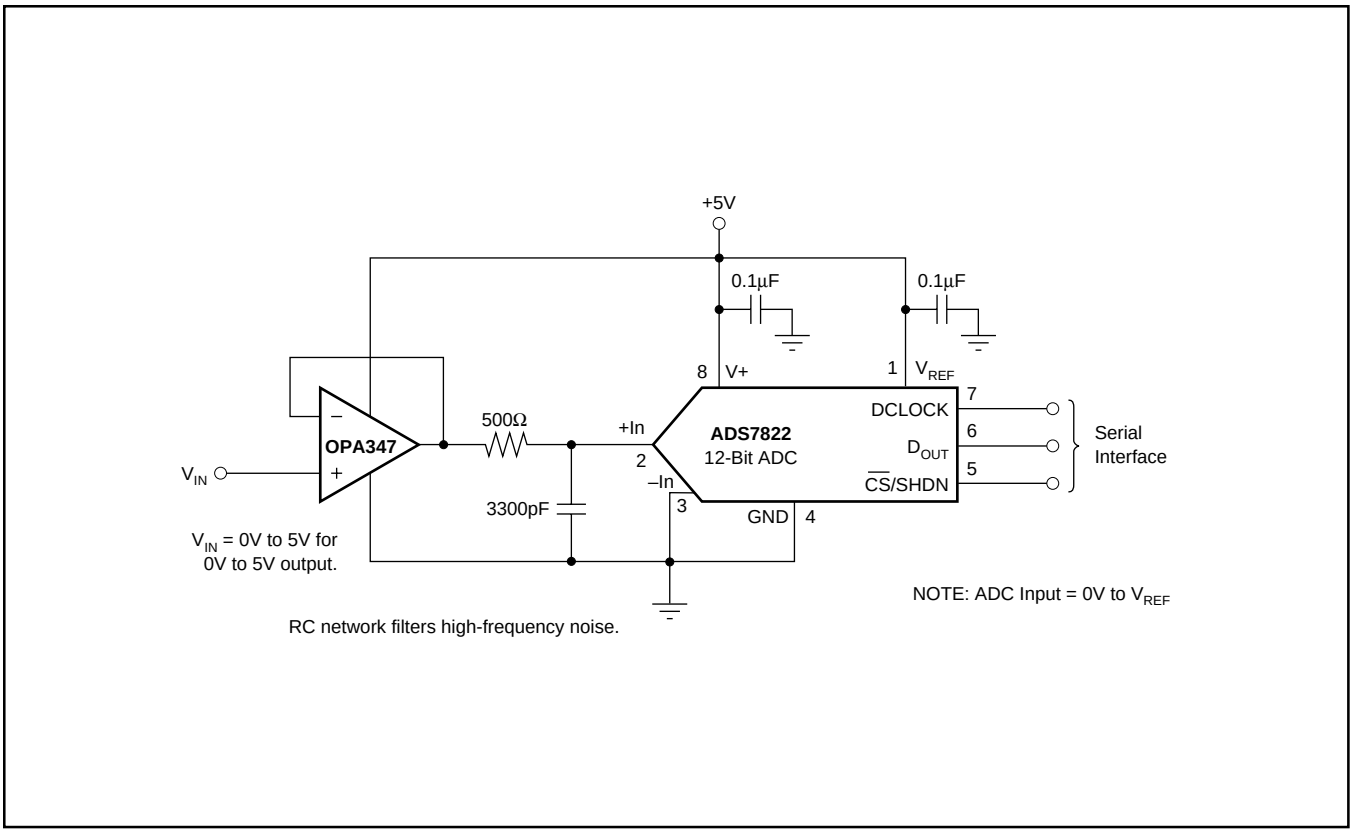


FIGURE 8. OPA347 in Noninverting Configuration Driving ADS7822.

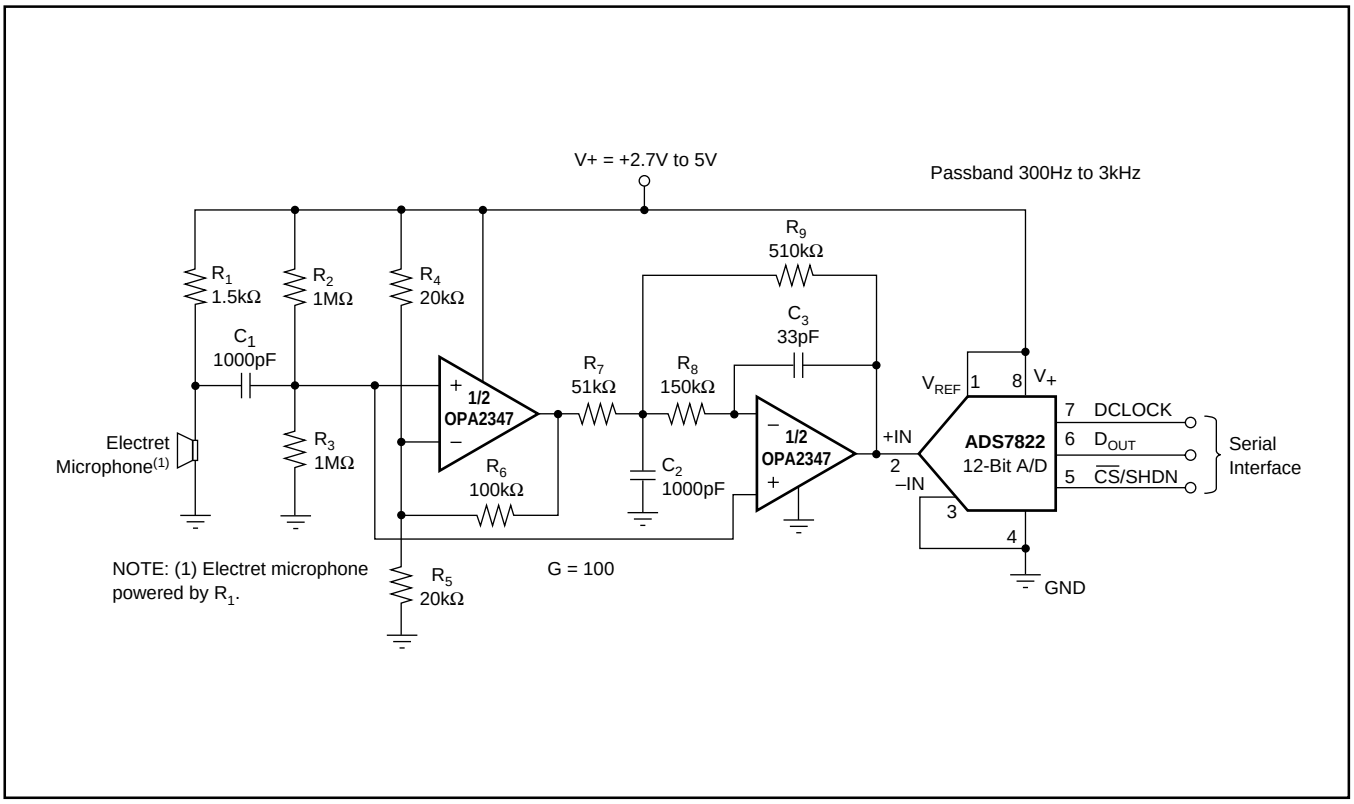


FIGURE 9. Speech Bandpass Filtered Data Acquisition System.

OPA2347 WCSP PACKAGE

The OPA2347YED and OPA2347YZDR are die-level packages using bump-on-pad technology. The OPA2347YED device has tin-lead balls; the OPA2347YZDR has lead-free balls. Unlike devices that are in plastic packages, these devices have no molding compound, lead frame, wire bonds, or leads. Using standard surface-mount assembly procedures, the WCSP can be mounted to a printed circuit board without additional under fill. Figures 10 and 11 detail pinout and package marking.

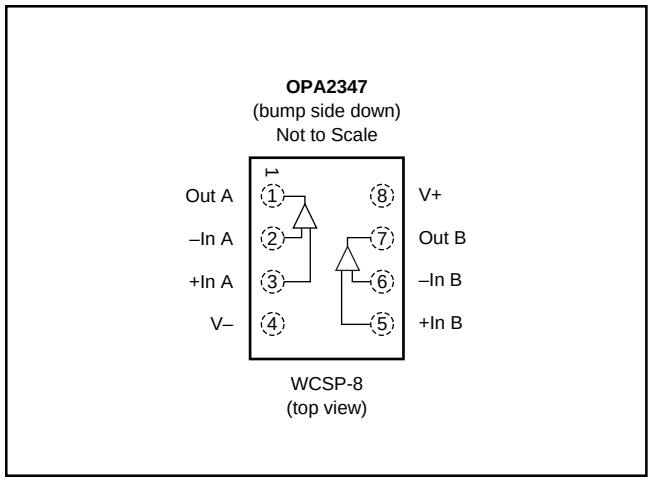


FIGURE 10. Pin Description.

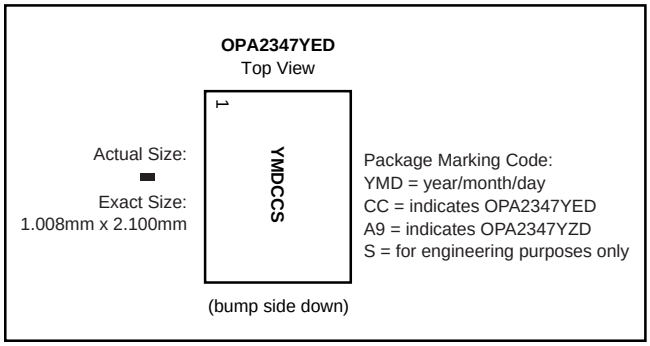


FIGURE 11. Top View Package Marking.

PHOTOSENSITIVITY

Although the OPA2347YED/YZD package has a protective backside coating that reduces the amount of light exposure on the die, unless fully shielded, ambient light will still reach the active region of the device. Input bias current for the OPA2347YED/YZD package is specified in the absence of light. Depending on the amount of light exposure in a given application, an increase in bias current, and possible increases in offset voltage should be expected. In circuit board tests under ambient light conditions, a typical increase in bias current reached 100pA. Flourescent lighting may introduce noise or hum due to their time varying light output. Best practice should include end-product packaging that provides shielding from possible light souces during operation.

RELIABILITY TESTING

To ensure reliability, the OPA2347YED and OPA2347YZDR devices have been verified to successfully pass a series of reliability stress tests. A summary of JEDEC standard reliability tests is shown in Table I.

TEST	CONDITION	ACCEPT CRITERIA (ACTUAL)	SAMPLE SIZE
Temperature Cycle	–40°C to 125°C, 1 Cycle/hr, 15 Minute Ramp(1) 10 Minute Dwell	500 (1600) Cycles, R < 1.2X from R_0	36
Drop	50cm	10 (129) Drops, R < 1.2X from R_0	8
Key Push	100 Cycles/min, 1300 με, Displacement = 2.7mm Max	5K (6.23K) Cycles, R < 1.2X from R_0	8
3 Point Bend	Strain Rate 5 mm/min, 85 mm Span	R < 1.2X from R_0	8
NOTE: (1) Per IPC9701.			

TABLE I. Reliability Test Results.

LAND PATTERNS AND ASSEMBLY

The recommended land pattern for the OPA2347YED package is detailed in Figure 12 with specifications listed in Table II. The maximum amount of force during assembly should be limited to 30 grams of force per bump.

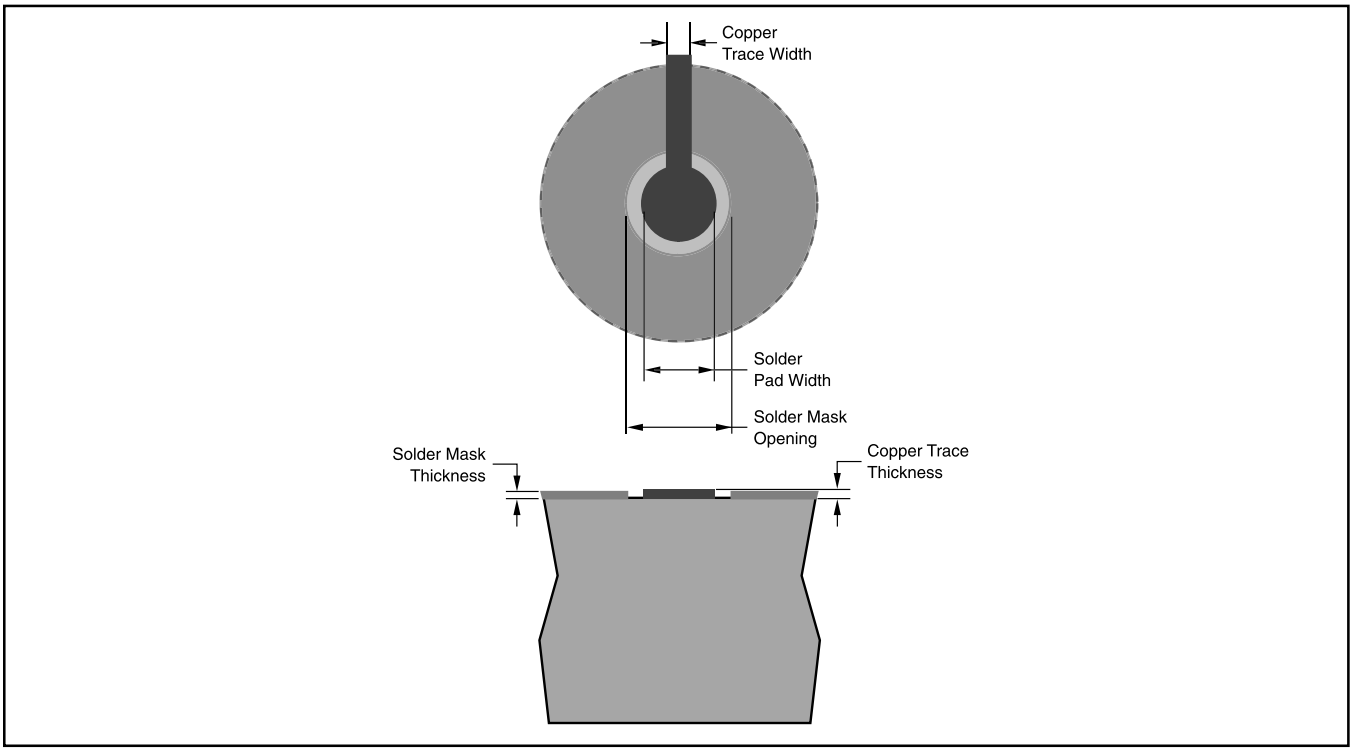


FIGURE 12. Recommended Land Area.

SOLDER PAD DEFINITION	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Non-Solder Mask Defined (NSMD)	275µm (+0.0, –25µm)	375µm (+0.0, –25µm)	1 oz max	275µm X 275µm, sq	125µm Thick
NOTES: (1) Circuit traces from NSMD-defined PWB lands should be less tham 100µm (preferrably = 75µm) wide in the exposed area inside the solder mask opening. Wider trace widths will reduce device stand off and impact reliability. (2) Recommended solder paste is type 3 or type 4. (3) Best reliability results are achieved when the PWB laminate glass transistion temperature is above the operating range of the intended application. (4) For PWB using an Ni/Au surface finish, the gold thickness should be less than 0.5um to avoid solder embrittlement and a reduction in thermal fatigue performance. (5) Solder mask thickness should be less than 20um on top of the copper circuit pattern. (6) Best solder stencil performance will be achieved using laser-cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control. (7) Trace routing away from the WLCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.					

TABLE II. Recommended Land Pattern.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2347EA/250	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47	Samples
OPA2347EA/250G4	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47	Samples
OPA2347EA/3K	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47	Samples
OPA2347EA/3KG4	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	B47	Samples
OPA2347UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA	Samples
OPA2347UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA	Samples
OPA2347UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 2347UA	Samples
OPA2347YZDR	ACTIVE	DSBGA	YZD	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		(A9, OPA2347)	Samples
OPA2347YZDT	ACTIVE	DSBGA	YZD	8	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 125	OPA2347	Samples
OPA347NA/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47	Samples
OPA347NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A47	Samples
OPA347PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	OPA347PA	Samples
OPA347PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	OPA347PA	Samples
OPA347SA/250	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47	Samples
OPA347SA/3K	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47	Samples
OPA347SA/3KG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	S47	Samples
OPA347UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 347UA	Samples
OPA347UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 347UA	Samples
OPA4347EA/250	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4347EA/2K5	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA 4347EA	Samples
OPA4347UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA	Samples
OPA4347UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA4347UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

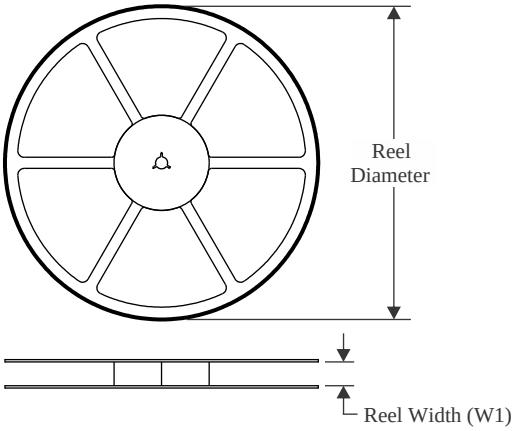
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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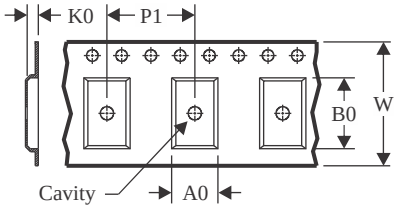
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

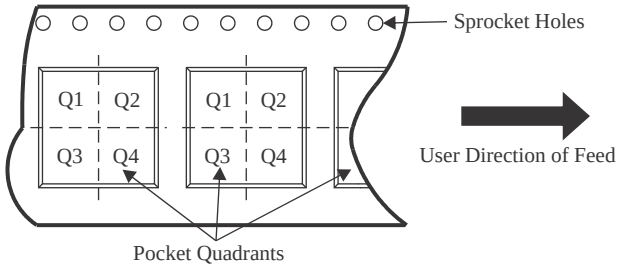


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

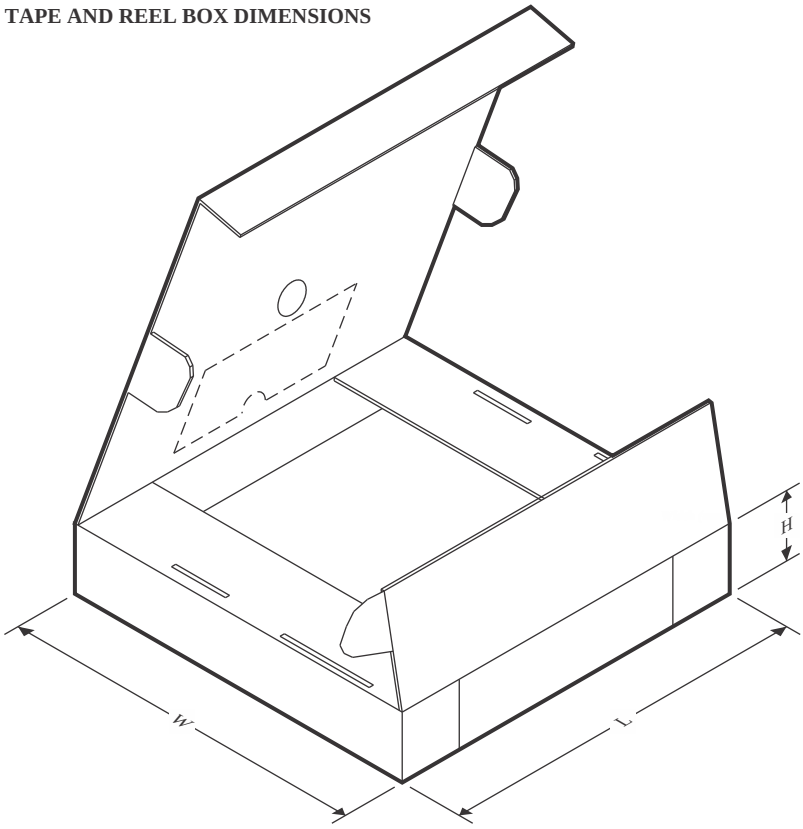
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2347EA/250	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2347EA/3K	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2347UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2347YZDR	DSBGA	YZD	8	3000	178.0	9.2	1.23	2.27	0.73	4.0	8.0	Q1
OPA2347YZDT	DSBGA	YZD	8	250	178.0	9.2	1.23	2.27	0.73	4.0	8.0	Q1
OPA347NA/250	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA347NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA347SA/250	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA347SA/3K	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA347UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4347EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4347EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4347UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

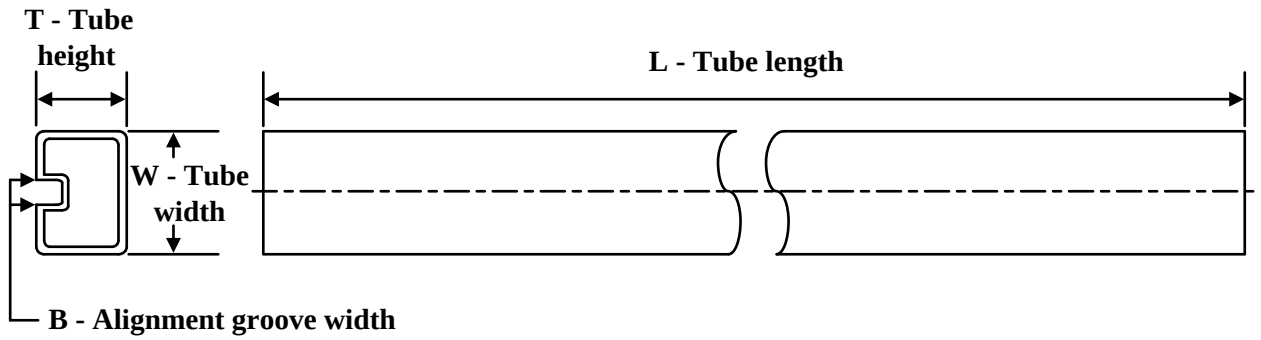
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2347EA/250	SOT-23	DCN	8	250	200.0	183.0	25.0
OPA2347EA/3K	SOT-23	DCN	8	3000	200.0	183.0	25.0
OPA2347UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2347YZDR	DSBGA	YZD	8	3000	220.0	220.0	35.0
OPA2347YZDT	DSBGA	YZD	8	250	220.0	220.0	35.0
OPA347NA/250	SOT-23	DBV	5	250	445.0	220.0	345.0
OPA347NA/3K	SOT-23	DBV	5	3000	445.0	220.0	345.0
OPA347SA/250	SC70	DCK	5	250	200.0	183.0	25.0
OPA347SA/3K	SC70	DCK	5	3000	200.0	183.0	25.0
OPA347UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4347EA/250	TSSOP	PW	14	250	210.0	185.0	35.0
OPA4347EA/2K5	TSSOP	PW	14	2500	356.0	356.0	35.0
OPA4347UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

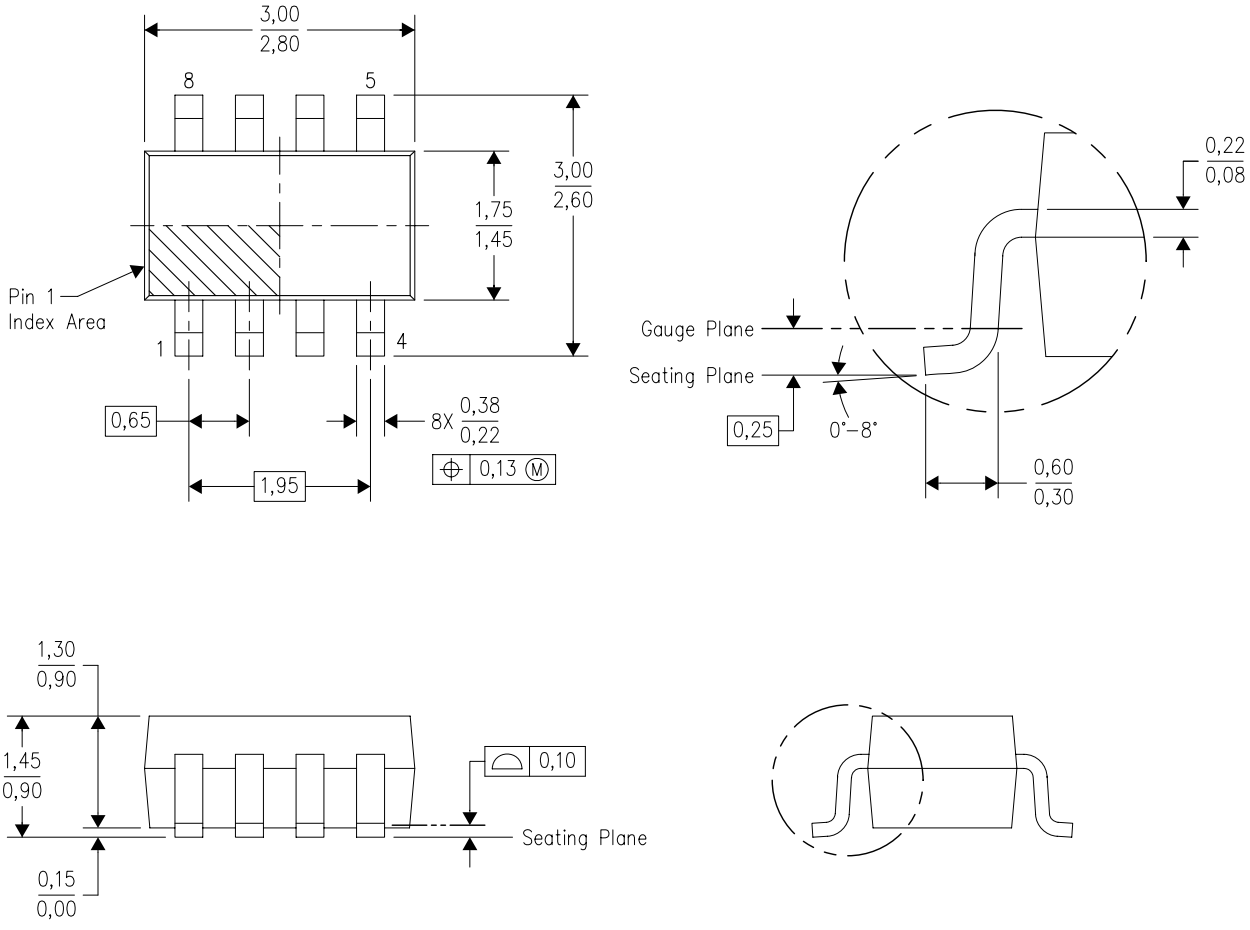
TUBE



*All dimensions are nominal

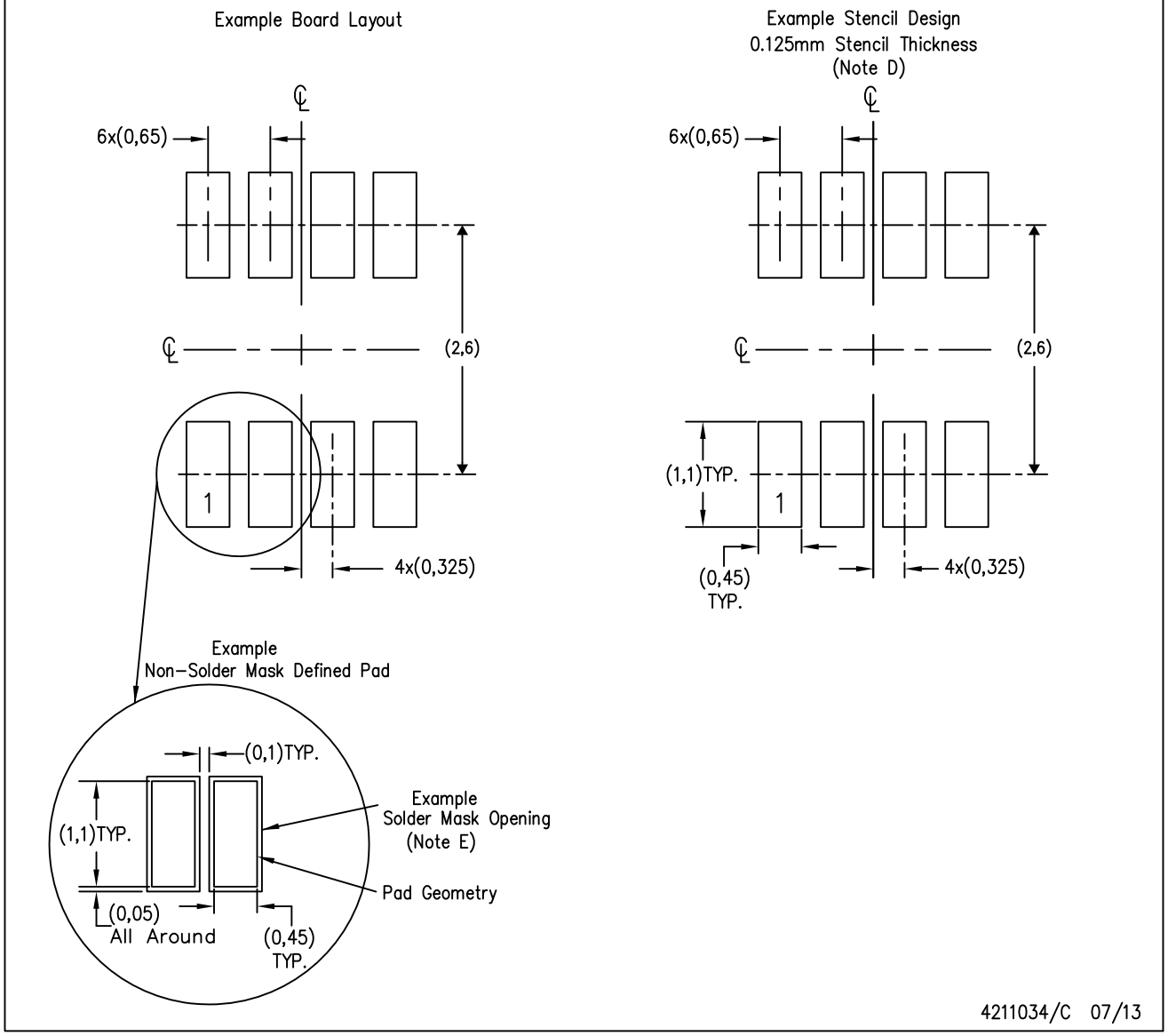
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2347UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA347PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA347PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA347UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA4347UA	D	SOIC	14	50	506.6	8	3940	4.32

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



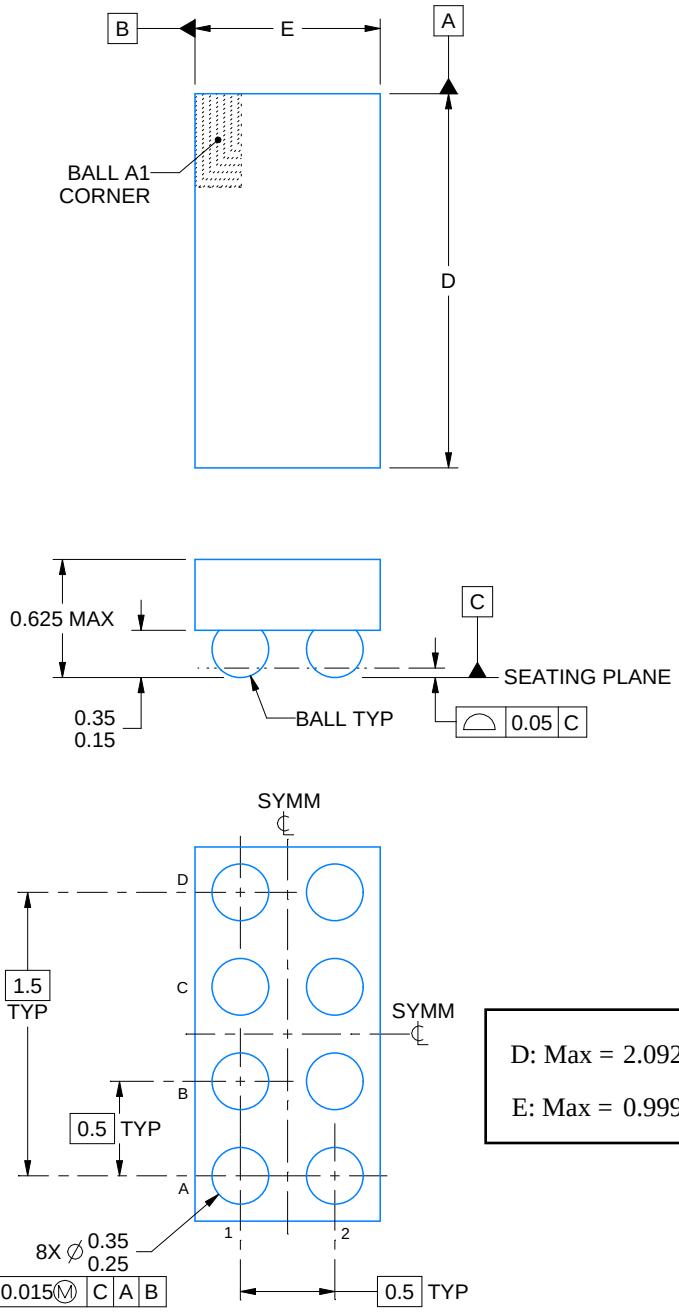
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

YZD0008

DSBGA - 0.625 mm max height

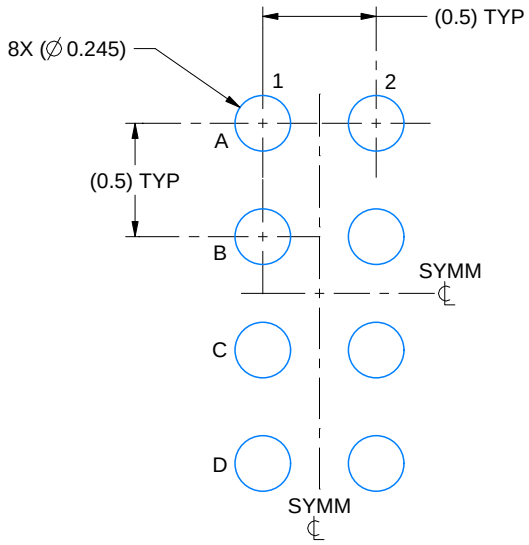
DIE SIZE BALL GRID ARRAY



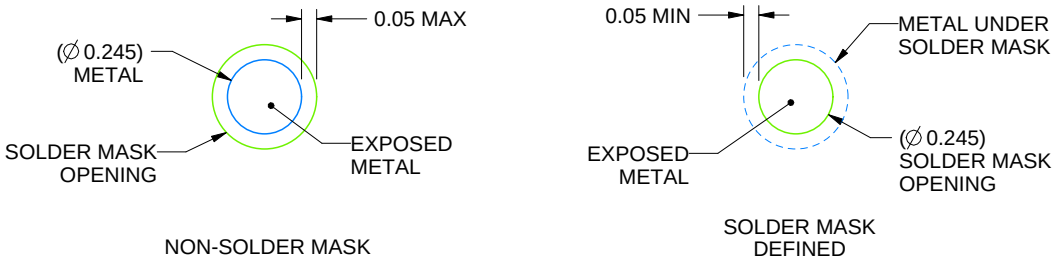
4219545/A 12/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4219545/A 12/2018

NOTES: (continued)

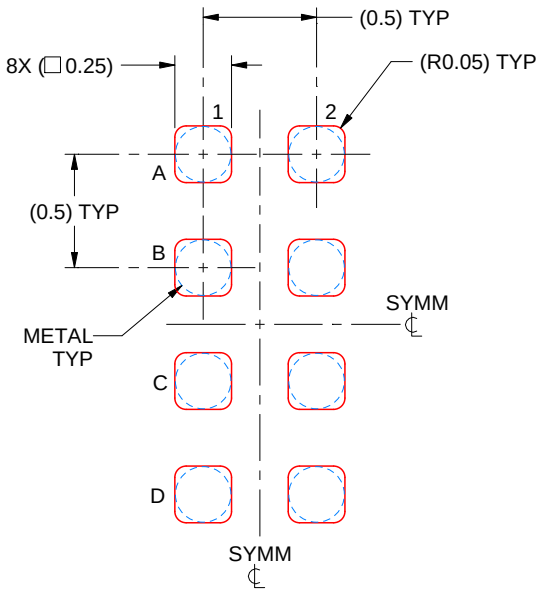
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZD0008

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4219545/A 12/2018

NOTES: (continued)

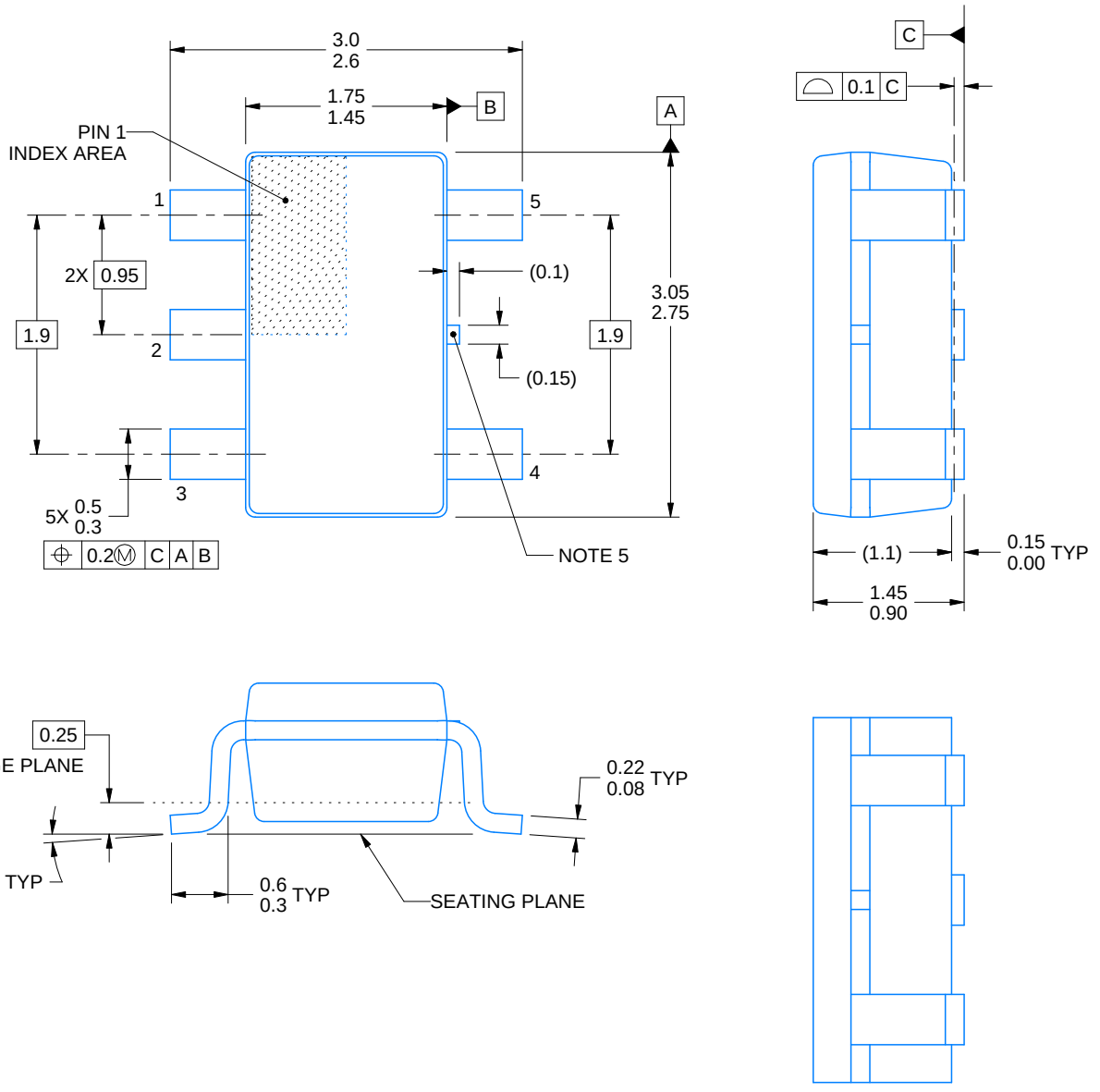
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

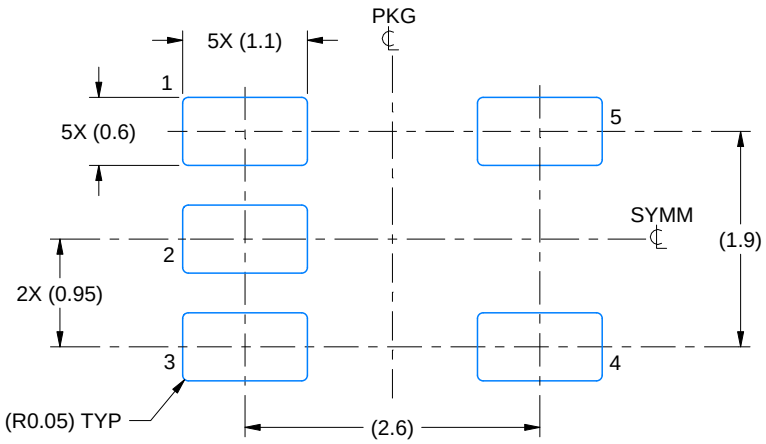


ALTERNATIVE PACKAGE SINGULATION VIEW

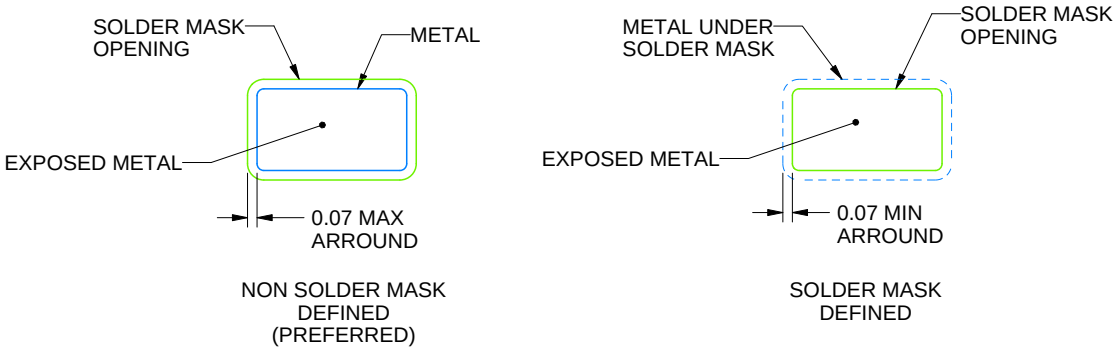
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

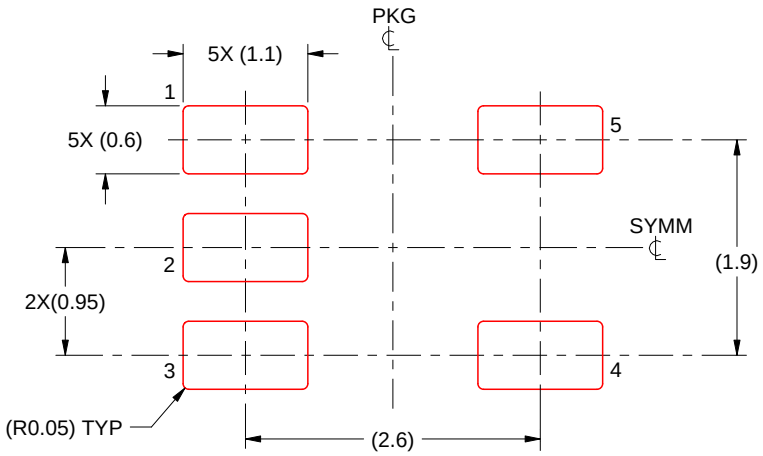


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

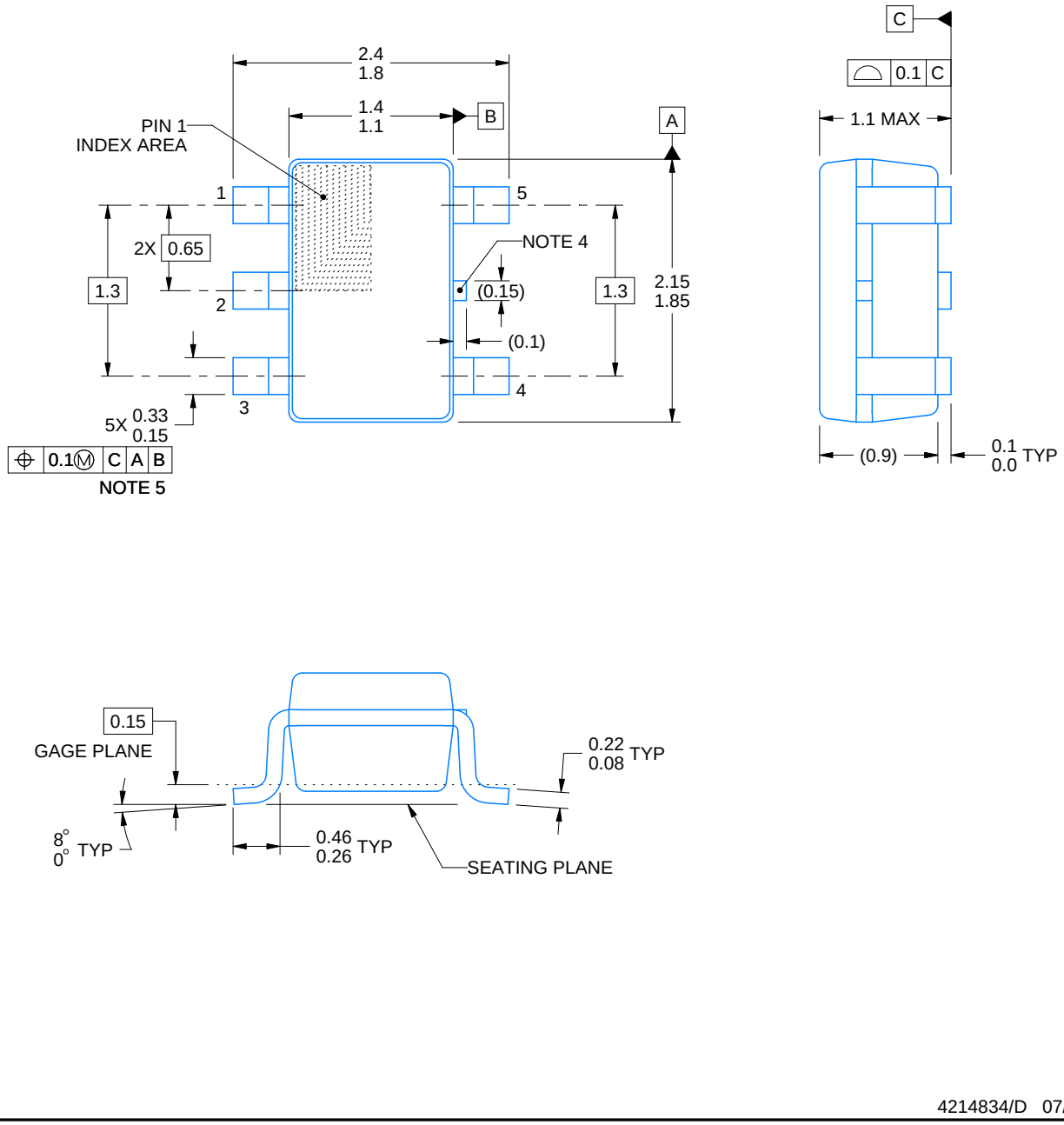
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

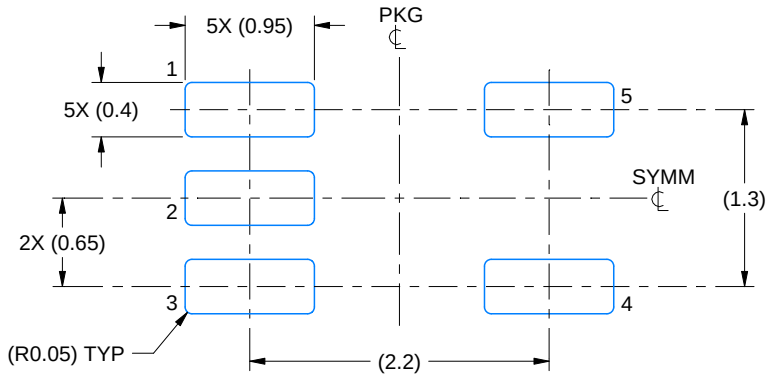
SMALL OUTLINE TRANSISTOR



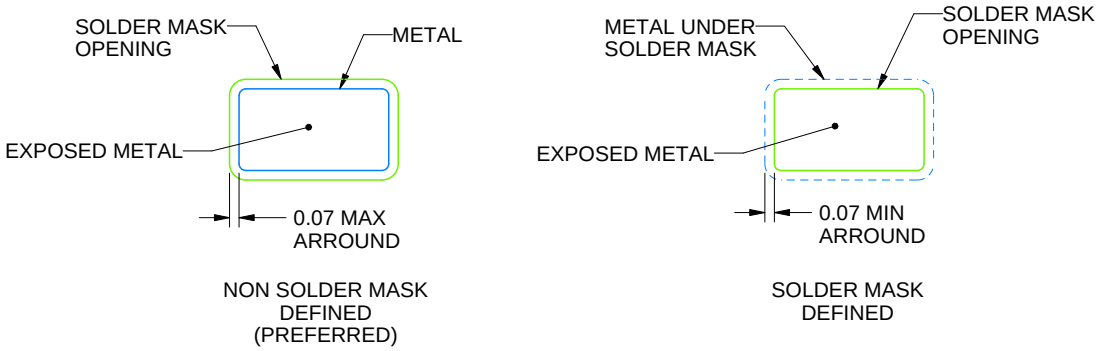
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

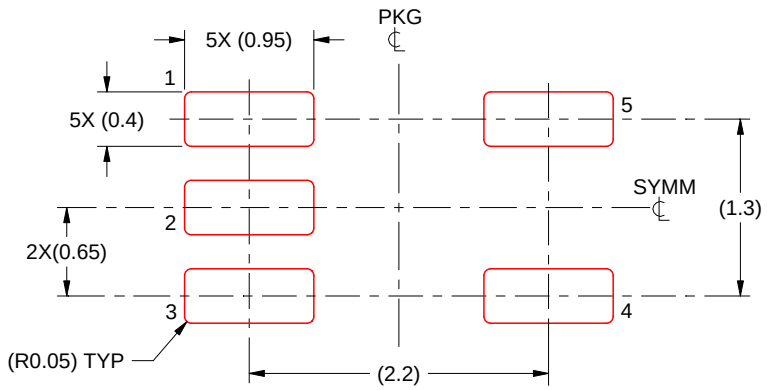


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



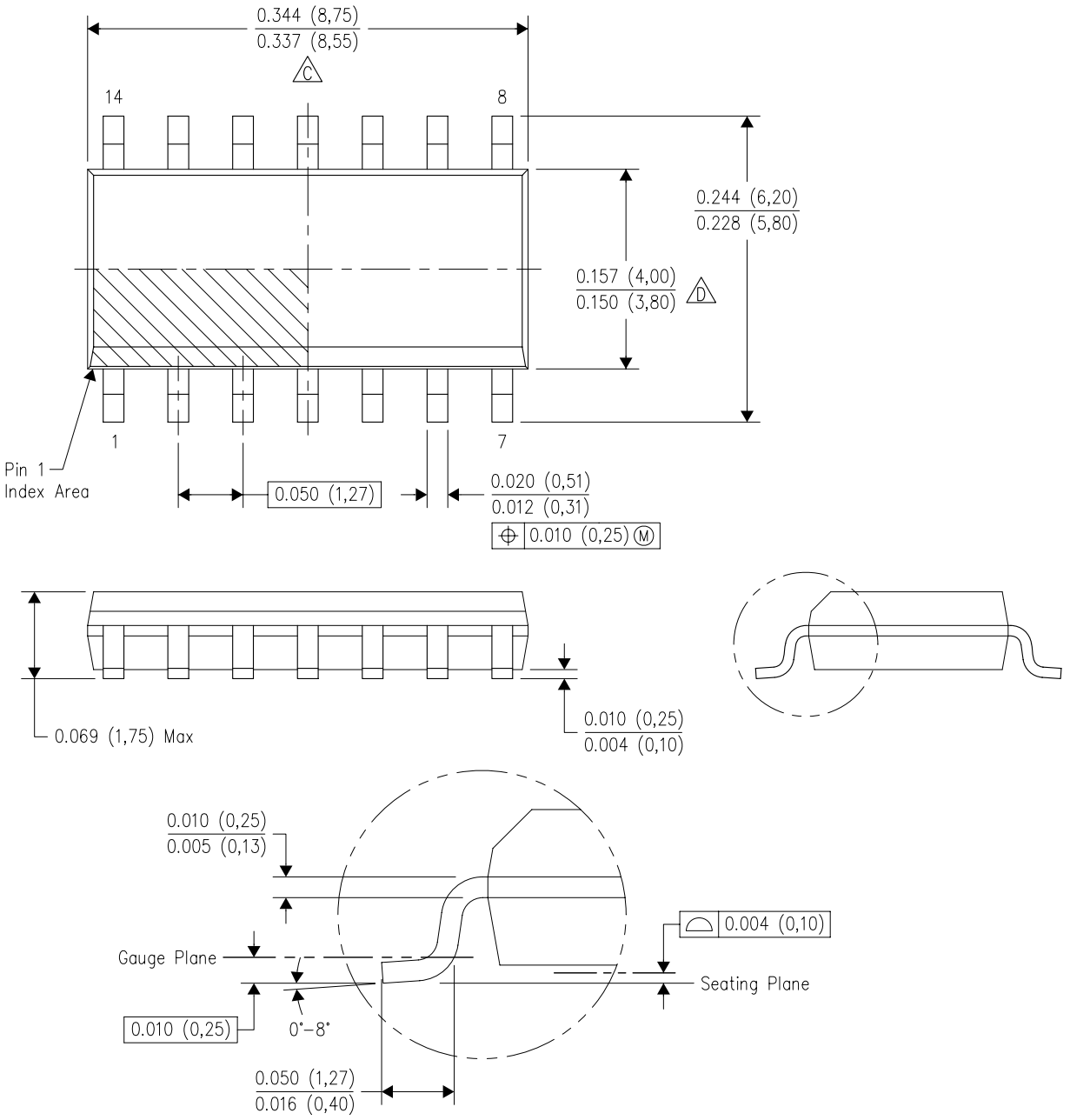
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

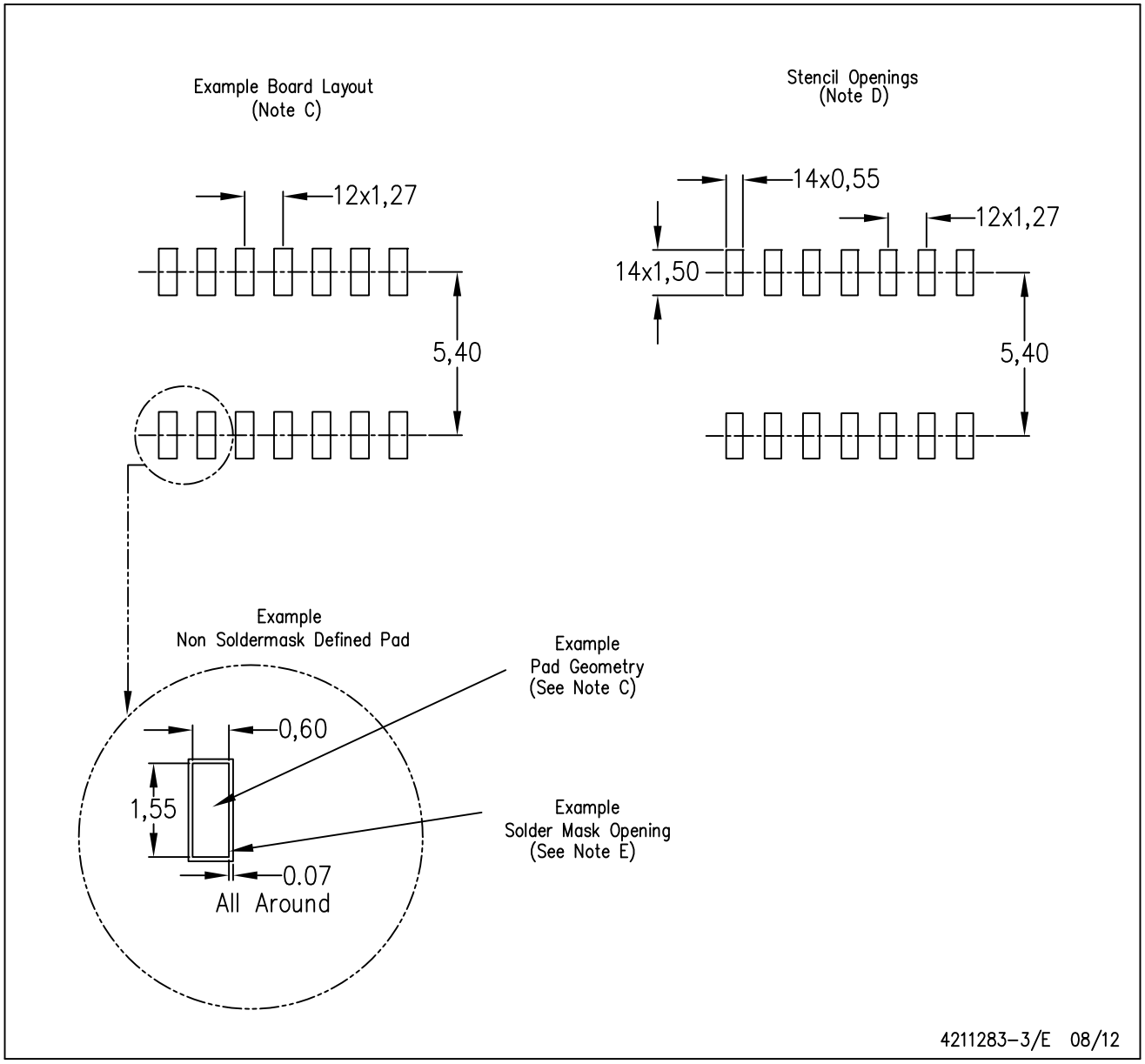
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

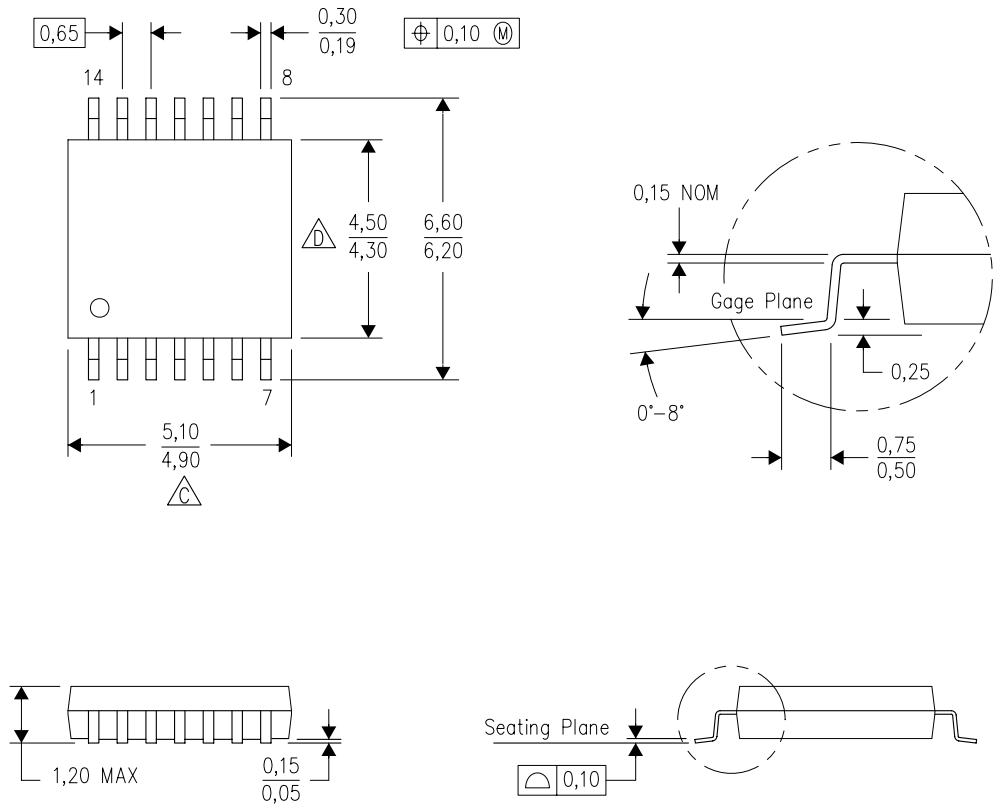
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

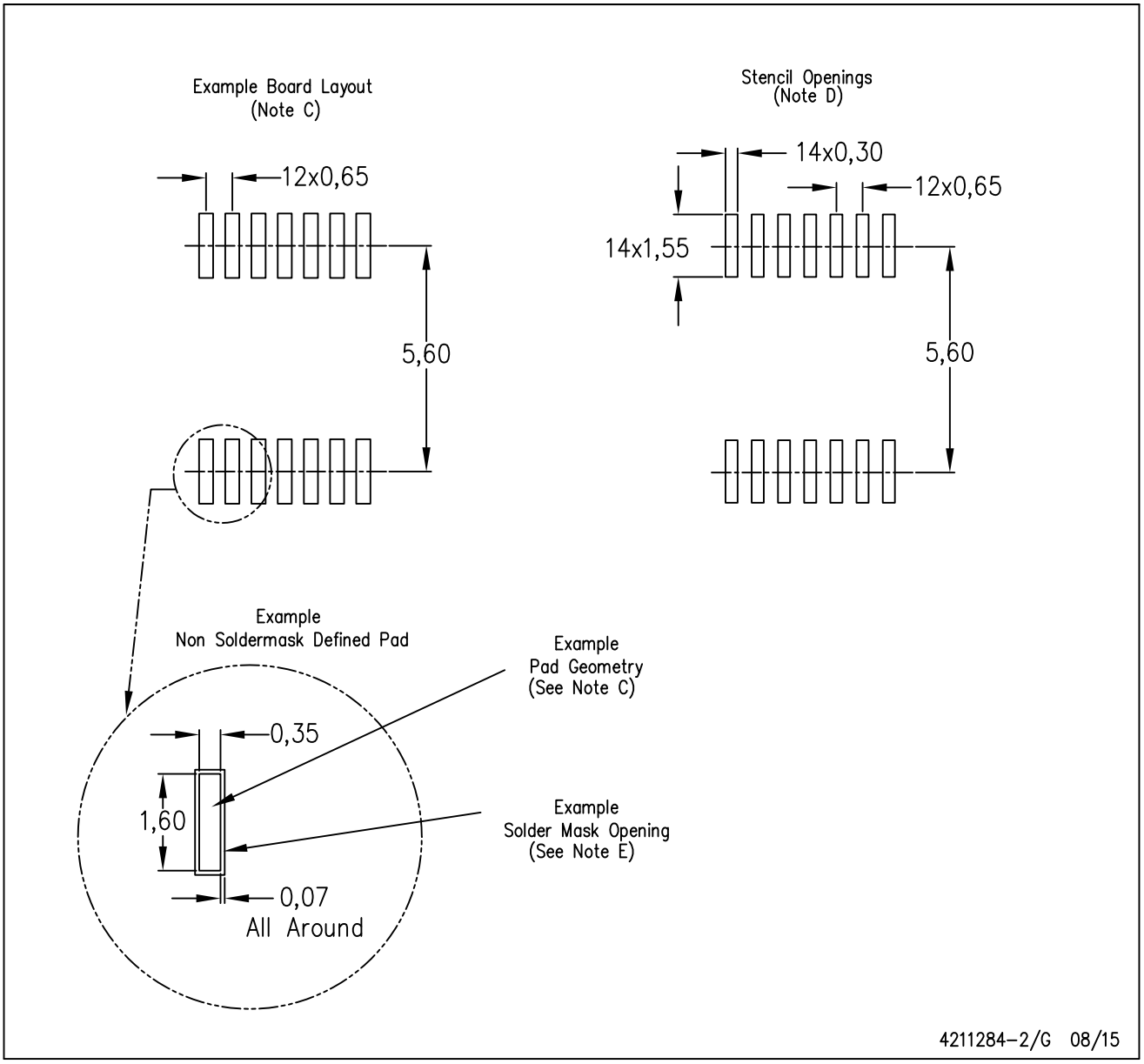
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



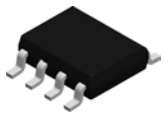
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

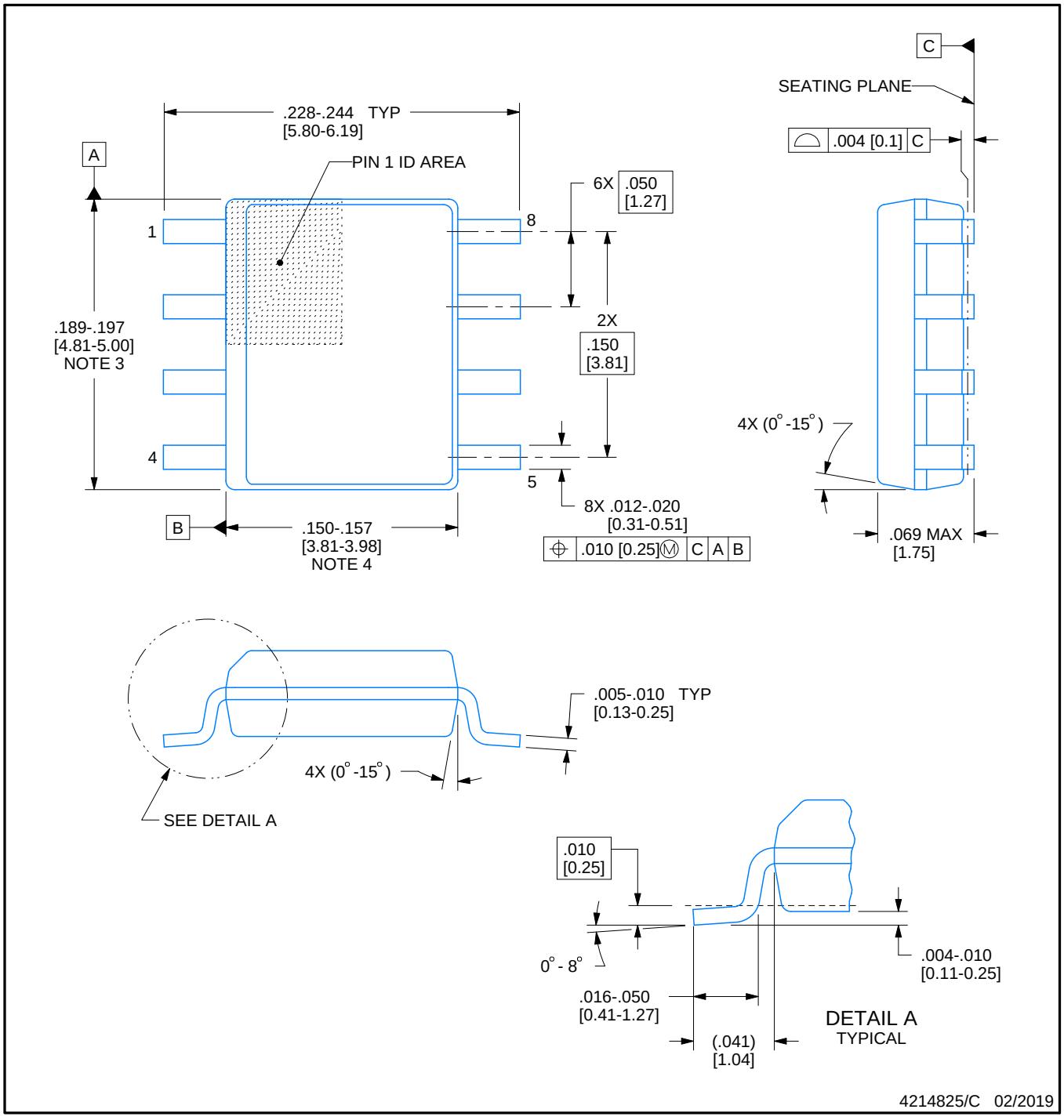


PACKAGE OUTLINE

D0008A

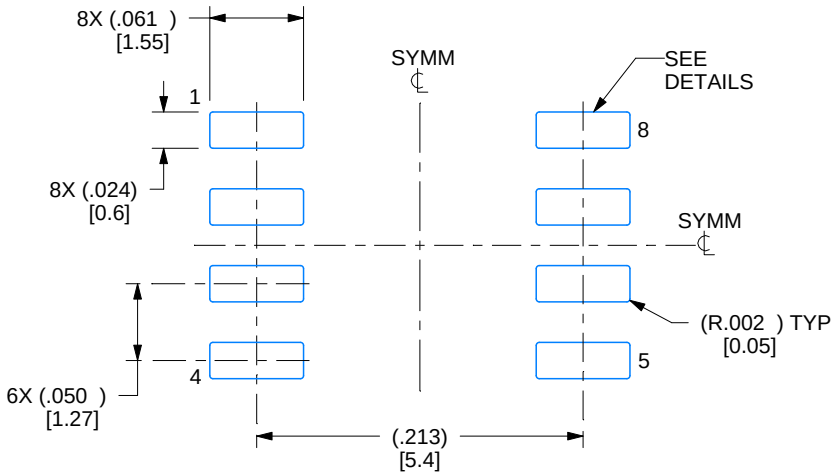
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

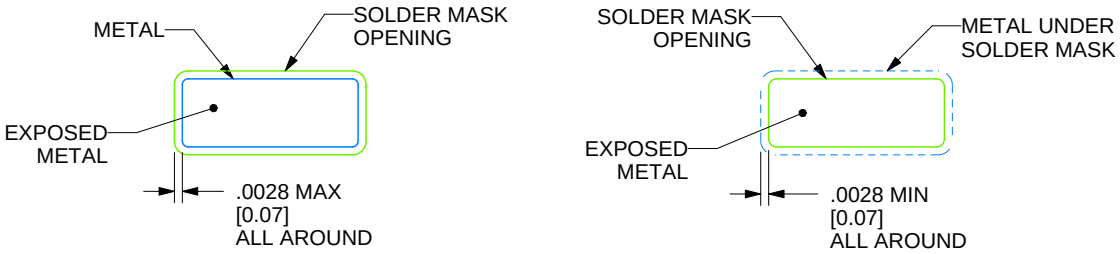


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

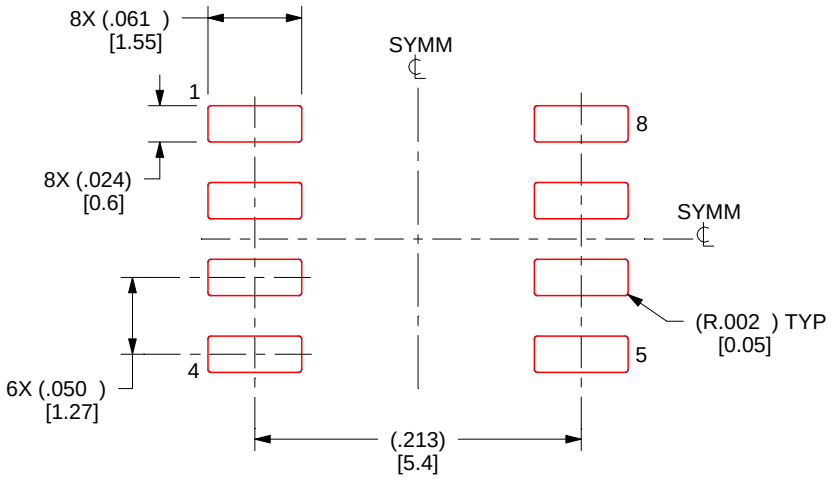
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



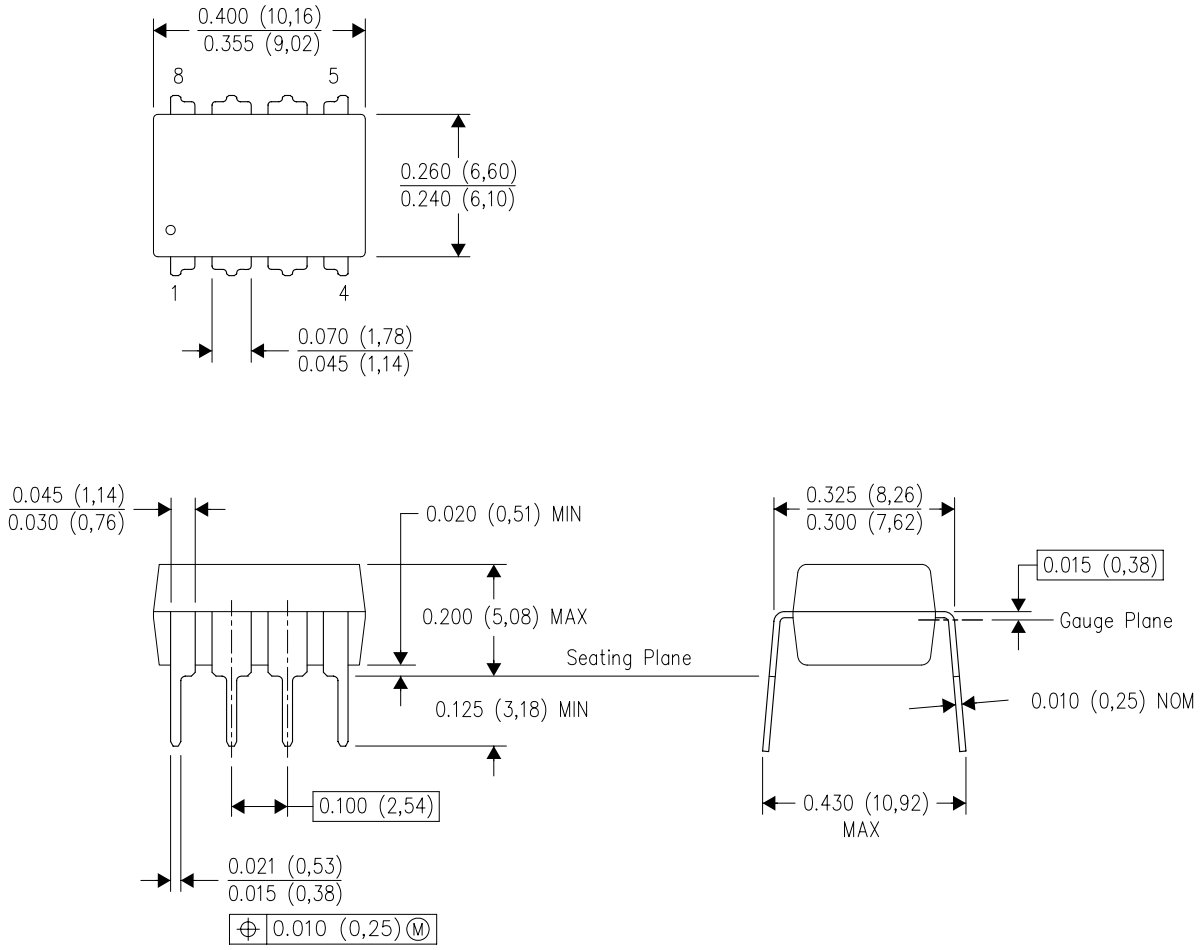
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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