Wide-Bandwidth, DC Restoration Circuit

Check for Samples: OPA615

FEATURES

- **PROPAGATION DELAY: 1.9ns**
- **BANDWIDTH:**
  OTA: 710MHz
  Comparator: 730MHz
- **LOW INPUT BIAS CURRENT: ±1μA**
- **SAMPLE-AND-HOLD SWITCHING TRANSIENTS: ±5mV**
- **SAMPLE-AND-HOLD FEEDTHROUGH REJECTION: 100dB**
- **CHARGE INJECTION: 40fC**
- **HOLD COMMAND DELAY TIME: 2.5ns**
- **TTL/CMOS HOLD CONTROL**

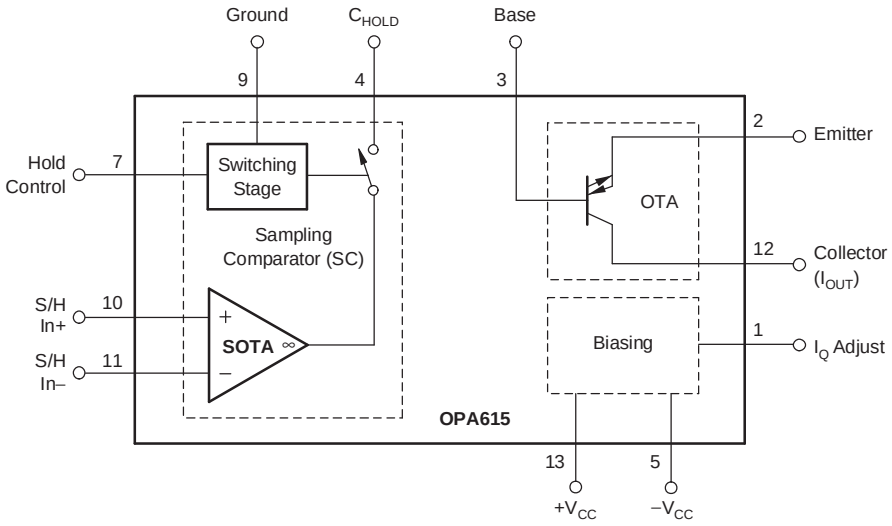
APPLICATIONS

- **BROADCAST/HDTV EQUIPMENT**
- **TELECOMMUNICATIONS EQUIPMENT**
- **HIGH-SPEED DATA ACQUISITION**
- **CAD MONITORS/CCD IMAGE PROCESSING**
- **NANOSECOND PULSE INTEGRATOR/PEAK DETECTOR**
- **PULSE CODE MODULATOR/DEMODULATOR**
- **COMPLETE VIDEO DC LEVEL RESTORATION**
- **SAMPLE-AND-HOLD AMPLIFIER**
- **SHC615 UPGRADE**

DESCRIPTION

The OPA615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low-frequency hum suppression of wideband amplifiers or buffers. Although it is designed to stabilize the performance of video signals, the circuit can also be used as a sample-and-hold amplifier, high-speed integrator, or peak detector for nanosecond pulses. The device features a wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast and precise sampling comparator that together set a new standard for high-speed applications. Both the OTA and the sampling comparator can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal voltage-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nanoseconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain trade-offs to be optimized.

The OPA615 is available in both an SO-14 surface-mount and an MSOP-10 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA615	SO-14	D	–40°C to +85°C	OPA615ID	OPA615ID	Rails, 50
					OPA615IDR	Tape and Reel, 2500
OPA615	MSOP-10	DGS	–40°C to +85°C	BJT	OPA615IDGST	Tape and Reel, 250
					OPA615IDGSR	Tape and Reel, 2500

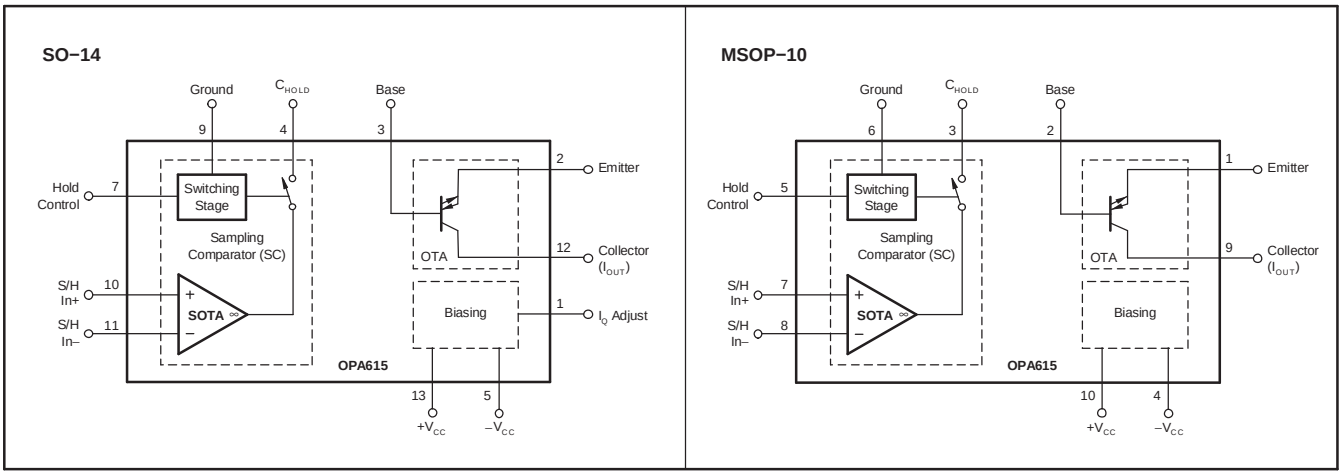
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±6.5V
Differential Input Voltage	$\pm V_S$
Common-Mode Input Voltage Range	$\pm V_S$
Hold Control Pin Voltage	$-V_S$ to $+V_S$
Storage Temperature Range	–65°C to +125°C
Junction Temperature (T_J)	+150°C
ESD Ratings:	
Human Body Model (HBM)(2)	1000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	150V

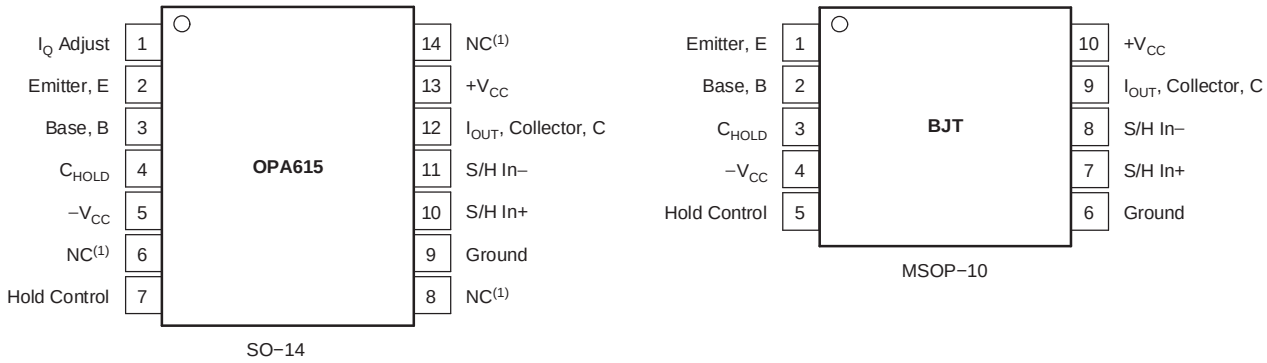
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Pin 2 for the SO-14 package and pin 1 for the MSOP-10 package > 500V HBM.

BLOCK DIAGRAMS



PIN CONFIGURATIONS

Top View



NOTE: (1) No Connection.

ELECTRICAL CHARACTERISTICS: V_S = ±5V

R_L = 100Ω, R_Q = 300Ω, and R_{IN} = 50Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA615ID, OPA615IDGS				UNIT	MIN/ MAX	TEST LEVEL (1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C (2)	0°C to 70°C (3)	–40°C to +85°C (3)			
AC PERFORMANCE (OTA)	See Figure 36b							
Small-Signal Bandwidth (B to E)	V_O = 200mV$_{PP}$, R_L = 500Ω	710				MHz	min	C
	V_O = 1.4V$_{PP}$, R_L = 500Ω	770				MHz	min	C
	V_O = 2.8V$_{PP}$, R_L = 500Ω	230				MHz	min	C
Large-Signal Bandwidth (B to E)	V_O = 5V$_{PP}$, R_L = 500Ω	200				MHz	min	C
Small-Signal Bandwidth (B to C)	G = +1, V_O = 200mV$_{PP}$, R_L = 100Ω	440				MHz	min	C
	G = +1, V_O = 1.4V$_{PP}$, R_L = 100Ω	475				MHz	min	C
	G = +1, V_O = 2.8V$_{PP}$, R_L = 100Ω	230				MHz	min	C
Large-Signal Bandwidth (B to C)	G = +1, V_O = 5V$_{PP}$, R_L = 100Ω	230				MHz	min	C
Rise-and-Fall Time (B to E)	V_O = 2V$_{PP}$, R_L = 500Ω	2				ns	max	C
Rise-and-Fall Time (B to C)	G = +1, V_O = 2V$_{PP}$, R_L = 100Ω	2				ns	max	C
Harmonic Distortion (B to E)	R_E = 100Ω							
2nd-Harmonic	V_O = 1.4V$_{PP}$, f = 30MHz	–62	–50	–48	–47	dBc	min	B
3rd-Harmonic	V_O = 1.4V$_{PP}$, f = 30MHz	–47	–40	–35	–33	dBc	min	B
Input Voltage Noise	Base Input, f > 100kHz	4.6	6.2	6.9	7.4	nV/√Hz	max	B
Input Current Noise	Base Input, f > 100kHz	2.5	3.1	3.6	3.9	pA/√Hz	max	B
Input Current Noise	Emitter Input, f > 100kHz	21	23	25	27	pA/√Hz	max	B
DC PERFORMANCE (OTA)	See Figure 37b							
Transconductance (V-base to I-collector)	V_B = ±5mV$_{PP}$, R_C = 0Ω, R_E = 0Ω	72	**65**	63	58	mA/V	min	A
B-Input Offset Voltage	V_B = 0V, R_C = 0V, R_E = 100Ω	±4	**±40**	±47	±50	mV	max	A
B-Input Offset Voltage Drift	V_B = 0V, R_C = 0V, R_E = 100Ω			±160	±160	µV/°C	max	B
B-Input Bias Current	V_B = 0V, R_C = 0V, R_E = 100Ω	±0.5	**±0.9**	±1.5	±1.7	µA	max	A
B-Input Bias Current Drift	V_B = 0V, R_C = 0V, R_E = 100Ω			±12	±12	nA/°C	max	B
E-Input Bias Current	V_B = 0V, V_C = 0V	±35	**±110**	±120	±135	µA	min	A
E-Input Bias Current Drift	V_B = 0V, V_C = 0V			±200	±250	nA/°C	max	B
C-Output Bias Current	V_B = 0V, V_C = 0V	±35	**±100**	±110	±125	µA	max	A
C-Output Bias Current	V_B = 0V, V_C = 0V			±200	±250	nA/°C	max	B
INPUT (OTA Base)	See Figure 37b							
Input Voltage Range	R_E = 100Ω	±3.4	**±3.2**	±3.1	±3.0	V	min	B
Input Impedance	B-Input	7 || 1.5				MΩ || pF	typ	C
OTA Power-Supply Rejection Ratio (–PSRR)	±V_S to V_{IO} at E-Input	54	**49**	47	46	dB	min	A
OUTPUT (OTA Collector)	See Figure 37b							
Output Voltage Compliance	I_E = 2mA	±3.5	**±3.4**	±3.4	±3.4	V	min	A
Output Current	V_C = 0V	±20	**±18**	±17	±17	mA	min	A
Output Impedance	V_C = 0V	1.2 || 2				MΩ || pF	typ	C
COMPARATOR PERFORMANCE								
AC Performance								
Output Current Bandwidth	I_O < 4mA$_{PP}$	730	520	480	400	MHz	min	B
Output Current Rise and Fall Time	I_{IO} = ±2mA$_{PP}$, R_L = 50Ω at C_{HOLD}	1.4	1.5	1.7	2	ns	max	B
Control Propagation Delay Time	Hold ≥ Track and Track ≥ Hold	2.5				ns	typ	C
Signal Propagation Delay Time	S/H In+ – S/H In– to C_{HOLD} Current	1.9				ns	typ	C
Input Differential Voltage Noise	S/H In+ – S/H In–	6	7.5	8	9	nV/√Hz	max	B
Charge Injection	Track-to-Hold	40				fC	typ	C
Feedthrough Rejection	Hold Mode, V_{IN} = 1V$_{PP}$, f < 20MHz	100				dB	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

R_L = 100Ω, R_Q = 300Ω, and R_{IN} = 50Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA615ID, OPA615IDGS				UNIT	MIN/ MAX	TEST LEVEL (1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C (2)	0°C to 70°C (3)	–40°C to +85°C (3)			
DC Performance								
Input Bias Current	S/H In+ = S/H In– = 0V	±1	**±3**	±3.5	±4.0	µA	max	A
Output Offset Current	S/H In+ = S/H In– = 0V, Track Mode	±10	**±50**	±70	±80	µA	max	A
Input Impedance	S/H In+ and S/H In–	200 || 1.2				kΩ || pF	typ	C
Input Differential Voltage Range	S/H In+ – S/H In–	±3.0				V	typ	C
Input Common-Mode Voltage Range	S/H In+ and S/H In–	±3.2				V	typ	C
Common-Mode Rejection Ratio (CMRR)		±2	**±50**	±55	±60	µA/V	max	A
Output Voltage Compliance	C_{HOLD} Pin	±3.5				V	typ	C
Output Current	C_{HOLD} Pin	±5	**±3**	±2.5	±2.0	mA	min	A
Output Impedance	C_{HOLD} Pin	0.5 || 1.2				MΩ || pF	typ	C
Transconductance	S/H In+ – S/H In– to C_{HOLD} Current V_{IN} = 300mV_{PP}	35	**21**	20	19	mA/V	min	A
Minimum Hold Logic High Voltage	Tracking High		**2**	2	2	V	max	A
Maximum Hold Logic Low Voltage	Holding Low		**0.8**	0.8	0.8	V	min	A
Logic High Input Current	V_{HOLD} = +5V	±0.5	**±1**	±1	±1.2	µA	max	A
Logic Low Input Current	V_{HOLD} = 0V	140	**200**	220	230	µA	max	A
Comparator Power-Supply Rejection Ratio (PSRR)	S/H In+ = S/H In– = 0V, Track Mode	±2	**±50**	±55	±60	µA/V	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Minimum Operating Voltage			**±4**	±4	±4	V	min	B
Maximum Operating Voltage			**±6.2**	±6.2	±6.2	V	max	A
Maximum Quiescent Current	R_Q = 300Ω(4)	13	**14**	16	17	mA	max	A
Minimum Quiescent Current	R_Q = 300Ω(4)	13	**12**	11	9	mA	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range D Package		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}	Junction-to-Ambient							
DGS MSOP-10		125				°C/W	typ	C
D SO-14		100				°C/W	typ	C

(4) SO-14 package only.

TYPICAL CHARACTERISTICS

T_A = +25°C and I_Q = 13mA, unless otherwise noted.

OTA

OTA TRANSCONDUCTANCE vs FREQUENCY

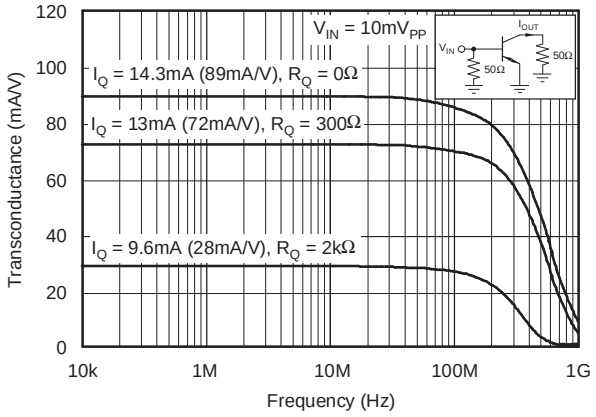


Figure 1.

OTA TRANSCONDUCTANCE vs QUIESCENT CURRENT

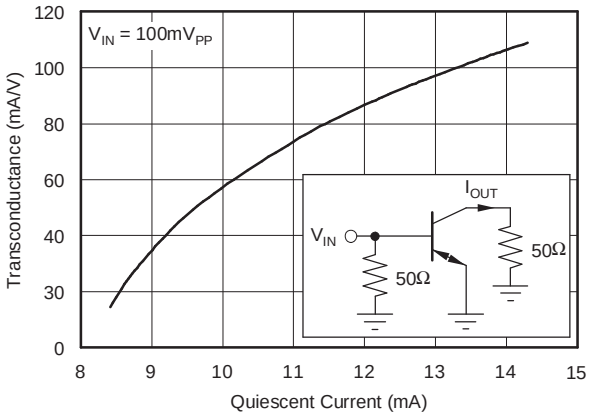


Figure 2.

OTA TRANSCONDUCTANCE vs INPUT VOLTAGE

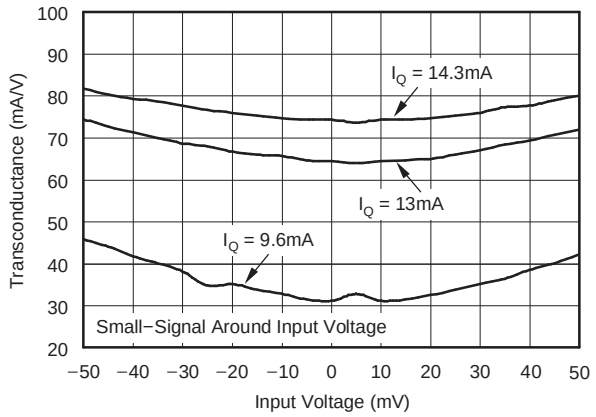


Figure 3.

OTA TRANSFER CHARACTERISTICS

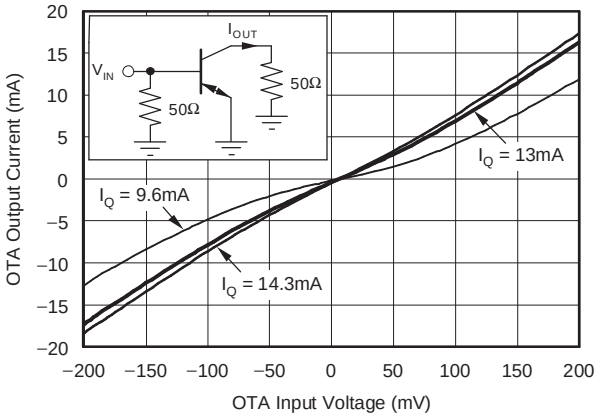


Figure 4.

OTA-C SMALL SIGNAL PULSE RESPONSE

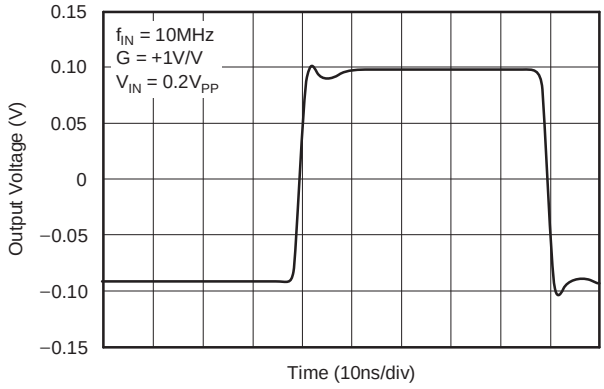


Figure 5.

OTA-C LARGE SIGNAL PULSE RESPONSE

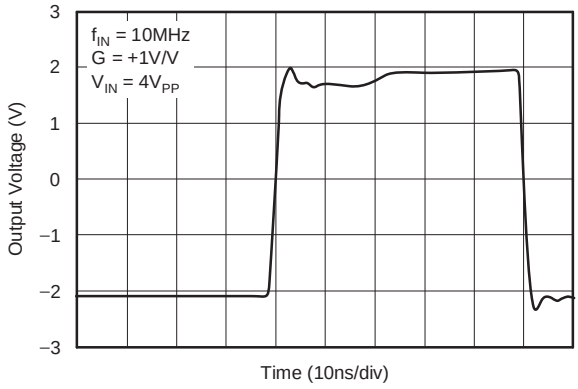


Figure 6.

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C and I_Q = 13mA, unless otherwise noted.

OTA B-INPUT RESISTANCE vs QUIESCENT CURRENT

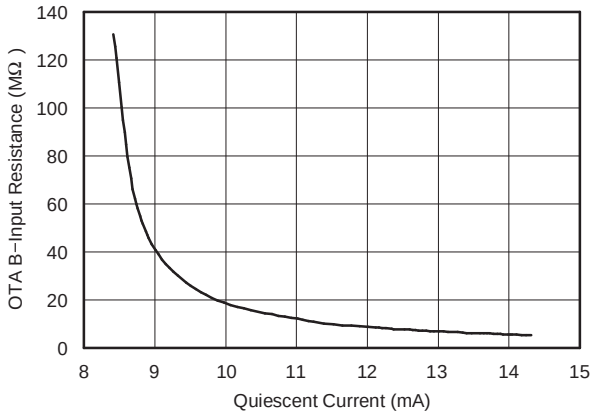


Figure 7.

OTA C-OUTPUT RESISTANCE vs QUIESCENT CURRENT

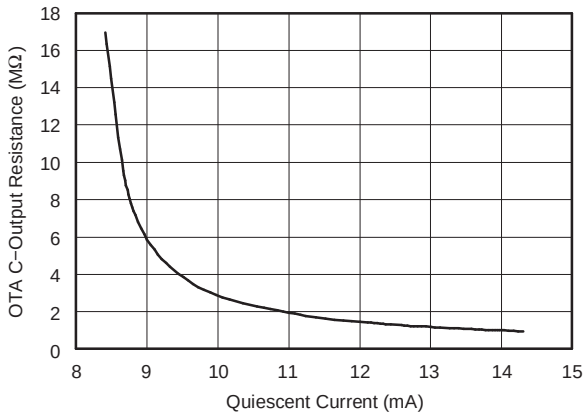


Figure 8.

OTA E-OUTPUT RESISTANCE vs QUIESCENT CURRENT

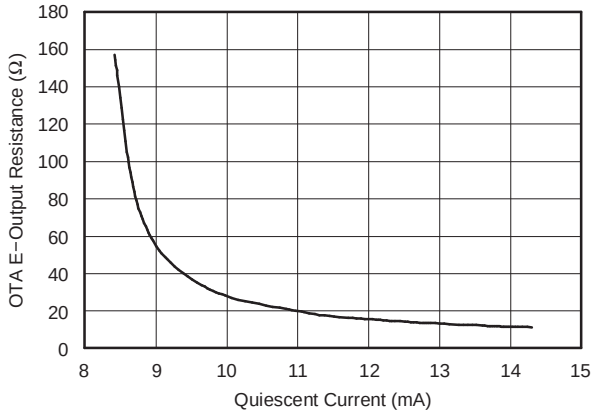


Figure 9.

OTA INPUT VOLTAGE AND CURRENT NOISE DENSITY

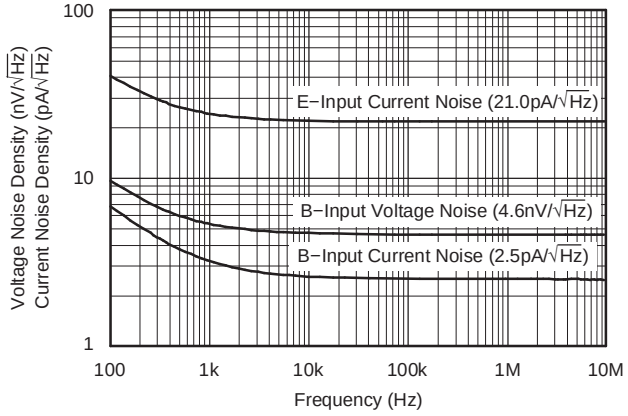


Figure 10.

OTA B-INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

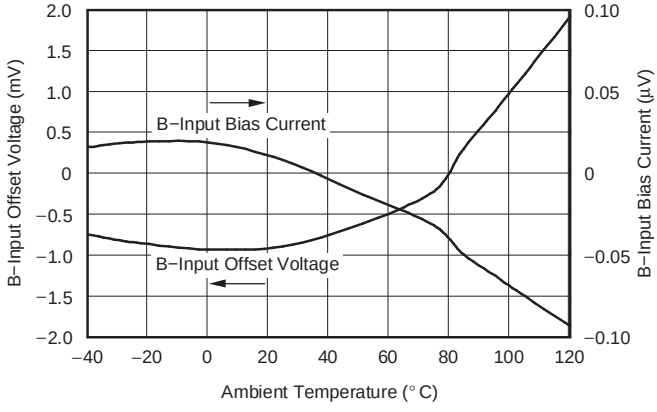


Figure 11.

OTA TRANSFER CHARACTERISTICS vs INPUT VOLTAGE

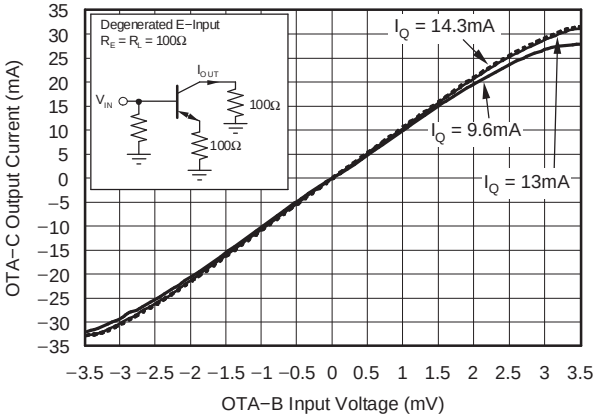


Figure 12.

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C and I_Q = 13mA, unless otherwise noted.

OTA-E OUTPUT FREQUENCY RESPONSE

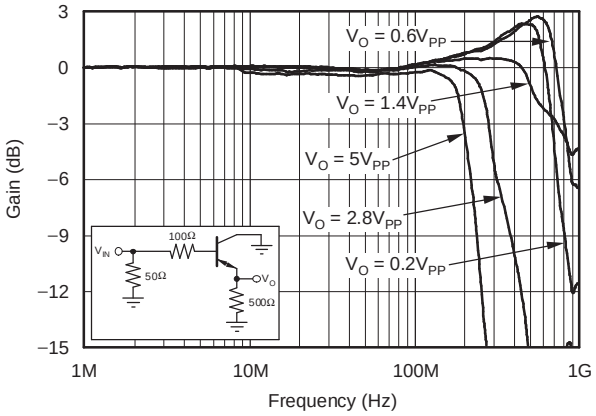


Figure 13.

OTA-E OUTPUT PULSE RESPONSE

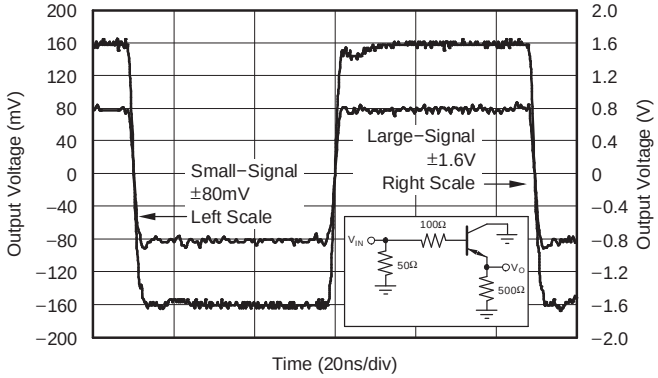


Figure 14.

OTA-C OUTPUT FREQUENCY RESPONSE

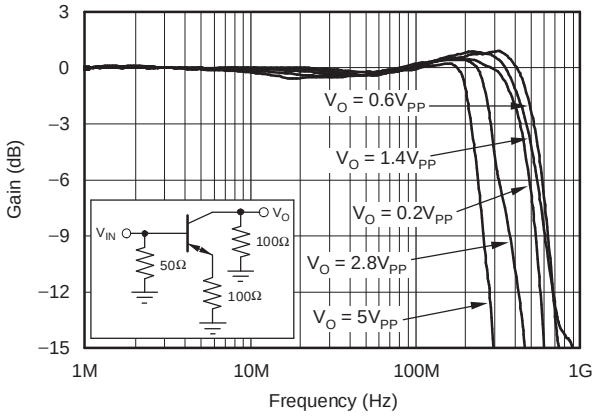


Figure 15.

OTA-E OUTPUT HARMONIC DISTORTION vs FREQUENCY

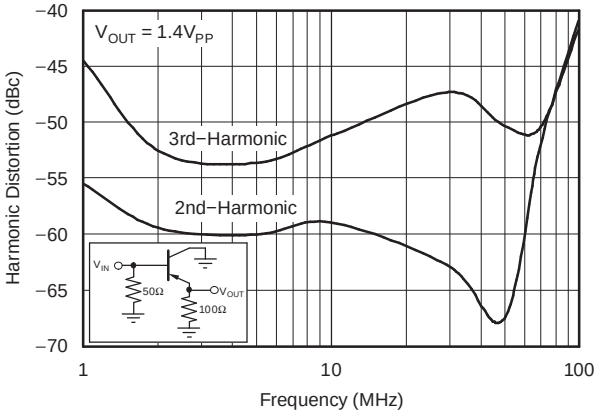


Figure 16.

OTA-C OUTPUT HARMONIC DISTORTION vs FREQUENCY

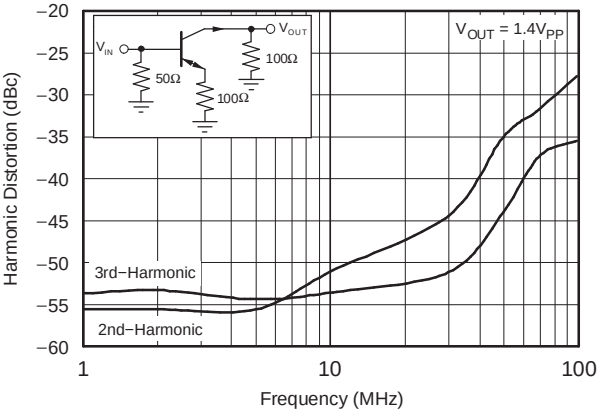


Figure 17.

OTA QUIESCENT CURRENT vs R_Q

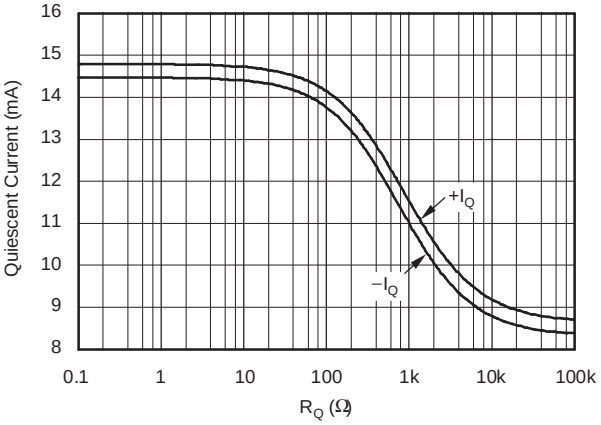


Figure 18.

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C and I_Q = 13mA, unless otherwise noted.

SOTA (Sampling Operational Transconductance Amplifier)

SOTA TRANSCONDUCTANCE vs FREQUENCY

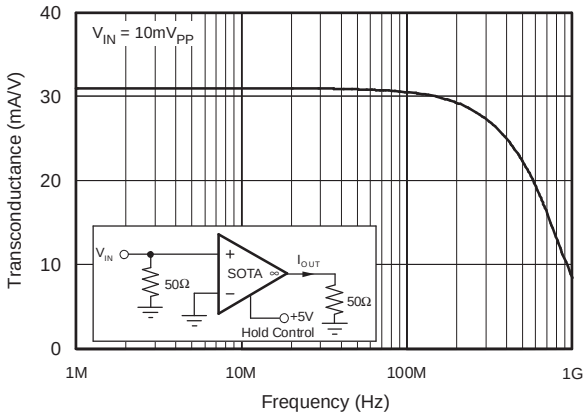


Figure 19.

SOTA TRANSCONDUCTANCE vs QUIESCENT CURRENT

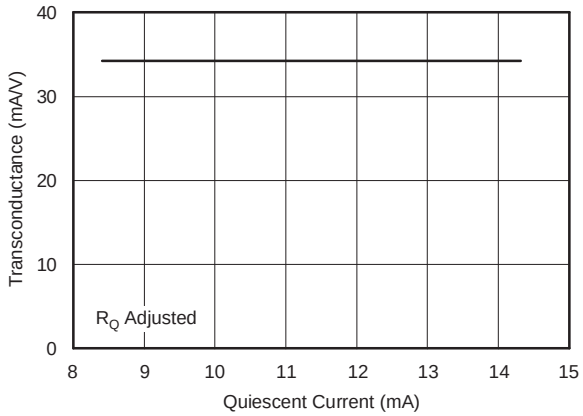


Figure 20.

SOTA TRANSCONDUCTANCE vs INPUT VOLTAGE

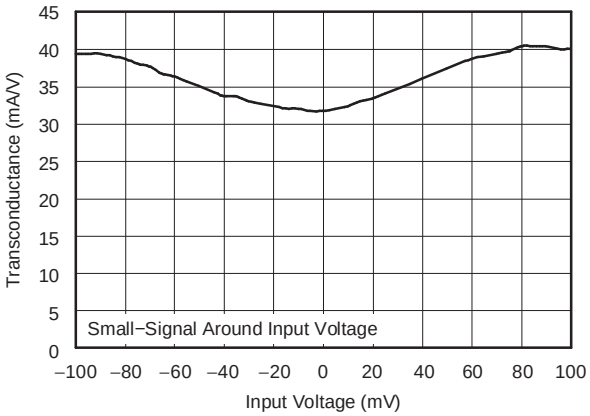


Figure 21.

SOTA TRANSFER CHARACTERISTICS

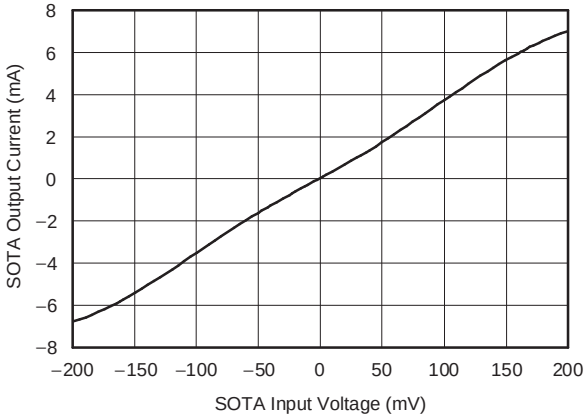


Figure 22.

SOTA PULSE RESPONSE

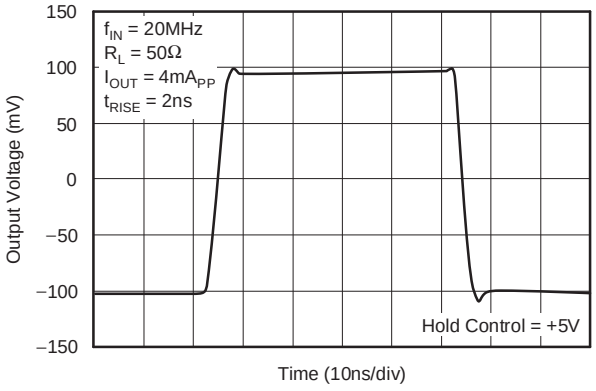


Figure 23.

SOTA PULSE RESPONSE

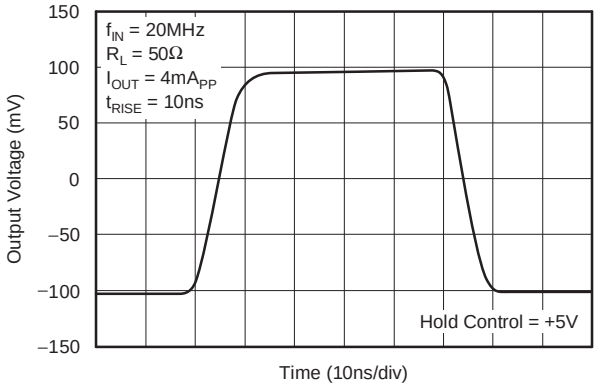


Figure 24.

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C and I_Q = 13mA, unless otherwise noted.

SOTA PROPAGATION DELAY vs OVERDRIVE

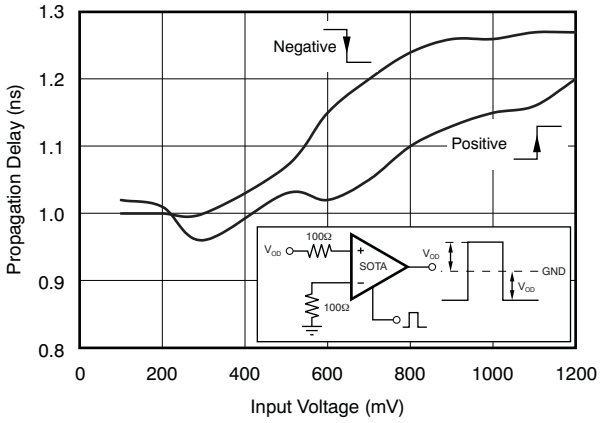


Figure 25.

SOTA PROPAGATION DELAY vs TEMPERATURE

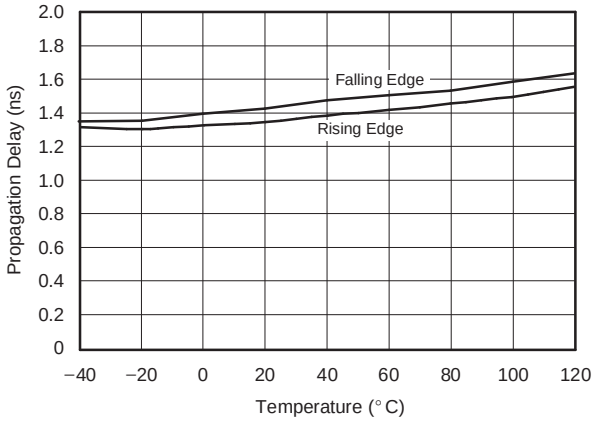


Figure 26.

SOTA PROPAGATION DELAY vs SLEW RATE

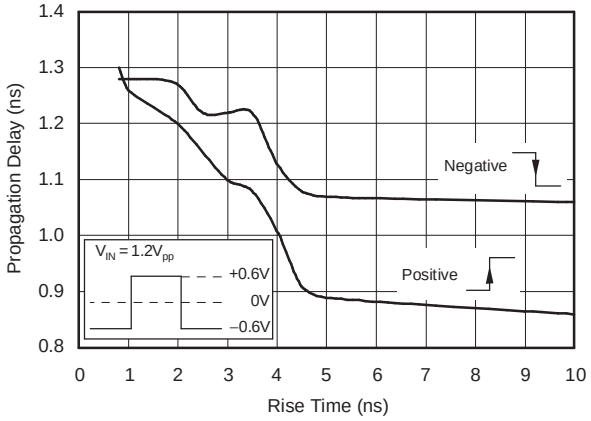


Figure 27.

SOTA SWITCHING TRANSIENTS

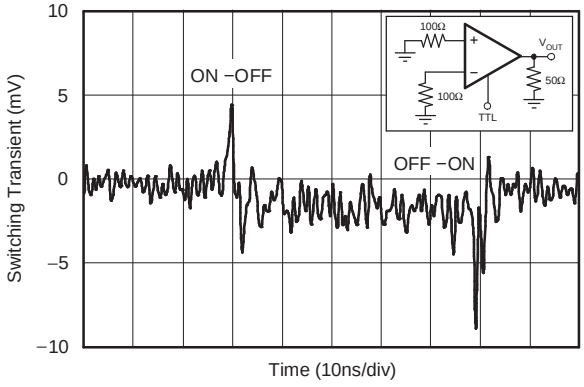


Figure 28.

SOTA HOLD COMMAND DELAY TIME

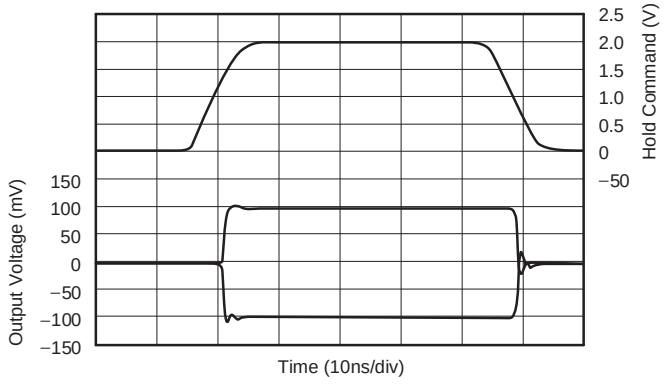


Figure 29.

SOTA BANDWIDTH vs OUTPUT CURRENT SWING

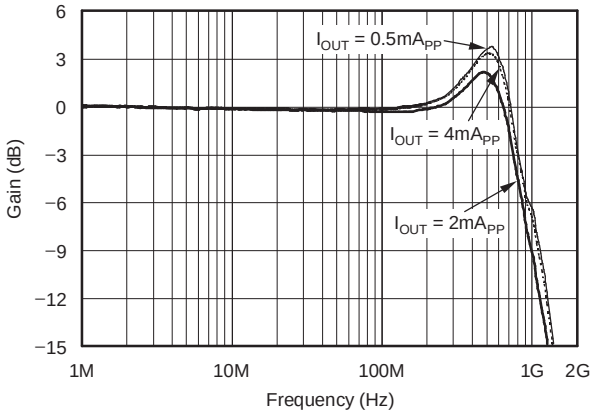


Figure 30.

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C and I_Q = 13mA, unless otherwise noted.

SOTA FEEDTHROUGH REJECTION vs FREQUENCY

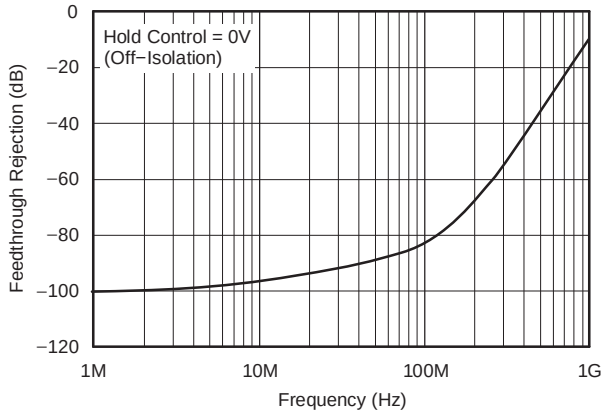


Figure 31.

SOTA COMMON-MODE REJECTION vs FREQUENCY

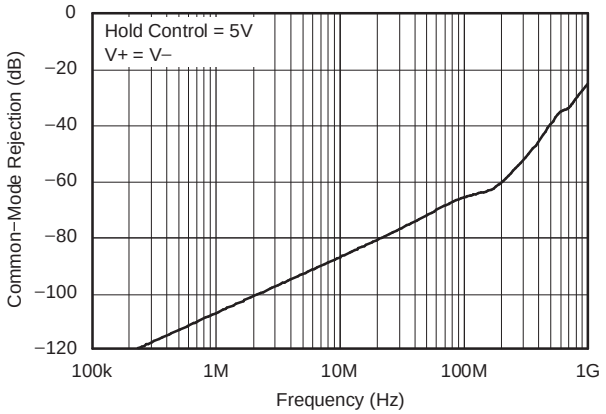


Figure 32.

SOTA INPUT BIAS CURRENT vs TEMPERATURE

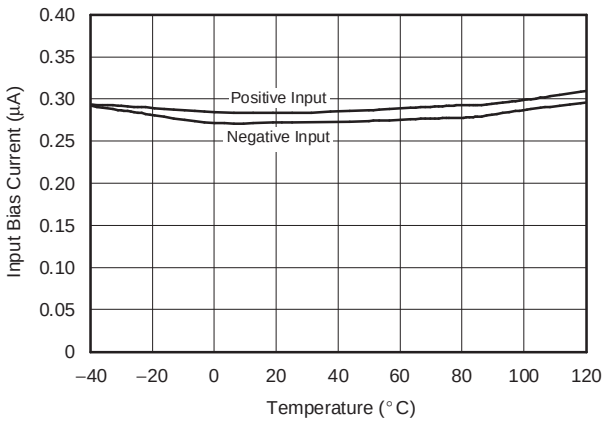


Figure 33.

SOTA OUTPUT BIAS CURRENT vs TEMPERATURE

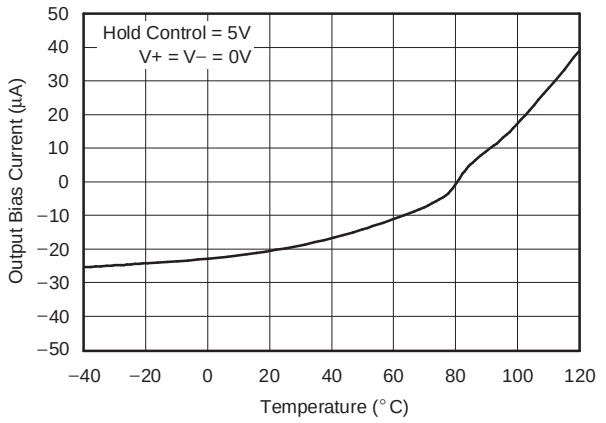


Figure 34.

DISCUSSION OF PERFORMANCE

The OPA615, which contains a wideband Operational Transconductance Amplifier (OTA) and a fast sampling comparator (SOTA), represents a complete subsystem for very fast and precise DC restoration, offset clamping and correction to GND or to an adjustable reference voltage, and low frequency hum suppression of wideband operational or buffer amplifiers.

Although the IC was designed to improve or stabilize the performance of complex, wideband video signals, it can also be used as a sample-and-hold amplifier, high-speed integrator, peak detector for nanosecond pulses, or as part of a correlated double sampling system. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and a fast and precise sampling comparator sets a new standard for high-speed sampling applications.

Both the OTA and the sampling comparator can be used as stand-alone circuits or combined to create more complex signal processing stages such as sample-and-hold amplifiers. The OPA615 simplifies the design of input amplifiers with high hum suppression; clamping or DC-restoration stages in professional broadcast equipment, high-resolution CAD monitors and information terminals; and signal processing stages for the energy and peak value of nanoseconds pulses. This device also eases the design of high-speed data acquisition systems behind a CCD sensor or in front of an analog-to-digital converter (ADC).

An external resistor on the SO-14 package, R_Q, allows the user to set the quiescent current. R_Q is connected from Pin 1 (I_Q adjust) to $-V_{CC}$. It determines the operating currents of the OTA section and controls the bandwidth and AC behavior as well as the transconductance of the OTA.

Besides the quiescent current setting feature, a Proportional-to-Absolute-Temperature (PTAT) supply current control will increase the quiescent current versus temperature. This variation holds the transconductance (g_m) of the OTA and comparator relatively constant versus temperature. The circuit parameters listed in the specification table are measured with R_Q set to 300Ω, giving a nominal quiescent current at 13mA. While not always shown in the application circuits, this R_Q = 300Ω is required to get the 13mA quiescent operating current.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) SECTION

OVERVIEW

The symbol for the OTA section is similar to that of a bipolar transistor, and the self-biased OTA can be viewed as either a quasi-ideal transistor or as a voltage-controlled current source. Application circuits for the OTA look and operate much like transistor circuits—the bipolar transistor is also a voltage-controlled current source. Like a transistor, it has three terminals: a high-impedance input (base) optimized for a low input bias current of 0.3µA, a low-impedance input/output (emitter), and the high-impedance current output (collector).

The OTA consists of a complementary buffer amplifier and a subsequent complementary current mirror. The buffer amplifier features a Darlington output stage and the current mirror has a cascoded output. The addition of this cascode circuitry increases the current source output resistance to 1.2MΩ. This feature improves the OTA linearity and drive capabilities. Any bipolar input voltage at the high impedance base has the same polarity and signal level at the low impedance buffer or emitter output. For the open-loop diagrams, the emitter is connected to GND; the collector current is then determined by the voltage between base and emitter times the transconductance. In application circuits (Figure 36b), a resistor R_E between the emitter and GND is used to set the OTA transfer characteristics.

The following formulas describe the most important relationships. r_e is the output impedance of the buffer amplifier (emitter) or the reciprocal of the OTA transconductance. Above ±5mA, the collector current, I_C, will be slightly less than indicated by the formula.

$$I_C = \frac{V_{IN}}{r_E + R_E} \quad \textit{or} \quad R_E = \frac{V_{IN}}{I_C} - r_E \tag{1}$$

The R_E resistor may be bypassed by a relatively large capacitor to maintain high AC gain. The parallel combination of R_E and this large capacitor form a high-pass filter, enhancing the high frequency gain. Other cases may require an RC compensation network in parallel to R_E to optimize the high-frequency response. The large-signal bandwidth (V_O = 1.4V_{PP}) measured at the emitter achieves 770MHz. The frequency response of the collector is directly related to the resistor value between the collector and GND; it decreases with increasing resistor values, because of the low-pass filter formed with the OTA C-output capacitance.

Figure 35 shows a simplified block diagram of the OPA615 OTA. Both the emitter and the collector outputs offer a drive capability of ±20mA for driving low impedance loads. The emitter output is not current-limited or protected. Momentary shorts to GND should be avoided, but are unlikely to cause permanent damage.

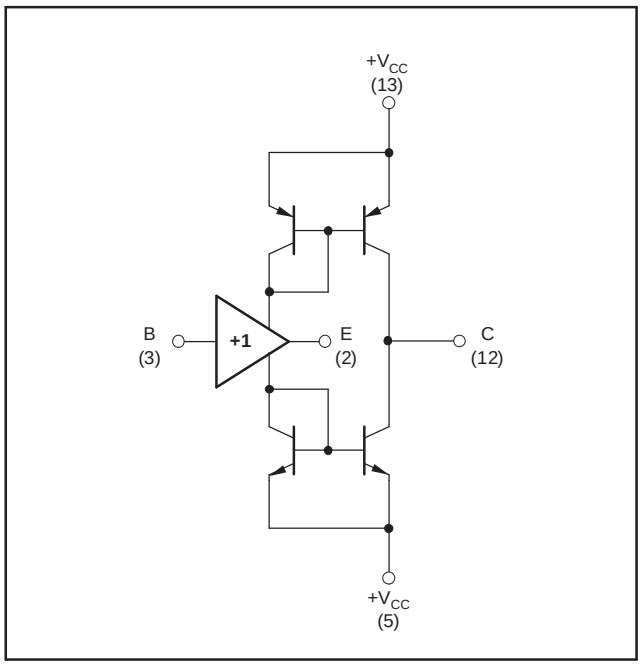


Figure 35. Simplified OTA Block Diagram

While the OTA function and labeling appear similar to those of a transistor, it offers essential distinctive differences and improvements: 1) The collector current flows out of the C terminal for a positive B-to-E input voltage and into it for negative voltages; 2) A common emitter amplifier operates in non-inverting mode while the common base operates in inverting mode; 3) The OTA is far more linear than a bipolar transistor; 4) The transconductance can be adjusted with an external resistor; 5) As a result of the PTAT biasing characteristic, the quiescent current increases as shown in the typical performance curve vs temperature and keeps the AC performance constant; 6) The OTA is self-biased and bipolar; and 7) The output current is approximately zero for zero differential input voltages. AC inputs centered on zero produce an output current centered on zero.

BASIC APPLICATION CIRCUITS

Most application circuits for the OTA section consist of a few basic types which are best understood by analogy to discrete transistor circuits. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes; common-E, common-B, and common-C (see Figure 36, Figure 37 and Figure 38). Figure 36 shows the OTA connected as a Common-E amplifier, which is equivalent to a common emitter transistor amplifier. Input and output can be ground-referenced without any biasing. The amplifier is noninverting because a current flowing out of the emitter will also flow out of the collector as a result of the current mirror shown in Figure 35.

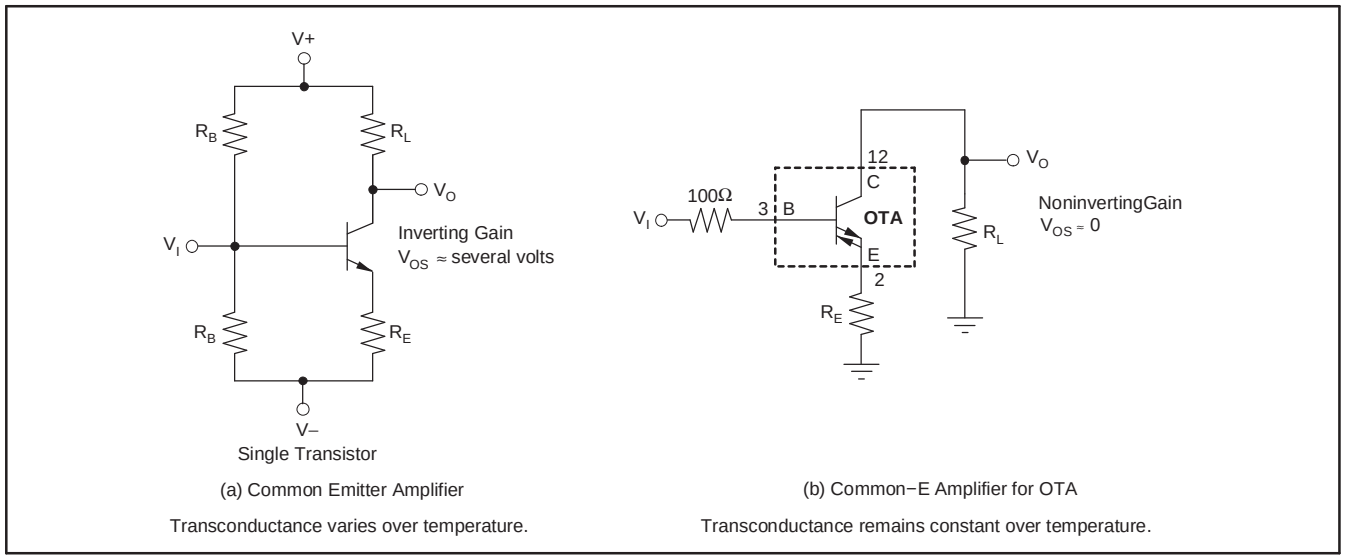


Figure 36. a) Common Emitter Amplifier Using a Discrete Transistor; b) Common-E Amplifier Using the OTA Portion of the OPA615

Figure 37 shows the Common-C amplifier. It constitutes an open-loop buffer with low offset voltage. Its gain is approximately 1 and will vary with the load.

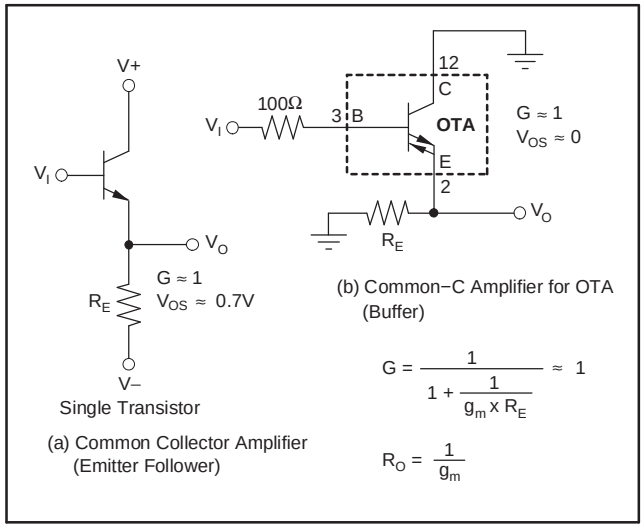


Figure 37. a) Common Collector Amplifier Using a Discrete Transistor; b) Common-C Amplifier Using the OTA Portion of the OPA615

Figure 38 shows the Common-B amplifier. This configuration produces an inverting gain, and the input is low-impedance. When a high impedance input is needed, it can be created by inserting a buffer amplifier (such as the BUF602) in series.

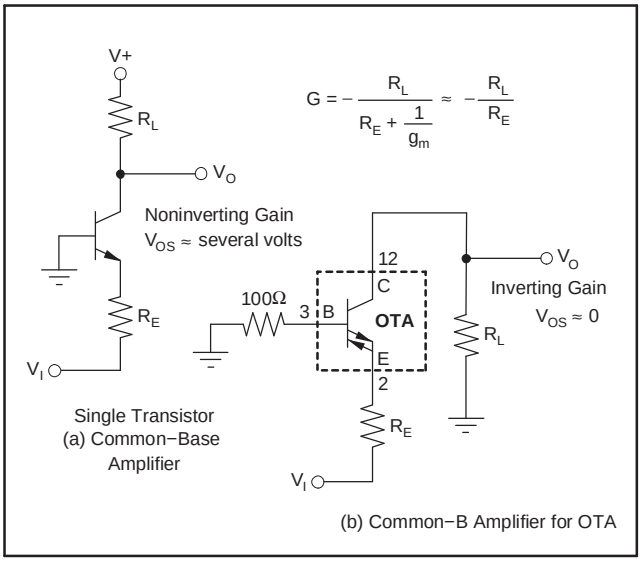


Figure 38. a) Common Base Amplifier Using a Discrete Transistor; b) Common-B Amplifier Using the OTA Portion of the OPA615

SAMPLING COMPARATOR

The OPA615 sampling comparator features a very short switching (2.5ns) propagation delay and utilizes a new switching circuit architecture to achieve excellent speed and precision.

It provides high impedance inverting and noninverting analog inputs, a high-impedance current source output and a TTL-CMOS-compatible Hold Control Input.

The sampling comparator consists of an operational transconductance amplifier (OTA), a buffer amplifier, and a subsequent switching circuit. This combination is subsequently referred to as the Sampling Operational Transconductance Amplifier (SOTA). The OTA and buffer amplifier are directly tied together at the buffer outputs to provide the two identical high-impedance inputs and high open-loop transconductance. Even a small differential input voltage multiplied with the high transconductance results in an output current—positive or negative—depending upon the input polarity. This characteristic is similar to the low or high status of a conventional comparator. The current source output features high output impedance, output bias current compensation, and is optimized for charging a capacitor in DC restoration, nanosecond integrators, peak detectors and S/H circuits. The typical comparator output current is ±5mA and the output bias current is minimized to typically ±10µA in the sampling mode.

This innovative circuit achieves the high slew rate representative of an open-loop design. In addition, the acquisition slew current for a hold or storage capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

The switching circuits in the OPA615 use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This design results in low aperture time sensitivity to the analog input signal, reduced power supply and analog switching noise. Sample-to-hold peak switching charge injection is 40fC.

The additional offset voltage or switching transient induced on a capacitor at the current source output by the switching charge can be determined by the following formula:

$$\text{Offset (V)} = \frac{\text{Charge (pC)}}{C_H\text{Total (pF)}} \quad (2)$$

The switching stage input is insensitive to the low slew rate performance of the hold control command and compatible with TTL/CMOS logic levels. With TTL logic high, the comparator is active, comparing the two input voltages and varying the output current accordingly. With TTL logic low, the comparator output is switched off, showing a very high impedance to the hold capacitor.

DESIGN-IN TOOLS

Demonstration Fixture

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA615. The demonstration fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 2.

Table 2. OPA615 Demonstration Fixtures

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA615ID	SO-14	DEM-OPA-SO-1C	SBOU039
OPA615IDGS	MSOP-10	DEM-OPA-MSOP-1A	SBOU042

The demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA615 product folder.

Macromodel and Applications Support

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA615 is available through the TI web page (www.ti.com). This model predicts typical small-signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The model includes the noise terms found in the electrical specifications of the data sheet. However, the model does not attempt to distinguish between package types in their small-signal AC performance. The applications department is also available for design assistance.

APPLICATION INFORMATION

The OPA615 operates from ±5V power supplies (±6.2V maximum). Absolute maximum is ±6.5V. Do not attempt to operate with larger power supply voltages or permanent damage may occur.

BASIC CONNECTIONS

Figure 39 shows the basic connections required for operation. These connections are not shown in subsequent circuit diagrams.

Power-supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See *Board Layout* at the end of the applications discussion for further suggestions on layout.

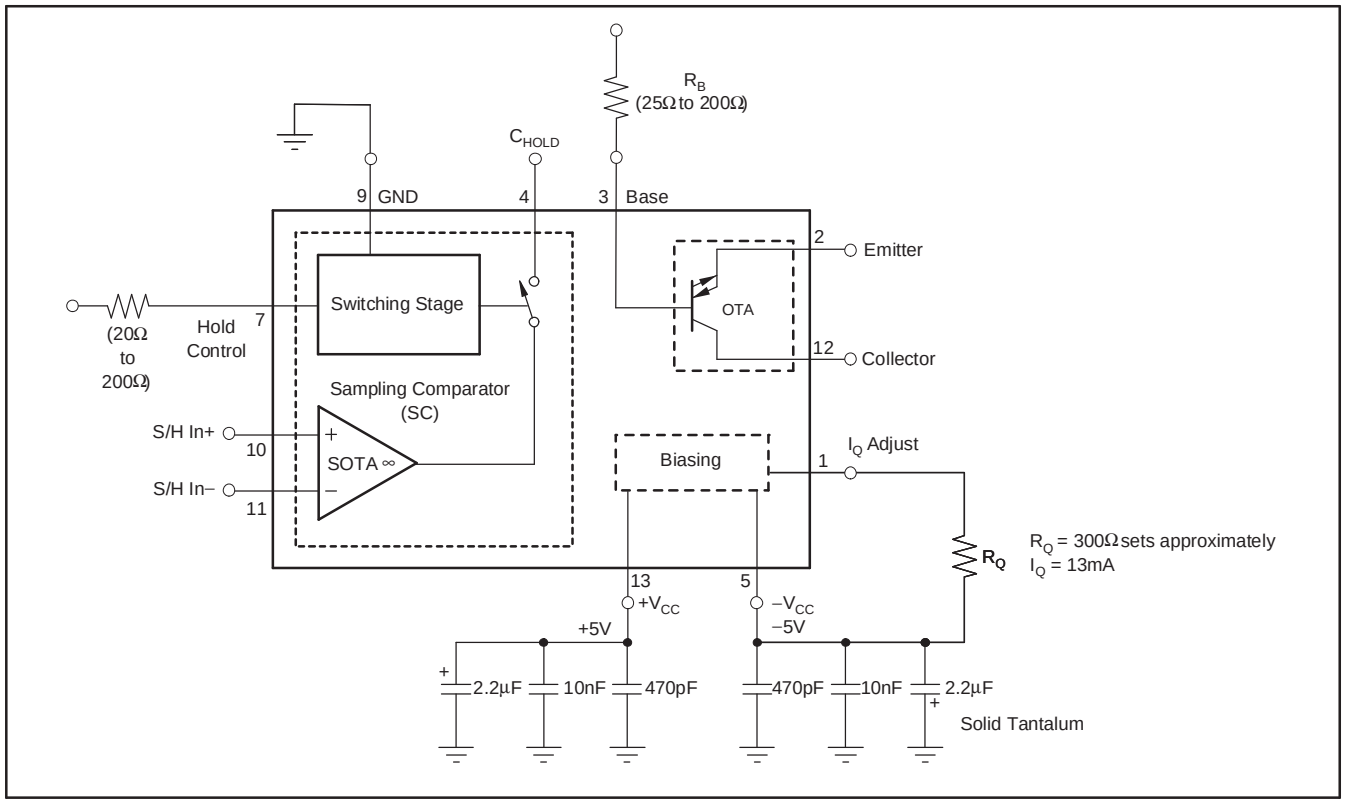


Figure 39. Basic Connections

DC-RESTORE SYSTEM

Figure 40 and Figure 41 offer two possible DC-restore systems using the OPA615. Figure 41 implements a DC-restore function as a unity-gain amplifier. As can be expected from its name, this DC-restore circuit does not provide any amplification.

In applications where some amplification is needed, consider using the circuit design shown in Figure 40.

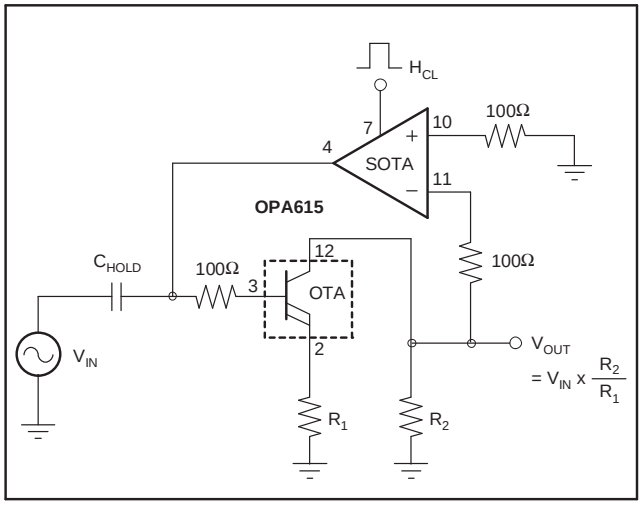


Figure 40. Complete DC Restoration System

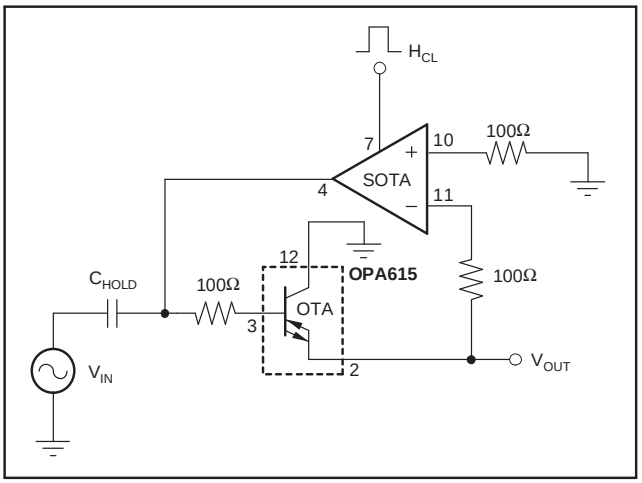


Figure 41. DC Restoration of a Buffer Amplifier

For either of these circuits to operate properly, the source impedance needs to be low, such as the one provided by the output of a closed-loop amplifier or buffer. Consider the video input signal shown in Figure 42, and the complete DC restoration system shown in Figure 40. This signal is amplified by the OTA section of the OPA615 by a gain of:

$$G = +\frac{R_2}{R_1}$$

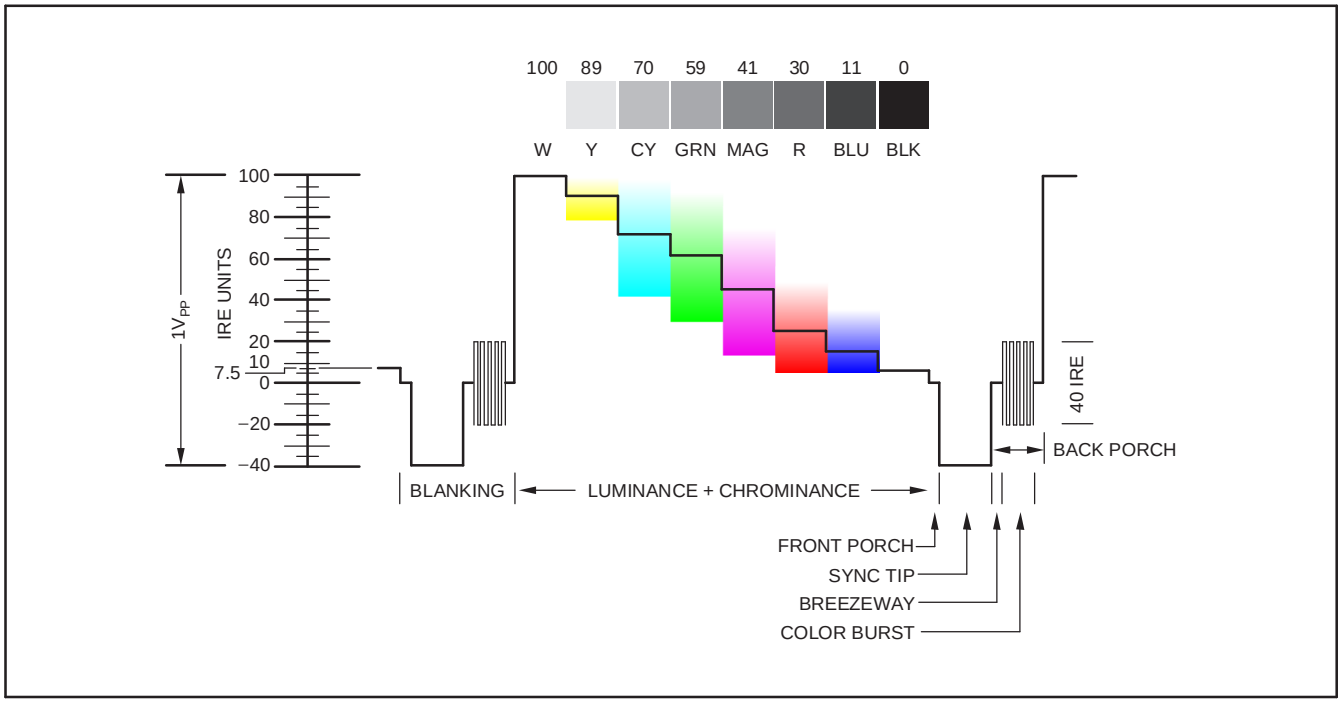


Figure 42. NTSC Horizontal Scan Line

The DC restoration is done by the SOTA section by sampling the output signal at an appropriate time. The sampled section of the signal is then compared to a reference voltage that appears on the non-inverting input of the SOTA (pin 10), or ground in Figure 40.

When the SOTA is sampling, it is charging or discharging the C_{HOLD} capacitor depending on the level of the output signal sampled. The detail of an appropriate timing is illustrated in Figure 43.

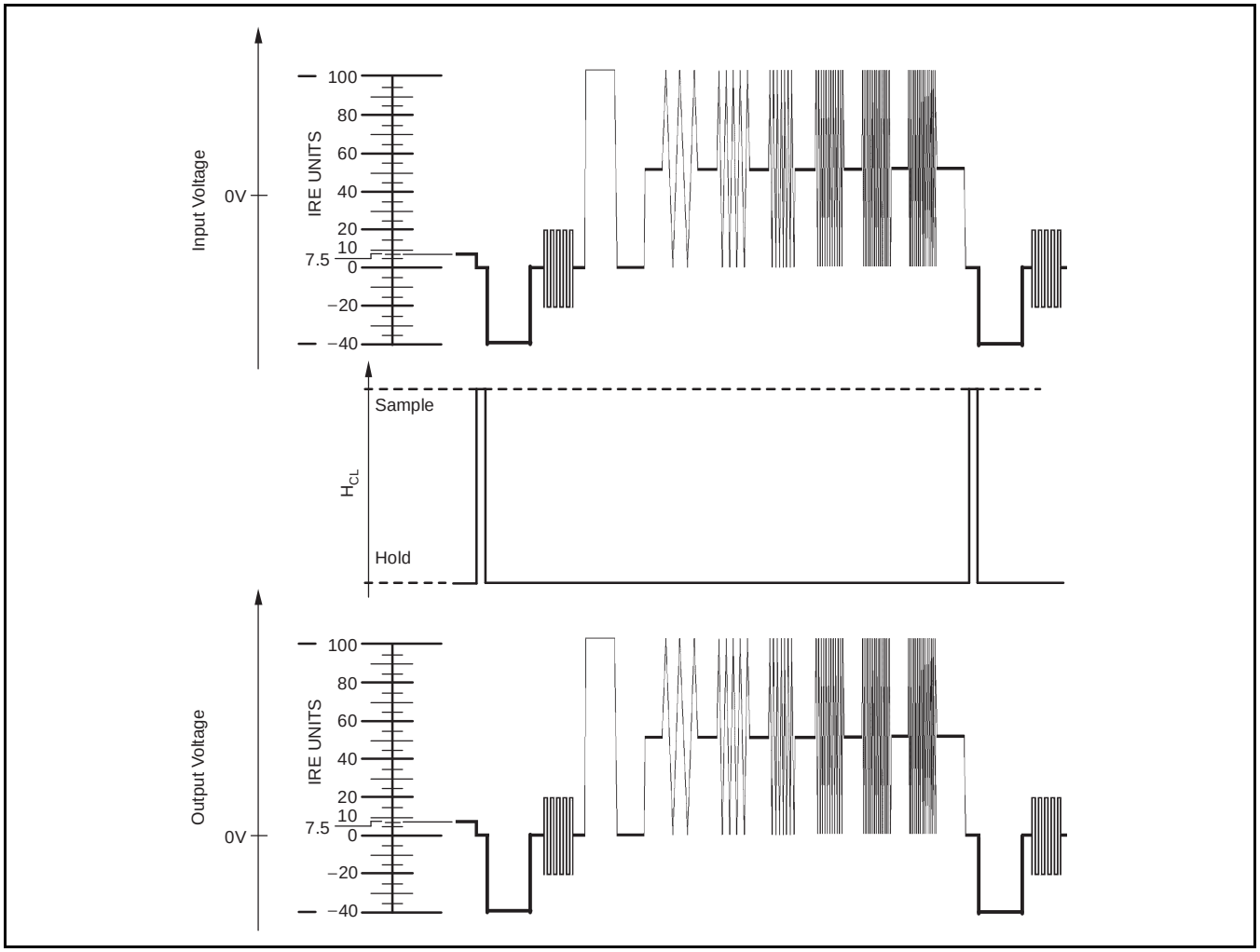


Figure 43. DC-Restore Timing

CLAMPED VIDEO/RF AMPLIFIER

Another circuit example for the preamplifier and the clamp circuit is shown in Figure 44. The preamplifier uses the wideband, low noise OPA656, again configured in a gain of +2V/V. Here, the OPA656 has a typical bandwidth of 200MHz with a settling time of about 21ns (0.02%) and offers a low bias current JFET input stage.

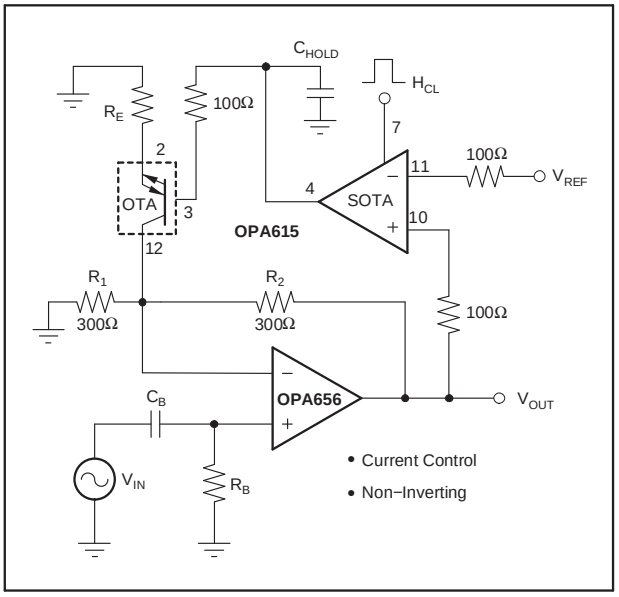


Figure 44. Clamped Video/RF Amplifier

The video signal passes through the capacitor C_B, blocking the DC component. To restore the DC level to the desired baseline, the OPA615 is used. The inverting input (pin 11) is connected to a reference voltage. During the high time of the clamp pulse, the switching comparator (SOTA) will compare the output of the op amp to the reference level. Any voltage difference between those pins will result in an output current that either charges or discharges the hold capacitor, C_{HOLD}. This charge creates a voltage across the capacitor, which is buffered by the OTA. Multiplied by the transconductance, the voltage will cause a current flow in the collector, C, terminal of the OTA. This current will level-shift the OPA656 up to the point where its output voltage is equal to the reference voltage. This level-shift also closes the control loop. Because of the buffer, the voltage across the C_{HOLD} stays constant and maintains the baseline correction during the off-time of the clamp pulse.

The external capacitor (C_{HOLD}) allows for a wide range of flexibility. By choosing small values, the circuit can be optimized for a short clamping period or with high values for a low droop rate. Another advantage of this circuit is that small clamp peaks at the output of the switching comparator are integrated and do not cause glitches in the signal path.

SAMPLE-AND-HOLD AMPLIFIER

With a control propagation delay of 2.5ns and 730MHz bandwidth, the OPA615 can be used advantageously in a high-speed sample-and-hold amplifier. Figure 45 illustrates this configuration.

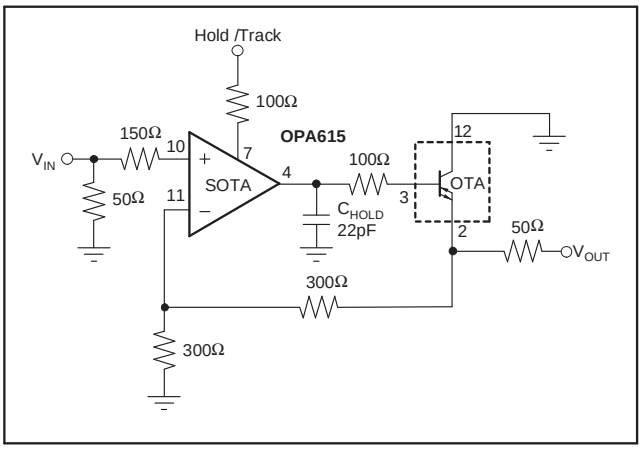


Figure 45. Sample-and-Hold Amplifier

To illustrate how the digitization is realized in the Figure 45 circuit, Figure 46 shows a 100kHz sinewave being sampled at a rate of 1MHz. The output signal used here is the I_{OUT} output driving a 50Ω load.

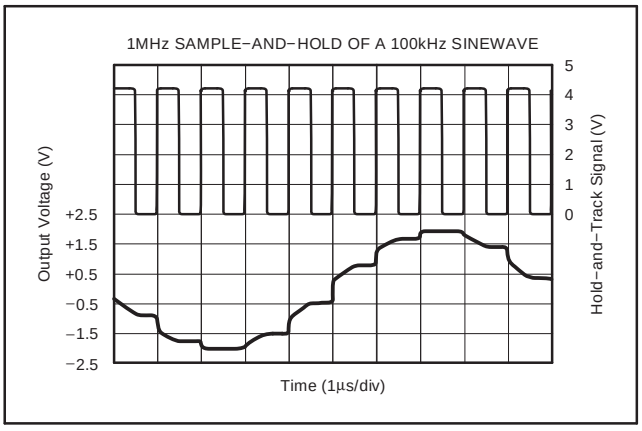


Figure 46. 1MHz Sample-and-Hold of a 100kHz Sine Wave

Integrator for ns-Pulses

The integrator for ns-pulses using the OPA615 (shown in Figure 47) makes use of the fast comparator and its current-mode output. Placing the hold-control high, a narrow pulse charges the capacitor, increasing the average output voltage. To minimize ripples at the inverting input and maximize the capacitor charge, a T-network is used in the feedback path.

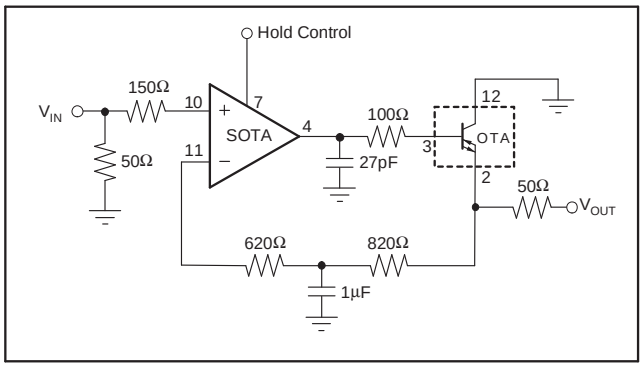


Figure 47. Integrator for ns-Pulses

Fast Pulse Peak Detector

A circuit similar to that shown in Figure 47 (the integrator for ns-pulses) can be devised to detect and isolate positive pulses from negative pulses. This circuit, shown in Figure 48, uses the OPA615 as well as the BUF602. This circuit makes use of diodes to isolate the positive-going pulses from the negative-going pulses and charge-different capacitors.

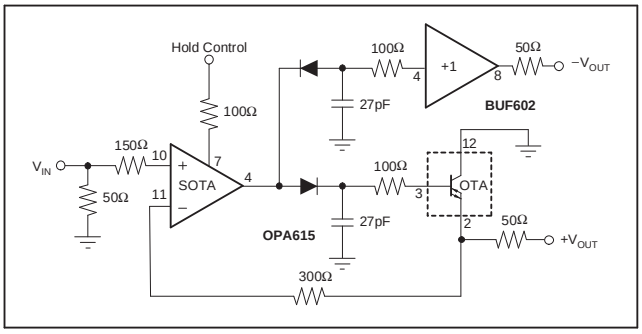


Figure 48. Fast Bipolar Peak Detector

Phase Detector for Fast PLL Systems

Figure 49 shows the circuit for a phase detector for fast PLL systems. Given a reference pulse train f_{REF} and a pulse train input signal f_{IN} out of phase, the SOTA of the OPA615 acts in this circuit as a comparator, either charging or discharging the capacitor. This voltage is then buffered by the OTA and fed to the VCO.

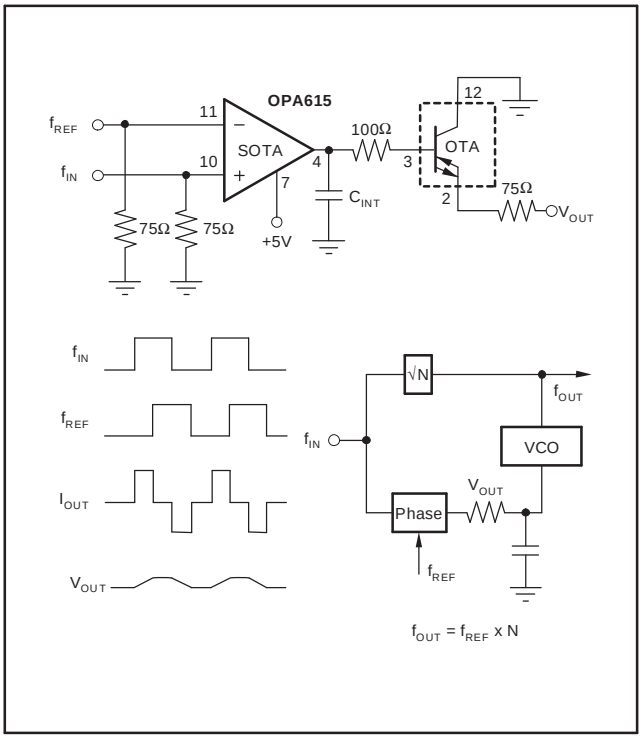


Figure 49. Phase Detector For Fast PLL-Systems

CORRELATED DOUBLE SAMPLER

Noise is the limiting factor for the resolution in a CCD system, where the kT/C noise is dominant (see Figure 51). To reduce this noise, imaging systems use a circuit called a *Correlated Double Sampler* (CDS). The name comes from the double sampling technique of the CCD charge signal. A CDS using two OPA615s and one OPA694 is shown in Figure 50. The first sample (S_1) is taken at the end of the reset period. When the reset switch opens again, the effective noise bandwidth changes because of the large difference in the switch R_{ON} and R_{OFF} resistance. This difference causes the dominating kT/C noise essentially to *freeze* in its last point.

The other sample (S_2) is taken during the video portion of the signal. Ideally, the two samples differ only by a voltage corresponding to the transferred charge signal. This is the video level minus the noise (ΔV).

The CDS function will eliminate the kT/C noise as well as much of the 1/f and white noise.

Figure 52 is a block diagram of a CDS circuit. Two sample-and-hold amplifiers and one difference amplifier constitute the correlated double sampler.

The signal coming from the CCD is applied to the two sample-and-hold amplifiers, with their outputs connected to the difference amplifier. The timing diagram clarifies the operation (see Figure 52). At time t_1, the sample and hold (S/H_1) goes into the hold mode, taking a sample of the reset level including the noise. This voltage (V_{RESET}) is applied to the noninverting input of the difference amplifier. At time t_2, the sample-and-hold (S/H_2) will take a sample of the video level, which is $V_{RESET} – V_{VIDEO}$. The output voltage of the difference amplifier is defined by the equation $V_{OUT} = V_{IN+} – V_{IN–}$. The sample of the reset voltage contains the kT/C noise, which is eliminated by the subtraction of the difference amplifier.

The double sampling technique also reduces the white noise. The white noise is part of the reset voltage (V_{RESET}) as well as of the video amplitude ($V_{RESET} – V_{VIDEO}$). With the assumption that the noise of the noise of the second sample was unchanged from the instant of the first sample, the noise amplitudes are the same and are correlated in time. Therefore, the noise can be reduced by the CDS function.

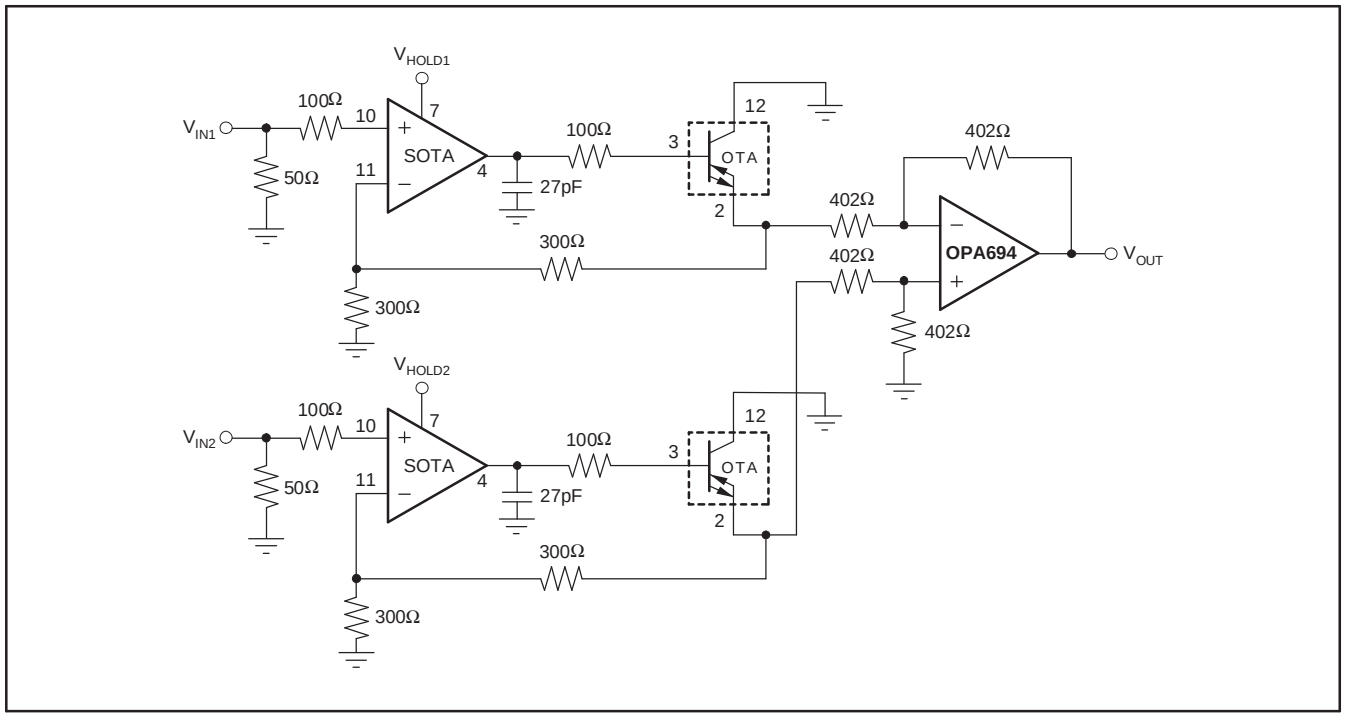


Figure 50. Correlated Double Sampler

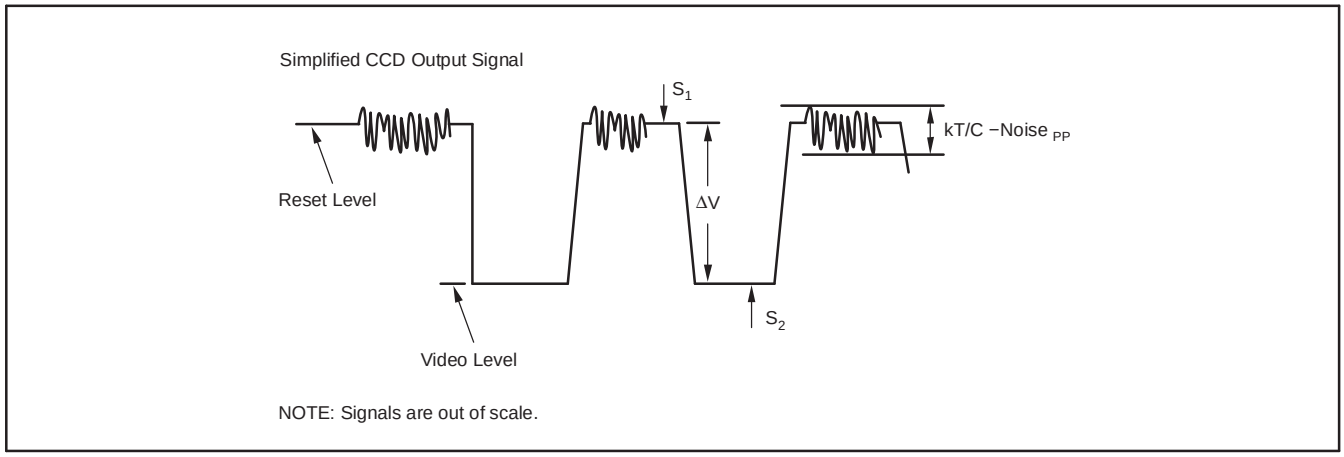


Figure 51. Improving SNR with Correlated Double Sampling

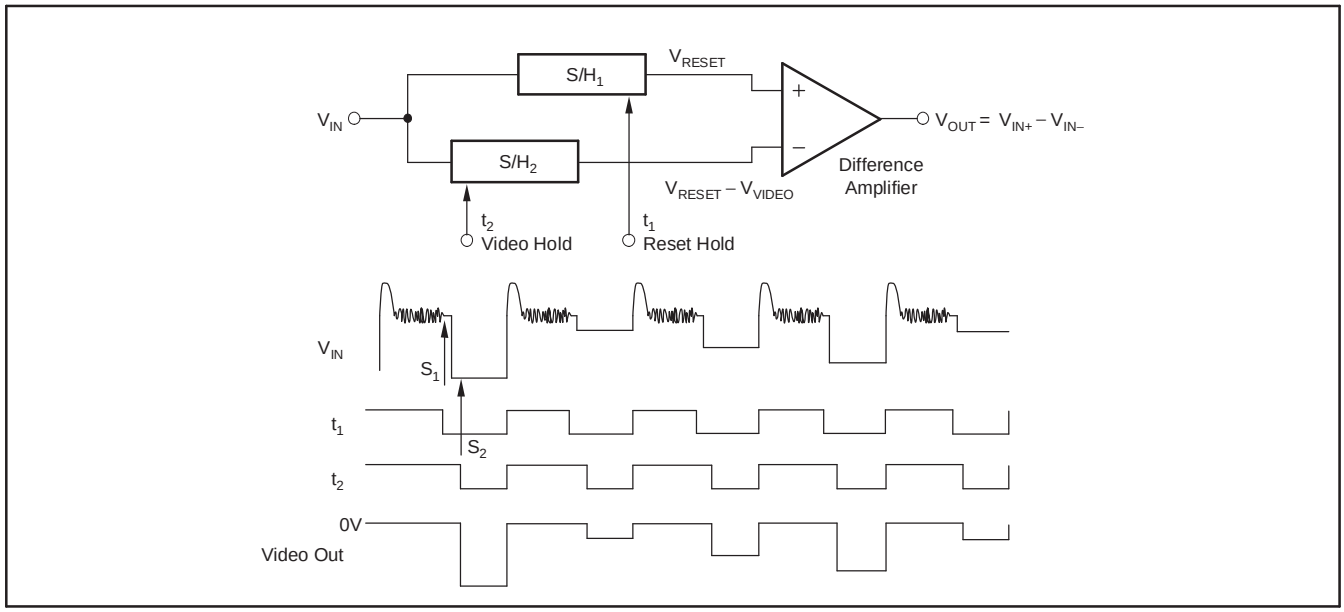


Figure 52. CDS: Circuit Concept

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA615 requires careful attention to printed circuit board (PCB) layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply-decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at a lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA615. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep these leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high frequency application. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them.

e) Socketing a high-speed part such as the OPA615 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA615 directly onto the PCB.

INPUT AND ESD PROTECTION

The OPA615 is built using a very high-speed, complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table where an absolute maximum ±6.5V supply is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 53.

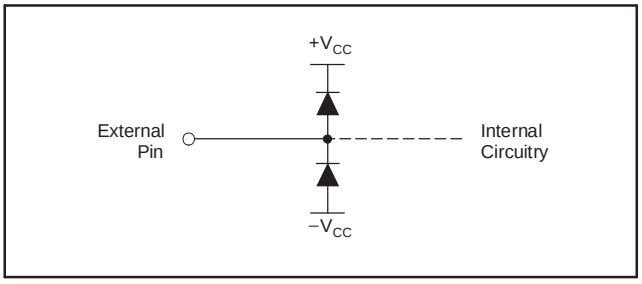


Figure 53. Internal ESD Protection

These diodes also provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA615), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2008) to Revision E **Page**

- Corrected y-axis title of Figure 25 10

Changes from Revision C (October 2006) to Revision D **Page**

- Changed rating for storage temperature range in Absolute Maximum Ratings table from –40°C to +125°C to –65°C to +125°C 2
- Clarified hold control pin voltage rating in Absolute Maximum Ratings table 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA615ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA615ID
OPA615ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA615ID
OPA615IDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BJT
OPA615IDGST.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BJT
OPA615IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA615ID
OPA615IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA615ID

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

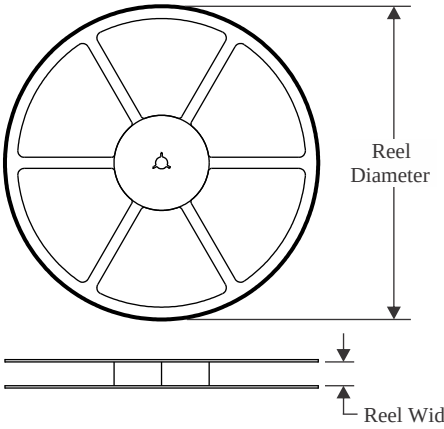
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

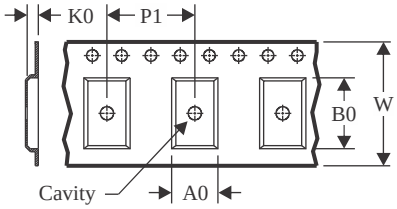
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

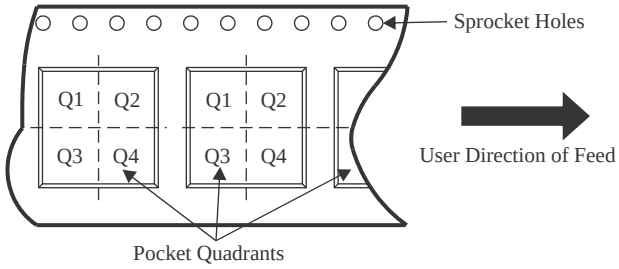


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

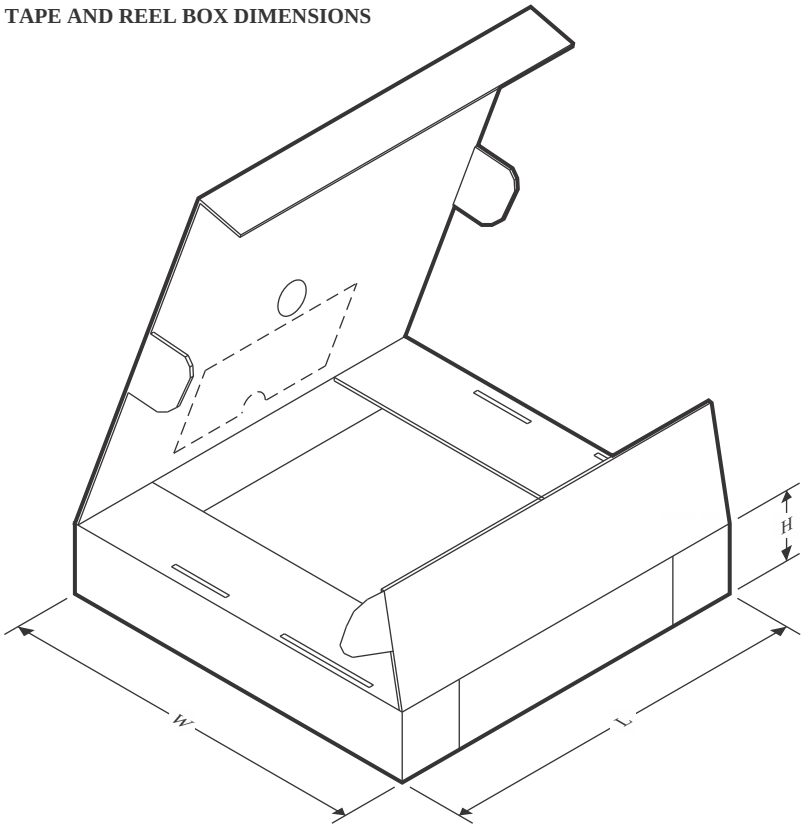
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA615IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA615IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

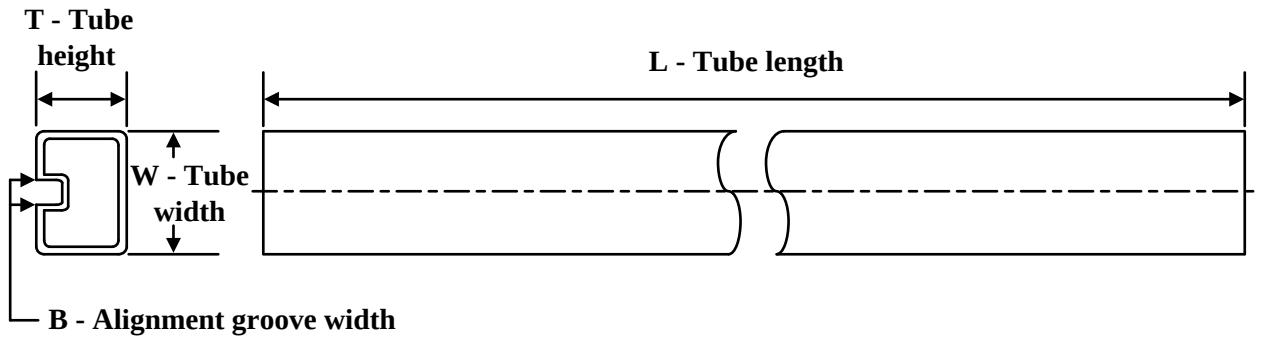
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

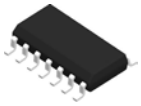
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA615IDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
OPA615IDR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA615ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA615ID.A	D	SOIC	14	50	506.6	8	3940	4.32

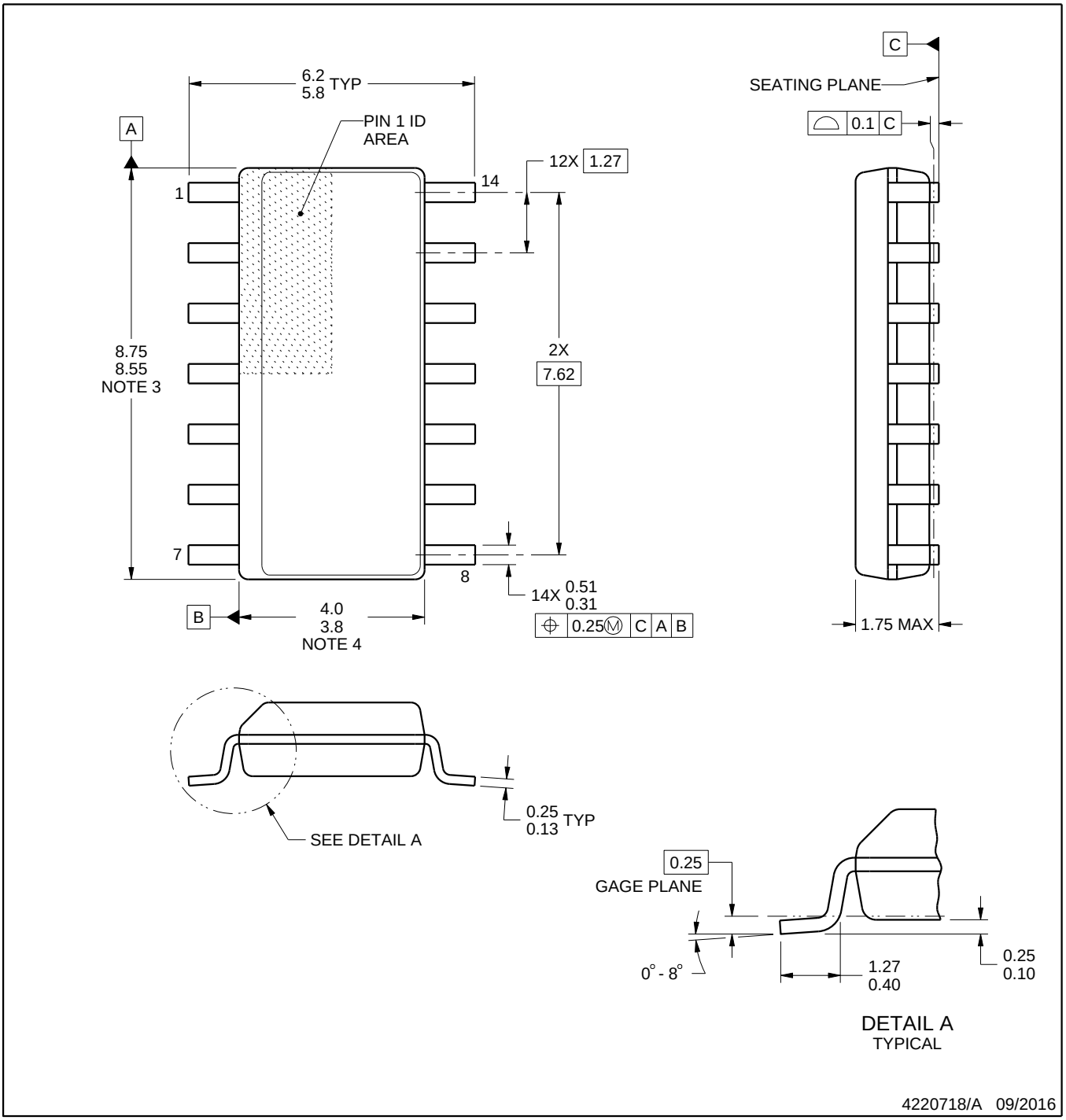


PACKAGE OUTLINE

D0014A

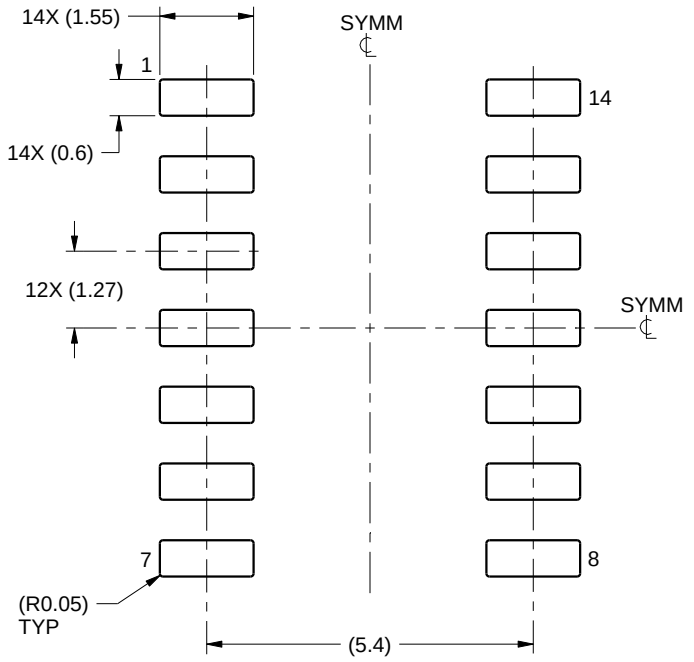
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

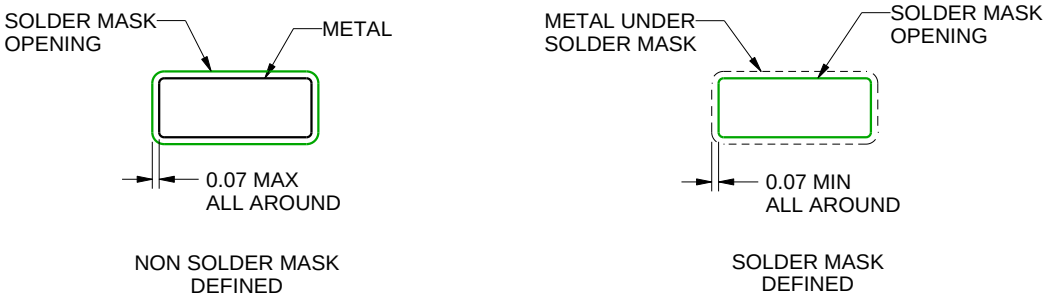


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

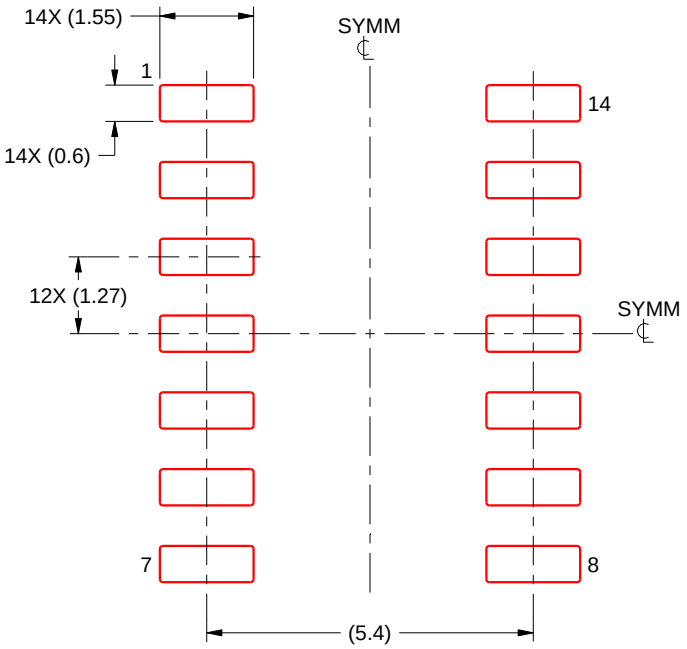
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

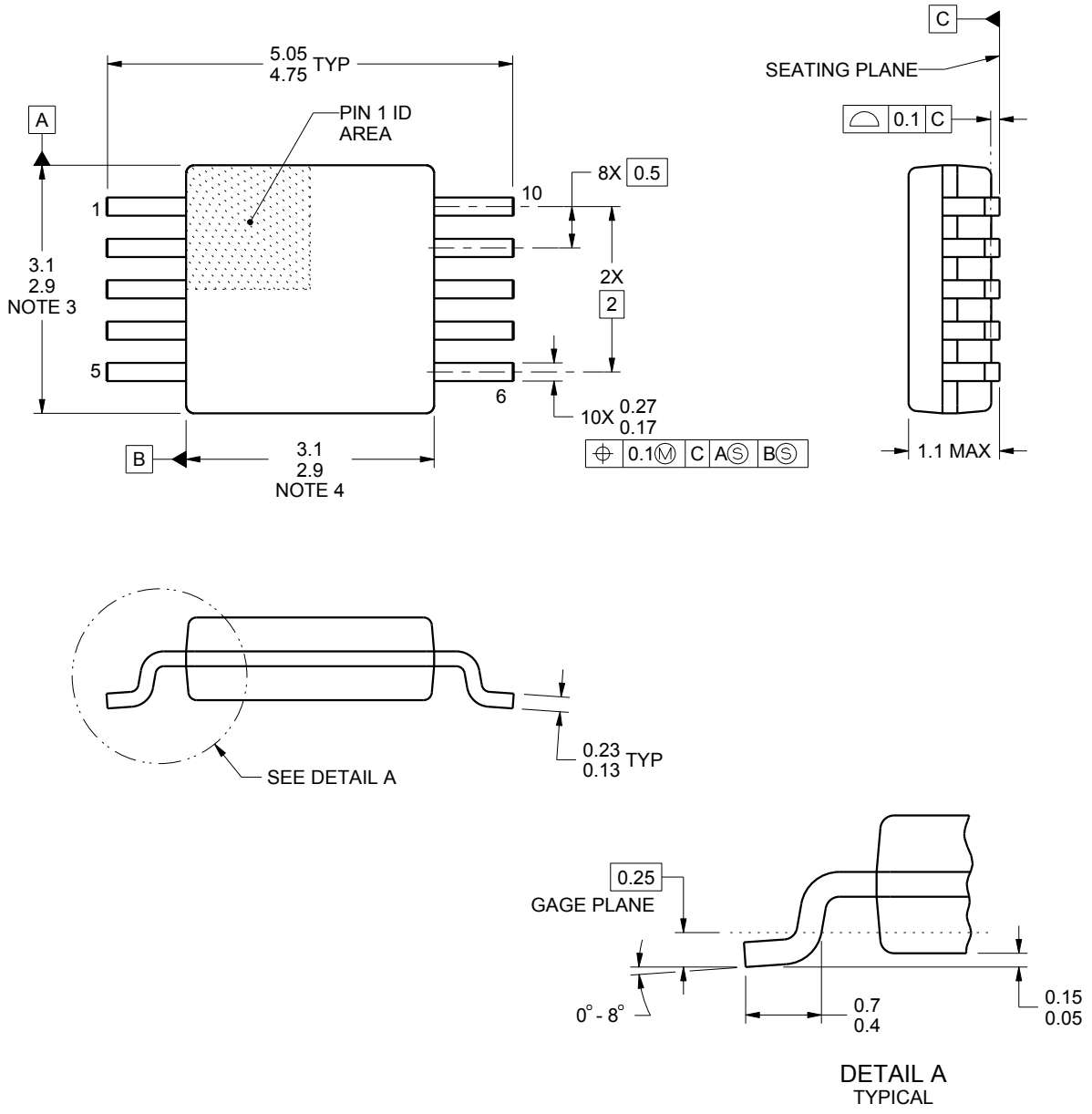
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

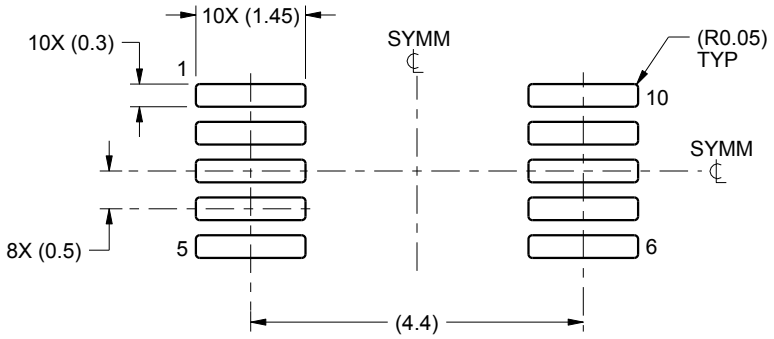
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

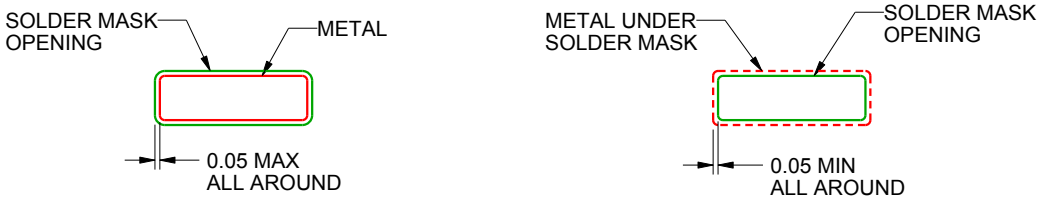


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

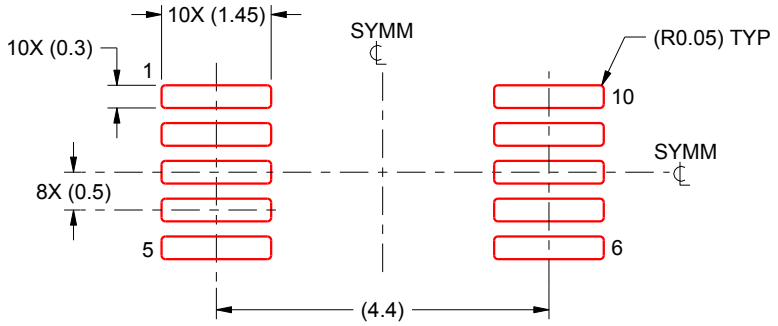


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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