PCA9544A 低電圧、4 チャネル、割り込みロジック搭載の I²C および SMBus マルチプレクサ

1 特長

- 1 対 4 の双方向変換スイッチ
- I²C バスおよび SMBus 互換
- 4 つのアクティブ LOW 割り込み入力
- アクティブ LOW の割り込み出力
- 3 本のアドレス・ピンにより、最大 8 個のデバイスを I²C バスに接続可能
- I²C バスによるチャネル選択
- 電源オン時にすべてのスイッチ・チャネルの接続解除
- 低い R_{ON} のスイッチ
- 1.8V、2.5V、3.3V、5V の各電圧のバス間での電圧レベル変換
- 電源オン時のグリッチなし
- 活線挿抜をサポート
- 小さいスタンバイ電流
- 2.3V～5.5V の動作電源電圧範囲
- 5.5V 許容の入力
- 0～400kHz のクロック周波数
- JESD 78 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン・モデル (A115-A)
  - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- サーバー
- ルーター (テレコム・スイッチング機器)
- ファクトリ・オートメーション
- I²C スレーブ・アドレス競合がある製品 (複数の同一温度センサなど)

3 概要

PCA9544A は、I²C バスで制御される 4 チャネル双方向変換マルチプレクサです。SCL/SDA 上流ペアが、4 つの下流ペア (チャネル) に展開されます。同時に選択可能な SCL/SDA ペアは 1 つで、プログラム可能な制御レジスタの値によって決定されます。4 つの割り込み入力 ($\overline{INT3}$～$\overline{INT0}$、各下流ペアに 1 つ) を備えています。1 つの割り込み出力 ($\overline{INT}$) が 4 つの割り込み入力の論理積として機能します。

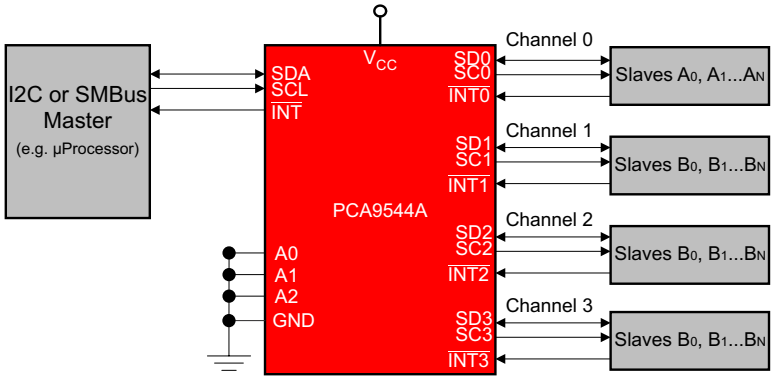
パワー・オン・リセット機能により、レジスタはデフォルト状態に戻り、I²C ステート・マシンが初期化され、どのチャネルも選択されていない状態になります。

スイッチのパス・ゲートは、PCA9544A から印加される最大の HIGH 電圧を、V_{CC} ピンを使用して制限できるように構成されています。これにより、ペアごとに異なるバス電圧を使用できるため、追加保護の必要なしに 1.8V、2.5V、3.3V のデバイスが 5V のデバイスと通信できます。外付けのプルアップ抵抗により、各チャネルに求められる電圧レベルにバスをプルアップします。すべての I/O ピンは 5V 許容です。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
PCA9544A	TVSOP (DGV) (20)	5.00mm × 4.40mm
	SOIC (DW) (20)	12.8mm × 7.50mm
	TSSOP (PW) (20)	6.50mm × 4.40mm
	VQFN (RGY) (20)	4.50mm x 3.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略図

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4 Revision History

Changes from Revision F (August 2019) to Revision G (March 2021) — **Page**

- Changed the PW packgae values in the *Thermal Information* table ... 4
- Added the RGY package values in the *Thermal Information* table ... 4
- Changed the V_{PORR} row in the *Electrical Characteristics* ... 6
- Added V_{PORF} row to the *Electrical Characteristics* ... 6
- Changed the I_{CC} Low inputs and High inputs values in the *Electrical Characteristics* ... 6
- Changed the ΔI_{CC} ($\overline{INT3}$–$\overline{INT0}$) MAX values From: 15 µA To: 20 µA in the *Electrical Characteristics* ... 6
- Changed the *Application Curves* ... 20
- Changed the *Power Supply Recommendations* ... 21

Changes from Revision E (June 2014) to Revision F (August 2019) — **Page**

- 「概要」のテキストを「PCA9544A は、～クワッド双方向変換スイッチです」から「*PCA9544A は、～4 チャネル双方向変換マルチプレクサです*」に変更 ... 1
- 「*製品情報*」表を変更 ... 1
- Deleted the RGW, GQN, and ZQN packages from the *Pin Configuration and Functions* section ... 3
- Moved T_{stg} to the *Absolute Maximum Ratings* ... 4
- Changed the *Handling Ratings* table to *ESD Ratings* table ... 4
- Added the *Thermal Information* table ... 4
- Changed the first paragraph of the *Overview* section ... 10
- Changed text From: "bidirectional translating switch" To: "bidirectional translating multiplexer" ... 12
- Changed text from: "One or several SCn/SDn downstream pairs or channels, are selected" To: "Only one SCn/SDn downstream pair, or channel, can be selected" in the *Control Register Definition* section ... 15
- Deleted sentence: "If multiple switches will be enabled.." from the second paragraph of the *Application Information* section ... 17

Changes from Revision D (February 2008) to Revision E (June 2014) — **Page**

5 Pin Configuration and Functions

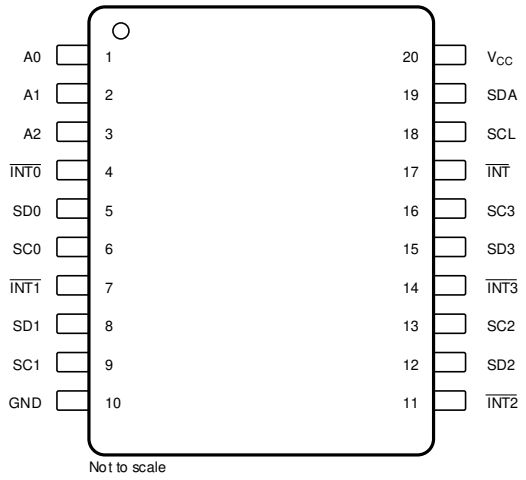


図 5-1. DGV, DW, or PW Package, TVSOP, SOIC, TSSOP (20 Pins), Top View

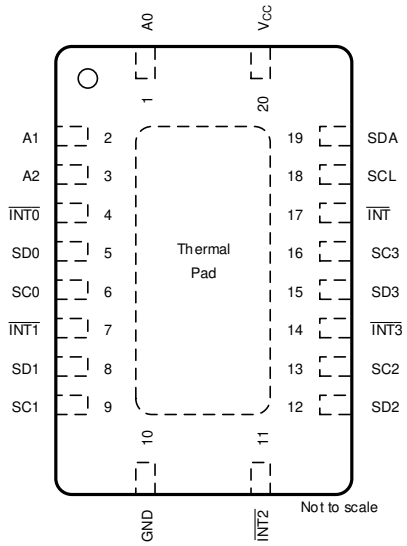


図 5-2. RGY Package, VQFN (20 Pins), Top View

表 5-1. Pin Functions

PIN		FUNCTION
NO.	NAME	
1	A0	Address input 0. Connect directly to V_{CC} or ground.
2	A1	Address input 1. Connect directly to V_{CC} or ground.
3	A2	Address input 2. Connect directly to V_{CC} or ground.
4	$\overline{INT0}$	Active-low interrupt input 0. Connect to V_{DPU0} (1) through a pull-up resistor.
5	SD0	Serial data 0. Connect to V_{DPU0} (1) through a pull-up resistor.
6	SC0	Serial clock 0. Connect to V_{DPU0} (1) through a pull-up resistor.
7	$\overline{INT1}$	Active-low interrupt input 1. Connect to V_{DPU1} (1) through a pull-up resistor.
8	SD1	Serial data 1. Connect to V_{DPU1} (1) through a pull-up resistor.
9	SC1	Serial clock 1. Connect to V_{DPU1} (1) through a pull-up resistor.
10	GND	Ground
11	$\overline{INT2}$	Active-low interrupt input 2. Connect to V_{DPU2} (1) through a pull-up resistor.
12	SD2	Serial data 2. Connect to V_{DPU2} (1) through a pull-up resistor.
13	SC2	Serial clock 2. Connect to V_{DPU2} (1) through a pull-up resistor.
14	$\overline{INT3}$	Active-low interrupt input 3. Connect to V_{DPU3} (1) through a pull-up resistor.
15	SD3	Serial data 3. Connect to V_{DPU3} (1) through a pull-up resistor.
16	SC3	Serial clock 3. Connect to V_{DPU3} (1) through a pull-up resistor.
17	$\overline{INT}$	Active-low interrupt output. Connect to V_{DPUM} (1) through a pull-up resistor.
18	SCL	Serial clock line. Connect to V_{DPUM} (1) through a pull-up resistor.
19	SDA	Serial data line. Connect to V_{DPUM} (1) through a pull-up resistor.
20	VCC	Supply power

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C reference voltage while V_{DPU0}-V_{DPU3} are the slave channel reference voltages.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range(2)	–0.5	7	V
I_I	Input current		±20	mA
I_O	Output current		±25	mA
	Continuous current through V_{CC}		±100	mA
	Continuous current through GND		±100	mA
P_{tot}	Total power dissipation		400	mW
T_A	Operating free-air temperature range	–40	85	°C
T_{stg}	Storage temperature range	–60	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	6	V
		A2–A0, $\overline{INT3}$– $\overline{INT0}$	0.7 × V_{CC}	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A2–A0, $\overline{INT3}$– $\overline{INT0}$	–0.5	0.3 × V_{CC}	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC(1)		PCA9544A				UNIT
		DGV	DW	PW	RGY	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92	58	118.2	62.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.9	41.9	62.7	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.5	40.3	69.3	39.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	18.1	7.7	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.6	40	68.8	39.8	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		PCA9544A				UNIT
		DGV	DW	PW	RGY	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	26.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{PORR}	Power-on reset voltage, V_{CC} rising(2)		No load,	$V_I = V_{CC}$ or GND			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling(2)		No load,	$V_I = V_{CC}$ or GND		0.8	1		V
V_{pass}	Switch output voltage		$V_{SWin} = V_{CC}$,	$I_{SWout} = -100$ µA	5 V		3.6		V
					4.5 V to 5.5 V	2.6		4.5	
					3.3 V		1.9		
					3 V to 3.6 V	1.6		2.8	
					2.5 V		1.5		
					2.3 V to 2.7 V	1.1		2	
I_{OH}	$\overline{INT}$		$V_O = V_{CC}$		2.3 V to 5.5 V			10	µA
I_{OL}	SCL, SDA		V_{OL} = 0.4 V		2.3 V to 5.5 V	3	7		mA
			V_{OL} = 0.6 V			6	10		
	$\overline{INT}$		V_{OL} = 0.4 V			3	7		
I_I	SCL, SDA		$V_I = V_{CC}$ or GND		2.3 V to 5.5 V			±1	µA
	SC3–SC0, SD3–SD0							±1	
	A2–A0							±1	
	$\overline{INT3}$– $\overline{INT0}$							±1	
I_{CC}	Operating mode	f_{SCL} = 100 kHz	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V		3	12	µA
					3.6 V		3	11	
					2.7 V		3	10	
	Standby mode	Low inputs	V_I = GND,	$I_O = 0$	5.5 V		1.6	2	
					3.6 V		1	1.3	
					2.7 V		0.7	1.1	
		High inputs	$V_I = V_{CC}$,	$I_O = 0$	5.5 V		1.6	2	
					3.6 V		1	1.3	
					2.7 V		0.7	1.1	
ΔI_{CC}	Supply-current change	$\overline{INT3}$– $\overline{INT0}$	One $\overline{INT3}$– $\overline{INT0}$ input at 0.6 V, Other inputs at V_{CC} or GND		2.3 V to 5.5 V		8	20	µA
			One $\overline{INT3}$– $\overline{INT0}$ input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				8	20	
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND				8	15	
			SCL or SDA inputs at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				8	15	
C_i	A2–A0		$V_I = V_{CC}$ or GND		2.3 V to 5.5 V		4.5	6	pF
	$\overline{INT3}$– $\overline{INT0}$						4.5	6	
$C_{io(OFF)}$ (3)	SCL, SDA		$V_I = V_{CC}$ or GND,	Switch OFF	2.3 V to 5.5 V		15	19	pF
	SC3–SC0, SD3–SD0						6	8	
R_{ON}	Switch-on resistance		V_O = 0.4 V,	I_O = 15 mA	4.5 V to 5.5 V	4	10	16	Ω
					3 V to 3.6 V	5	13	20	
			V_O = 0.4 V,	I_O = 10 mA	2.3 V to 2.7 V	7	16	45	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), T_A = 25°C.
(2) The power-on reset circuit resets the I^2C bus logic when $V_{CC} < V_{PORF}$.
(3) $C_{io(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

			STANDARD-MODE I²C BUS		FAST-MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0(1)		0(1)		µs
t_{icr}	I²C input rise time			1000	20 + 0.1C_b (2)	300	ns
t_{icf}	I²C input fall time			300	20 + 0.1C_b (2)	300	ns
t_{ocf}	I²C output fall time (10-pF to 400-pF bus)			300	20 + 0.1C_b (2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low)(3)	SCL low to SDA output low valid		1		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high)(3)	SCL low to SDA output high valid		0.6		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	µs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see 図 7-1).

6.7 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted) (see 図 7-1)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} (1)	Propagation delay time	R_{ON} = 20 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.3	ns
		R_{ON} = 20 Ω, C_L = 50 pF				1	
t_{iv}	Interrupt valid time(2)		$\overline{INTn}$	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time(2)		$\overline{INTn}$	$\overline{INT}$		2	µs

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) Data taken using a 4.7-kΩ pull-up resistor and 100-pF load (see 図 7-2).

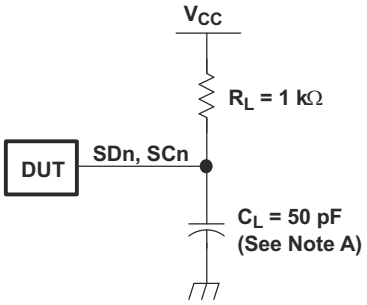
6.8 Interrupt Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

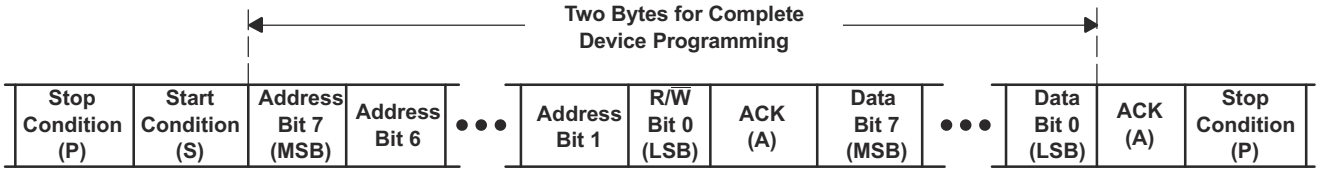
PARAMETER		MIN	MAX	UNIT
t_{PWRL}	Low-level pulse duration rejection of $\overline{INTn}$ inputs(1)	1		µs
t_{PWRH}	High-level pulse duration rejection of $\overline{INTn}$ inputs(1)	0.5		µs

(1) Data taken using a 4.7-kΩ pull-up resistor and 100-pF load (see 図 7-2).

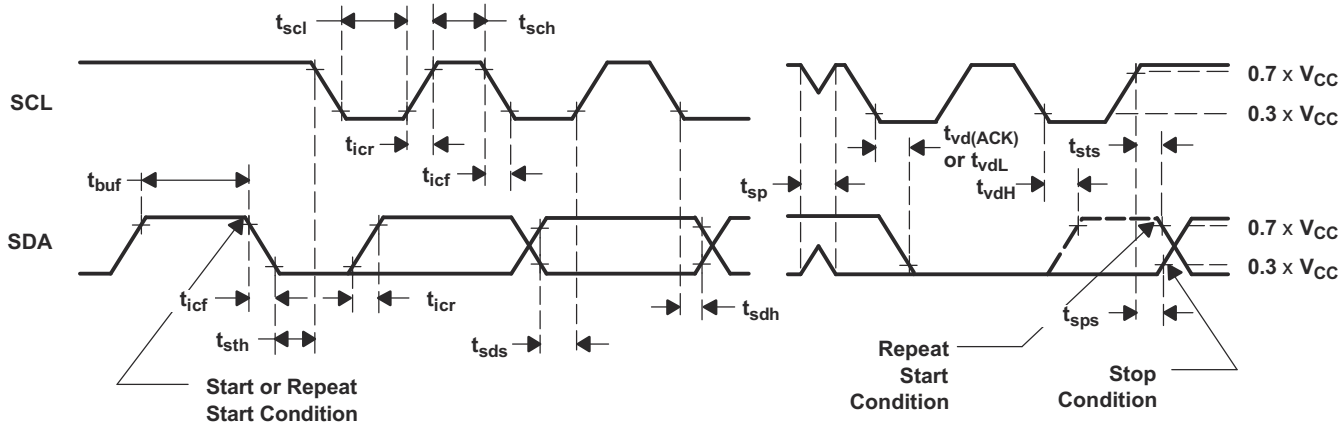
7 Parameter Measurement Information



I²C-Port Load Configuration



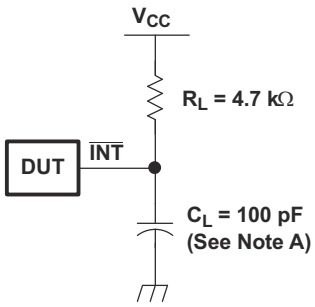
BYTE	DESCRIPTION
1	I²C address + R/W
2	Control register data



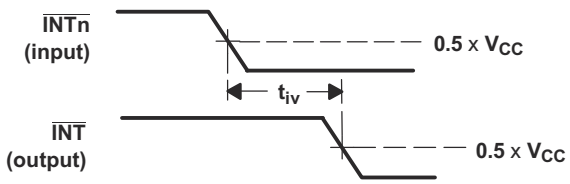
Voltage Waveforms

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns
C. The outputs are measured one at a time, with one transition per measurement.

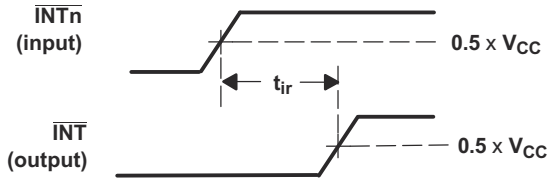
図 7-1. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms



Interrupt Load Configuration



Voltage Waveforms (t_{iv})



Voltage Waveforms (t_{ir})

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns

図 7-2. Interrupt Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

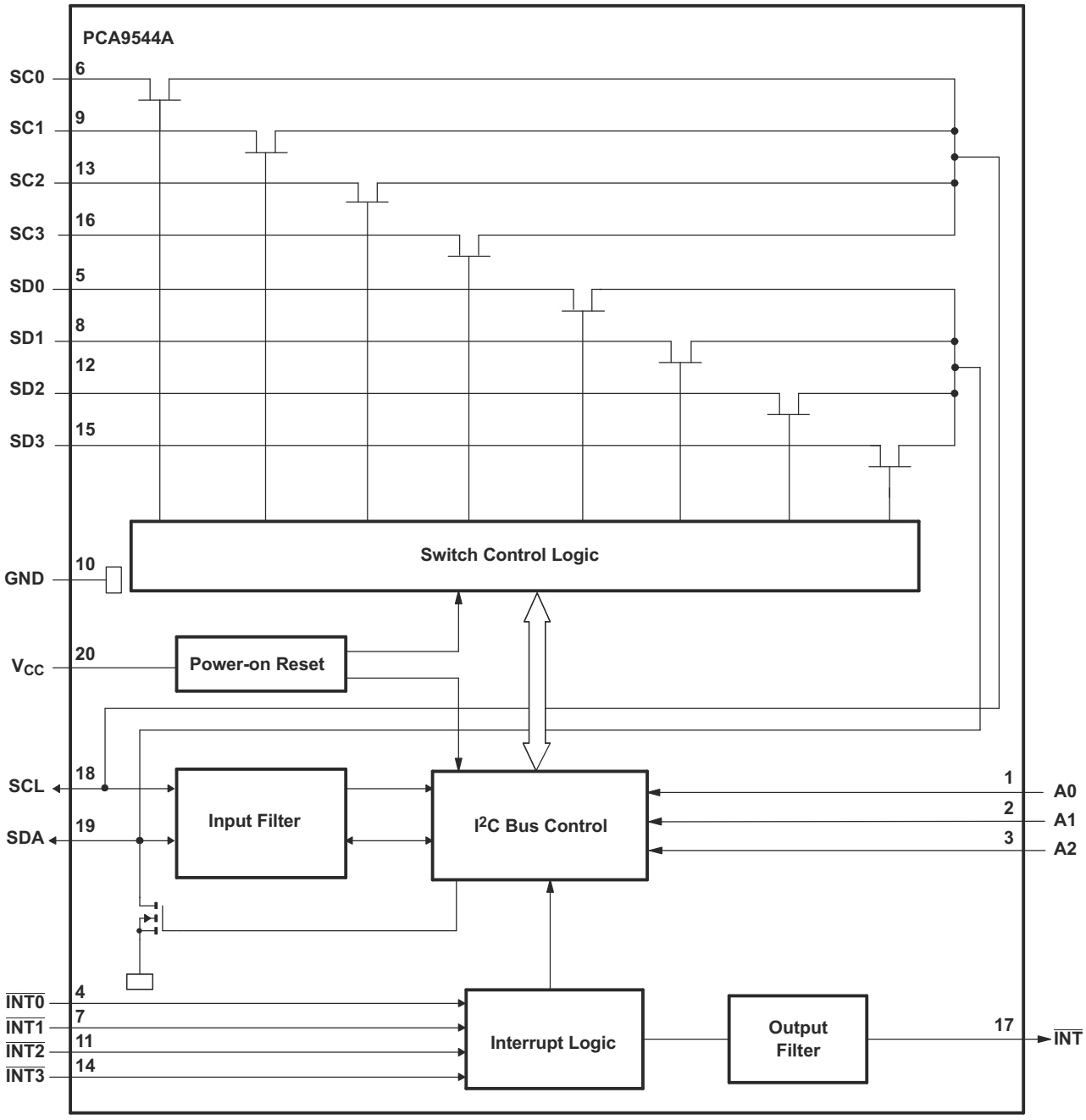
The PCA9544A is a 4-channel, bidirectional translating I^2C multiplexer. The master SCL/SDA signal pair is directed to one of the four channels of slave devices, SC0/SD0-SC3/SD3. Only one individual downstream channel can be selected of the four channels at a time. The PCA9544A also supports interrupt signals in order for the master to detect an interrupt on the $\overline{INT}$ output pin that can result from any of the slave devices connected to the $\overline{INT3}$- $\overline{INT0}$ input pins.

The device can be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR), which resets the state machine and allows the PCA9544A to recover should one of the downstream I^2C buses get stuck in a low state. A POR event causes all channels to be deselected.

The connections of the I^2C data path are controlled by the same I^2C master device that is switched to communicate with multiple I^2C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0-A2 pins), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The PCA9544A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

8.2 Functional Block Diagram



A. Pin numbers shown are for DGV, DW, PW, and RGY packages.

8.3 Feature Description

The PCA9544A is a 4-channel, bidirectional translating multiplexer for I^2C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9544A features I^2C control using a single 8-bit control register in which the three least significant bits control the enabling and disabling of the 4 switch channels of I^2C data flow. The PCA9544A also supports interrupt signals for each slave channel and this data is held in the four most significant bits of the control register. Depending on the application, voltage translation of the I^2C bus can also be achieved using the PCA9544A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^2C bus enters a fault state, the PCA9544A can be reset to resume normal operation by means of a power-on reset which results from cycling power to the device.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the PCA9544A in a reset condition until V_{CC} has reached V_{POR}. At this point, the reset condition is released, and the PCA9544A registers and I^2C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below V_{POR} to reset the device.

8.5 Programming

8.5.1 I^2C Interface

The I^2C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see 図 8-1).

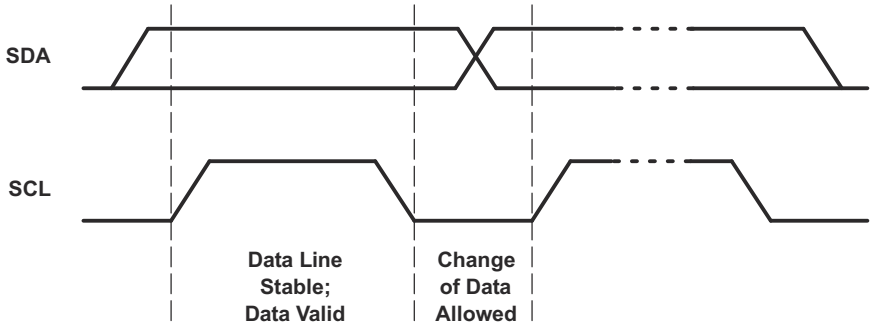


図 8-1. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see 図 8-2).

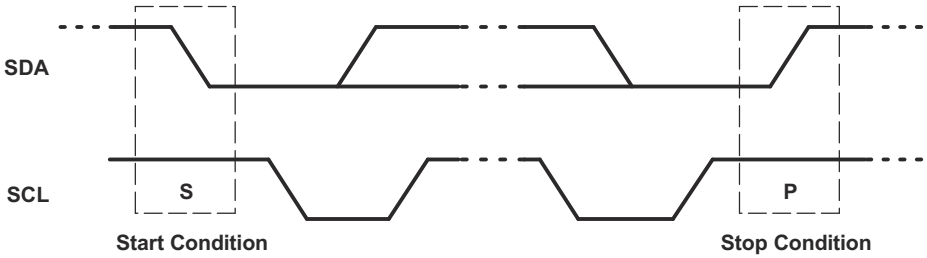


図 8-2. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see 図 8-3).

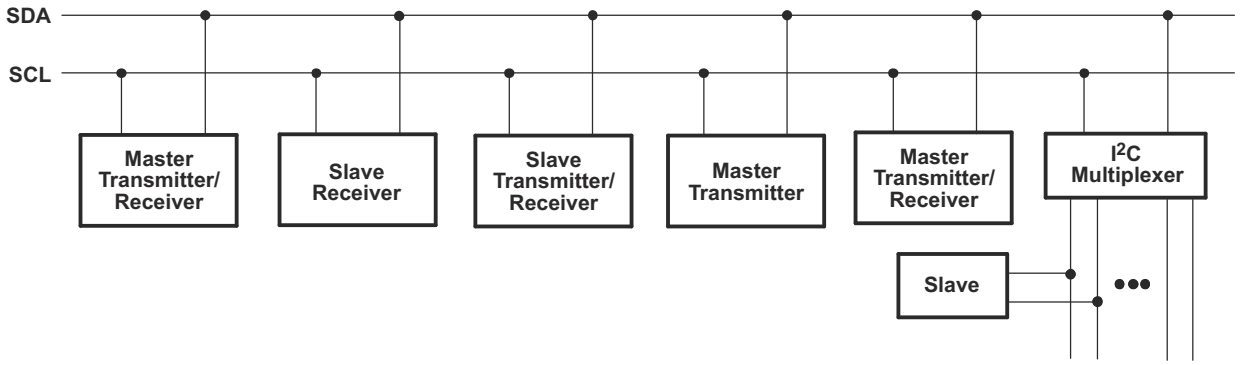


図 8-3. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an acknowledge (ACK) after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 8-4). Setup and hold times must be taken into account.

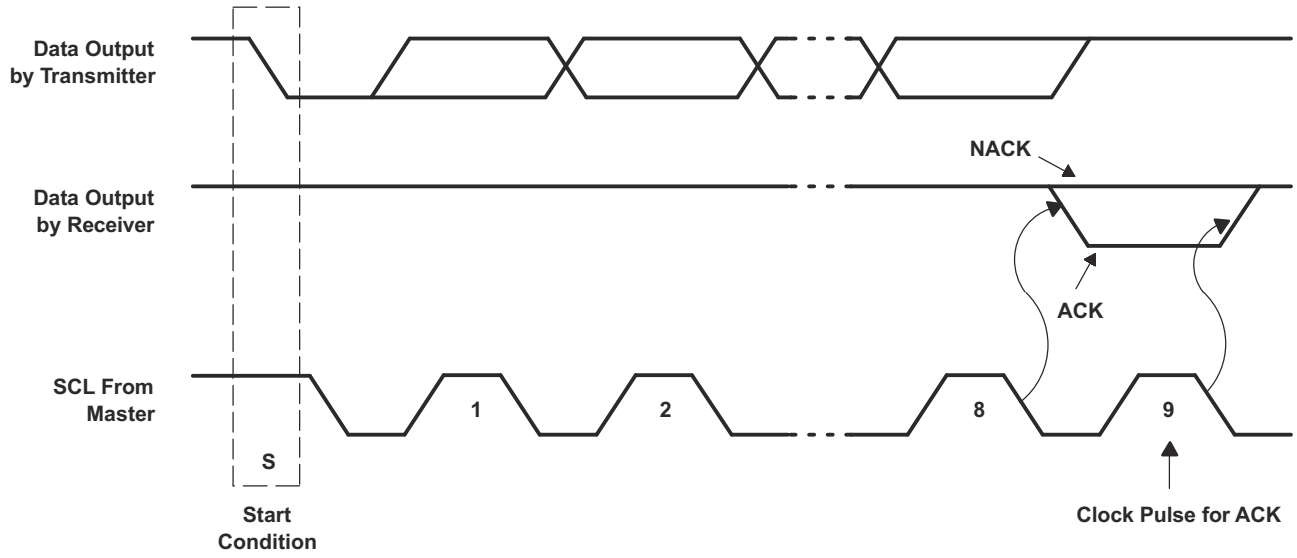


図 8-4. Acknowledgment on the I2C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Data is transmitted to the PCA9544A control register using the write mode shown in 図 8-5.

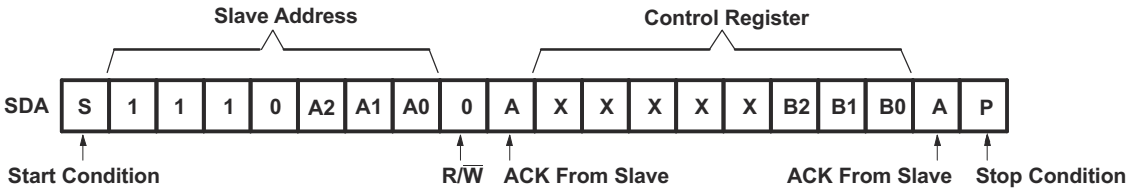


図 8-5. Write Control Register

Data is read from the PCA9544A control register using the read mode shown in 図 8-6.

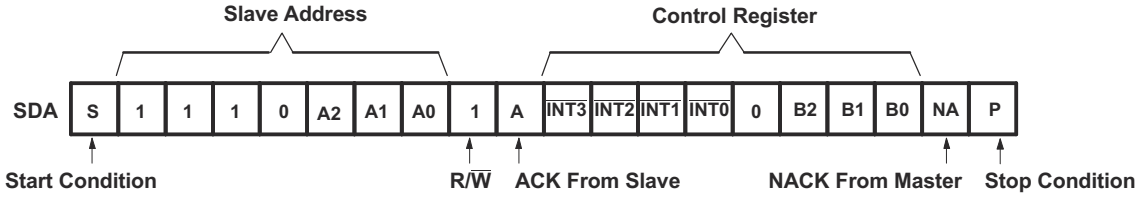


図 8-6. Read Control Register

8.6 Register Map

8.6.1 Control Register

8.6.1.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9544A is shown in 図 8-7. To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low.

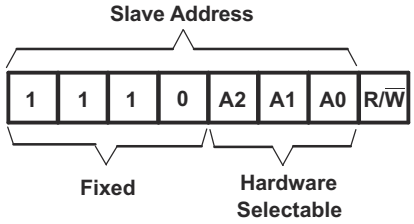


図 8-7. PCA9544A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

8.6.1.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9544A, which is stored in the control register. If multiple bytes are received by the PCA9544A, it saves the last byte received. This register can be written and read via the I^2C bus.

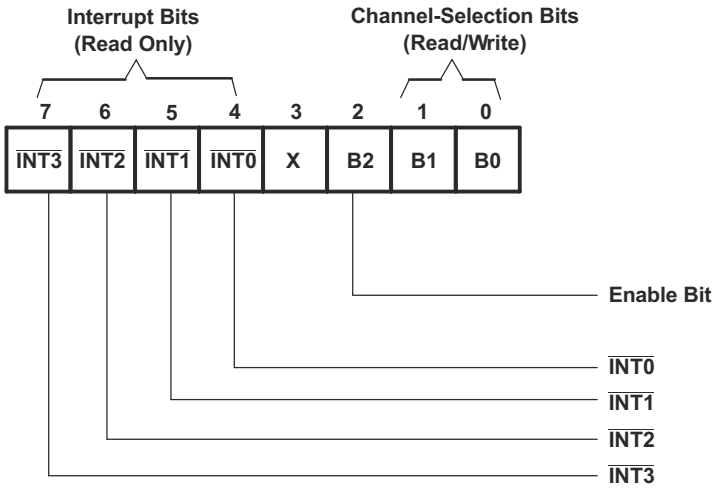


図 8-8. Control Register

8.6.1.3 Control Register Definition

Only one SCn/SDn downstream pair, or channel, can be selected by the contents of the control register (see 表 8-1). This register is written after the PCA9544A has been addressed. The three LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur right after the acknowledge cycle.

表 8-1. Control Register Write (Channel Selection), Control Register Read (Channel Status)(1)

$\overline{INT3}$	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$	D3	B2	B1	B0	COMMAND
X	X	X	X	X	0	X	X	No channel selected
X	X	X	X	X	1	0	0	Channel 0 enabled
X	X	X	X	X	1	0	1	Channel 1 enabled
X	X	X	X	X	1	1	0	Channel 2 enabled
X	X	X	X	X	1	1	1	Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up default state

(1) Only one channel may be selected at a time.

8.6.1.4 Interrupt Handling

The PCA9544A provides four interrupt inputs (one for each channel) and one open-drain interrupt output. When an interrupt is generated by any device, it is detected by the PCA9544A, and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register (see 表 8-2).

Bits 4–7 of the control register correspond to channels 0–3 of the PCA9544A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 causes bit 4 of the control register to be set on the read. The master then can address the PCA9544A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can reconfigure the PCA9544A to select this channel and locate the device generating the interrupt and clear it. Once the device responsible for the interrupt clears, the interrupt clears.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC}.

表 8-2. Control Register Read (Interrupt)(1)

$\overline{INT3}$	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$	D3	B2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X	X	X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X	X	X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

(1) Several interrupts can be active at the same time. For example, $\overline{INT3}$ = 0, $\overline{INT2}$ = 1, $\overline{INT1}$ = 1, $\overline{INT0}$ = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Applications of the PCA9544A contain an I^2C (or SMBus) master device and up to four I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I^2C bus contains many additional slave devices that do not result in I^2C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels.

9.2 Typical Application

A typical application of the PCA9544A contains anywhere from 1 to 5 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} – V_{DPU3}). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, V_{pass} = V_{DPUX}. Once the maximum V_{pass} is known, V_{cc} can be selected using 図 9-2. In an application where voltage translation is necessary, additional design requirements must be considered (See *Design Requirements*).

図 9-1 shows an application in which the PCA9544A can be used.

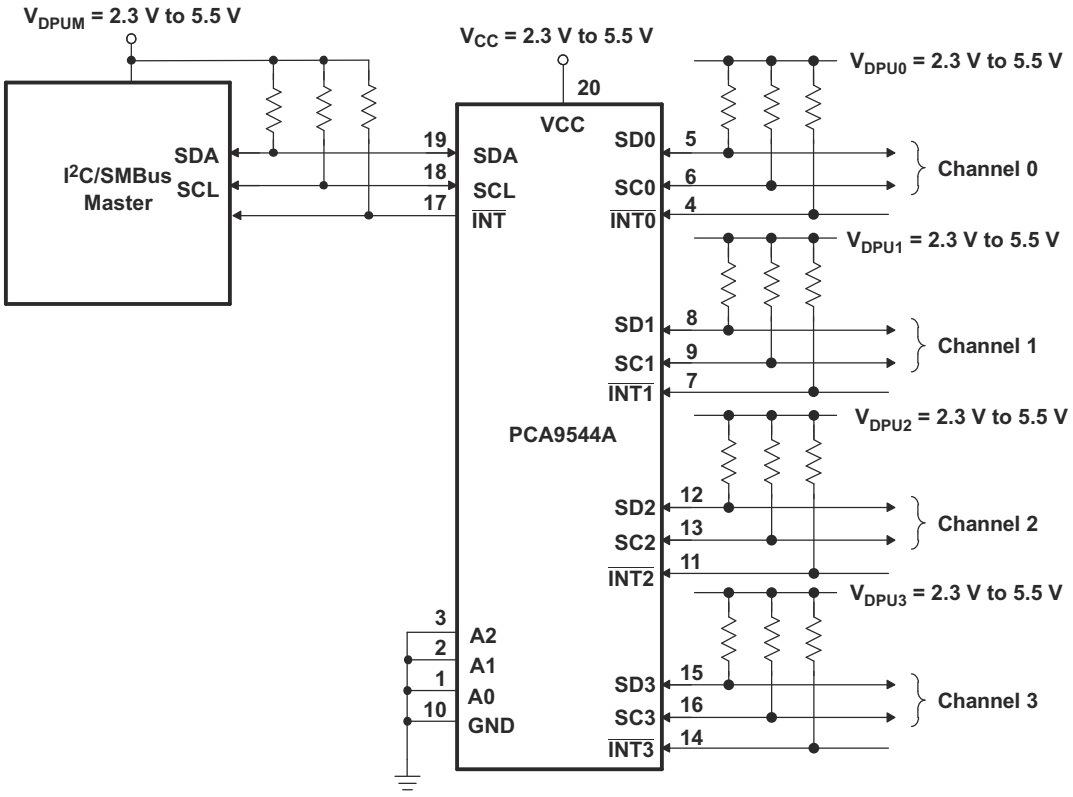


図 9-1. Typical Application

9.2.1 Design Requirements

The pull-up resistors on the $\overline{INT3}$- $\overline{INT0}$ terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0 and A1 terminals are hardware selectable to control the slave address of the PCA9544A. These terminals may be tied directly to GND or V_{CC} in the application.

If multiple slave channels are activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side are the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the PCA9544A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

図 9-2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the *Electrical Characteristics* section of this data sheet). In order for the PCA9544A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in 図 9-2, $V_{pass(max)}$ is 2.7 V when the PCA9544A supply voltage is 4 V or lower, so the PCA9544A supply voltage could be set to 3.3 V. pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see 図 9-1).

9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9544A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels are activated simultaneously, each of the slaves on all channels contributes to total bus capacitance.

9.2.3 Application Curves

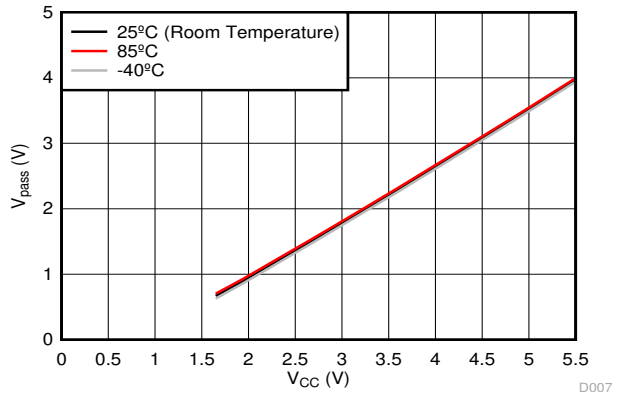
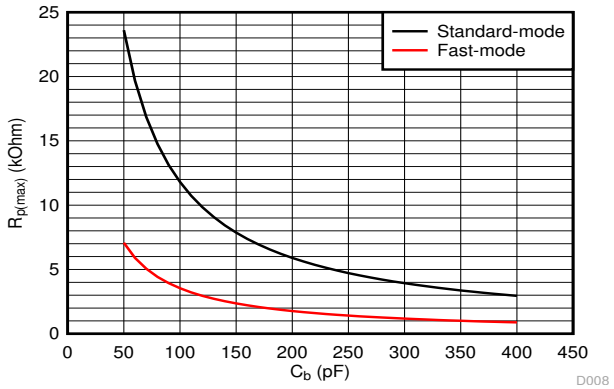


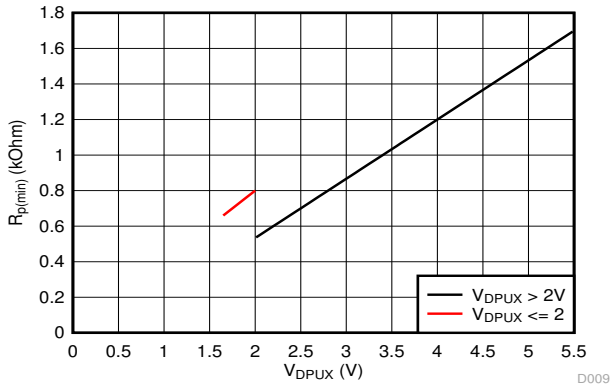
図 9-2. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

図 9-3. Maximum Pull-up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

図 9-4. Minimum Pull-up Resistance ($R_{p(min)}$) vs Pull-up Reference Voltage (V_{DPUX})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9544A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 図 10-1 and 図 10-2.

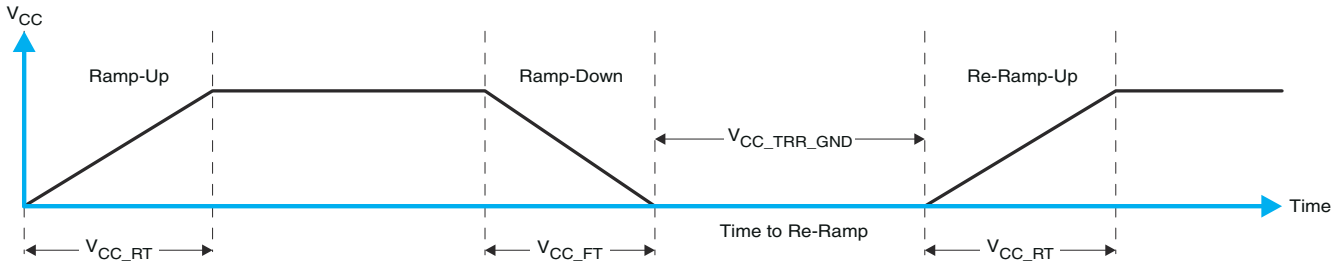


図 10-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

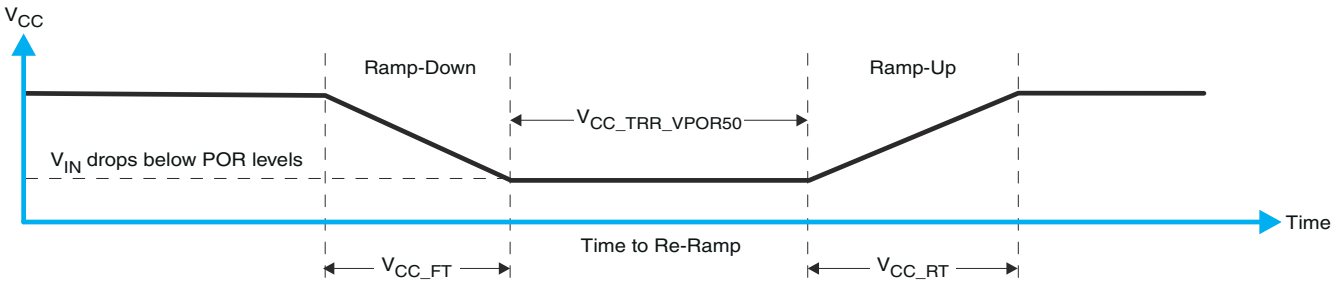


図 10-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 10-1 specifies the performance of the power-on reset feature for PCA9544A for both types of power-on reset.

表 10-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 図 10-1	1		100	ms
V_{CC_RT}	Rise rate	See 図 10-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 図 10-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 図 10-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See 図 10-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 図 10-3				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 図 10-3 and 表 10-1 provide more information on how to measure these specifications.

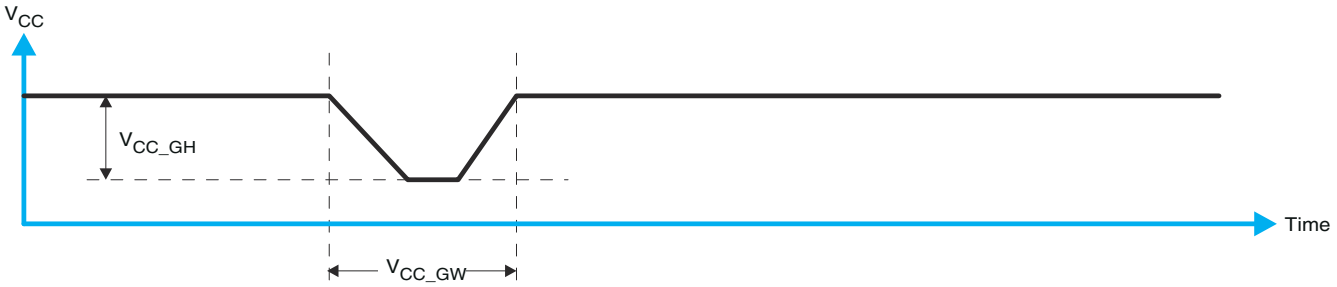


図 10-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 10-4 and 表 10-1 provide more details on this specification.

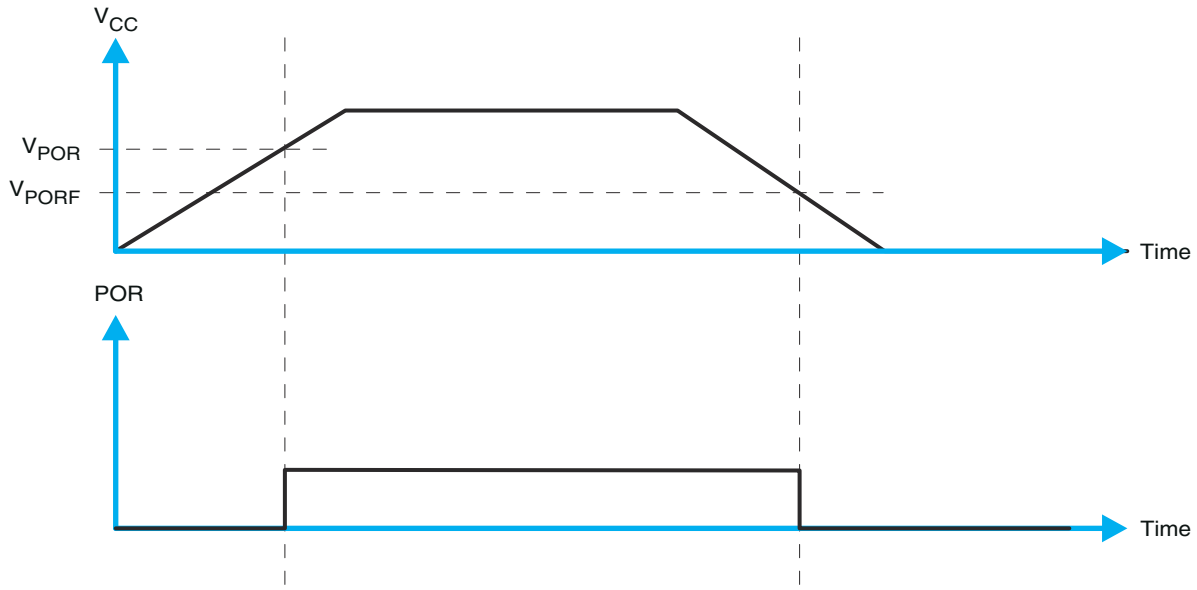


図 10-4. V_{POR}

11 Layout

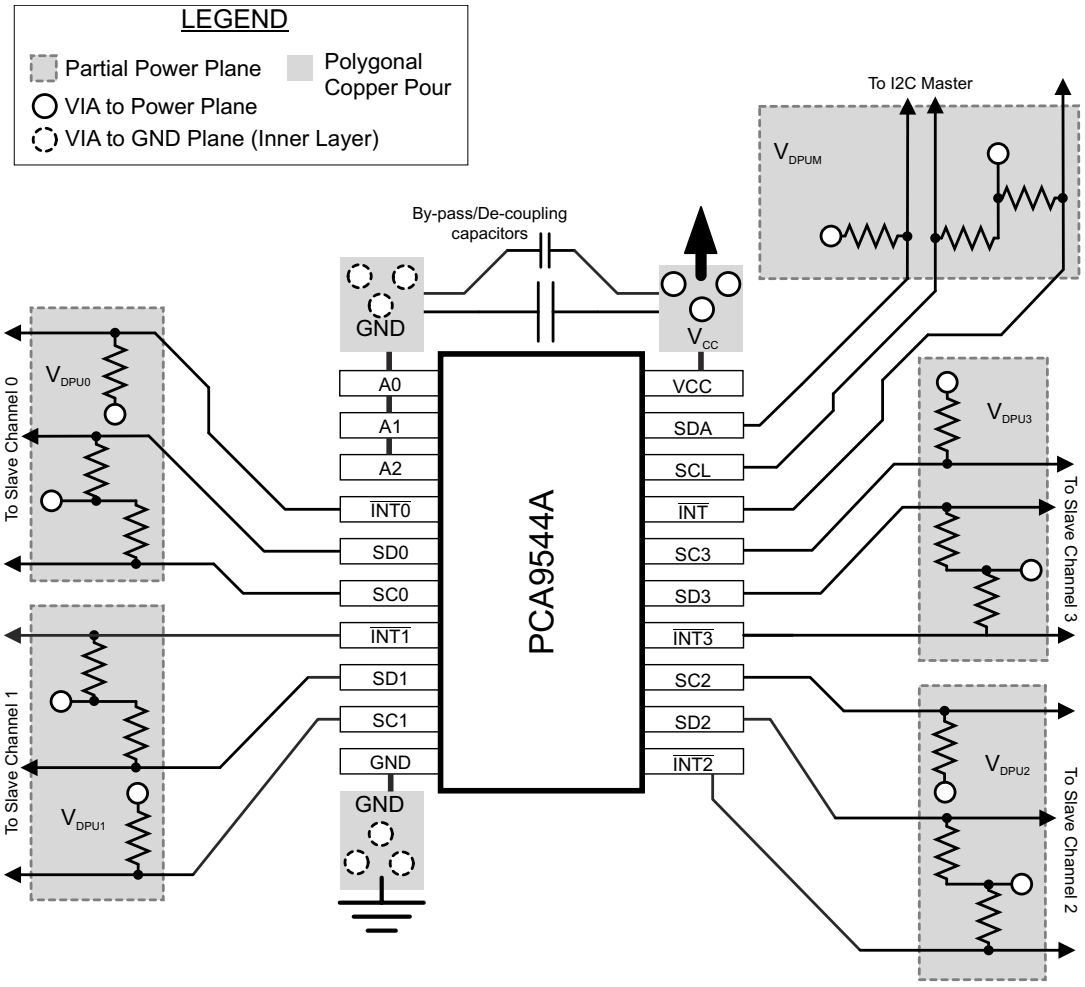
11.1 Layout Guidelines

For PCB layout of the PCA9544A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, data lines (SCn, SDn and $\overline{INT}$n) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

11.2 Layout Example



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.5 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9544ADGVR	NRND	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD544A
PCA9544ADGVR.A	NRND	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD544A
PCA9544ADW	NRND	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9544A
PCA9544ADW.A	NRND	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9544A
PCA9544ADWR	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9544A
PCA9544ADWR.A	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9544A
PCA9544APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD544A
PCA9544APWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD544A
PCA9544APWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD544A
PCA9544APWT	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	PD544A
PCA9544ARGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD544A
PCA9544ARGYR.B	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD544A
PCA9544ARGYRG4	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD544A
PCA9544ARGYRG4.B	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD544A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

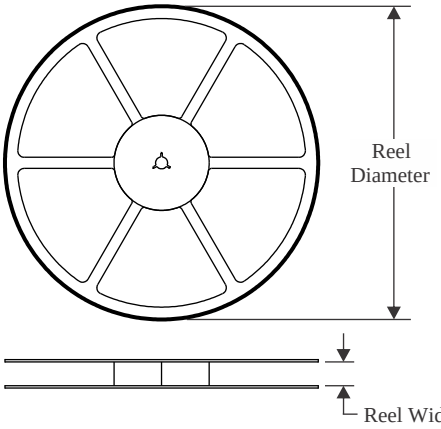
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

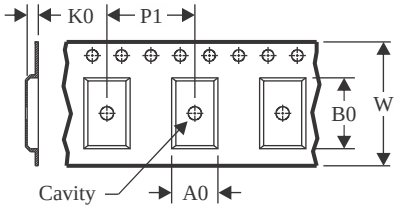
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

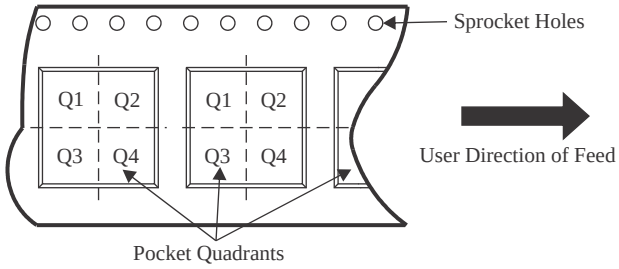


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

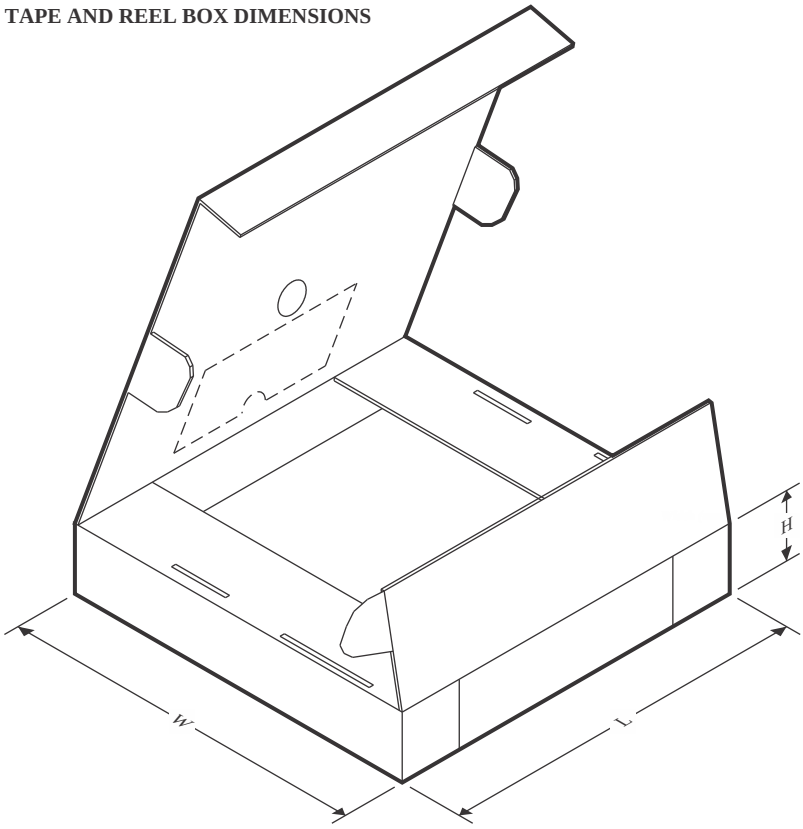
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9544ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9544ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
PCA9544APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
PCA9544ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
PCA9544ARGYRG4	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

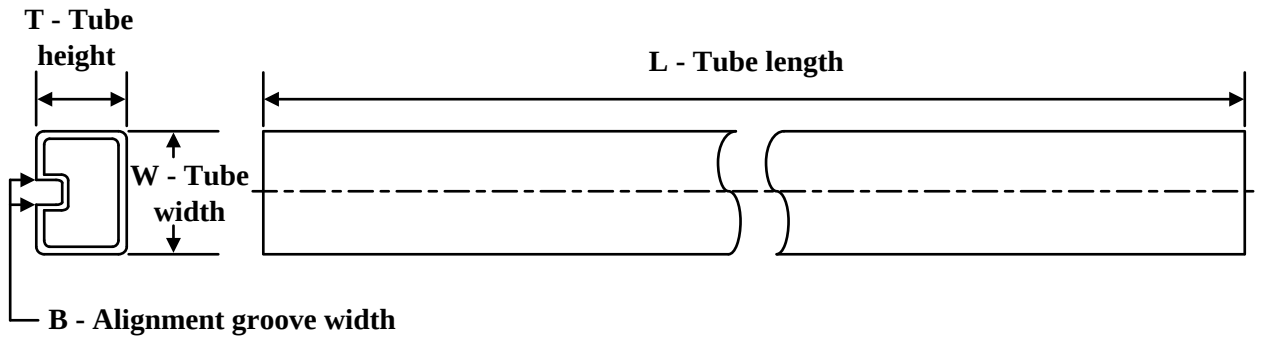
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9544ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
PCA9544ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
PCA9544APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
PCA9544ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0
PCA9544ARGYRG4	VQFN	RGY	20	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

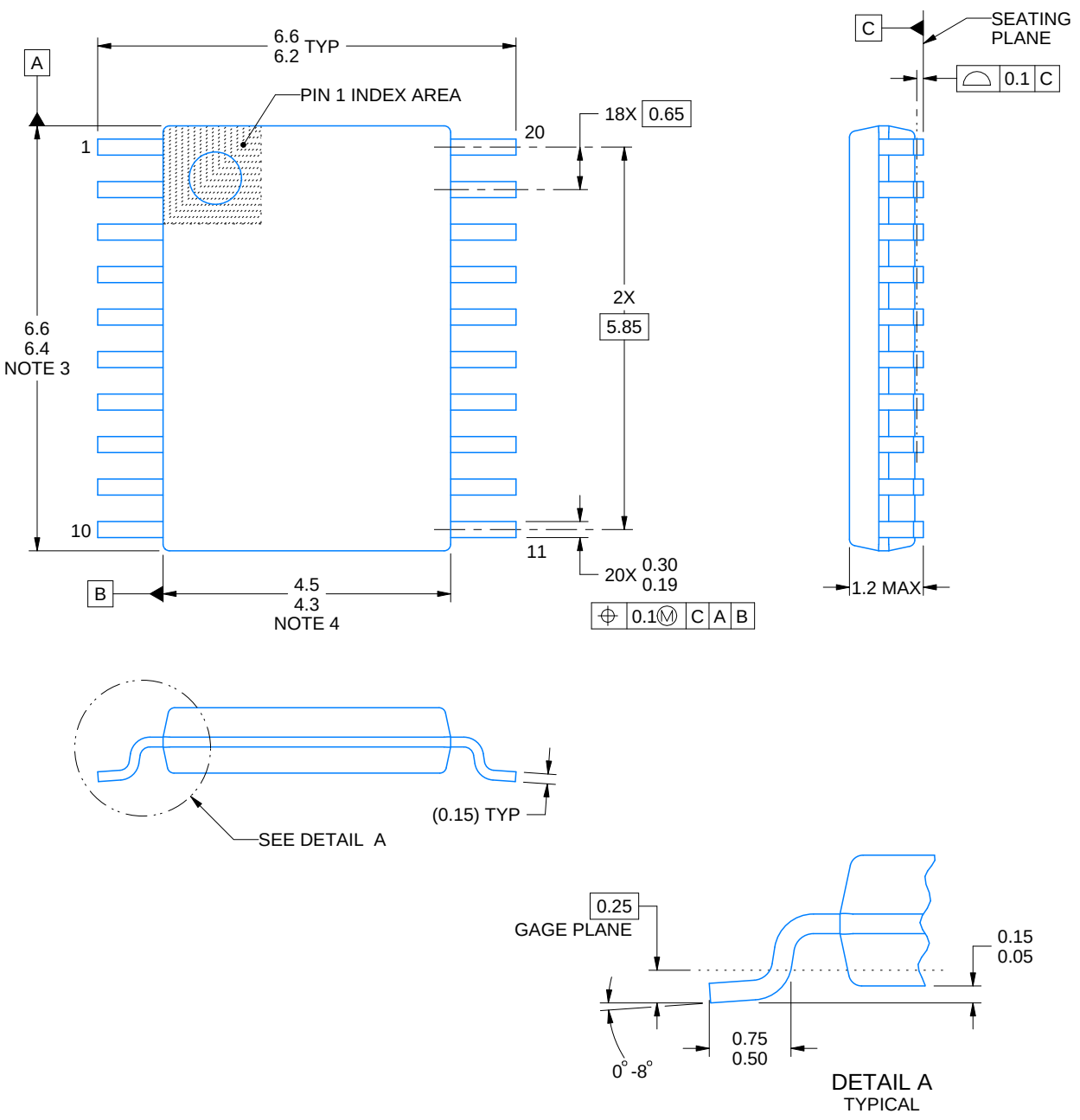
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9544ADW	DW	SOIC	20	25	507	12.83	5080	6.6
PCA9544ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6

PACKAGE OUTLINE

PW0020A

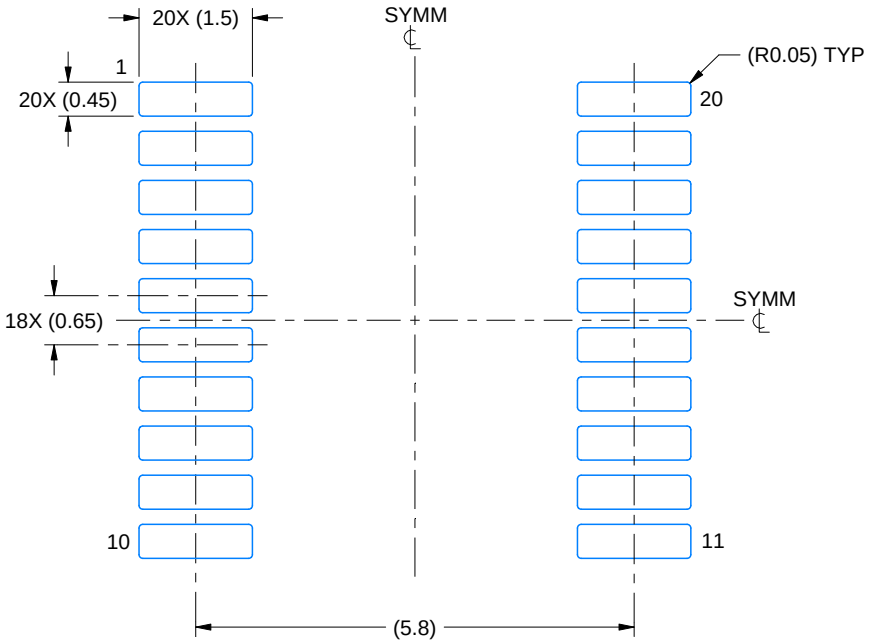
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



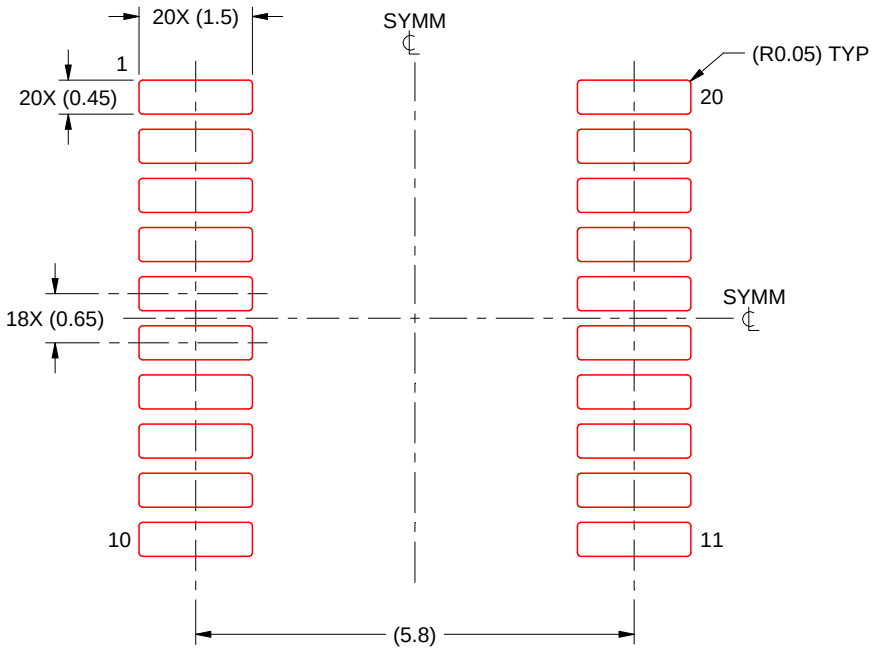
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

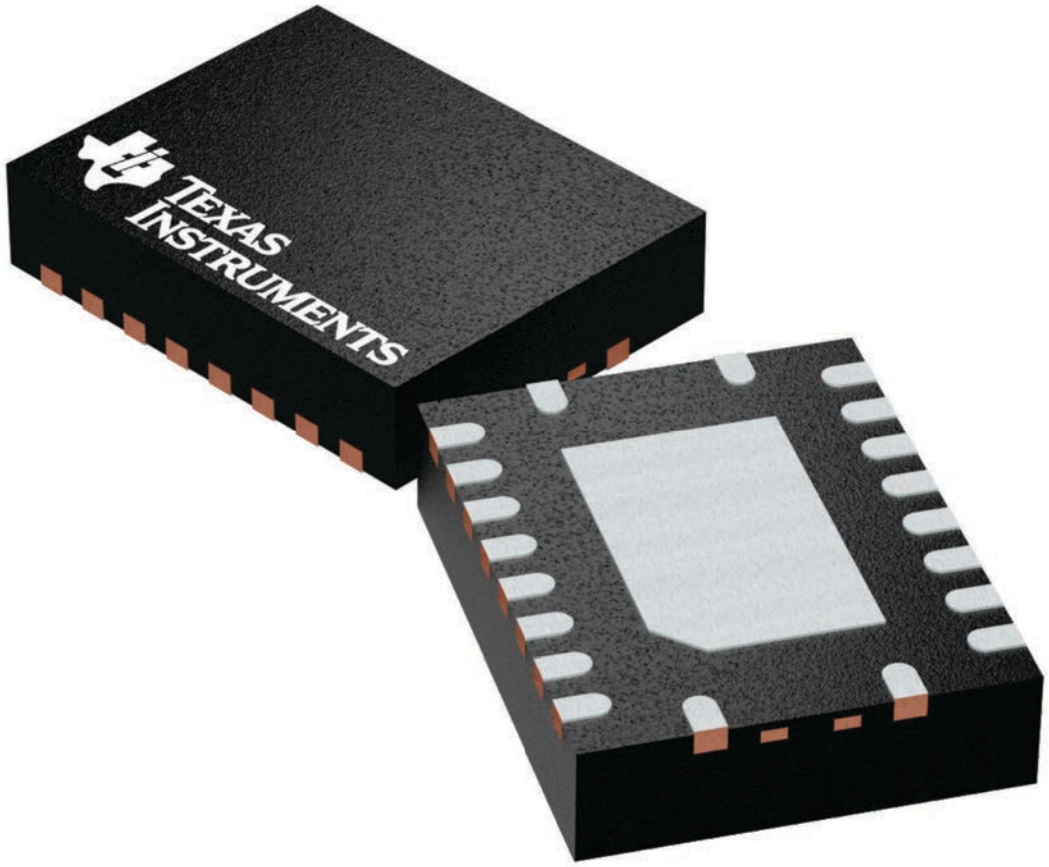
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



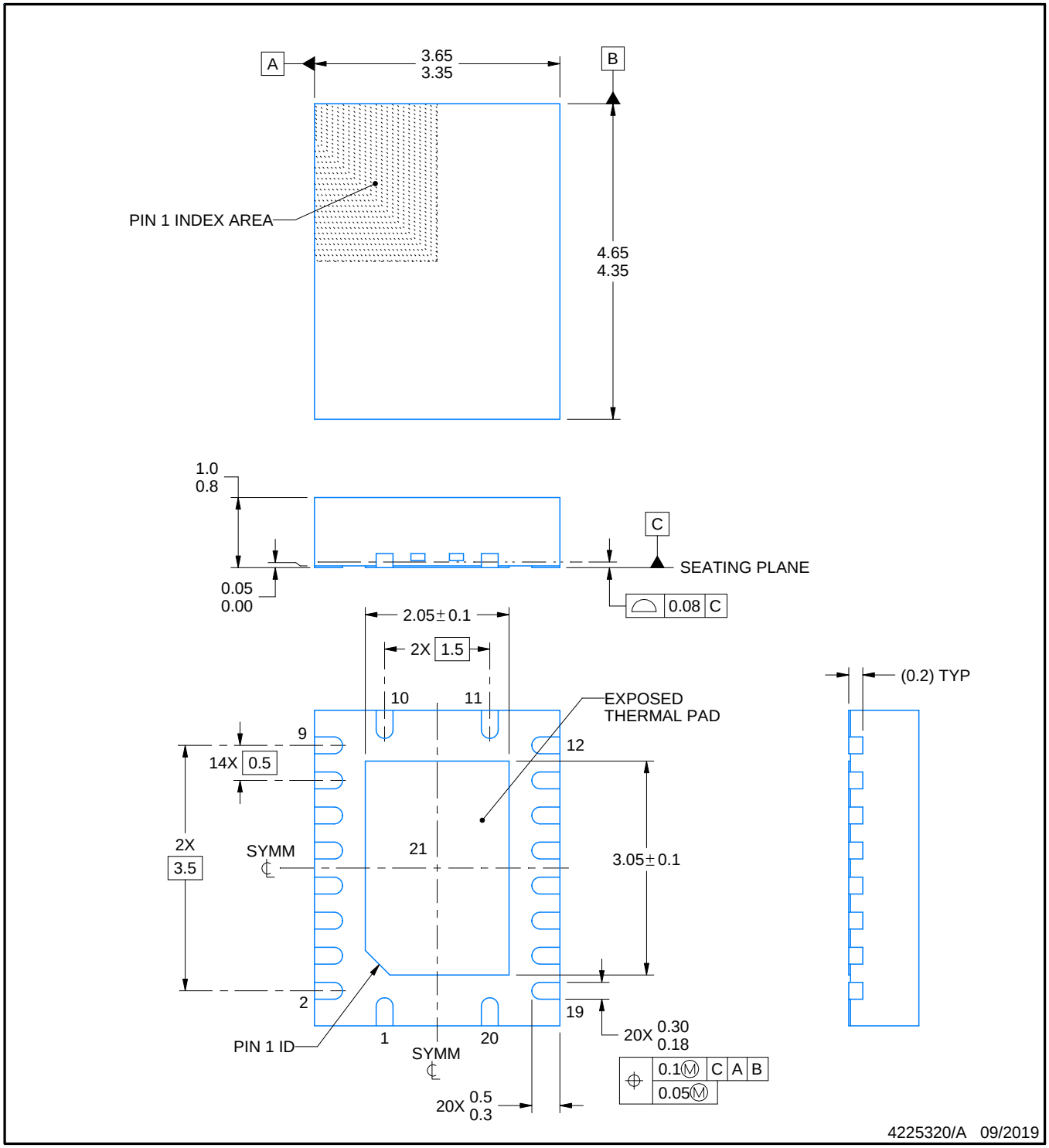
4225264/A

PACKAGE OUTLINE

RGY0020A

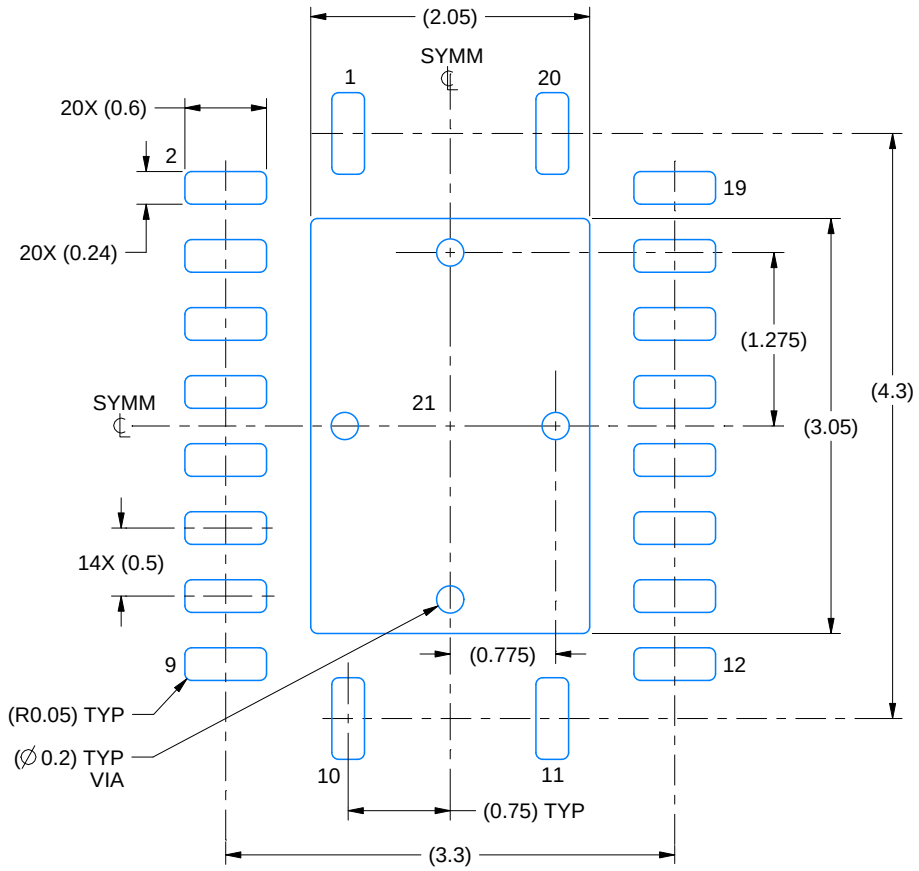
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

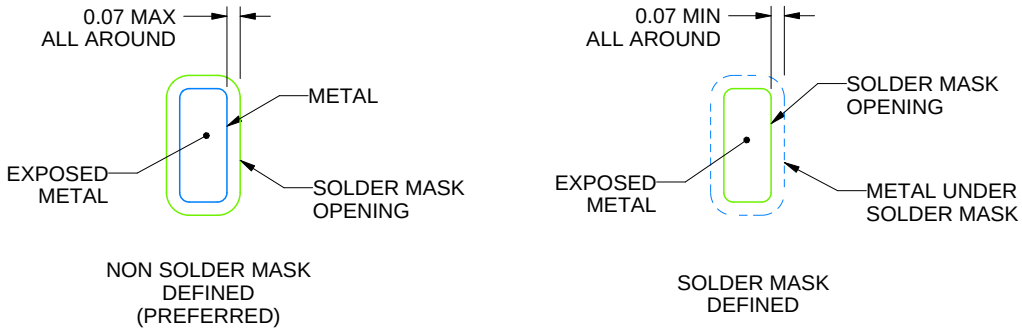


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

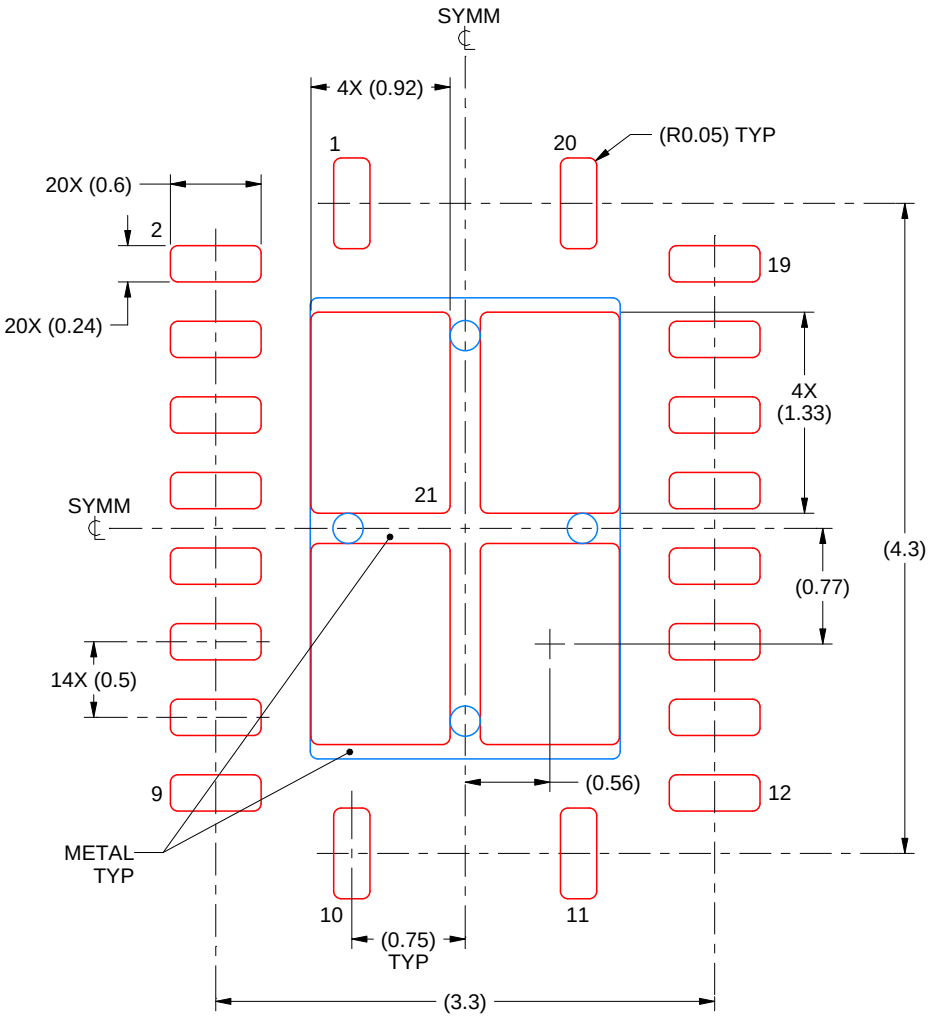


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



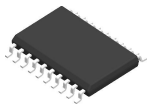
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

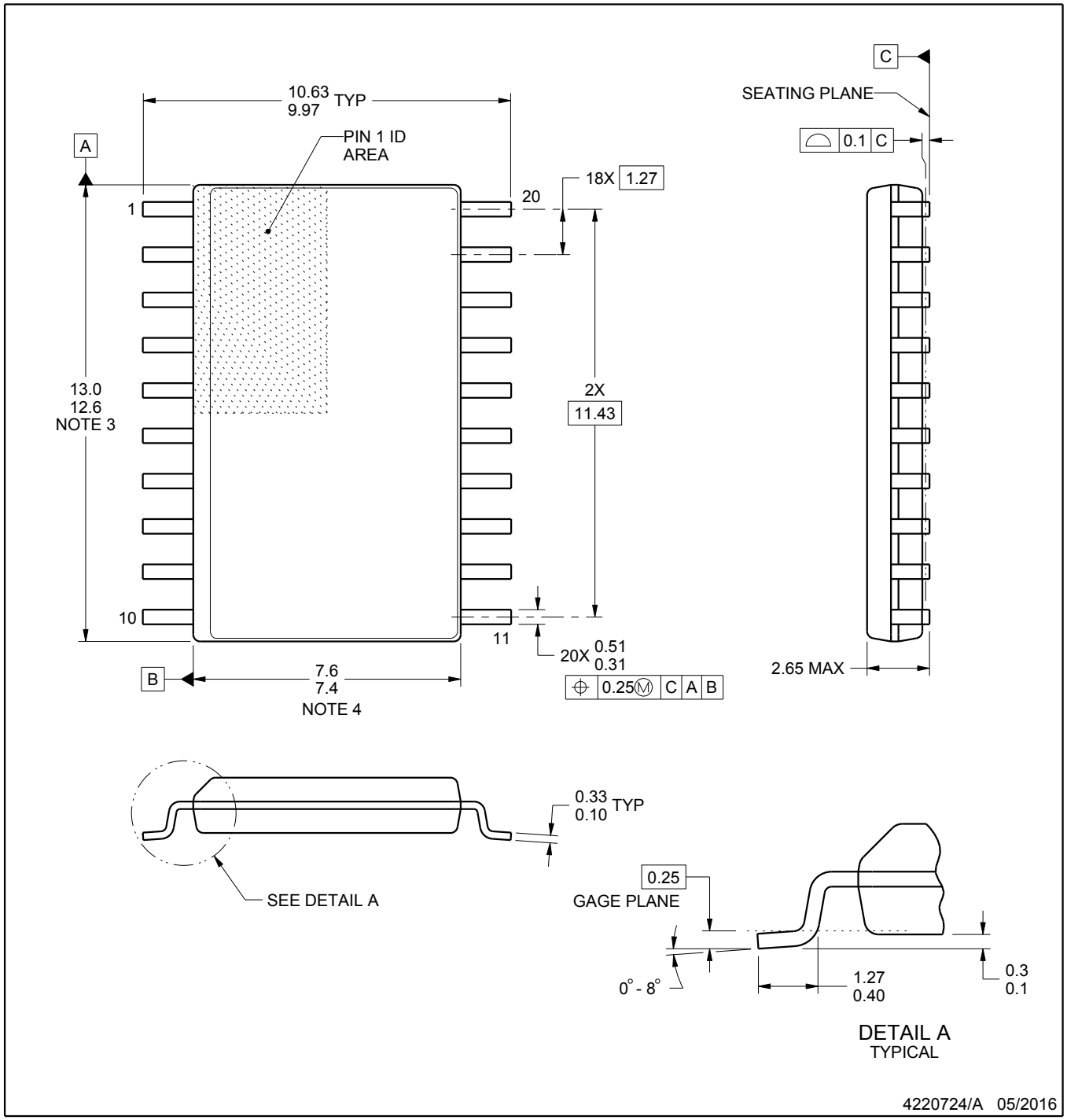


PACKAGE OUTLINE

DW0020A

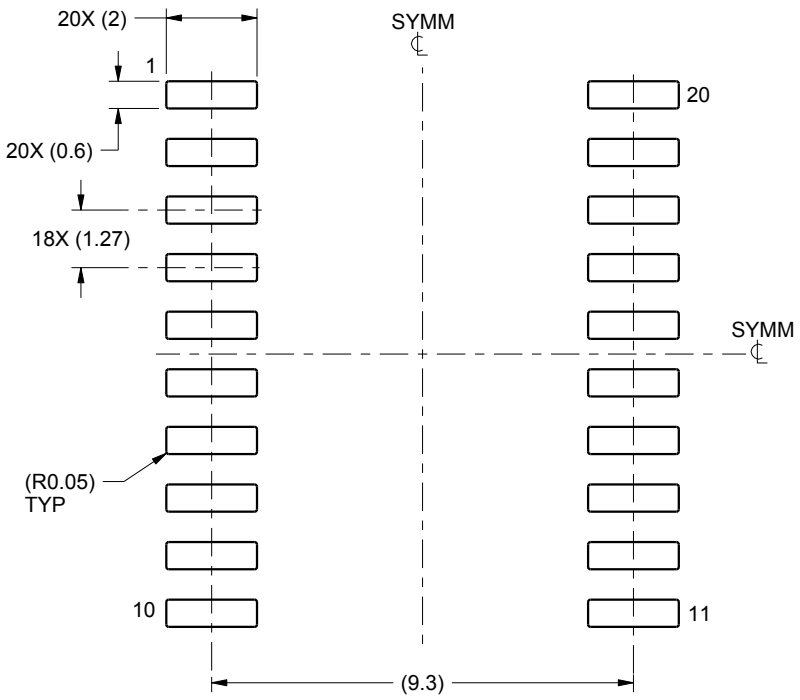
SOIC - 2.65 mm max height

SOIC

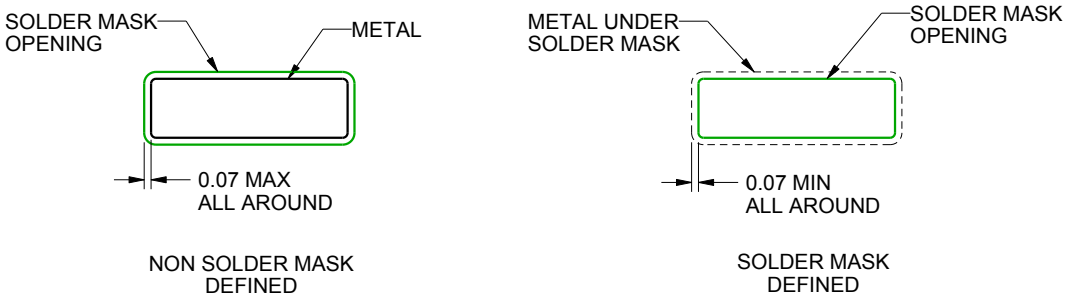


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

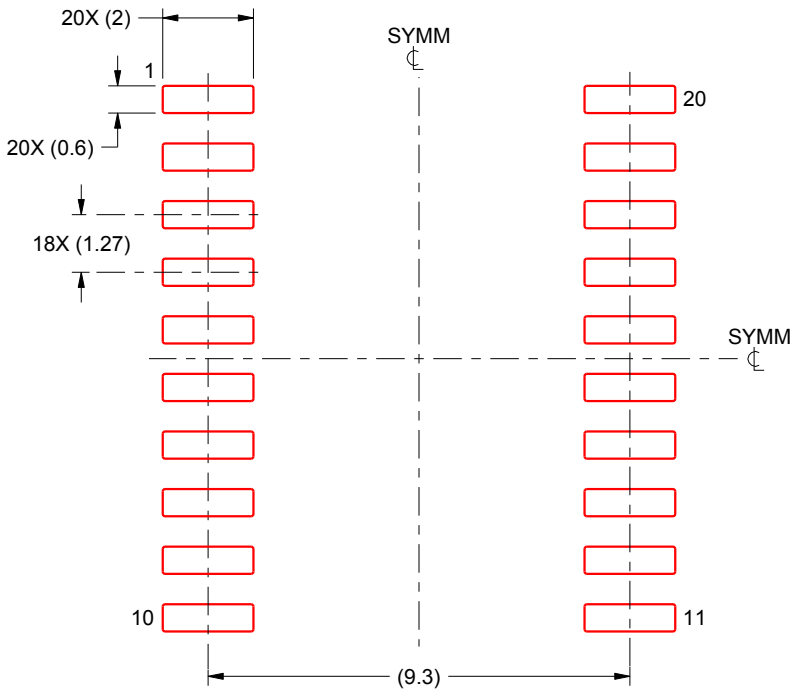


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月