

- State-of-the-Art **EPIC-IIIB™** BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32$ -mA  $I_{OH}$ ,  $64$ -mA  $I_{OL}$ )
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

### description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

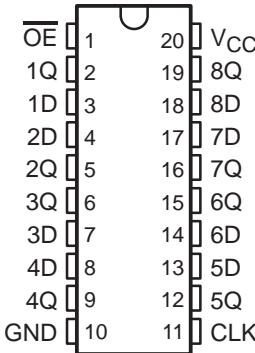
The eight flip-flops of the SN54ABT374 and SN74ABT374A are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

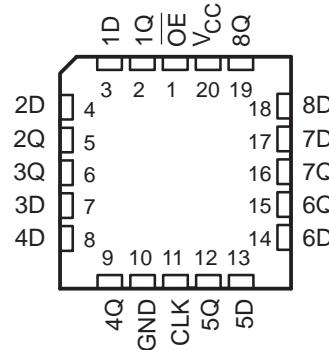
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT374 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT374A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT374 . . . J OR W PACKAGE  
SN74ABT374A . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABT374 . . . FK PACKAGE  
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

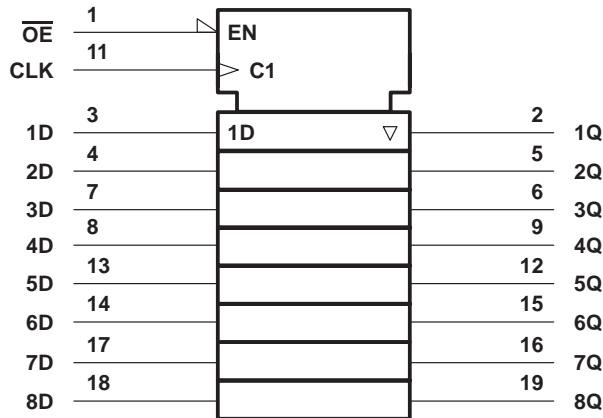
**SN54ABT374, SN74ABT374A  
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

SCBS111G – FEBRUARY 1991 – REVISED JANUARY 1997

FUNCTION TABLE  
(each flip-flop)

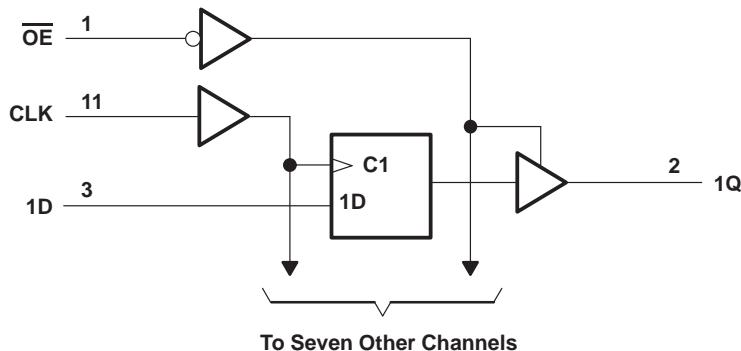
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



**SN54ABT374, SN74ABT374A**  
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V	
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V	
Current into any output in the low state, $I_O$ : SN54ABT374 .....	96 mA	
SN74ABT374A .....	128 mA	
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	115°C/W	
DW package .....	97°C/W	
N package .....	67°C/W	
PW package .....	128°C/W	
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

**recommended operating conditions (see Note 3)**

		SN54ABT374		SN74ABT374A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**SN54ABT374, SN74ABT374A  
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TA = 25°C			SN54ABT374		SN74ABT374A		UNIT
		MIN	TYPT†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5		2.5		2.5		V
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3		3		3		
	V <sub>CC</sub> = 4.5 V   I <sub>OH</sub> = -24 mA		2		2				
	I <sub>OH</sub> = -32 mA		2*				2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V   I <sub>OL</sub> = 48 mA			0.55		0.55			V
	I <sub>OL</sub> = 64 mA			0.55*				0.55	
V <sub>hys</sub>			100						mV
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1		±1		±1		µA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		10‡		10‡		10‡		µA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V		-10‡		-10‡		-10‡		µA
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V		±100				±100		µA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V   Outputs high			50		50		50	µA
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		250		250		250	µA
		Outputs low		30		30		30	mA
		Outputs disabled		250		250		250	µA
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		3.5						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		6.5						pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This data sheet limit may vary among suppliers.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

t <sub>clock</sub>	Clock frequency	SN54ABT374				UNIT	
		V <sub>CC</sub> = 5 V, TA = 25°C		MIN	MAX		
		MIN	MAX				
t <sub>w</sub>	Pulse duration	CLK high or low	3.3	3.3		ns	
t <sub>su</sub>	Setup time before CLK↑	Data high	2	2.5		ns	
		Data low	2	2.5			
t <sub>h</sub>	Hold time after CLK↑	Data high or low	2	2.5		ns	

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT374A			UNIT	
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	
			MIN	MAX			
f <sub>clock</sub>	Clock frequency		0	150	0	150	MHz
t <sub>W</sub>	Pulse duration	CLK high or low	3.3	3.3			ns
t <sub>su</sub>	Setup time before CLK↑	Data high	1	1			ns
		Data low	1.9	1.9			
t <sub>h</sub>	Hold time after CLK↑	Data high or low	2.1†	2.1†			ns

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT374			UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX
			MIN	TYP	MAX	
f <sub>max</sub>			150	200	150	MHz
t <sub>PLH</sub>	CLK	Q	2.2	4.2	5.7	ns
			3.1	5.1	6.6	
t <sub>PHL</sub>	OE	Q	1.2	3.2	4.7	ns
			2.3	4.7	6.2	
t <sub>PZH</sub>	OE	Q	2.3	4.5	6.1	ns
			1.9	4.5	6	
t <sub>PZL</sub>					1	7
t <sub>PHZ</sub>						
t <sub>PLZ</sub>						

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

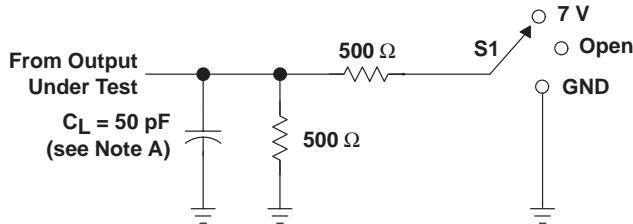
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT374A			UNIT
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX
			MIN	TYP	MAX	
f <sub>max</sub>			150	200	150	MHz
t <sub>PLH</sub>	CLK	Q	2.2	4.2	5.7	ns
			3.1	5.1	6.6	
t <sub>PHL</sub>	OE	Q	1.2	3.2	4.7	ns
			2.7	4.7	6.2	
t <sub>PZH</sub>	OE	Q	2.5	4.5	6	ns
			2	4.5	6	
t <sub>PZL</sub>						
t <sub>PHZ</sub>						
t <sub>PLZ</sub>						

† This data sheet limit may vary among suppliers.

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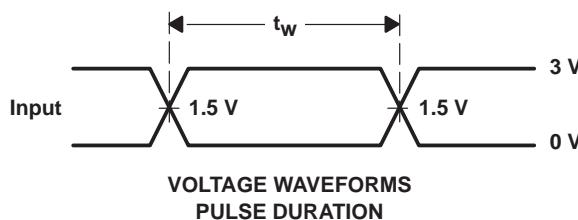
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**PARAMETER MEASUREMENT INFORMATION**

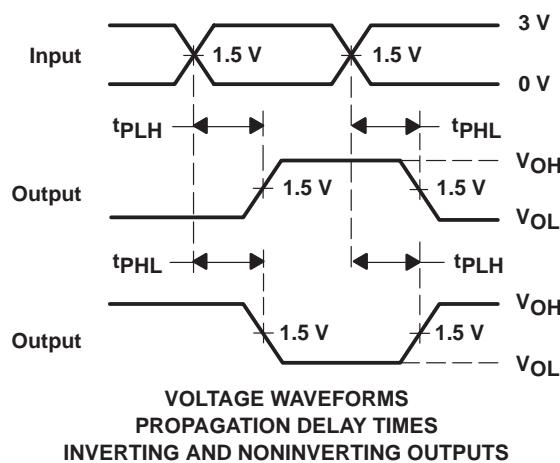
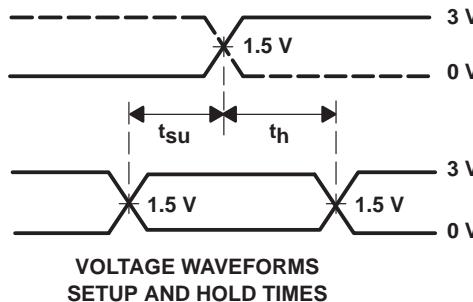


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

LOAD CIRCUIT



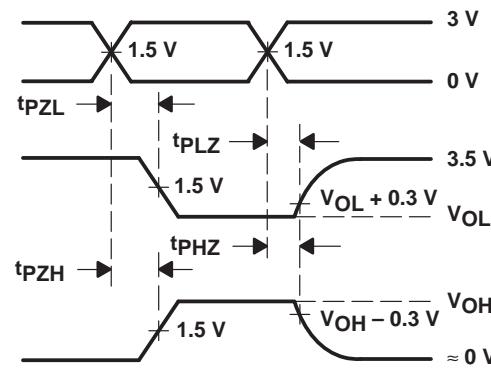
Timing Input



Output Control

Output Waveform 1  
S1 at 7 V  
(see Note B)

Output Waveform 2  
S1 at Open  
(see Note B)



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9314901Q2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9314901Q2A SNJ54ABT374FK
5962-9314901QRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9314901QR A SNJ54ABT374J
5962-9314901QSA	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9314901QS A SNJ54ABT374W
SN74ABT374ABR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SN74ABT374ABR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SN74ABT374ABRG4	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SN74ABT374ABRG4.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SN74ABT374ADW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374ADW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374ADWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374ADWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374ADWRE4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374ADWRG4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374AN	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT374AN
SN74ABT374AN.B	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT374AN
SN74ABT374ANSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374ANSR.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT374A
SN74ABT374APW	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SN74ABT374APW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SN74ABT374APWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SN74ABT374APWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB374A
SNJ54ABT374FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9314901Q2A SNJ54ABT374FK

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ABT374J	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9314901QR A SNJ54ABT374J
SNJ54ABT374W	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9314901QS A SNJ54ABT374W

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

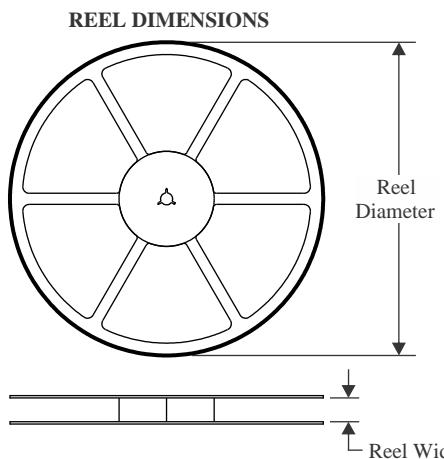
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

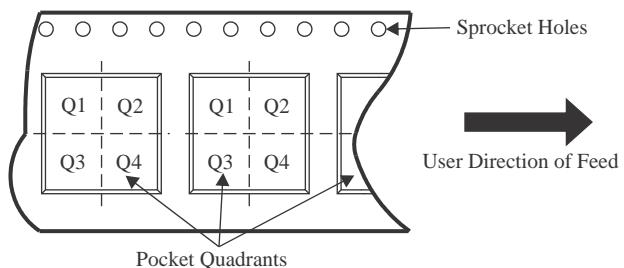
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT374ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT374ADBRG4	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT374ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ABT374APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT374ABR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT374ADB RG4	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT374ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ABT374ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ABT374APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9314901Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9314901QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ABT374ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT374ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT374AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT374AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT374APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74ABT374APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT374FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT374W	W	CFP	20	25	506.98	26.16	6220	NA

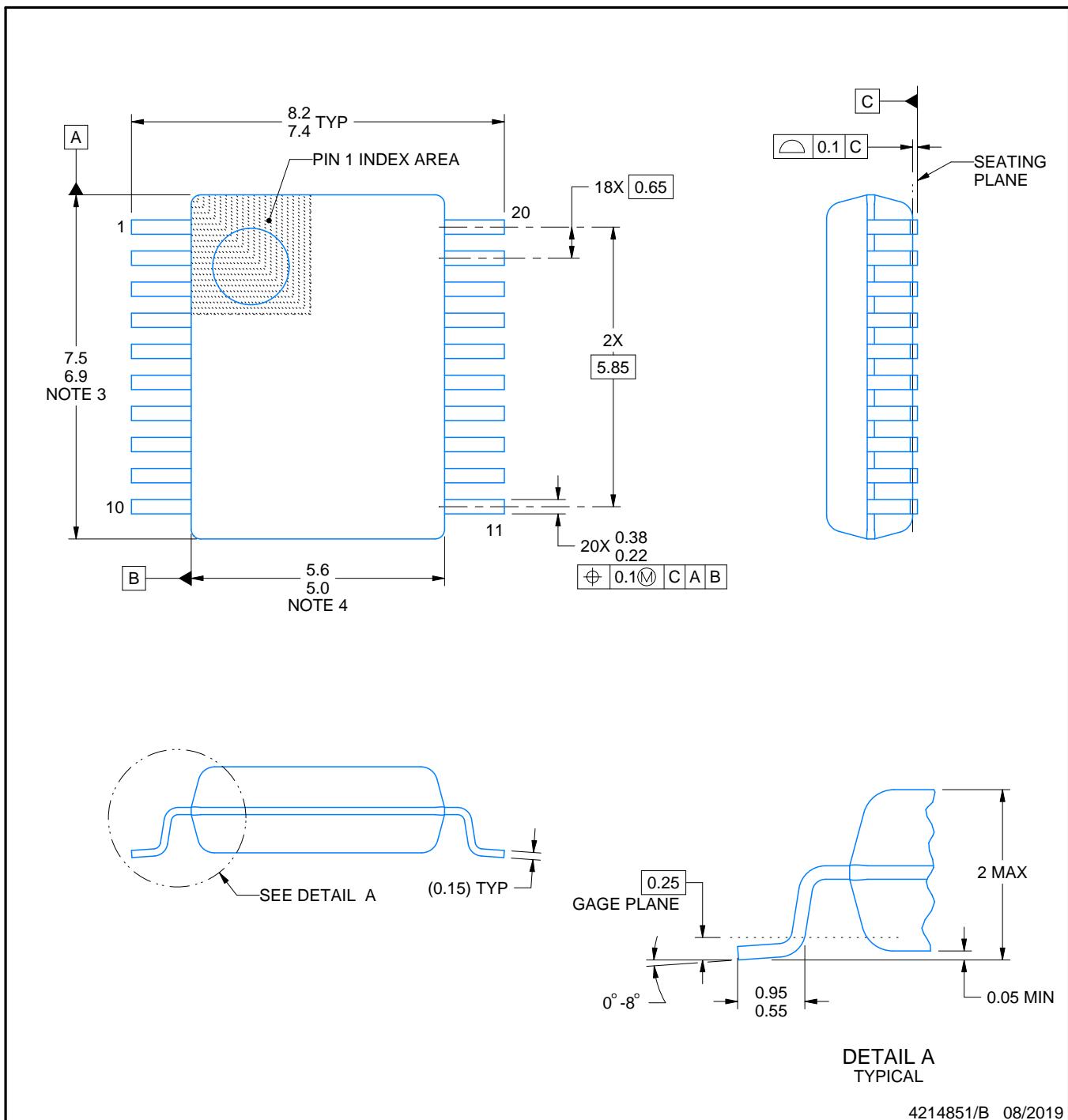
# PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

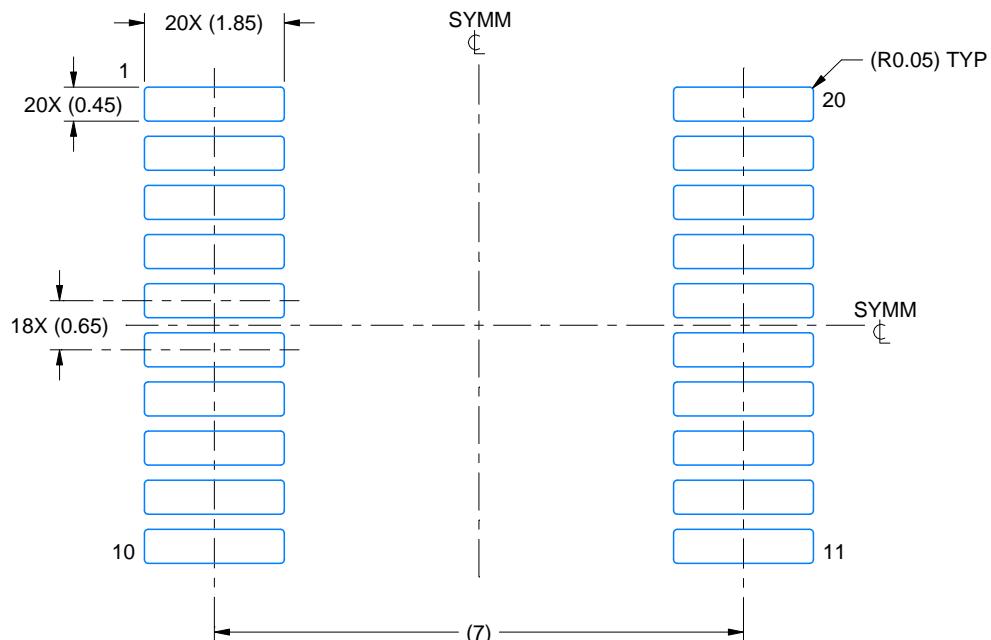
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

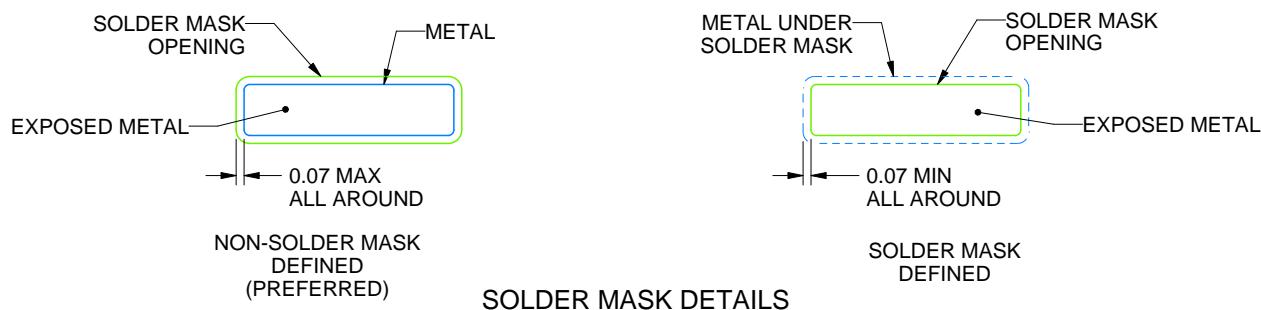
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

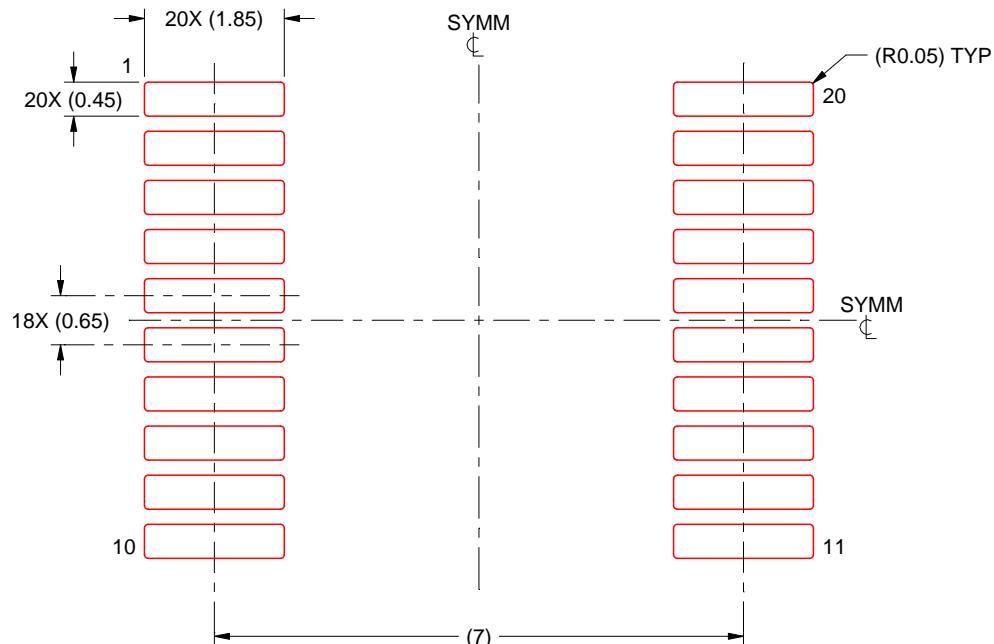
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

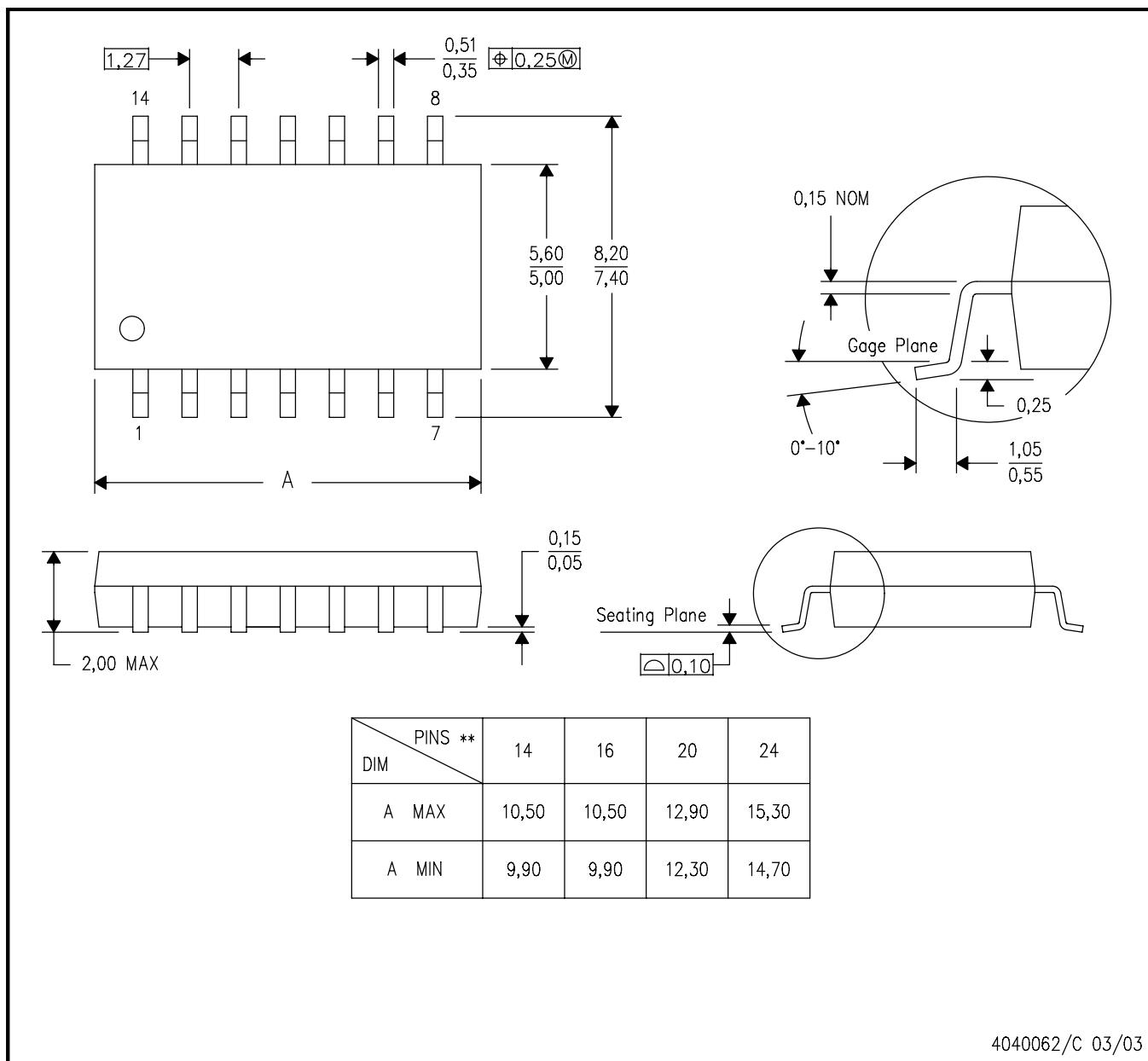
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



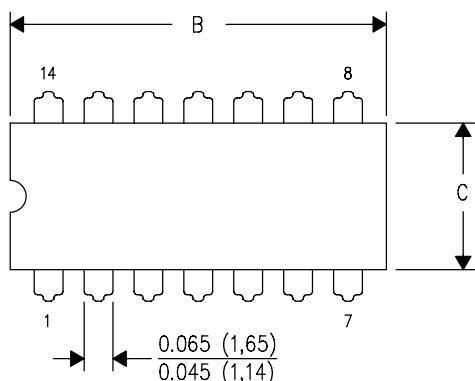
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

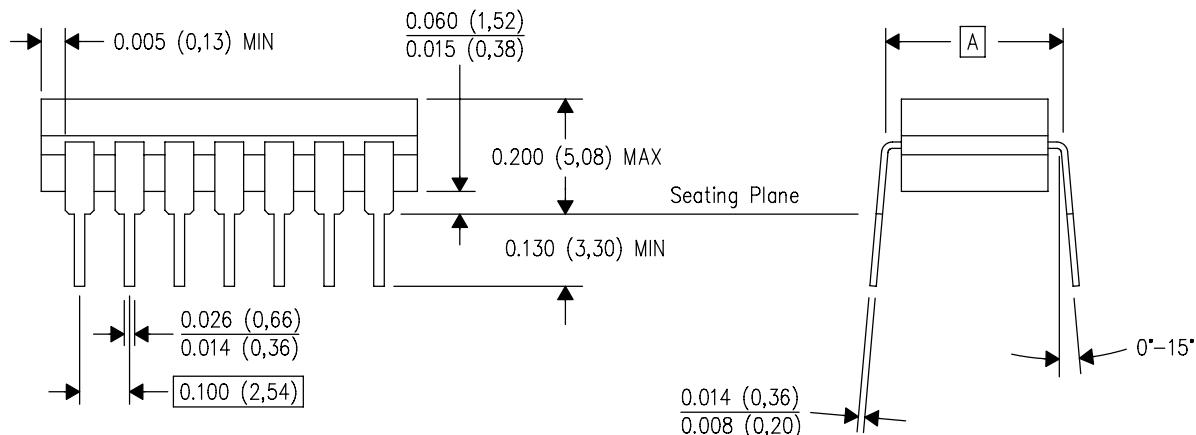
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# GENERIC PACKAGE VIEW

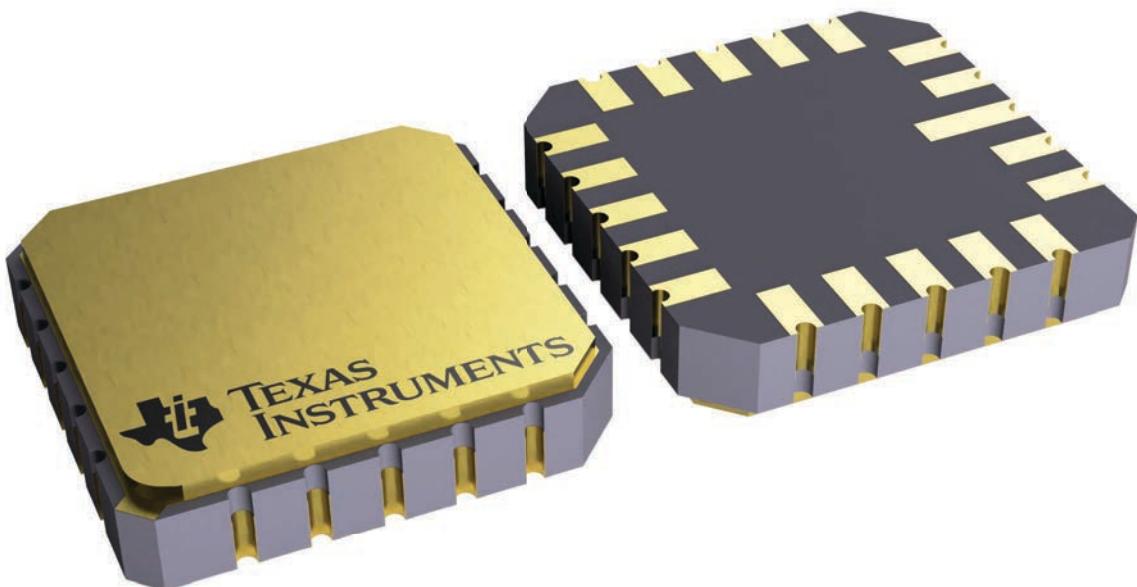
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

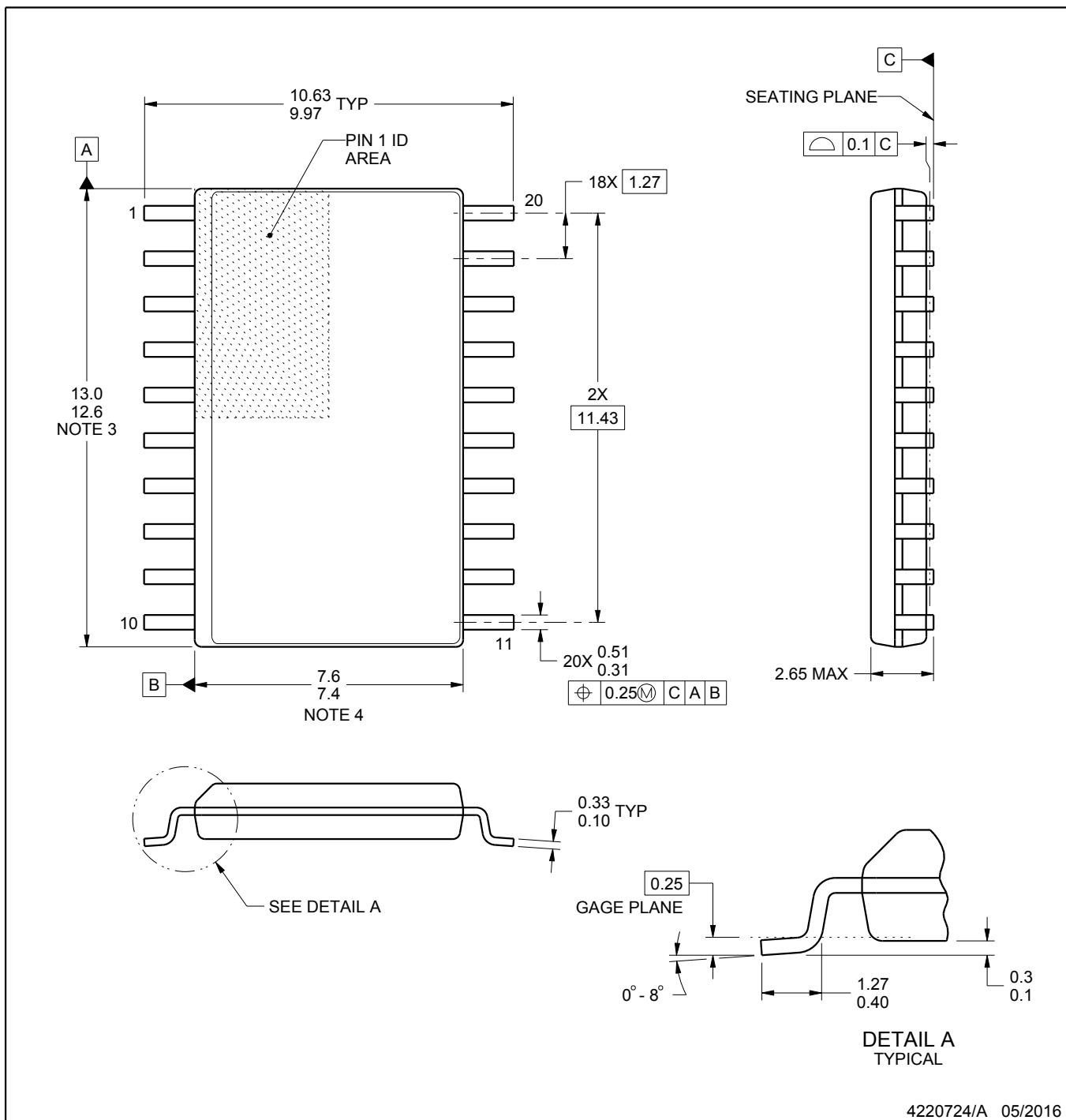
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

## NOTES:

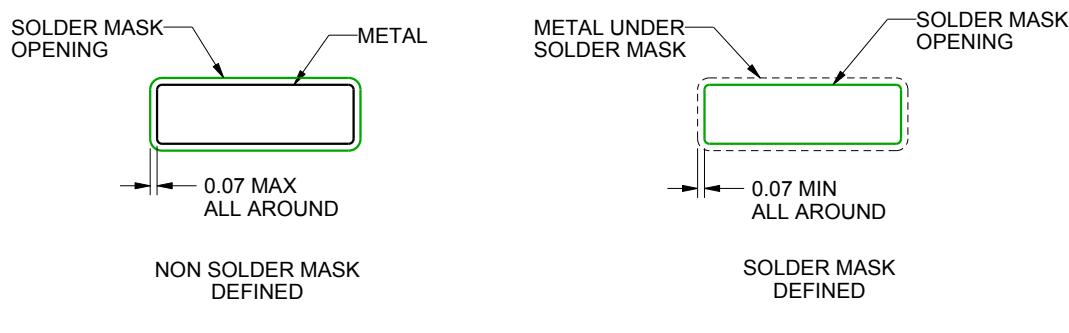
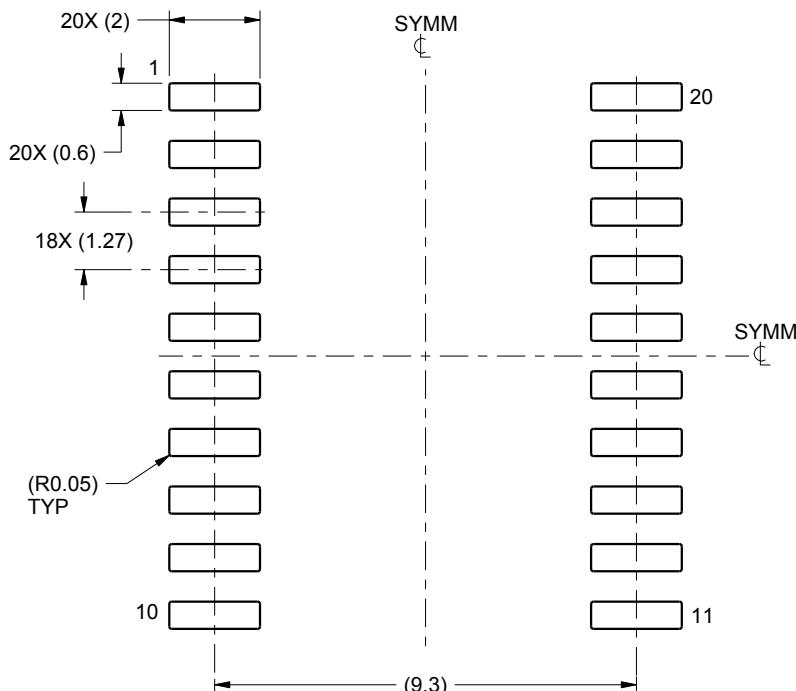
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

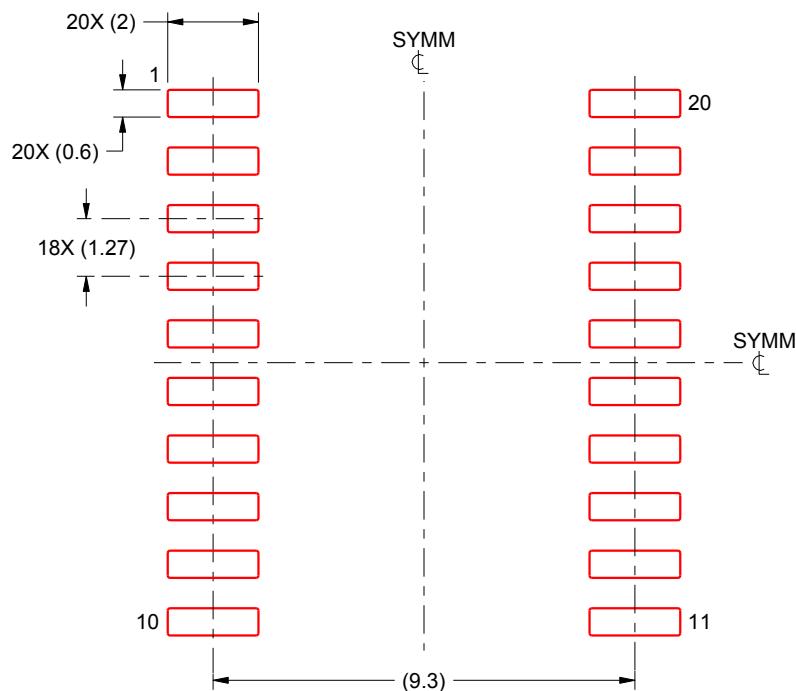
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

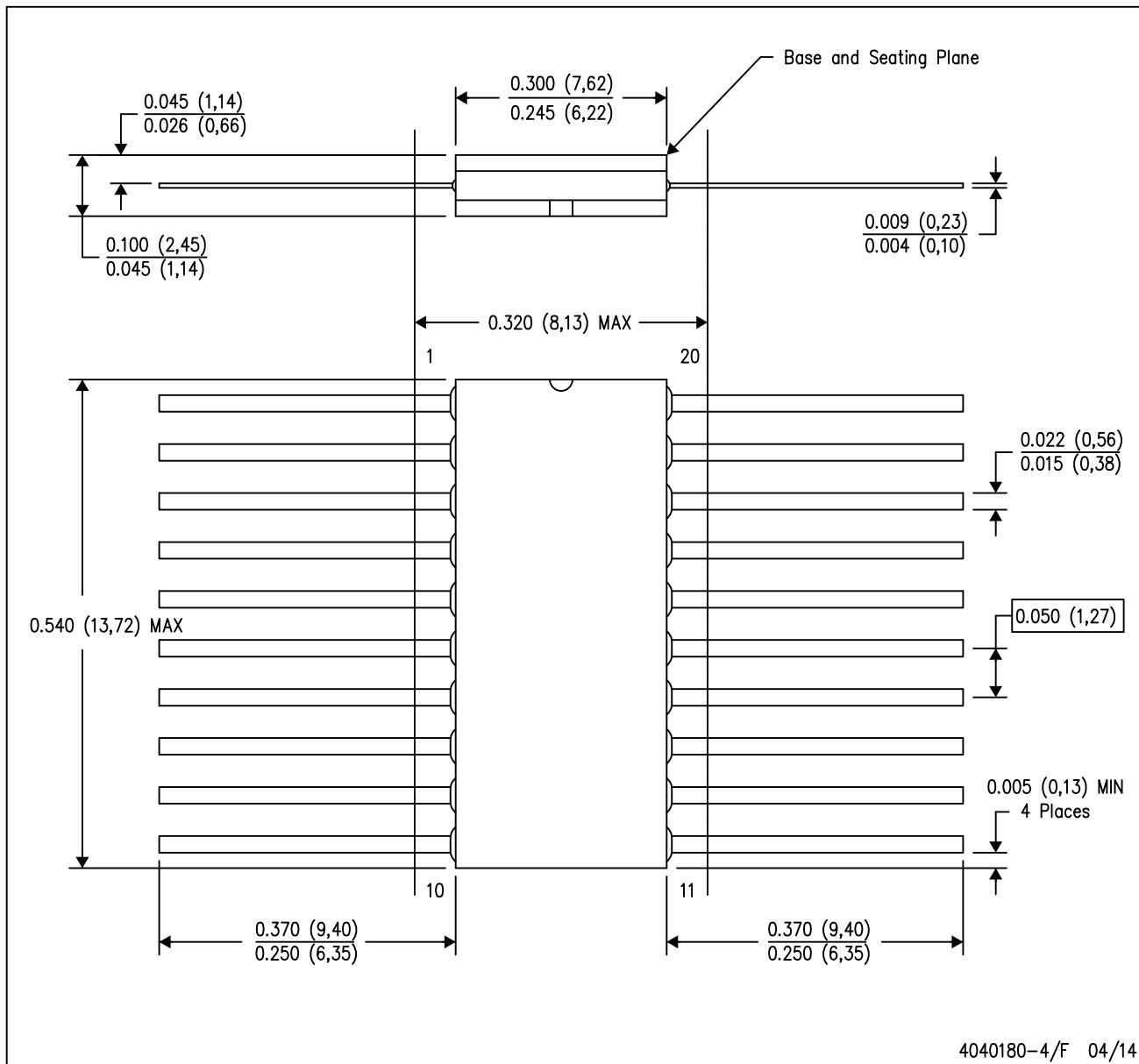
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

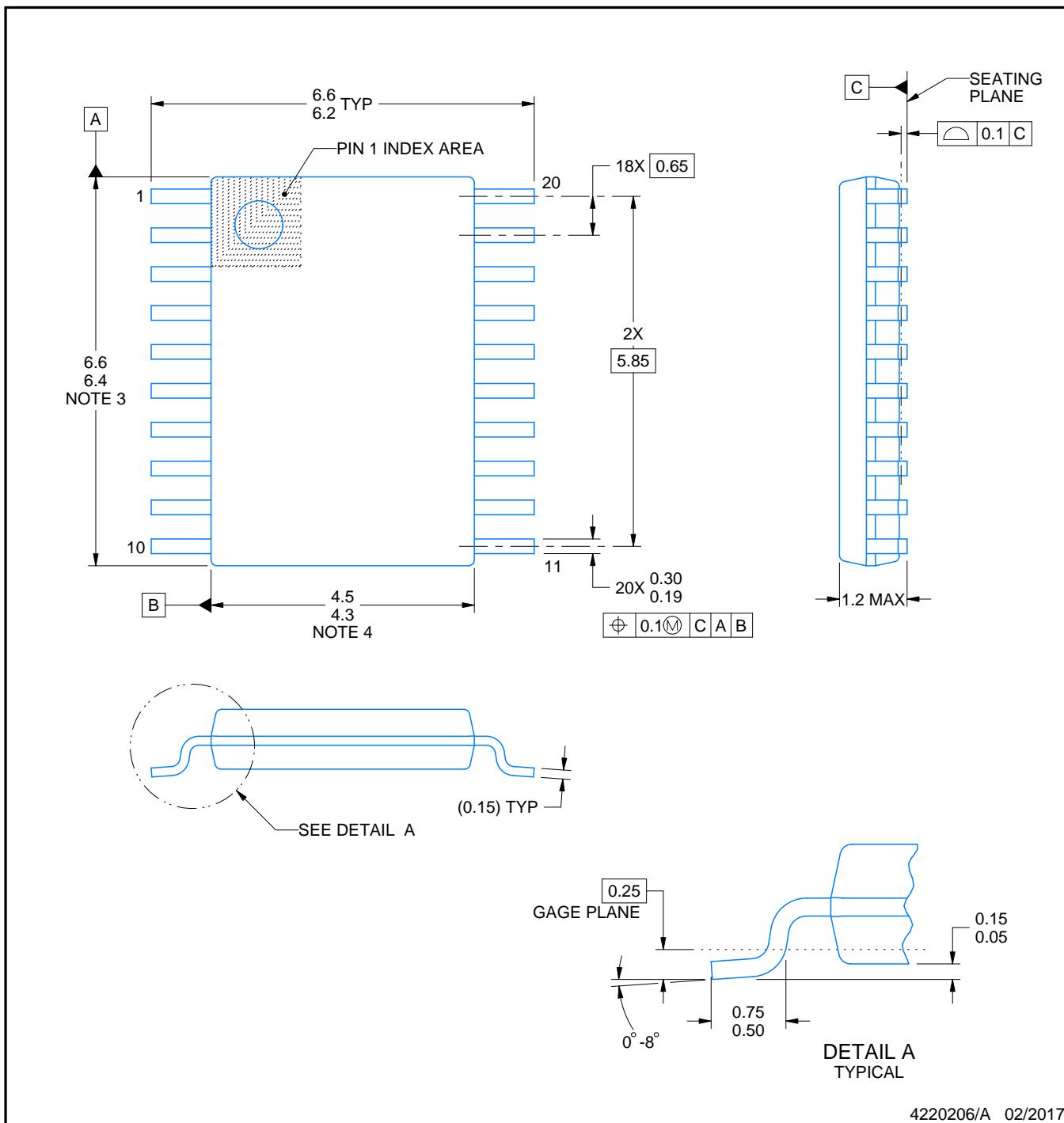
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

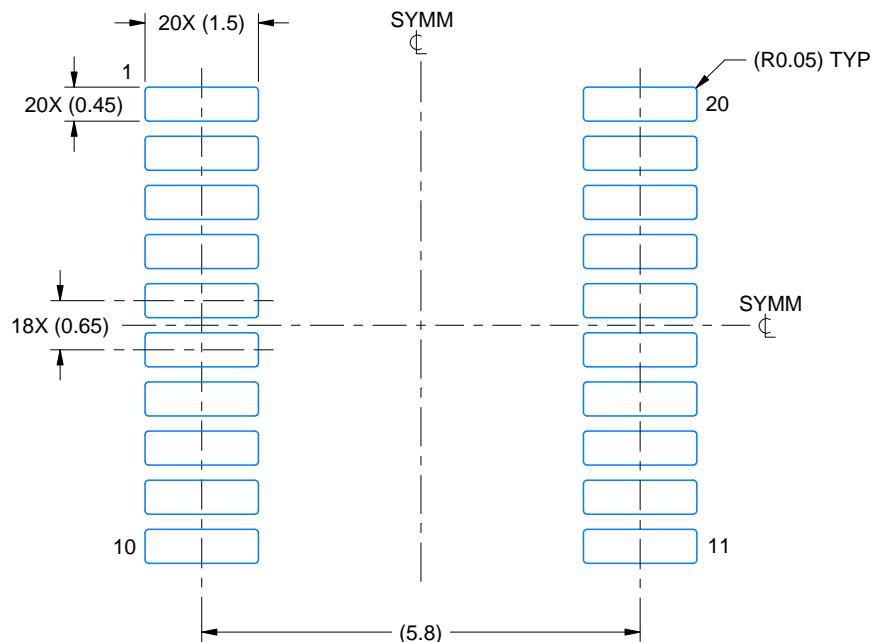
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

## EXAMPLE BOARD LAYOUT

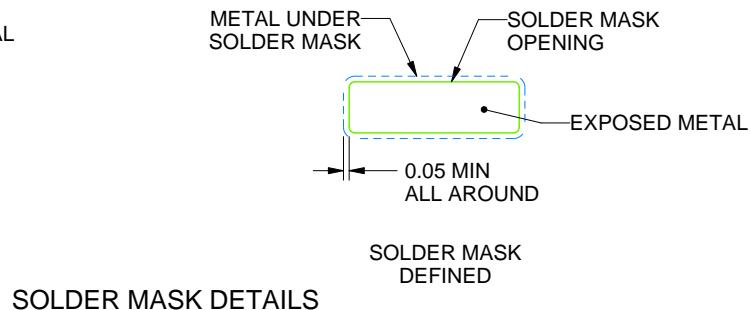
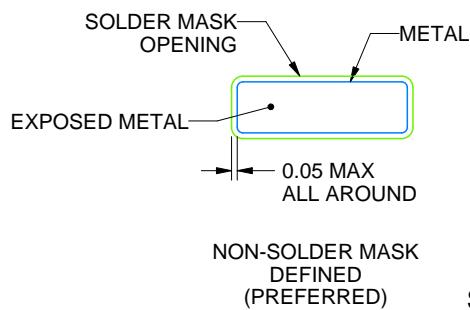
**PW0020A**

## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

#### NOTES: (continued)

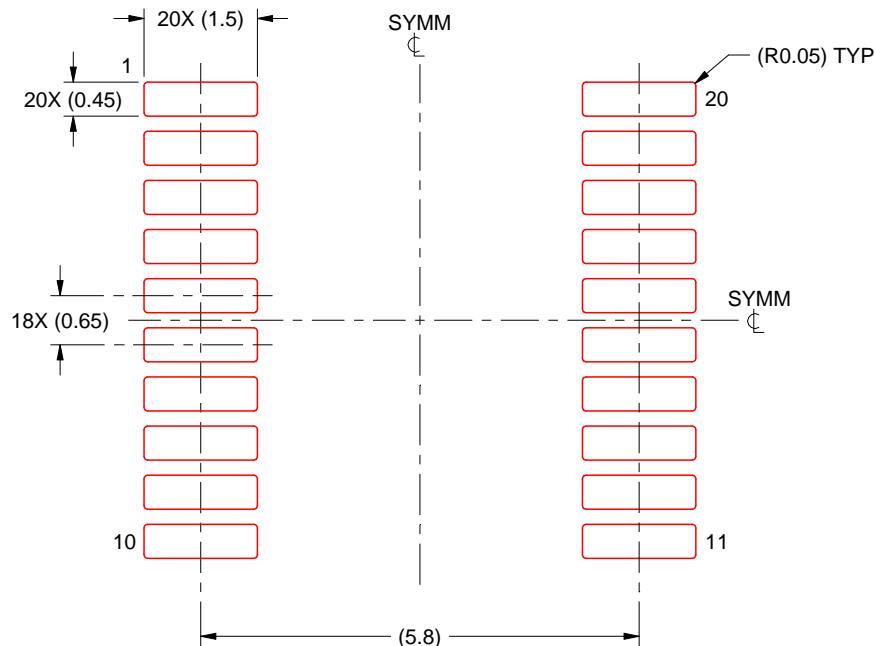
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025