

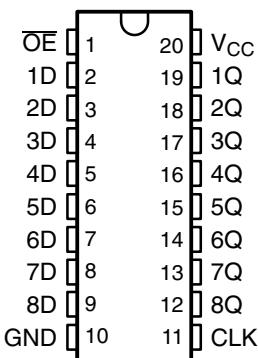
SN54ABT574, SN74ABT574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS191F – JANUARY 1991 – REVISED SEPTEMBER 2003

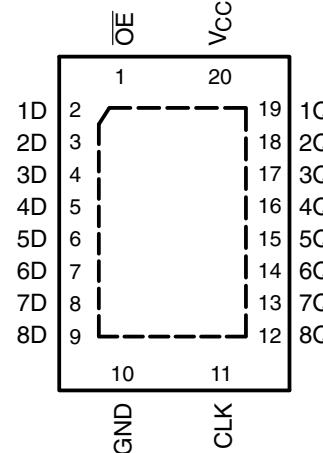
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54ABT574 . . . J OR W PACKAGE
SN74ABT574A . . . DB, DW, N, NS,
OR PW PACKAGE

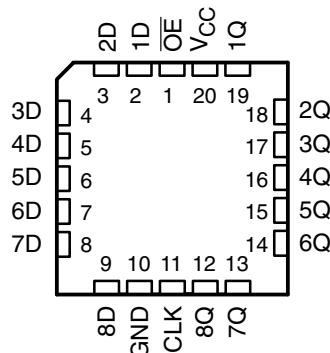
(TOP VIEW)



SN74ABT574A . . . RGY PACKAGE
(TOP VIEW)



SN54ABT574 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ABT574AN	SN74ABT574AN
	QFN – RGY	Tape and reel	SN74ABT574ARGYR	AB574A
	SOIC – DW	Tube	SN74ABT574ADW	
		Tape and reel	SN74ABT574ADWR	ABT574A
	SOP – NS	Tape and reel	SN74ABT574ANSR	ABT574A
	SSOP – DB	Tape and reel	SN74ABT574ADBR	AB574A
	TSSOP – PW	Tube	SN74ABT574APW	
		Tape and reel	SN74ABT574APWR	AB574A
	VFBGA – GQN		SN74ABT574AGQNR	
		Tape and reel	SN74ABT574AZQNR	AB574A
-55°C to 125°C	CDIP – J	Tube	SNJ54ABT574J	SNJ54ABT574J
	CFP – W	Tube	SNJ54ABT574W	SNJ54ABT574W
	LCCC – FK	Tube	SNJ54ABT574FK	SNJ54ABT574FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The eight flip-flops of the SN54ABT574 and SN74ABT574A are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

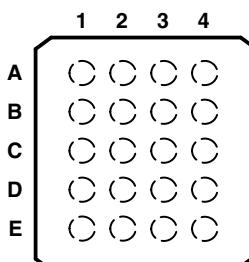
\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

SN74ABT574A . . . GQN OR ZQN PACKAGE

(TOP VIEW)



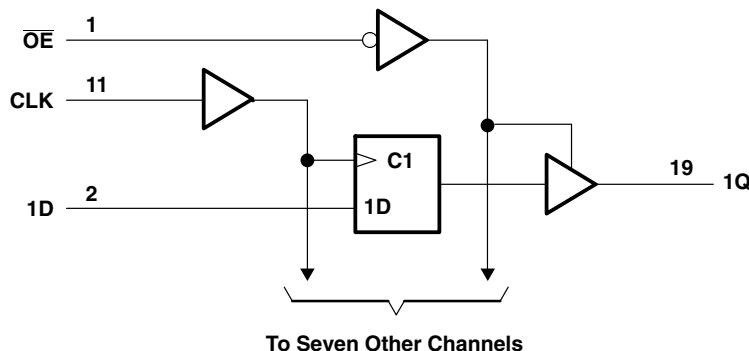
terminal assignments

	1	2	3	4
A	1D	\overline{OE}	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	CLK	8Q

FUNCTION TABLE (each flip-flop)

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, N, NS, PW, RGY, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JEDEC 51-7.
 3. The package thermal impedance is calculated in accordance with JEDEC 51-5.

recommended operating conditions (see Note 4)

		SN54ABT574		SN74ABT574A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2	V
V _{IL}	Low-level input voltage			0.8	0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			-24	-32	mA
I _{OL}	Low-level output current			48	64	mA
Δt/ΔV	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT574		SN74ABT574A		UNIT
		MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2		-1.2		-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -3 \text{ mA}$		2.5		2.5		2.5		V
	$V_{CC} = 5 \text{ V}$, $I_{OH} = -3 \text{ mA}$		3		3		3		
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2		2				
		$I_{OH} = -32 \text{ mA}$	2*				2		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 48 \text{ mA}$		0.55		0.55			V
		$I_{OL} = 64 \text{ mA}$		0.55*				0.55	
V_{hys}			100						mV
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = V_{CC}$ or GND			± 1		± 1		± 1	μA
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			10 [‡]		10 [‡]		10 [‡]	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.5 \text{ V}$			-10 [‡]		-10 [‡]		-10 [‡]	μA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5 \text{ V}$			± 100		± 500		± 100	μA
I_{CEX}	$V_{CC} = 5.5 \text{ V}$, $V_O = 5.5 \text{ V}$	Outputs high		50		50		50	μA
$I_O^§$	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high	1	250		250		250	μA
		Outputs low	24	30		30		30	mA
		Outputs disabled	0.5	250		250		250	μA
$\Delta I_{CC}^{¶}$	$V_{CC} = 5.5 \text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5		1.5		1.5	mA
C_i	$V_I = 2.5 \text{ V}$ or 0.5 V			3.5					pF
C_o	$V_O = 2.5 \text{ V}$ or 0.5 V			6.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5 \text{ V}$.

‡ This data-sheet limit may vary among suppliers.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ABT574			UNIT	
		$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$		MIN		
		MIN	MAX			
f_{clock}	Clock frequency		150	150	MHz	
t_w	Pulse duration, CLK high or low		3.3	3.3	ns	
t_{su}	Setup time, data before CLK↑	High	1.5	1.5	ns	
		Low	2	2		
t_h	Hold time, data after CLK↑	High or low	2	2	ns	

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN74ABT574A			UNIT
				V _{CC} = 5 V, T _A = 25°C		MIN	MAX
				MIN	MAX		
f _{clock}	Clock frequency			150	150	150	MHz
t _w	Pulse duration, CLK high or low			3.3	3.3	3.3	ns
t _{su}	Setup time, data before CLK↑		High	1	1	1	ns
			Low	1.5	1.5	1.5	
t _h	Hold time, data after CLK↑	High or low		1.8 [†]	1.8 [†]	1.8 [†]	ns

[†] This data-sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT574			UNIT	
			V _{CC} = 5 V, T _A = 25°C		MIN	MAX	
			MIN	TYP			
f _{max}			150	200	150	150	MHz
t _{PLH}	CLK	Q	2.2	3.9	6.2	2.2	ns
			3	4.8	7	3	
t _{PHL}	OE	Q	1	3.3	5	1	ns
			2.5	4.7	5.9	2.5	
t _{PZH}	OE	Q	2.4	4.9	6.2	2.4	ns
			2	4	5.8	2	
t _{PZL}	OE	Q	2.4	4.9	6.2	2.4	ns
			2	4	5.8	2	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

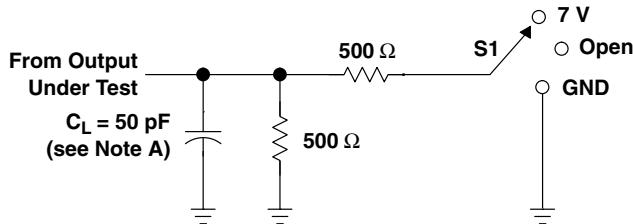
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT574A			UNIT	
			V _{CC} = 5 V, T _A = 25°C		MIN	MAX	
			MIN	TYP			
f _{max}			150	200	150	150	MHz
t _{PLH}	CLK	Q	2.2	3.9	6.2	2.2	ns
			3	4.8	6.6	3	
t _{PHL}	OE	Q	1	3.3	4.3	1	ns
			2.1 [†]	4.7	5.9	2.1 [†]	
t _{PZH}	OE	Q	2.4	4.9	6.2	2.4	ns
			2	4	5.8	2	
t _{PZL}	OE	Q	2.4	4.9	6.2	2.4	ns
			2	4	5.8	2	

[†] This data-sheet limit may vary among suppliers.

SN54ABT574, SN74ABT574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

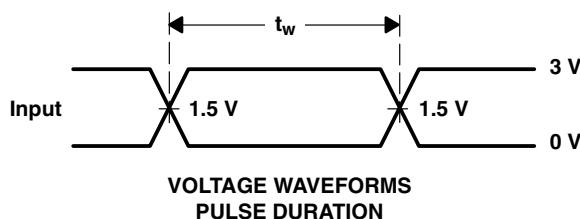
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PARAMETER MEASUREMENT INFORMATION

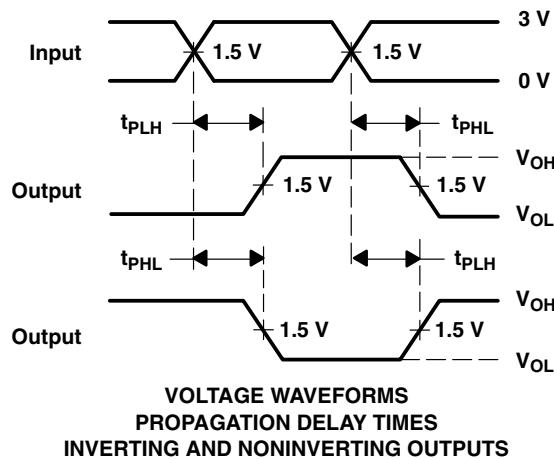
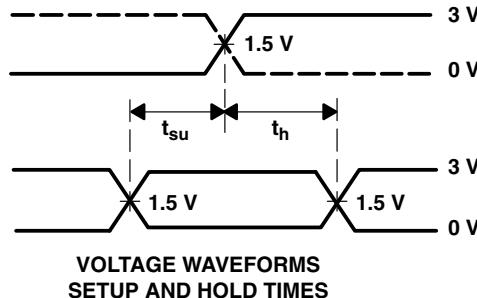


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT



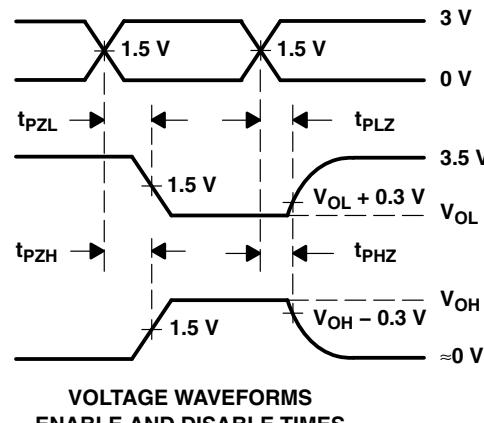
Timing Input



Output Control

Output Waveform 1
S1 at 7 V
(see Note B)

Output Waveform 2
S1 at Open
(see Note B)



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9322001Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322001Q2A SNJ54ABT574FK
5962-9322001QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322001QR A SNJ54ABT574J
5962-9322001QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322001QS A SNJ54ABT574W
SN74ABT574ABR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SN74ABT574ABR.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SN74ABT574ABRG4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SN74ABT574ABRG4.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SN74ABT574ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT574A
SN74ABT574ADW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT574A
SN74ABT574ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT574A
SN74ABT574ADWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT574A
SN74ABT574ADWRE4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT574A
SN74ABT574AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT574AN
SN74ABT574AN.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT574AN
SN74ABT574ANE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT574AN
SN74ABT574ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT574A
SN74ABT574ANSR.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT574A
SN74ABT574APW	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SN74ABT574APW.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SN74ABT574APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SN74ABT574APWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB574A
SNJ54ABT574FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322001Q2A SNJ54ABT574FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ABT574J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322001QR A SNJ54ABT574J
SNJ54ABT574W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322001QS A SNJ54ABT574W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

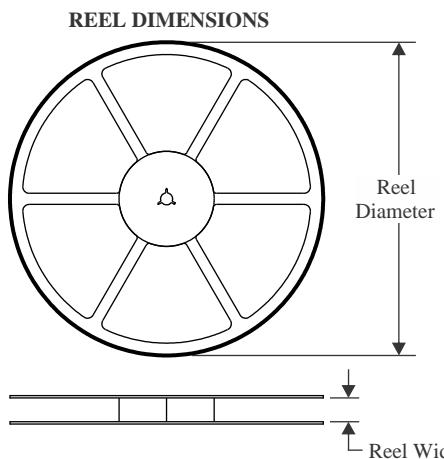
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

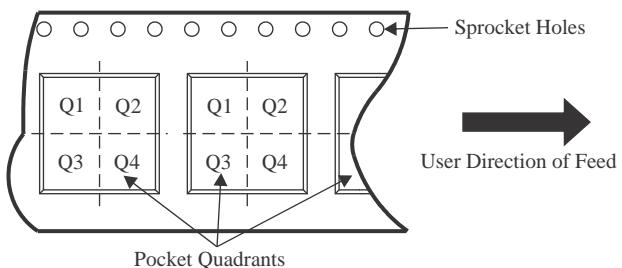
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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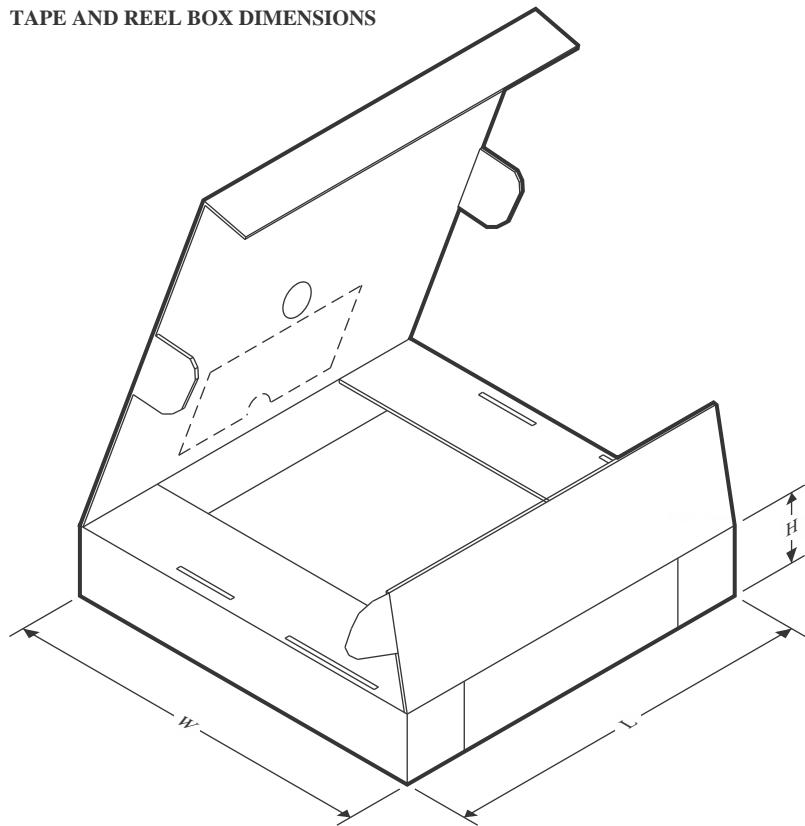
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


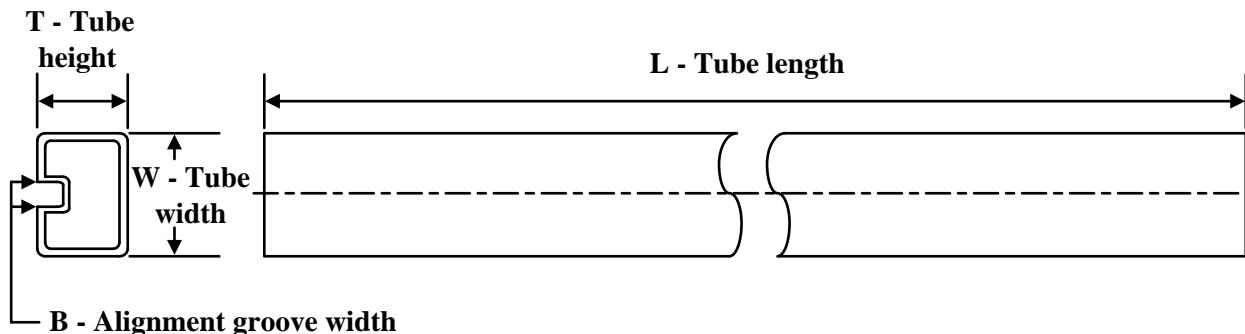
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT574ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT574ADBRG4	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT574ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT574ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ABT574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT574ABR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT574ADB RG4	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT574ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ABT574ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ABT574APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

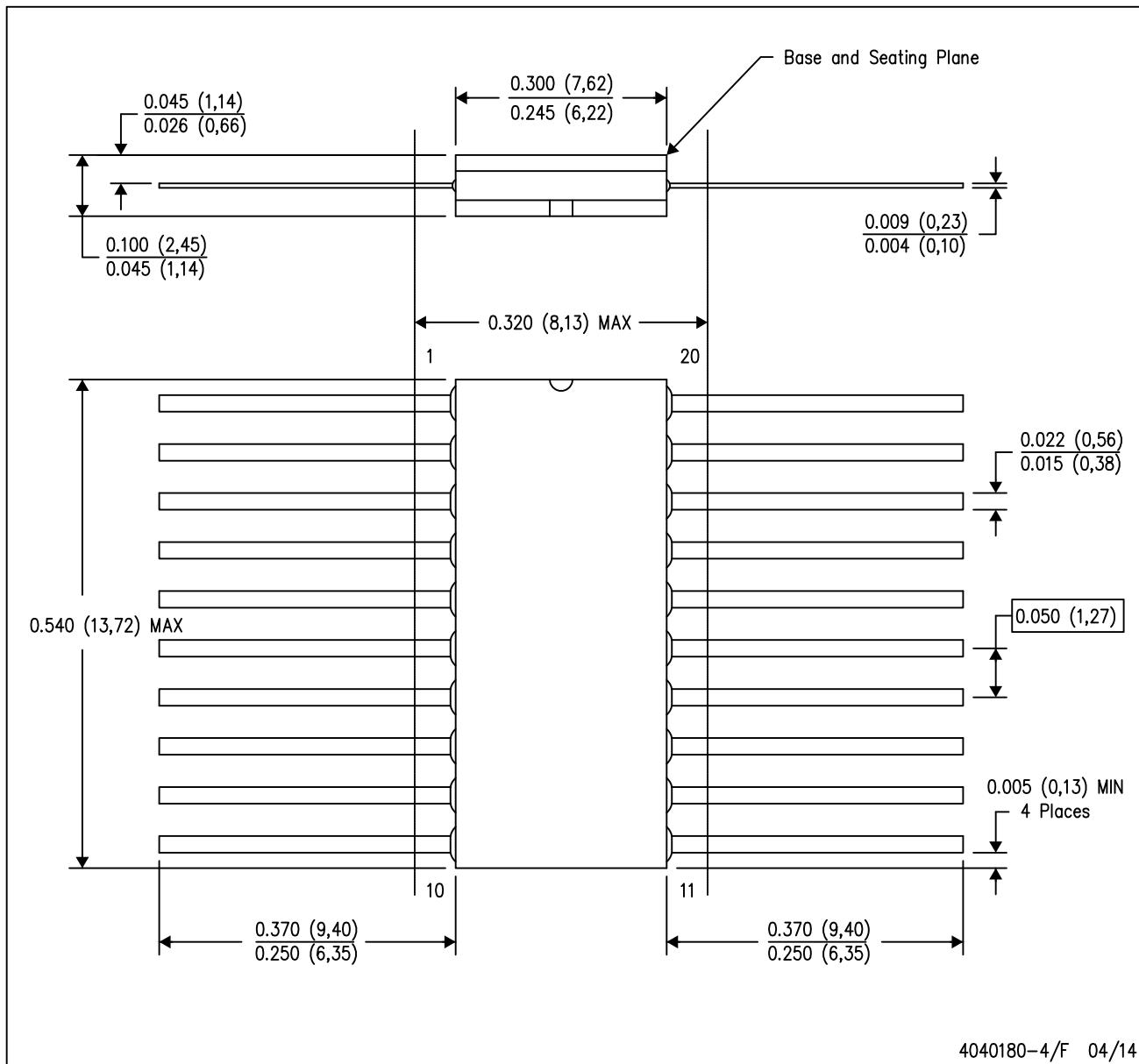
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-9322001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9322001QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ABT574ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT574ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT574AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT574AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT574ANE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT574APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74ABT574APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT574FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT574W	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

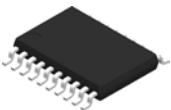


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

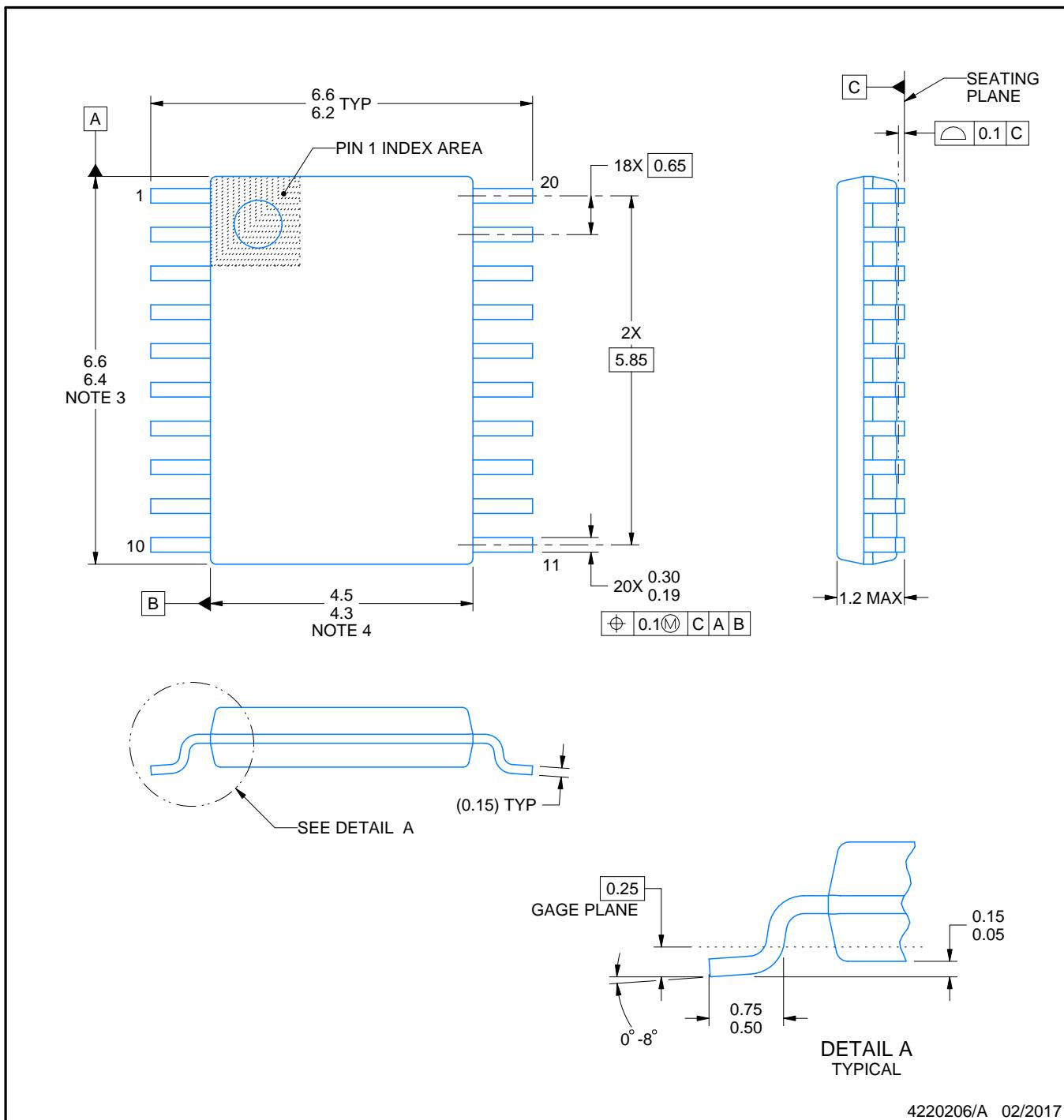
PACKAGE OUTLINE

PW0020A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

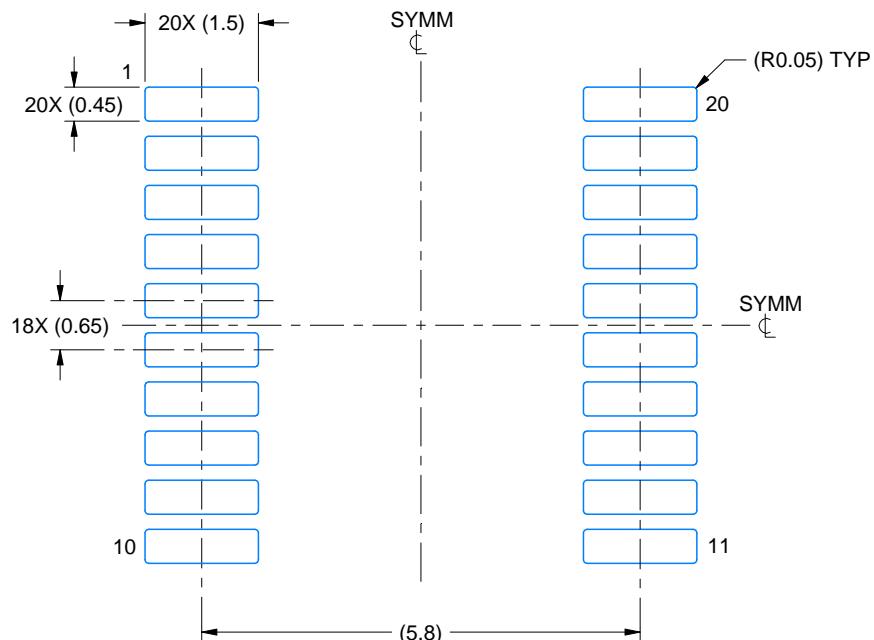
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

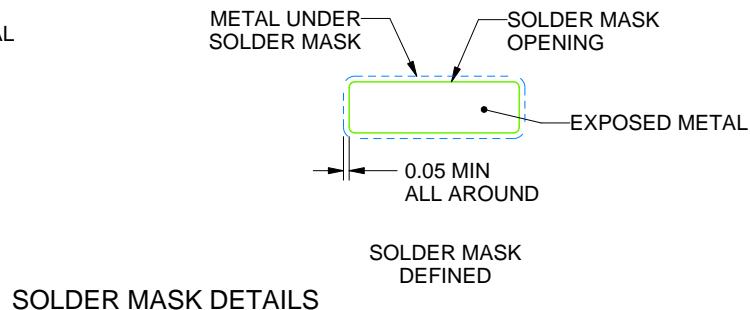
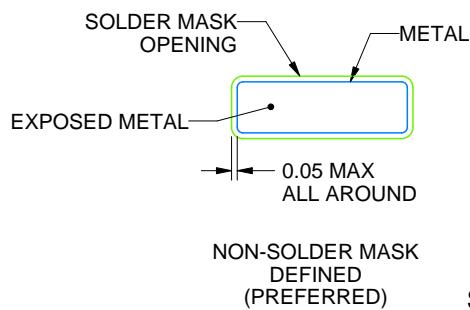
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

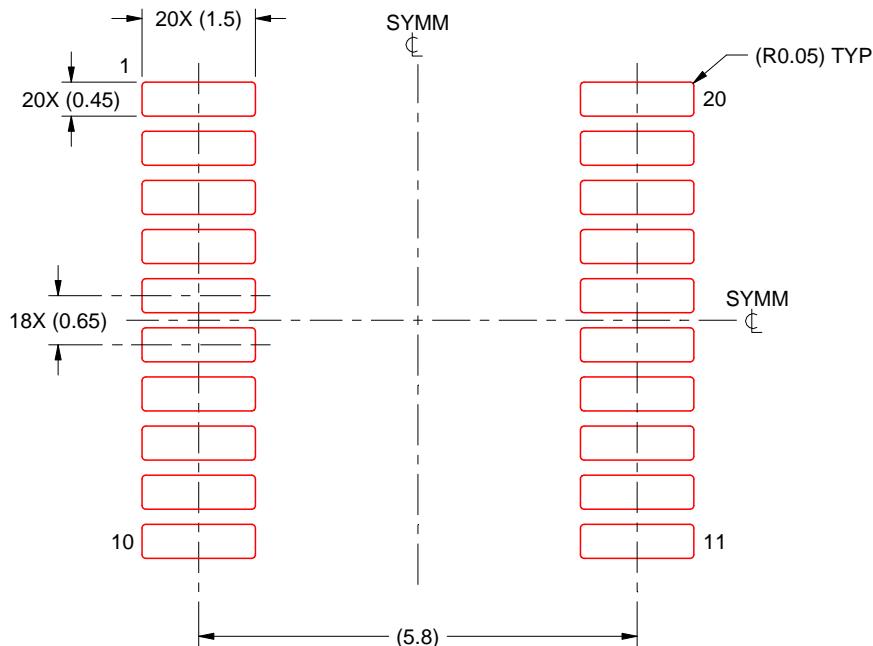
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

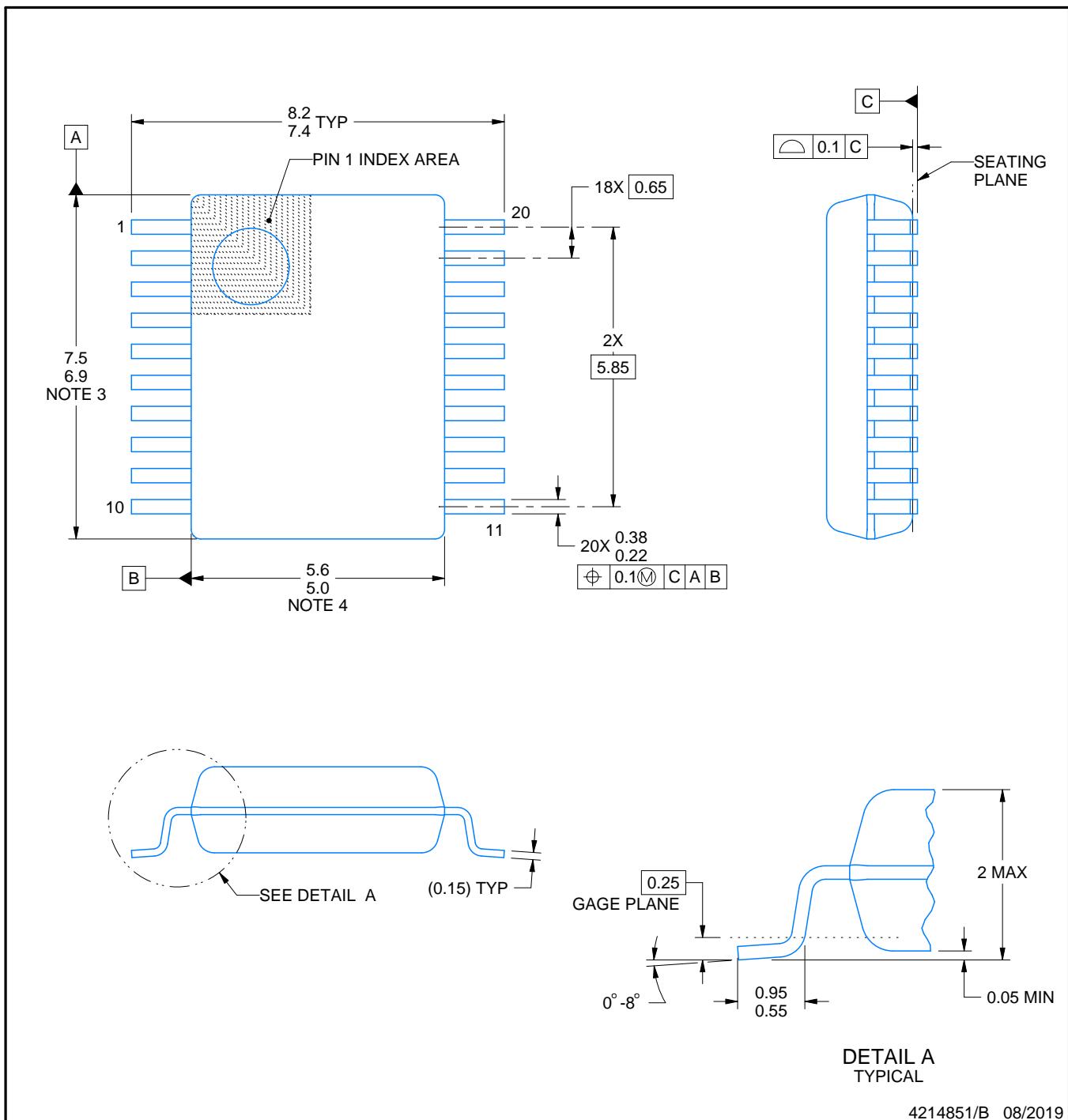
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

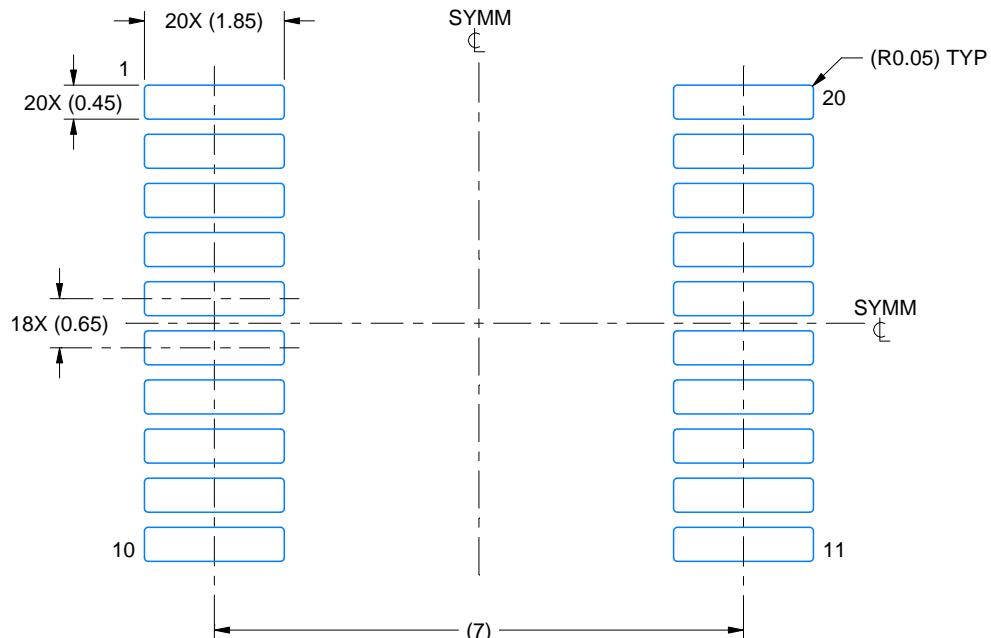
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

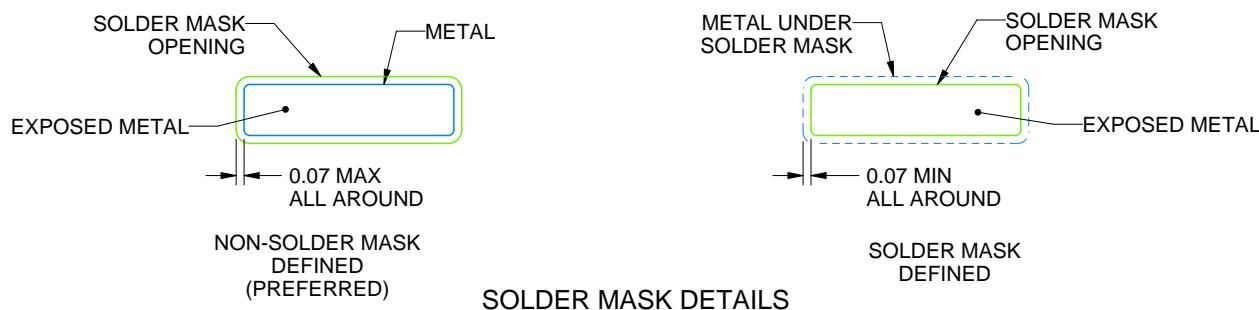
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

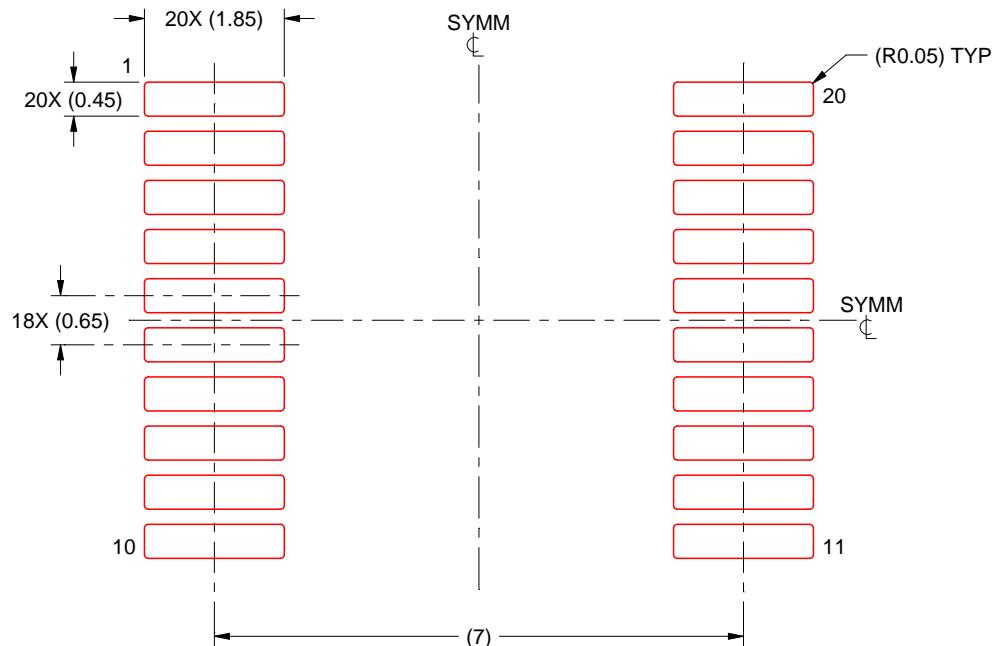
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

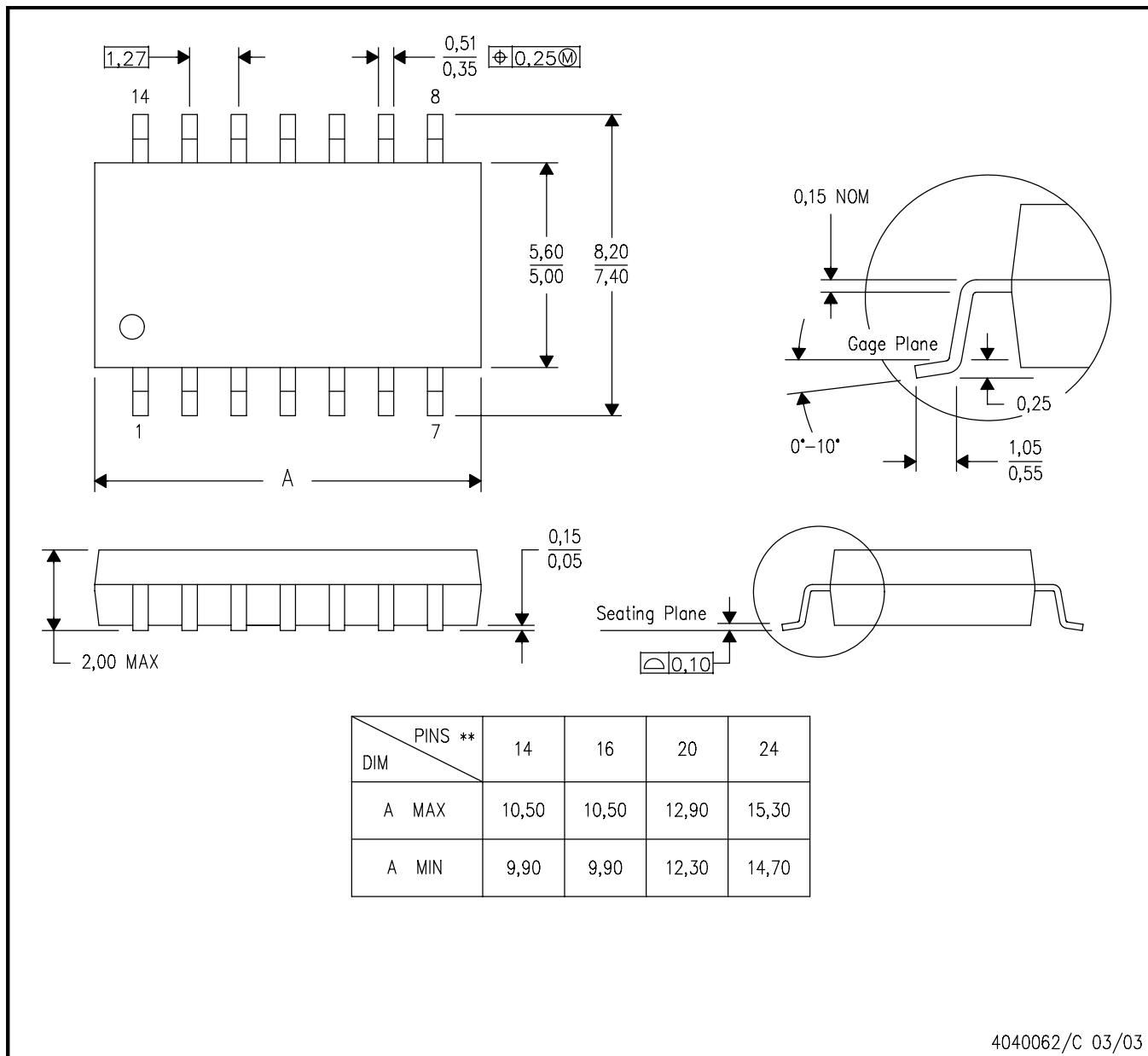
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

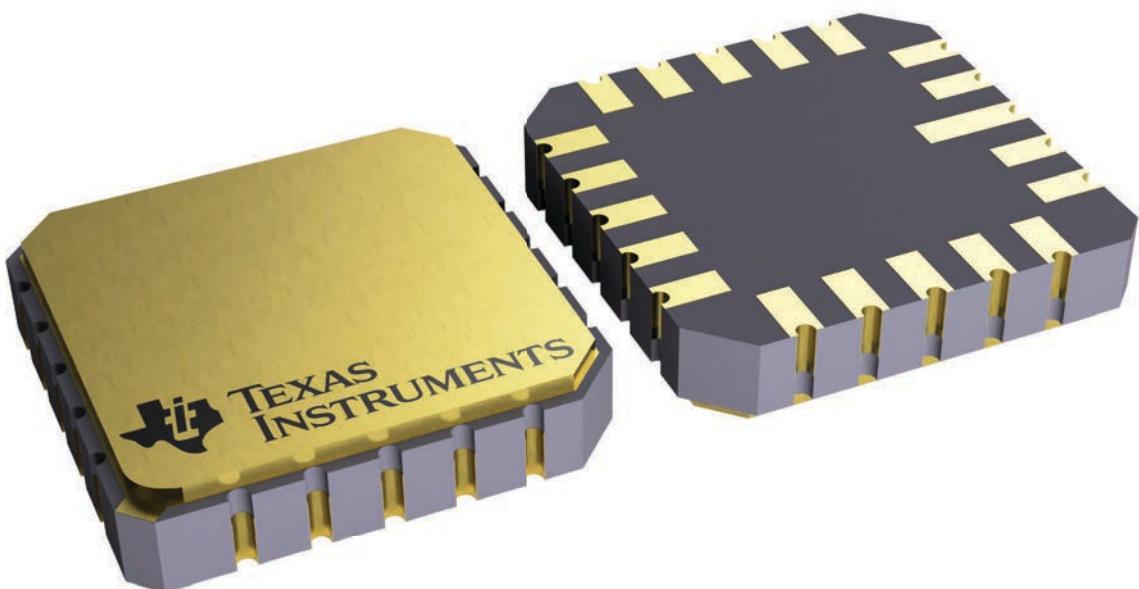
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

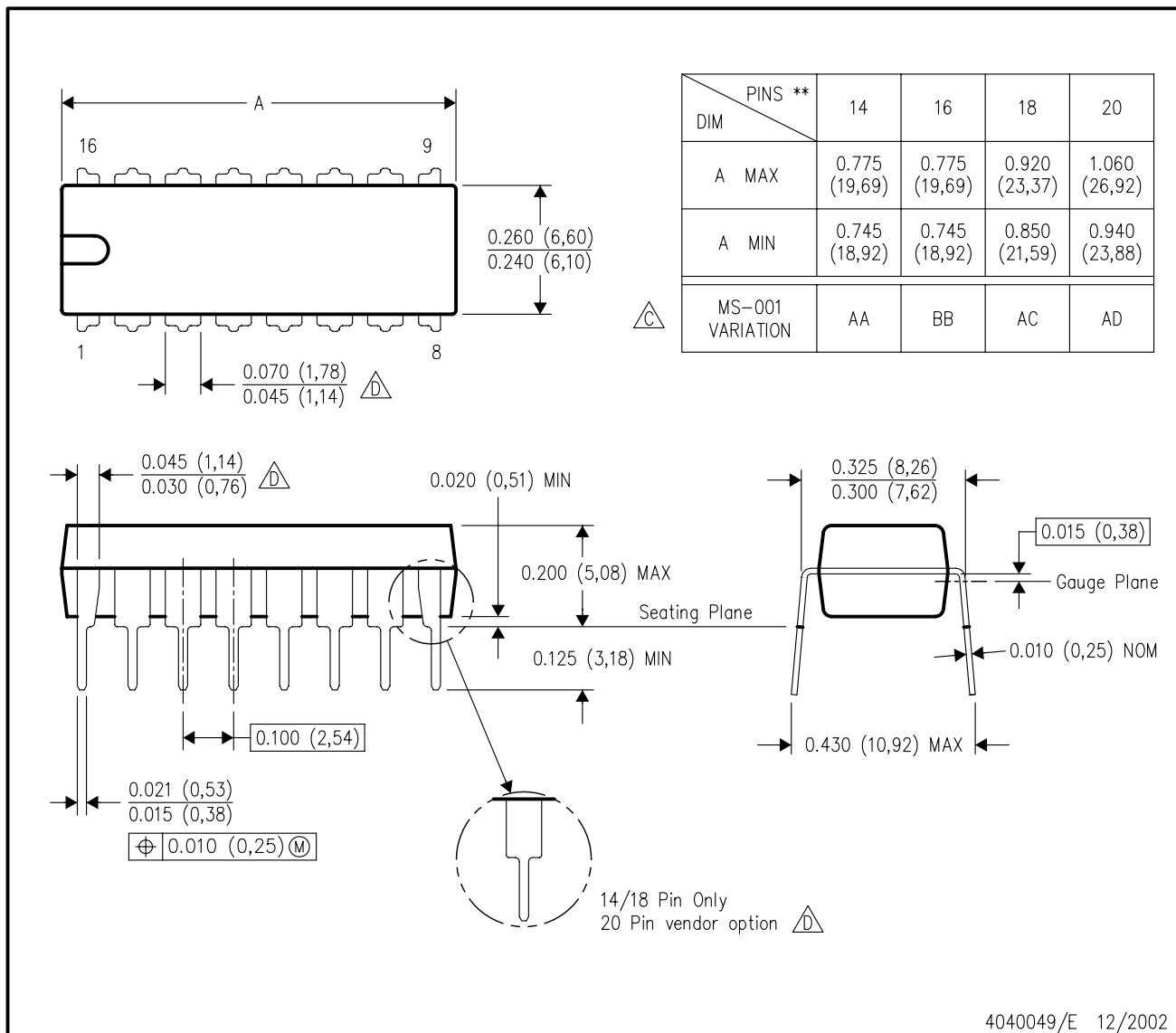


4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

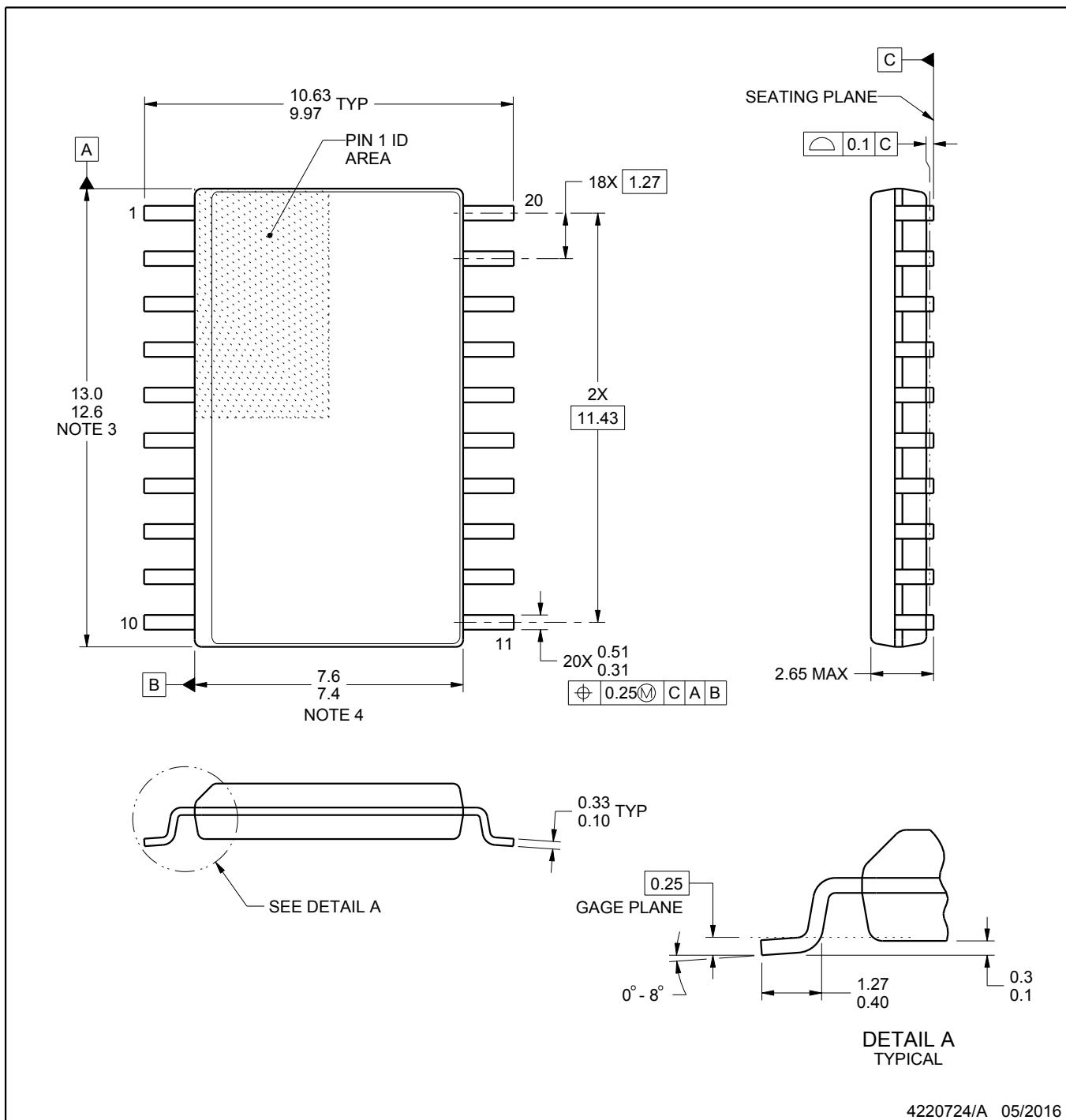
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

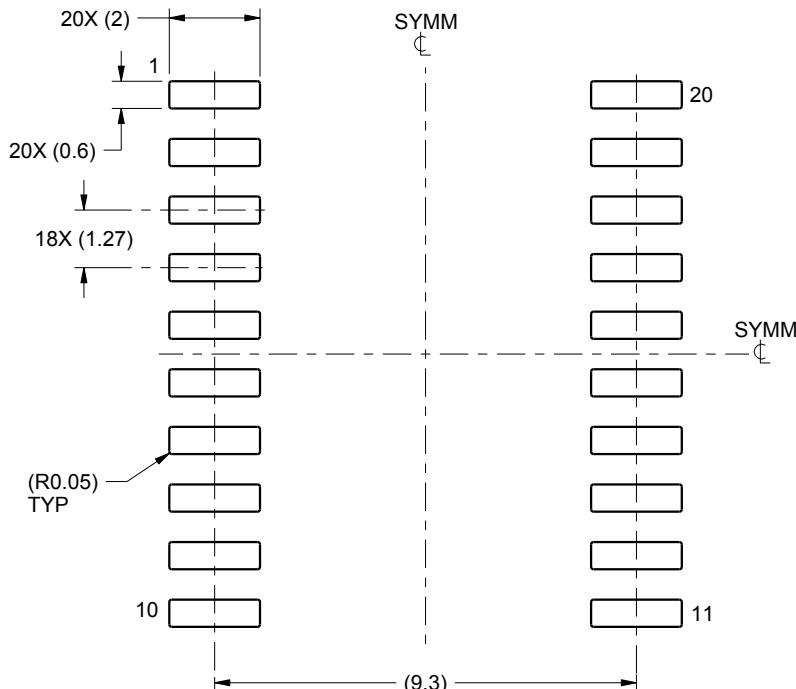
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

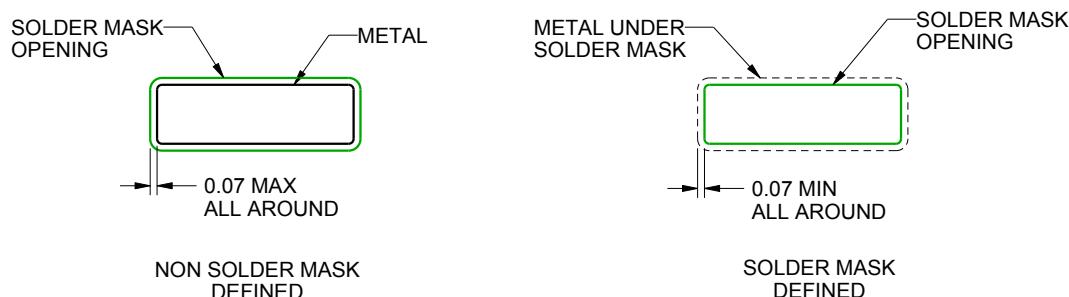
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

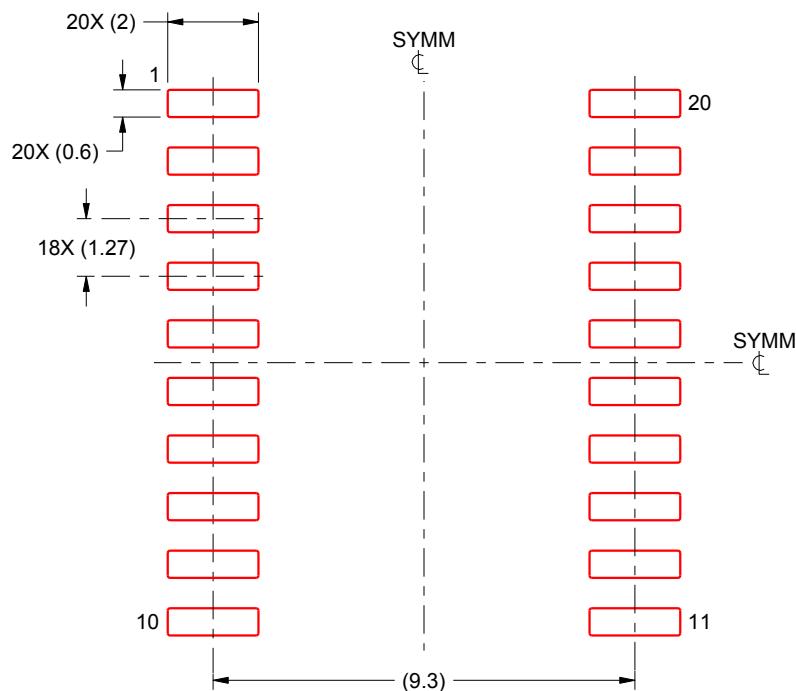
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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