

# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS245A – DECEMBER 1982 – REVISED JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Low-Power Versions of 'ALS245 Series
- 'ALS1245 Series Is Identical to 'ALS1645 Series
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

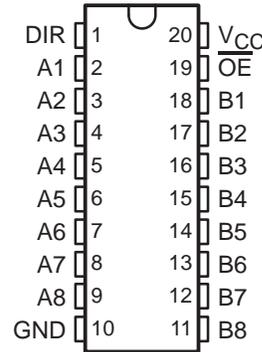
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The SN54ALS1245A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS1245A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

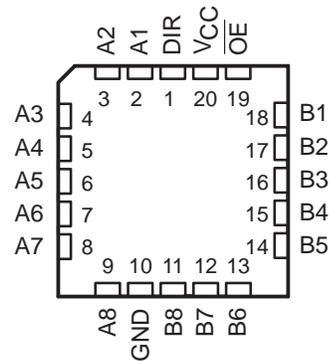
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54ALS1245A . . . J PACKAGE  
SN74ALS1245A . . . DW OR N PACKAGE  
(TOP VIEW)



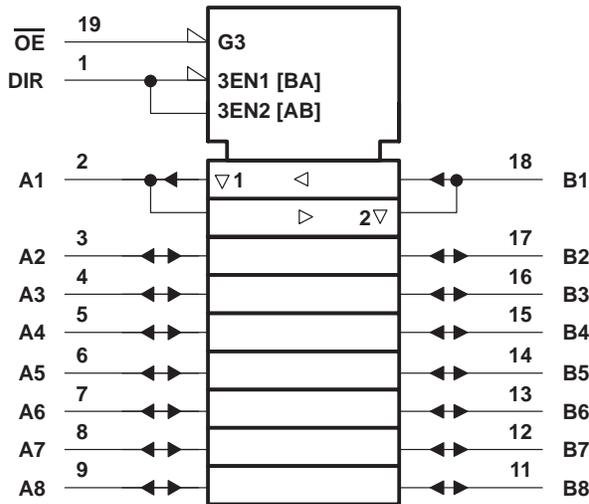
SN54ALS1245A . . . FK PACKAGE  
(TOP VIEW)



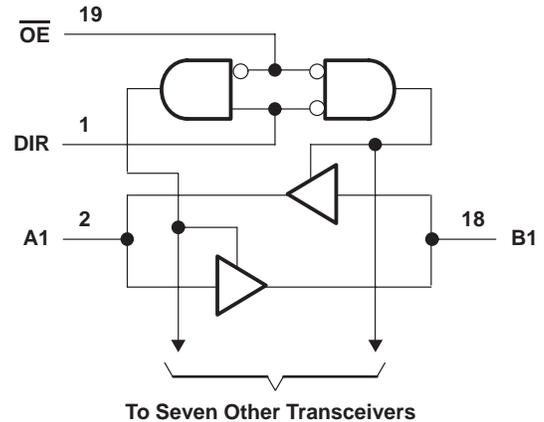
# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS1245A	-55°C to 125°C
SN74ALS1245A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

	SN54ALS1245A			SN74ALS1245A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$I_{OH}$ High-level output current			-12			-15	mA
$I_{OL}$ Low-level output current			8			16	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS1245A		SN74ALS1245A		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.5		-1.5	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$		V	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.2	2.4		3.2
		$I_{OH} = -12\text{ mA}$	2				
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 8\text{ mA}$	0.25	0.4	0.25	0.4	V
		$I_{OL} = 16\text{ mA}$			0.35	0.5	
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$	0.1		0.1	mA
	A or B ports		$V_I = 5.5\text{ V}$	0.1		0.1	
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	20		20		$\mu\text{A}$
	A or B ports‡		20		20		
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$	-0.1		-0.1		mA
	A or B ports‡		-0.1		-0.1		
$I_{O}^{\S}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-20	-112	-30	-112	mA	
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	21	33	21	30	mA
		Outputs low	23	36	23	33	
		Outputs disabled	25	40	25	36	

† All typical values are  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

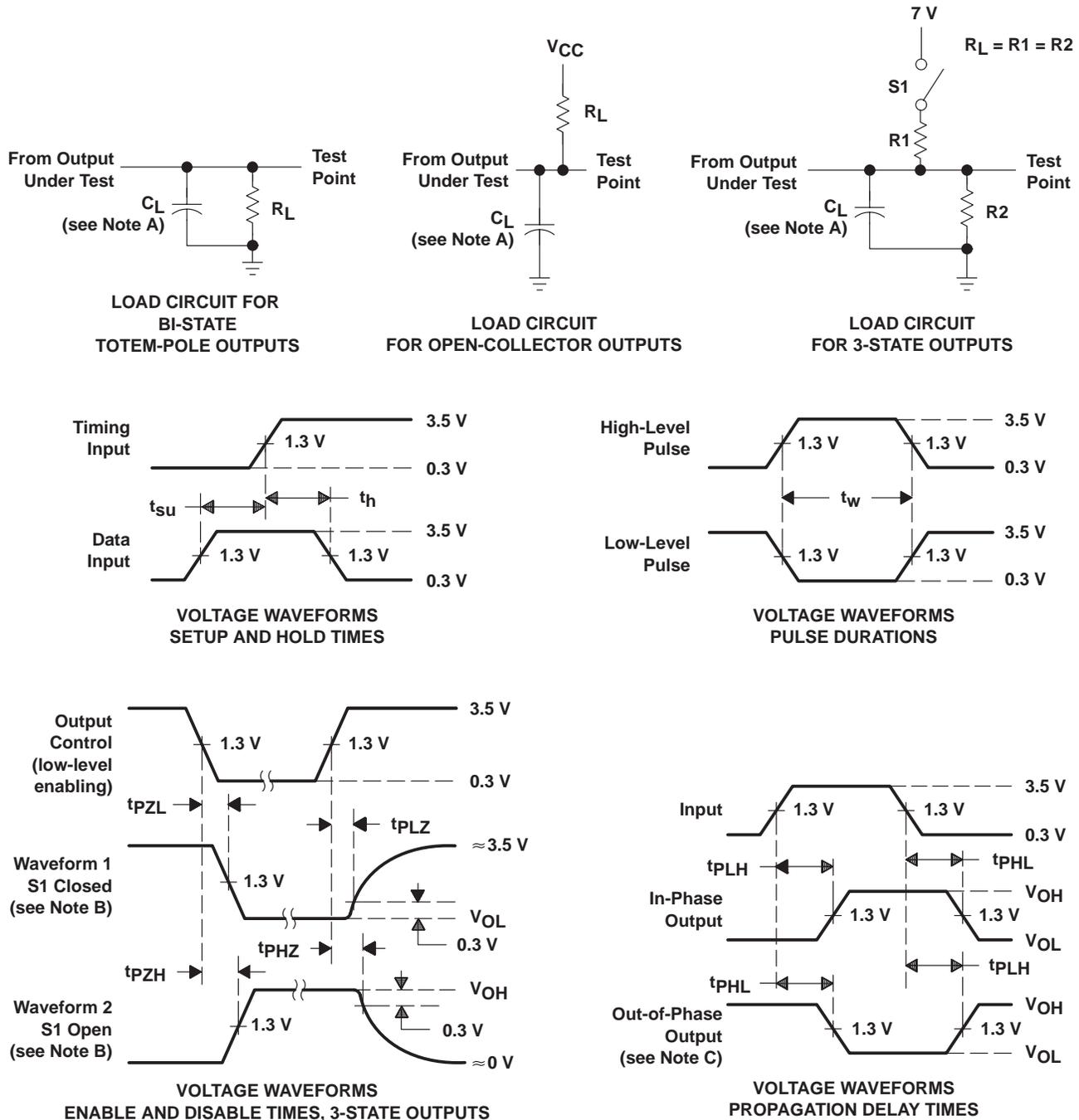
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}^{\parallel}$				UNIT
			SN54ALS1245A		SN74ALS1245A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	2	19	2	13	ns
$t_{PHL}$			2	15	2	13	
$t_{PZH}$	$\overline{OE}$	A or B	8	30	8	25	ns
$t_{PZL}$			8	29	8	25	
$t_{PHZ}$	$\overline{OE}$	A or B	2	14	2	12	ns
$t_{PLZ}$			3	30	3	18	

<sup>||</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-88737012A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-88737012A SNJ54ALS 1245AFK
<a href="#">5962-8873701RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8873701RA SNJ54ALS1245AJ
<a href="#">SN74ALS1245AN</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS1245AN
SN74ALS1245AN.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS1245AN
<a href="#">SNJ54ALS1245AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-88737012A SNJ54ALS 1245AFK
SNJ54ALS1245AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-88737012A SNJ54ALS 1245AFK
<a href="#">SNJ54ALS1245AJ</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8873701RA SNJ54ALS1245AJ
SNJ54ALS1245AJ.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8873701RA SNJ54ALS1245AJ

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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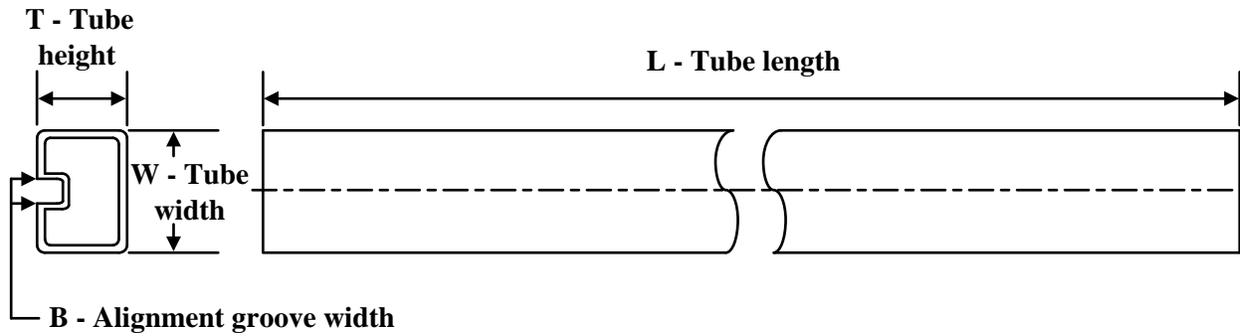
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**OTHER QUALIFIED VERSIONS OF SN54ALS1245A, SN74ALS1245A :**

- Catalog : [SN74ALS1245A](#)
- Military : [SN54ALS1245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-88737012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS1245AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS1245AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS1245AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS1245AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA



## GENERIC PACKAGE VIEW

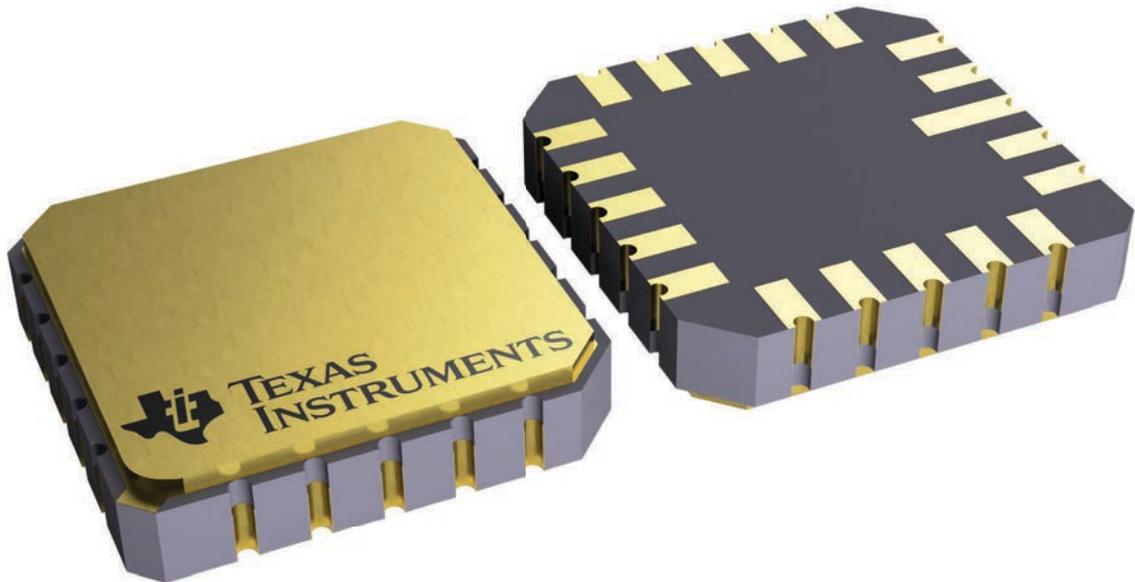
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

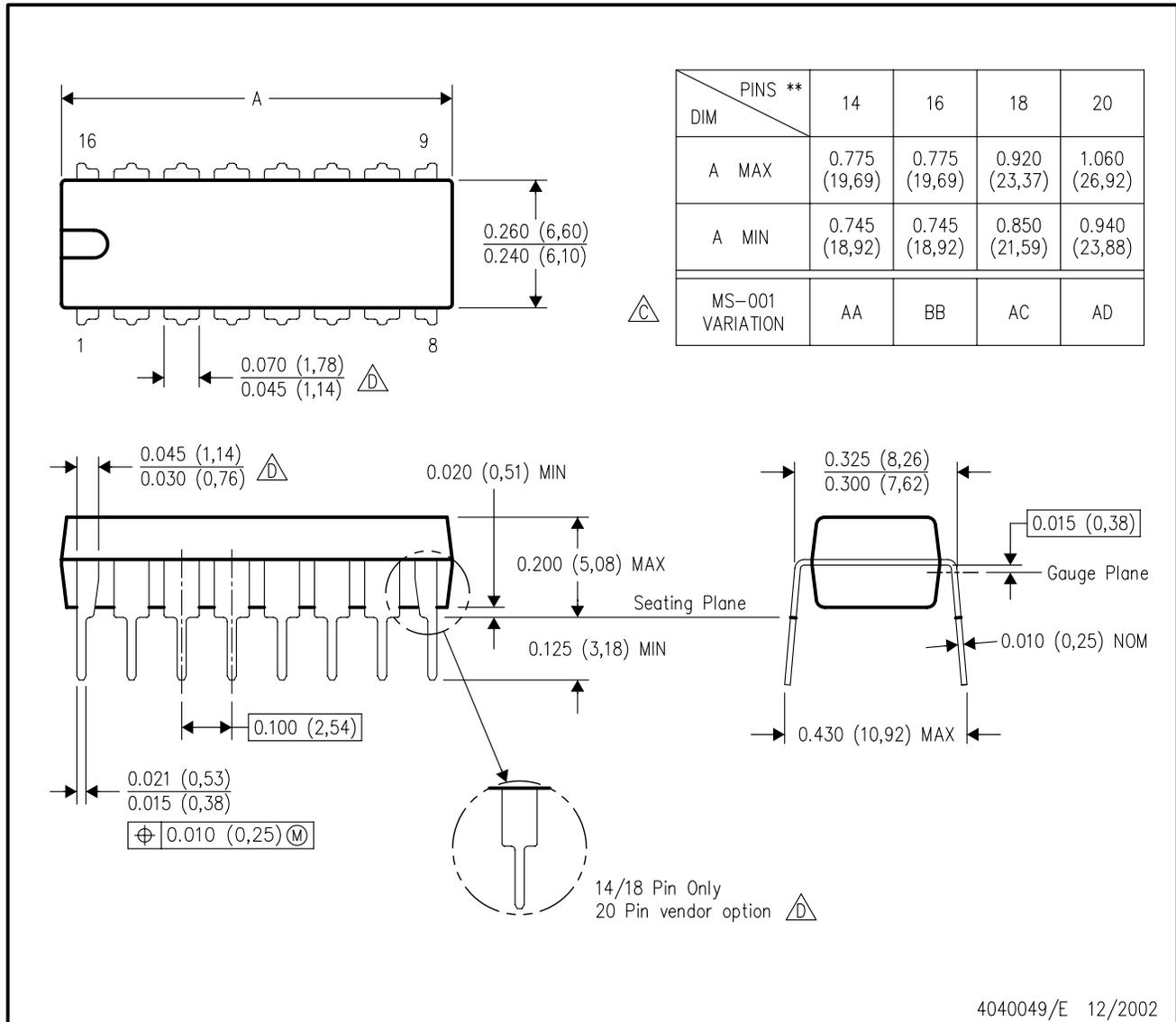


4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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