

SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS048D – DECEMBER 1989 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- True Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

description

These octal D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

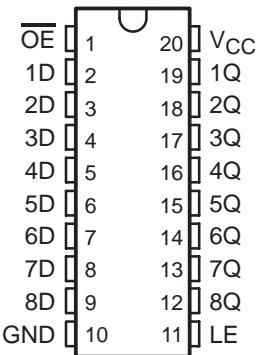
While the latch-enable (LE) input is high, outputs (Q) respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

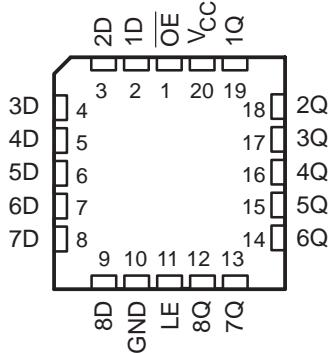
\overline{OE} does not affect internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS573C and SN54AS573A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS573C and SN74AS573A are characterized for operation from 0°C to 70°C .

SN54ALS573C, SN54AS573A . . . J OR W PACKAGE
SN74ALS573C, SN74AS573A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS573C, SN54AS573A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (each latch)			
INPUTS			OUTPUT Q
\overline{OE}	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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 **TEXAS
INSTRUMENTS**

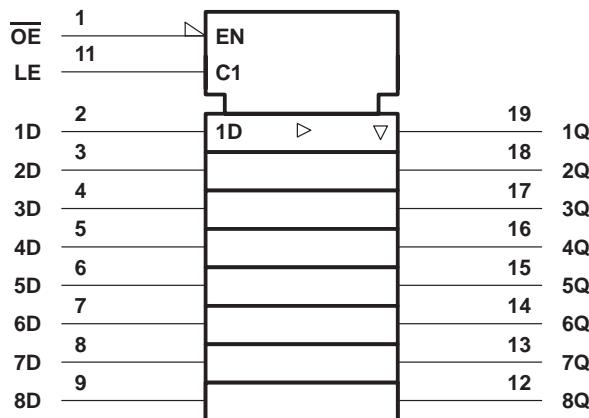
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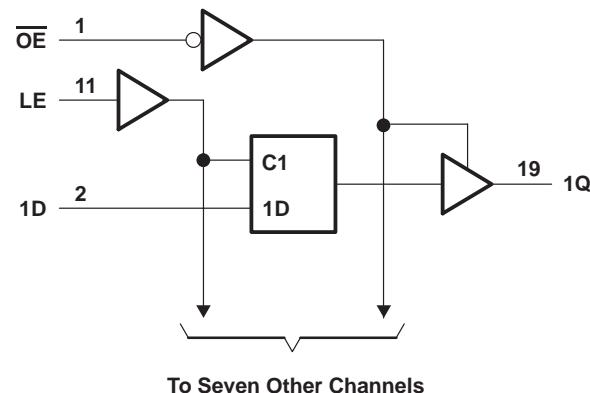
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS573C	-55°C to 125°C
SN74ALS573C	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS573C			SN74ALS573C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, LE high	25			10			ns
t_{su}	Setup time, data before LE \downarrow	10			10			ns
t_h	Hold time, data after LE \downarrow	7			7			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A
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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS573C			SN74ALS573C			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$	$V_{CC} - 2$			$V_{CC} - 2$			V
		$I_{OH} = -1 \text{ mA}$	2.4	3.3				
		$I_{OH} = -2.6 \text{ mA}$			2.4	3.2		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$			-20			-20	μA
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.13			-0.1	mA
I_O^{\ddagger}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-20	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	10	17	10	17		mA
		Outputs low	15	24	15	24		
		Outputs disabled	16	27	16	27		

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\$}$				UNIT	
			SN54ALS573C		SN74ALS573C			
			MIN	MAX	MIN	MAX		
t_{PLH}	D	Q	2	20	2	14	ns	
			2	17	2	14		
t_{PHL}	LE	Q	8	33	6	20	ns	
			8	24	6	19		
t_{PZH}	\overline{OE}	Q	4	28	3	18	ns	
			4	21	4	18		
t_{PZL}	\overline{OE}	Q	2	20	1	10	ns	
			3	26	1	15		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS573A			SN74AS573A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			32			48	mA
t _w [*]	Pulse duration, LE high		5.5		4.5			ns
t _{su} [*]	Setup time, data before LE↓		2		2			ns
t _h [*]	Hold time, data after LE↓		3		3			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS573A			SN74AS573A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2.4	3.2				
		$I_{OH} = -15 \text{ mA}$			2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 32 \text{ mA}$	0.28	0.5				V
		$I_{OL} = 48 \text{ mA}$					0.33	
							0.5	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			50			50	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$			-50			-50	μA
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.1			-0.5	mA
$I_O^§$	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	56	93	56	93		mA
		Outputs low	55	90	55	90		
		Outputs disabled	65	106	65	106		

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

† At typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
 § The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

**SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS**

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R1 = 500\text{ }\Omega,$ $R2 = 500\text{ }\Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN54AS573A		SN74AS573A			
			MIN	MAX	MIN	MAX		
t_{PLH}	D	Q	3	11	3	8	ns	
t_{PHL}			3	8	3	7		
t_{PLH}	LE	Q	6	16.5	6	13	ns	
t_{PHL}			4	9	4	7.5		
t_{PZH}	\overline{OE}	Q	2	8	2	6.5	ns	
t_{PZL}			4	11	4	9.5		
t_{PHZ}	\overline{OE}	Q	2	8	2	6.5	ns	
t_{PLZ}			2	8	2	7		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**

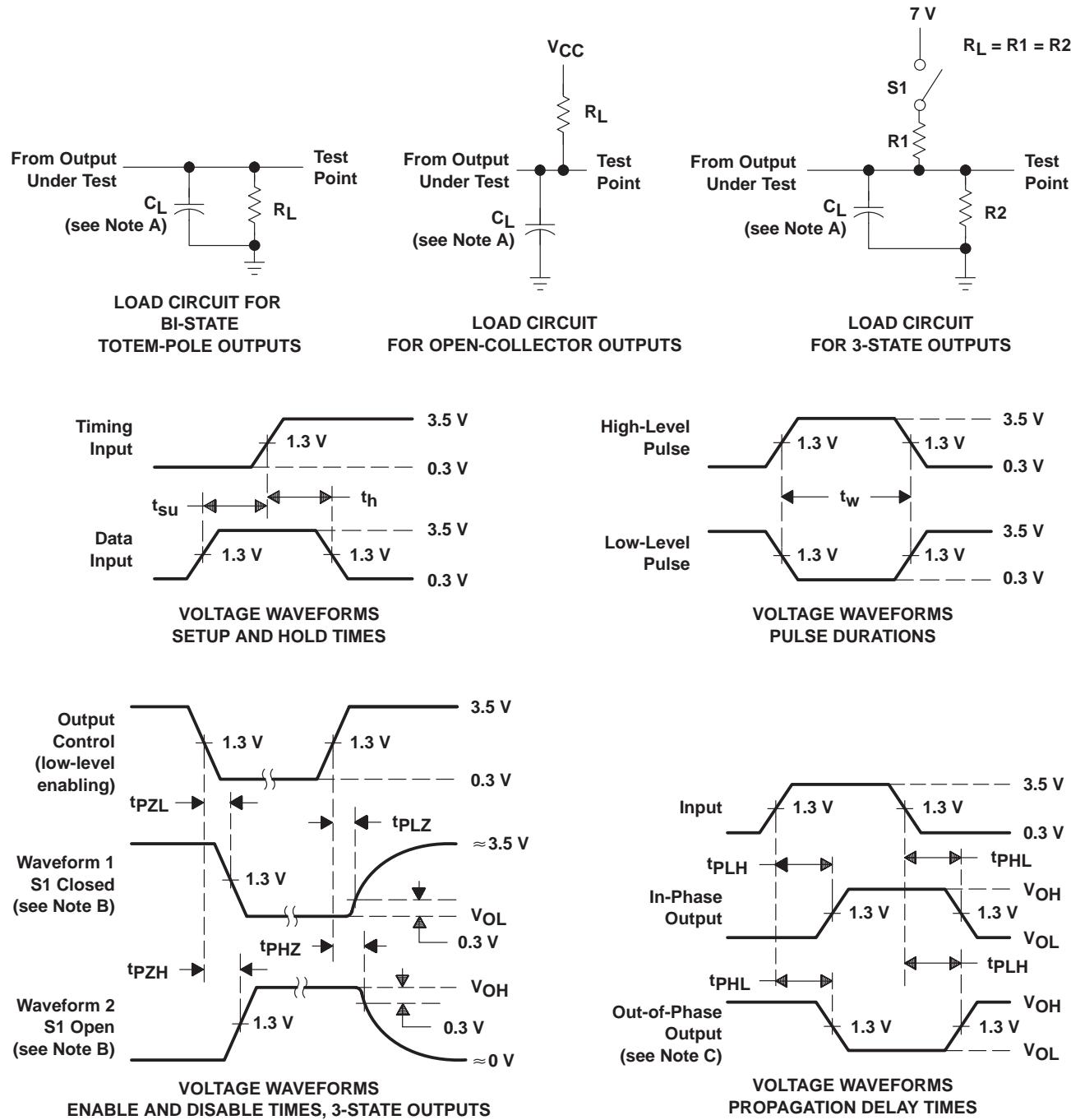


Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84012012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84012012A SNJ54ALS 573CFK
8401201RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401201RA SNJ54ALS573CJ
8401201SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401201SA SNJ54ALS573CW
JM38510/38201B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38201B2A
JM38510/38201B2A.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38201B2A
JM38510/38201BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38201BRA
JM38510/38201BRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38201BRA
M38510/38201B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38201B2A
M38510/38201BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38201BRA
SN54ALS573CJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS573CJ
SN54ALS573CJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS573CJ
SN54AS573AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS573AJ
SN54AS573AJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS573AJ
SN74ALS573CDBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	G573C
SN74ALS573CDBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	G573C
SN74ALS573CDW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	ALS573C
SN74ALS573CDWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C
SN74ALS573CDWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C
SN74ALS573CN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS573CN
SN74ALS573CN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS573CN
SN74ALS573CNE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS573CN
SN74ALS573CNSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS573CNSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C
SN74ALS573CNSRE4	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS573C
SN74AS573ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS573A
SN74AS573ADW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS573A
SN74AS573AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS573AN
SN74AS573AN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS573AN
SNJ54ALS573CFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84012012A SNJ54ALS 573CFK
SNJ54ALS573CFK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84012012A SNJ54ALS 573CFK
SNJ54ALS573CJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401201RA SNJ54ALS573CJ
SNJ54ALS573CJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401201RA SNJ54ALS573CJ
SNJ54ALS573CW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401201SA SNJ54ALS573CW
SNJ54ALS573CW.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401201SA SNJ54ALS573CW
SNJ54AS573AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS573AJ
SNJ54AS573AJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS573AJ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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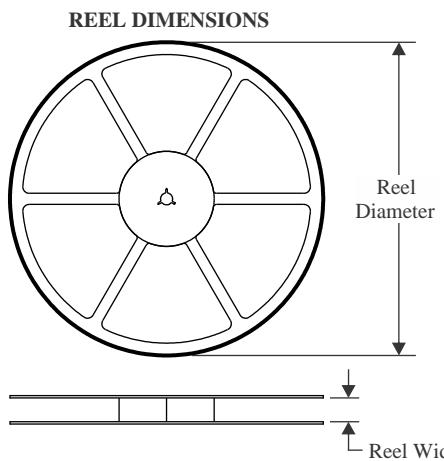
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS573C, SN54AS573A, SN74ALS573C, SN74AS573A :

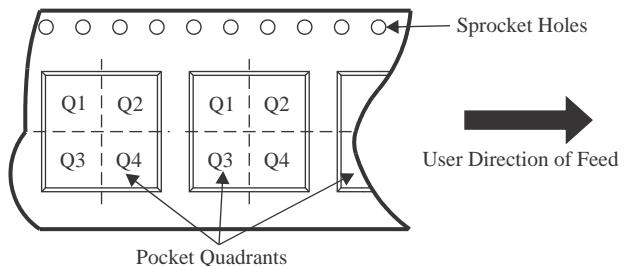
- Catalog : [SN74ALS573C](#), [SN74AS573A](#)
- Military : [SN54ALS573C](#), [SN54AS573A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


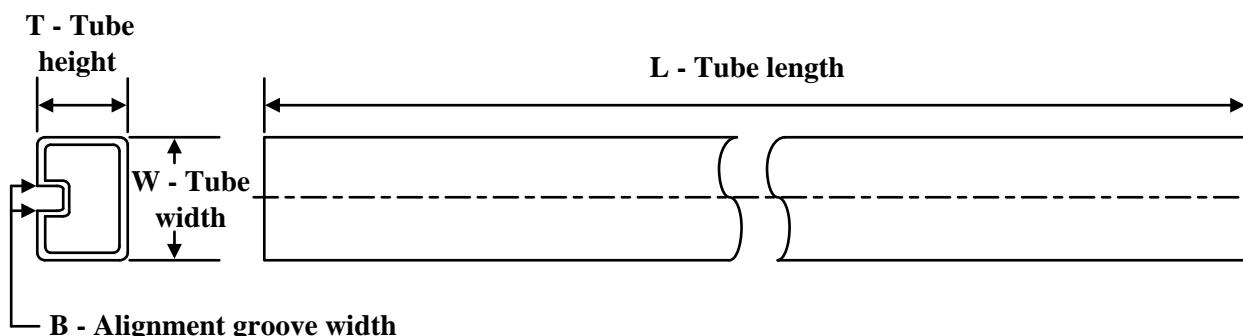
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS573CDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ALS573CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS573CNSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS573CDBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ALS573CDWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS573CNSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE


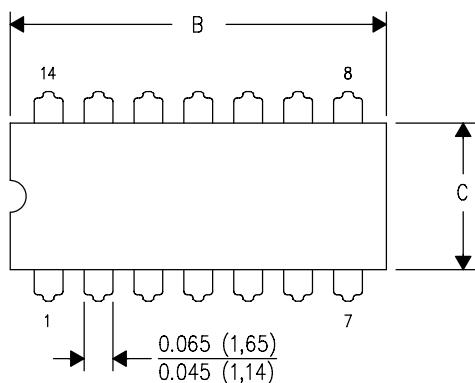
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84012012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8401201SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/38201B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/38201B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/38201B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS573CN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS573CN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS573CNE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS573ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS573ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS573AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS573AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS573CFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS573CFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS573CW	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS573CW.A	W	CFP	20	25	506.98	26.16	6220	NA

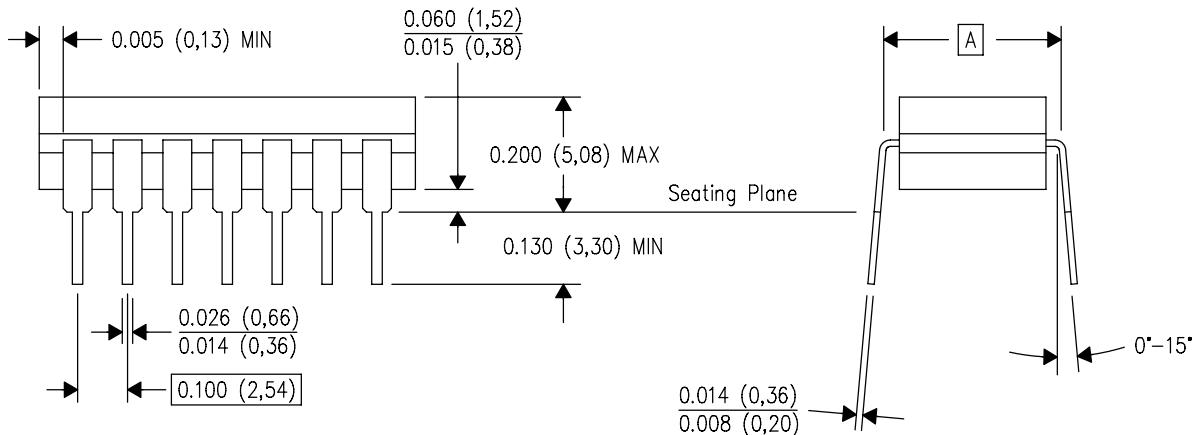
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

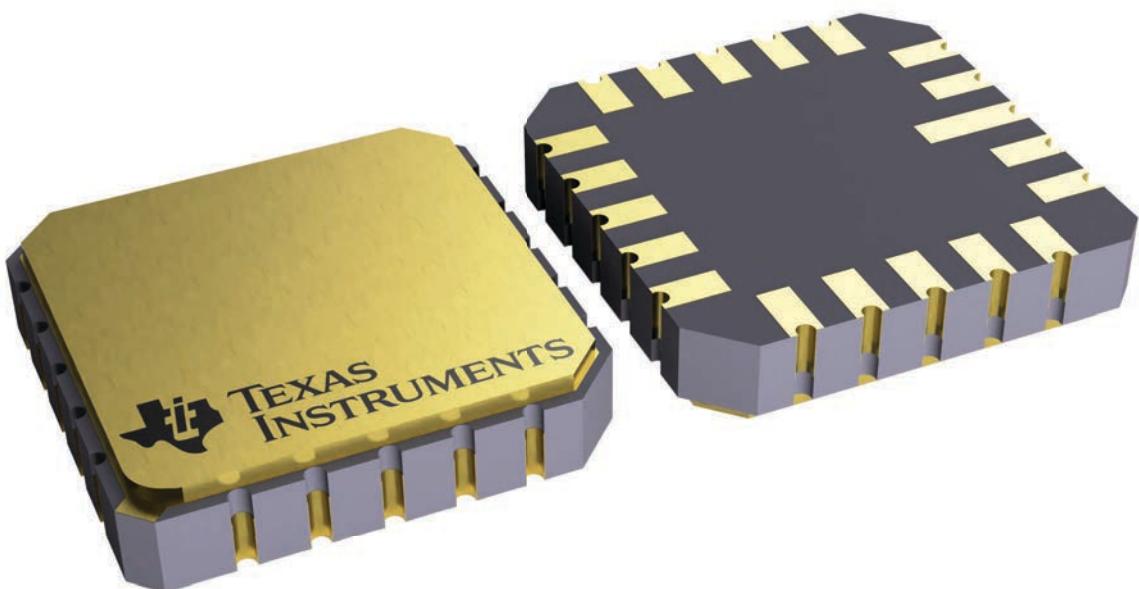
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

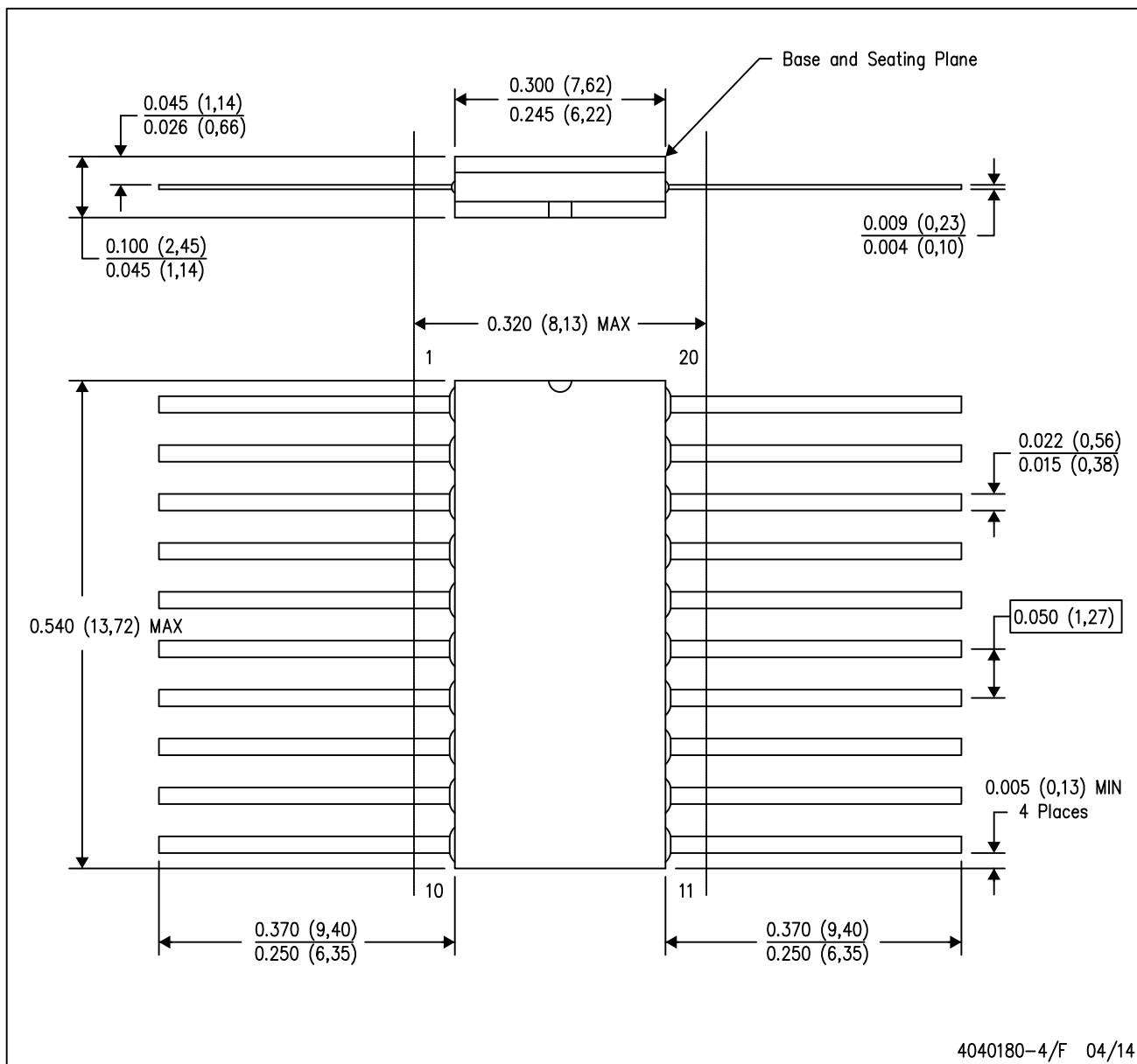
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

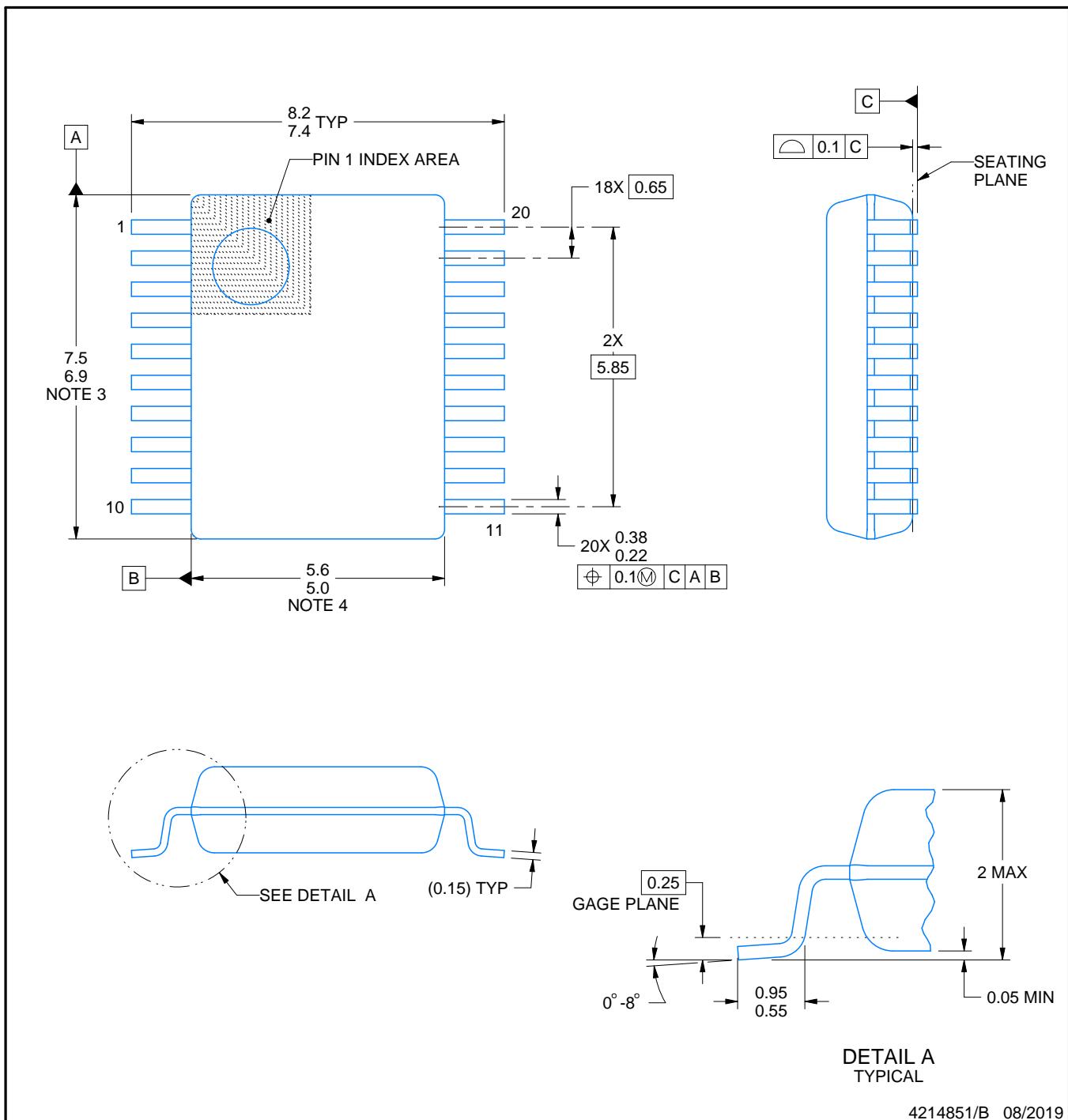
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

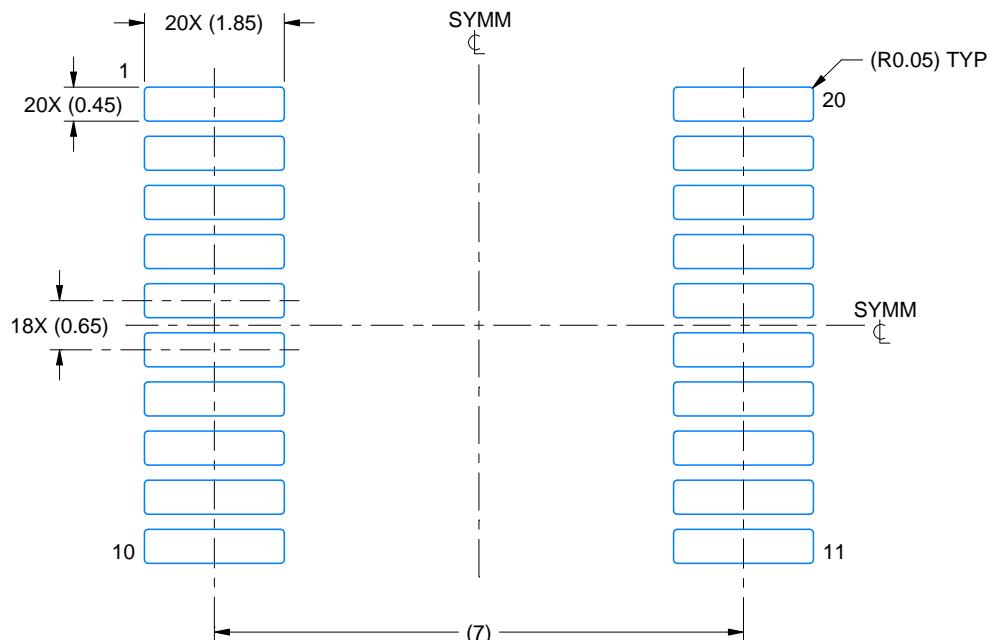
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

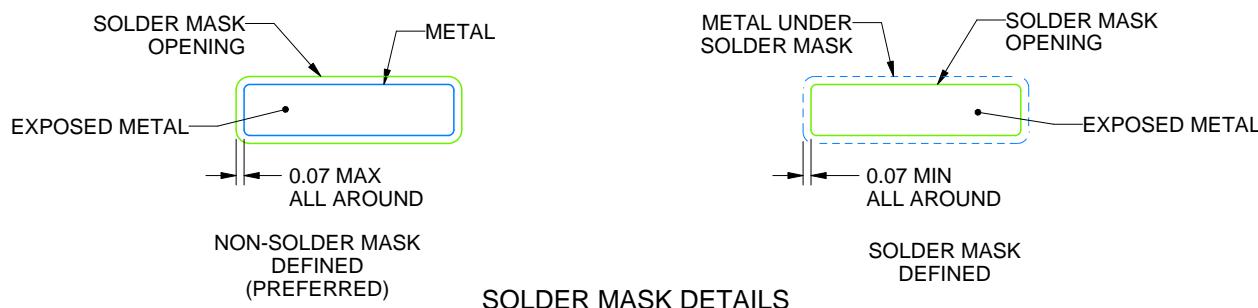
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

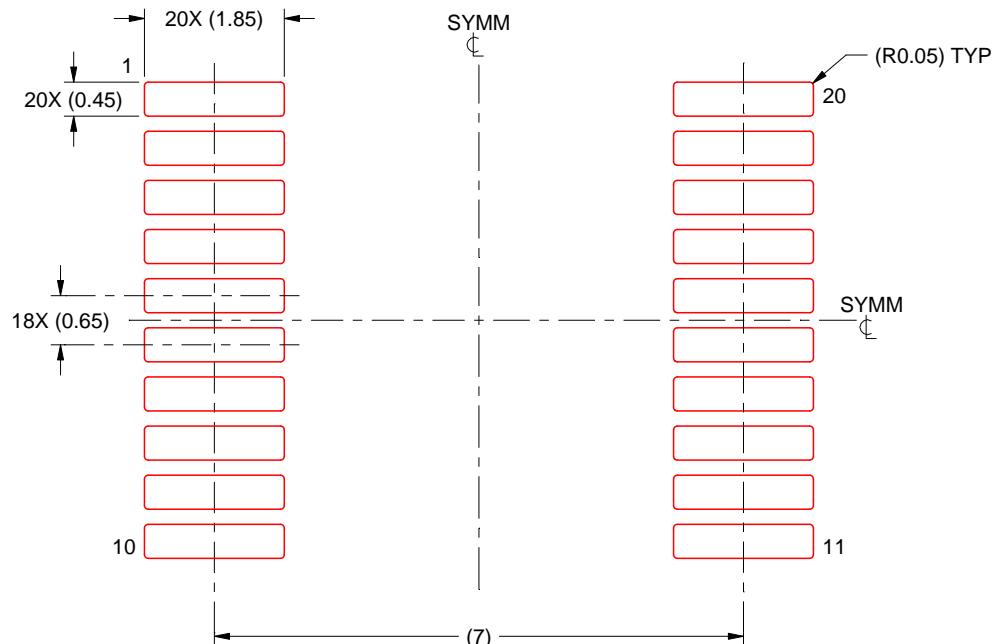
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

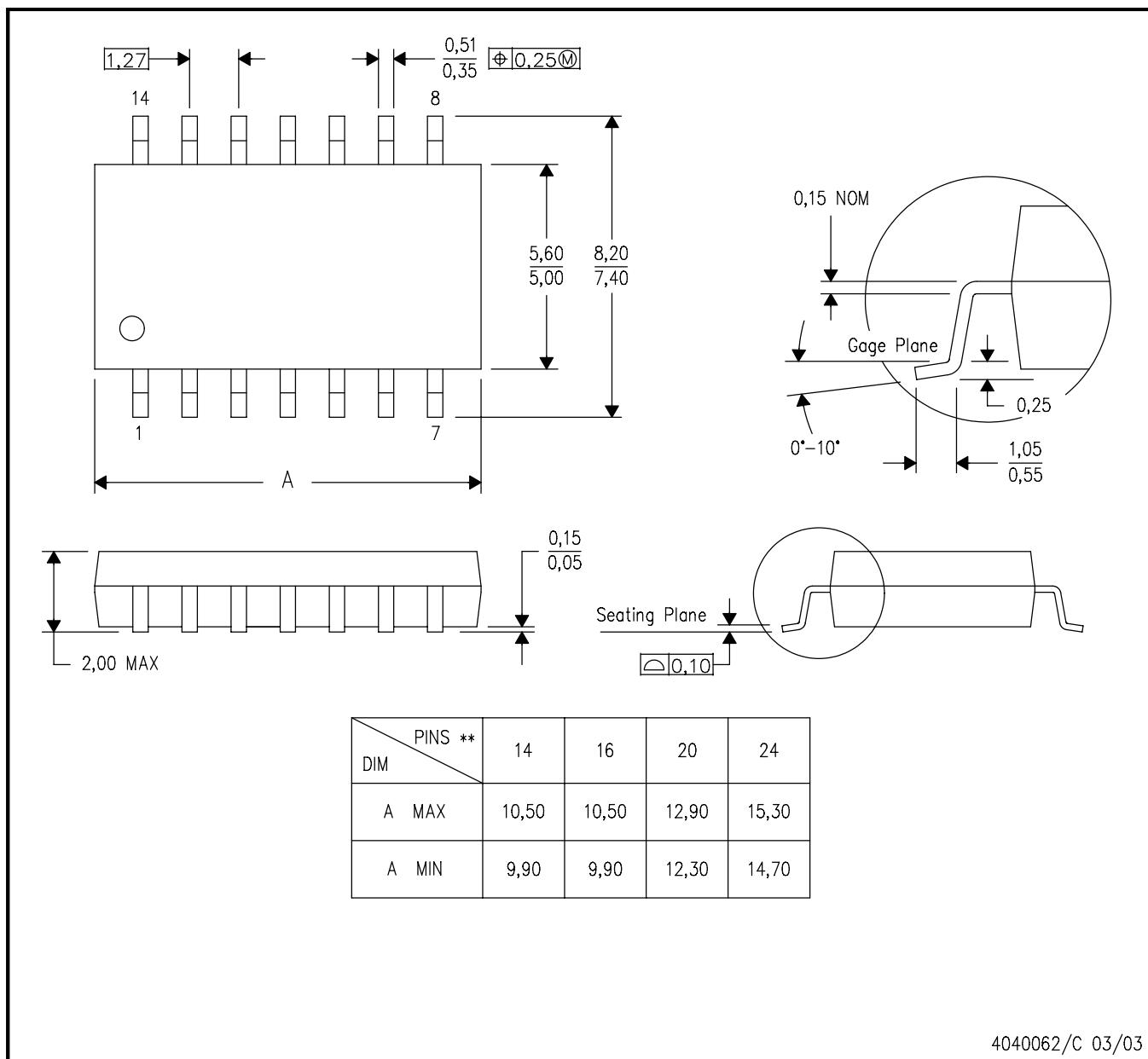
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

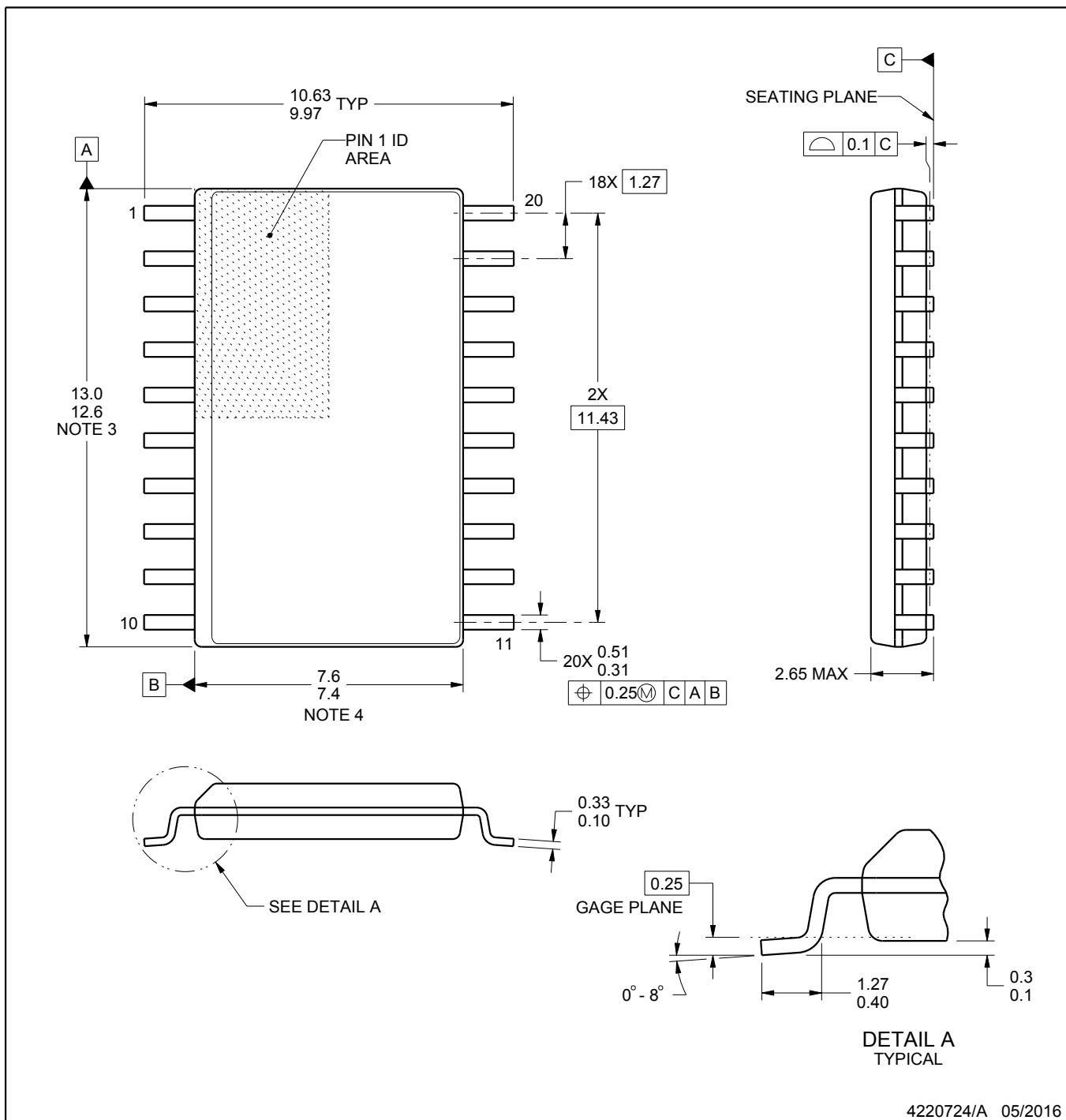
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

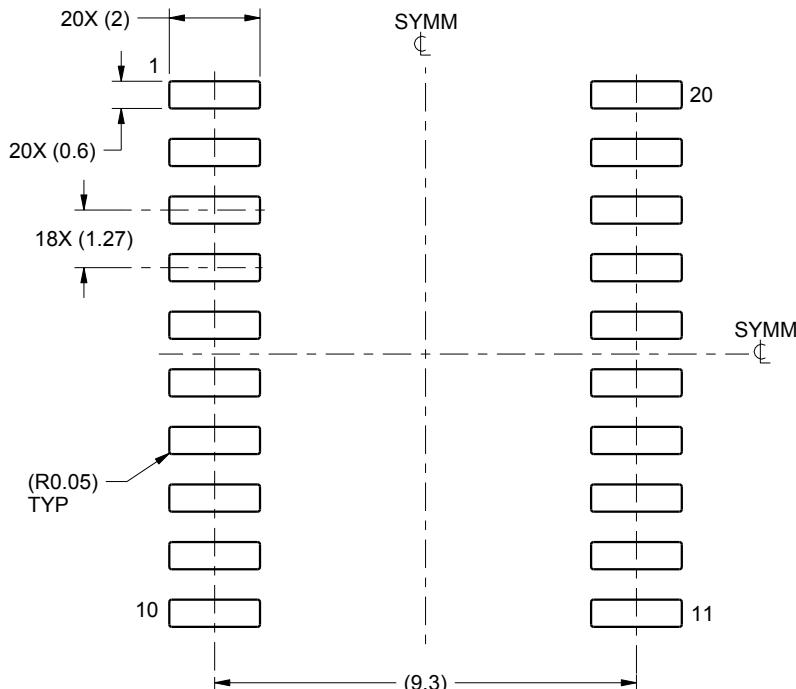
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

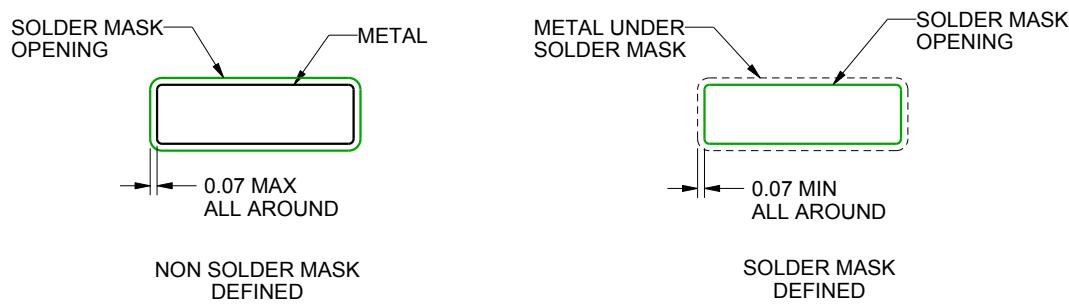
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

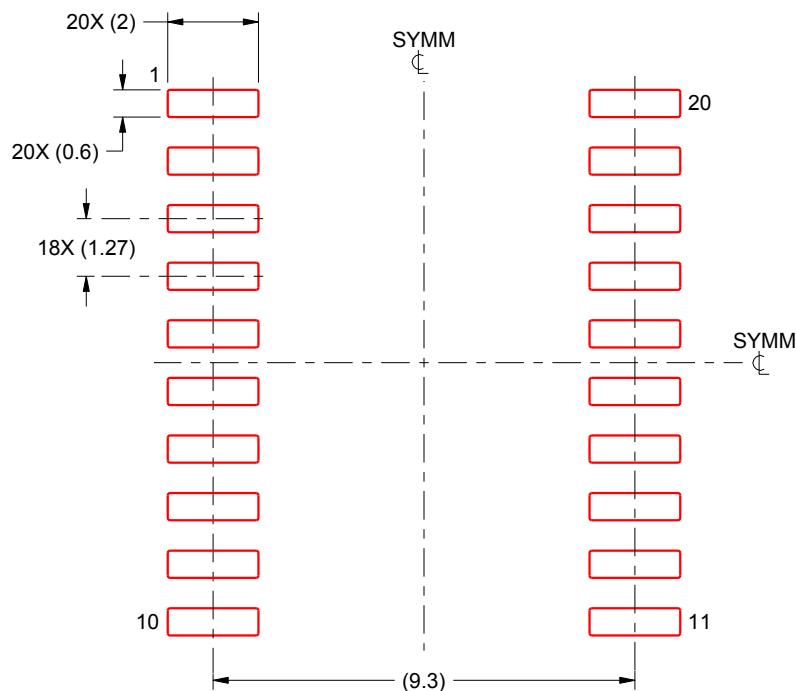
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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