

## SNx4HC05 オープン・ドレイン出力、ヘキサ・インバータ

### 1 特長

- バッファ付き入力
- 広い動作電圧範囲: 2V~6V
- 広い動作温度範囲:  
-40°C~+85°C
- 最大 10 個の LSTTL 負荷ファンアウトに対応
- LSTTL ロジック IC に比べて消費電力を大幅削減

### 2 アプリケーション

- 反転クロック入力の同期
- デジタル信号の反転

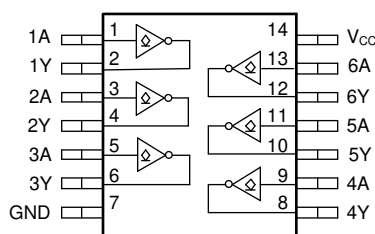
### 3 概要

このデバイスには、オープン・ドレイン出力を備えた 6 つの独立したインバータが内蔵されています。各ゲートはブール関数  $Y = \bar{A}$  を正論理で実行します。

#### 製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN74HC05DR	SOIC (14)	8.70mm × 3.90mm
SN74HC05NR	PDIP (14)	19.30mm × 6.40mm
SN74HC05NSR	SO (14)	10.20mm × 5.30mm
SN74HC05PWR	TSSOP (14)	5.00mm × 4.40mm
SN54HC05JR	CDIP (14)	21.30mm × 7.60mm
SN54HC05FKR	LCCC (20)	8.90mm × 8.90mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能とピン配置



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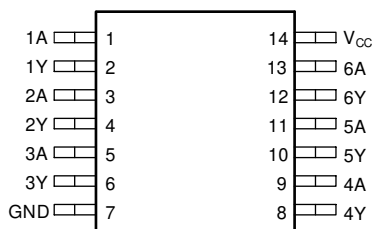
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## 4 Revision History

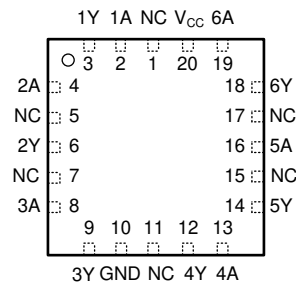
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision E (March 2015) to Revision F (April 2021)</b>	<b>Page</b>
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	<b>1</b>
• 新しいデータシート標準に更新.....	<b>1</b>
• R <sub>θJA</sub> increased for the D, NS, and PW packages and decreased for the N package.....	<b>5</b>
<b>Changes from Revision D (August 2003) to Revision E (March 2015)</b>	<b>Page</b>
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	<b>1</b>

## 5 Pin Configuration and Functions



**5-1. D, N, NS, PW, or J Package**  
**14-Pin SOIC, PDIP, SO, TSSOP, or CDIP**  
**Top View**



**5-2. FK Package**  
**20-Pin LCCC**  
**Top View**

## Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D, N, NS, PW, or J	FK		
1A	1	2	Input	Channel 1, Input A
1Y	2	3	Output	Channel 1, Output Y
2A	3	4	Input	Channel 2, Input A
2Y	4	6	Output	Channel 2, Output Y
3A	5	8	Input	Channel 3, Input A
3Y	6	9	Output	Channel 3, Output Y
GND	7	10	—	Ground
4Y	8	12	Output	Channel 4, Output Y
4A	9	13	Input	Channel 4, Input A
5Y	10	14	Output	Channel 5, Output Y
5A	11	16	Input	Channel 5, Input A
6Y	12	18	Output	Channel 6, Output Y
6A	13	19	Input	Channel 6, Input A
V <sub>CC</sub>	14	20	—	Positive Supply
NC		1, 5, 7, 11, 15, 17	—	Not internally connected

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		−0.5	7	V
$I_{IK}$	Input clamp current <sup>(2)</sup>	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
$I_{OK}$	Output clamp current <sup>(2)</sup>	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		±25	mA
	Continuous current through $V_{CC}$ or GND			±50	mA
$T_J$	Junction temperature <sup>(3)</sup>			150	°C
$T_{stg}$	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	–	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5			V
		$V_{CC} = 4.5$ V	3.15			
		$V_{CC} = 6$ V	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V			0.5	V
		$V_{CC} = 4.5$ V			1.35	
		$V_{CC} = 6$ V			1.8	
$V_I$	Input voltage		0		$V_{CC}$	V
$V_O$	Output voltage		0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise and fall rate	$V_{CC} = 2$ V			1000	ns
		$V_{CC} = 4.5$ V			500	
		$V_{CC} = 6$ V			400	
$T_A$	Operating free-air temperature	SN54HC05	−55		125	°C
		SN74HC05	−40		125	

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74HC05				UNIT
		D (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	62.6	122.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.0	50.3	81.8	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5	42.3	83.8	94.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	45.5	30.0	45.4	25.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	89.1	42.1	83.4	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics - 74

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

Operating free-air temperature range, typical values measured at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).														
PARAMETER		TEST CONDITIONS		$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
					25°C			−40°C to 85°C			−40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$I_{OH}$	Output voltage	$V_I = V_{IH}$ or $V_{IL}$	$V_O = V_{CC}$	6 V	0.01	0.5			5			5	μA	
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$	2 V	0.002	0.1			0.1			0.1	V	
				4.5 V	0.001	0.1			0.1	0.1				
				6 V	0.001	0.1			0.1	0.1				
			$I_{OL} = 4\ \text{mA}$	4.5 V	0.17	0.26			0.33	0.33				
				6 V	0.15	0.26			0.33	0.33				
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0		6 V		±0.1			±1			±1	μA	
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0	$I_O = 0$	6 V		2			20			20	μA	
$C_i$	Input capacitance			2 V to 6 V		3	10			10			10	pF

## 6.6 Electrical Characteristics - 54

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT			
					25°C			−40°C to 85°C			−55°C to 125°C						
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
I <sub>OH</sub>	Output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub>	6 V	0.01			0.5			5			10			μA

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.002	0.1	0.1			0.1			V	
				4.5 V	0.001	0.1	0.1			0.1				
				6 V	0.001	0.1	0.1			0.1				
			I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26	0.33			0.4				
			I <sub>OL</sub> = 5.2 mA	6 V	0.15	0.26	0.33			0.4				
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V	±0.1			±1			±1			μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0	I <sub>O</sub> = 0	6 V	2			20			40			μA
C <sub>i</sub>	Input capacitance			2 V to 6 V	3	10	10			10			pF	

## 6.7 Switching Characteristics - 74

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		FROM	TO	V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	Propagation delay low-to-high	A	Y	2 V	60	115	145			160			ns	
				4.5 V	13	23	29			31				
				6 V	10	20	25			28				
t <sub>PHL</sub>	Propagation delay high-to-low	A	Y	2 V	45	85	105			120			ns	
				4.5 V	9	17	21			23				
				6 V	8	14	18			21				
t <sub>t</sub>	Transition-time		Y	2 V	38	75	95			110			ns	
				4.5 V	8	15	19			22				
				6 V	6	13	16			19				

## 6.8 Switching Characteristics - 54

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		FROM	TO	V <sub>CC</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT
					25°C			−40°C to 85°C			−55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	Propagation delay low-to-high	A	Y	2 V	60	115	145			175			ns	
				4.5 V	13	23	29			35				
				6 V	10	20	25			30				
t <sub>PHL</sub>	Propagation delay high-to-low	A		2 V	45	85	105			130			ns	
				4.5 V	9	17	21			26				
				6 V	8	14	18			22				
t <sub>t</sub>	Transition-time		Y	2 V	38	75	95			110			ns	
				4.5 V	8	15	19			22				
				6 V	6	13	16			19				

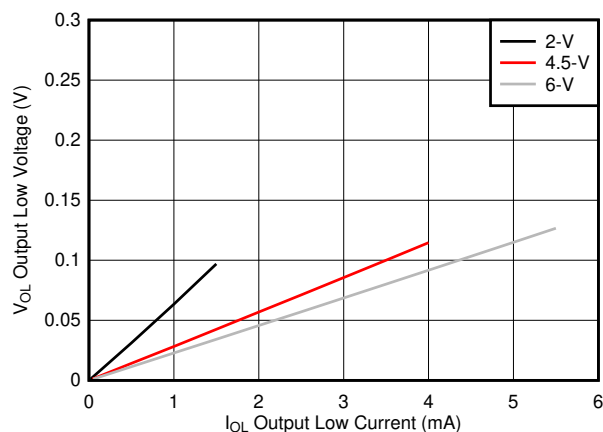
## 6.9 Operating Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance per gate	No load	2 V to 6 V		20		pF

## 6.10 Typical Characteristics

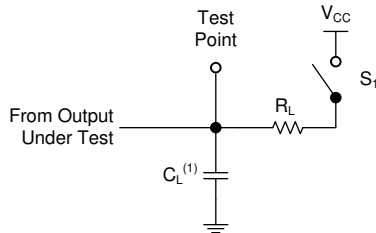
$T_A = 25^\circ\text{C}$



**6-1. Typical output voltage in the low state ( $V_{OL}$ )**

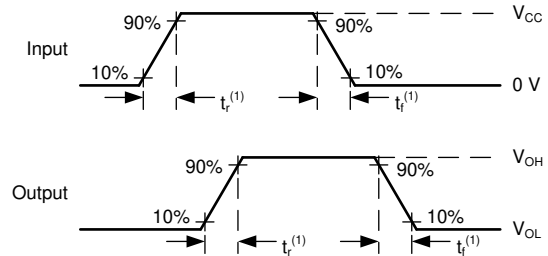
## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_f < 6 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.



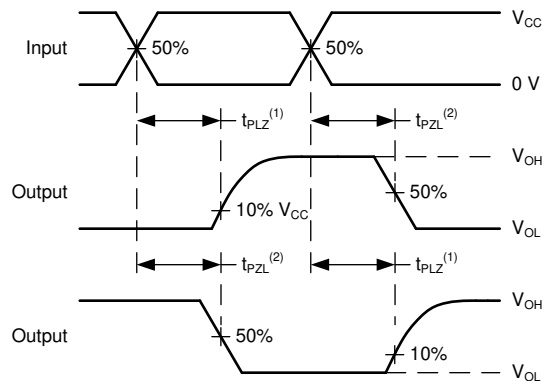
A.  $C_L = 50 \text{ pF}$  and includes probe and jig capacitance.

**FIG 7-1. Load Circuit**



A.  $t_t$  is the greater of  $t_r$  and  $t_f$ .

**FIG 7-2. Voltage Waveforms Transition Times**



A. The maximum between  $t_{PLH}$  and  $t_{PHL}$  is used for  $t_{pd}$ .

**FIG 7-3. Voltage Waveforms Propagation Delays**

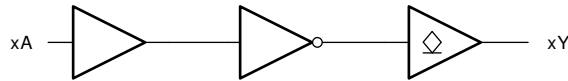


## 8 Detailed Description

### 8.1 Overview

This device contains six independent inverters with open-drain outputs. Each gate performs the Boolean function  $Y = \bar{A}$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 CMOS Open-Drain Outputs

The open-drain output allows the device to sink current to GND but not to source current from  $V_{CC}$ . When the output is not actively pulling the line low, it will go into a high impedance state. This allows the device to be used for a wide variety of applications, including up-translation and down-translation, as the output voltage can be determined by an external pull-up resistor.

The current drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

The SN74HC05 can drive a load with a total capacitance less than or equal to the maximum load listed in the [Switching Characteristics - 74](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

#### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics - 74](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics - 74](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [図 8-1](#).

#### 注意

Voltages beyond the values specified in the [セクション 6.1](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

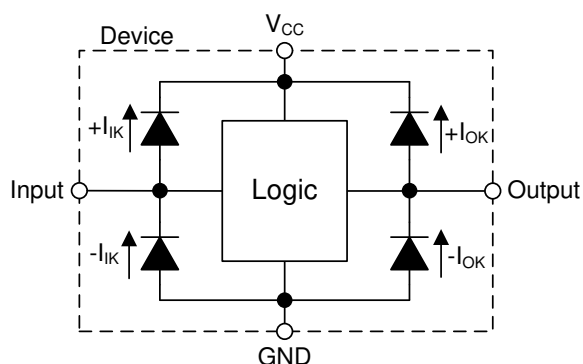


図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.4 Device Functional Modes

表 8-1. Function Table

INPUT	OUTPUT
A	Y
L	Hi-Z
H	L

## 9 Application and Implementation

### 注

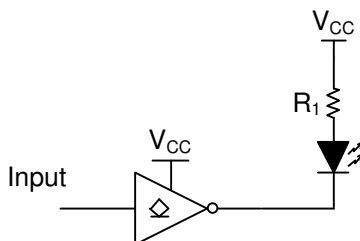
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### 9.1 Application Information

In this application, one open-drain inverter is used as shown in [Figure 9-1](#). The other five channels can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

This device is used to directly control an LED. The LED is on when the input is high, and off when the input is low.

### 9.2 Typical Application



**Figure 9-1. Typical application schematic**

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics - 74](#).

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HC05 plus the maximum supply current,  $I_{CC}$ , listed in [Electrical Characteristics - 74](#). The logic device can only sink as much current as is provided by the external pull-up resistor or other supply source. Be sure not to exceed the maximum total current through GND listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

### 注意

The maximum junction temperature,  $T_J(\text{max})$  listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

##### 9.2.1.2 Input Considerations

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the

SN74HC05, as specified in the [Electrical Characteristics - 74](#), and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HC05 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [Recommended Operating Conditions](#).

Refer to [セクション 8.3](#) for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the [Electrical Characteristics - 74](#). The plot in provides a typical relationship between output voltage and current for this device.

Open-drain outputs can be directly connected together to produce a wired-AND. This is possible because the outputs cannot source current, and thus can never be in bus-contention.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to [セクション 8.3](#) for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in [セクション 11](#).
2. Ensure the capacitive load at the output is  $\leq 70$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC05 to the receiving device.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

### 9.2.3 Application Curves

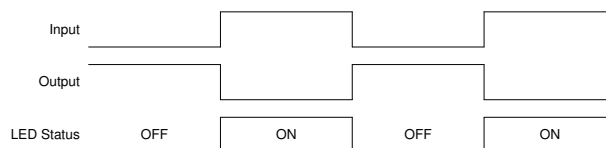


図 9-2. Typical application timing diagram

## 10 Power Supply Recommendations

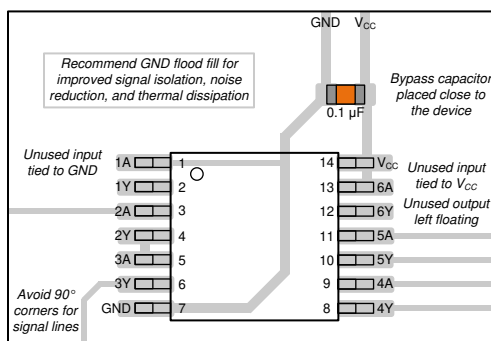
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [セクション 6.3](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [図 11-1](#).

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example



**図 11-1. Example layout for the SN74HC05**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

### 12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 12.3 Trademarks

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### 12.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.5 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-88718012A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88718012A SNJ54HC 05FK
<a href="#">5962-8871801CA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8871801CA SNJ54HC05J
<a href="#">SN54HC05J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC05J
SN54HC05J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC05J
<a href="#">SN74HC05D</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 125	HC05
<a href="#">SN74HC05DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HC05
SN74HC05DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
<a href="#">SN74HC05DRG4</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
SN74HC05DRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
<a href="#">SN74HC05DT</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 125	HC05
<a href="#">SN74HC05N</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74HC05N
SN74HC05N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74HC05N
SN74HC05NE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74HC05N
<a href="#">SN74HC05NSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
SN74HC05NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
SN74HC05NSRE4	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
<a href="#">SN74HC05PWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HC05
SN74HC05PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
<a href="#">SN74HC05PWRG4</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
SN74HC05PWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05
<a href="#">SN74HC05PWT</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 125	HC05
<a href="#">SN74HCS05DYYR</a>	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS05
SN74HCS05DYYR.A	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS05

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SNJ54HC05FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-88718012A SNJ54HC 05FK
SNJ54HC05FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-88718012A SNJ54HC 05FK
<a href="#">SNJ54HC05J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8871801CA SNJ54HC05J
SNJ54HC05J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8871801CA SNJ54HC05J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54HC05, SN74HC05 :**

- Catalog : [SN74HC05](#)
- Military : [SN54HC05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC05DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC05PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC05PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS05DYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

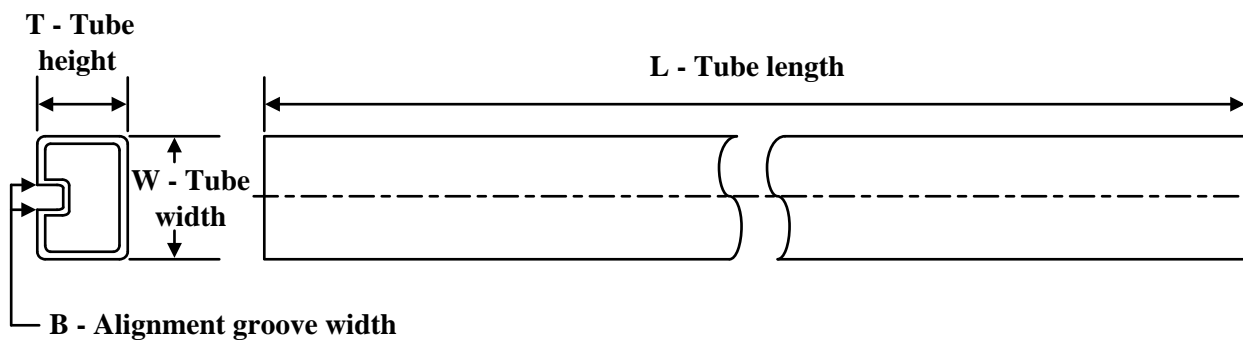
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC05DRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74HC05NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HC05PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HC05PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HCS05DYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-88718012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC05N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC05N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC05N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC05N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC05NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC05NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54HC05FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC05FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



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# EXAMPLE BOARD LAYOUT

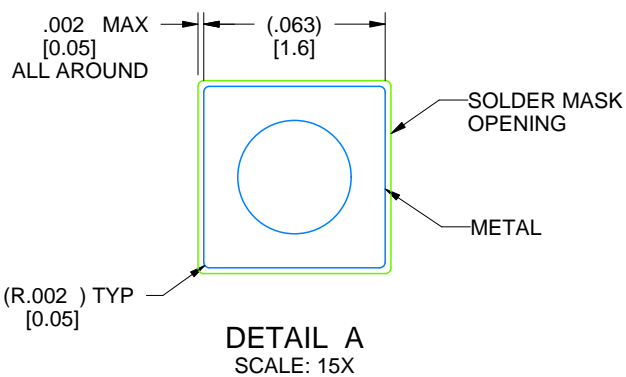
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017



N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

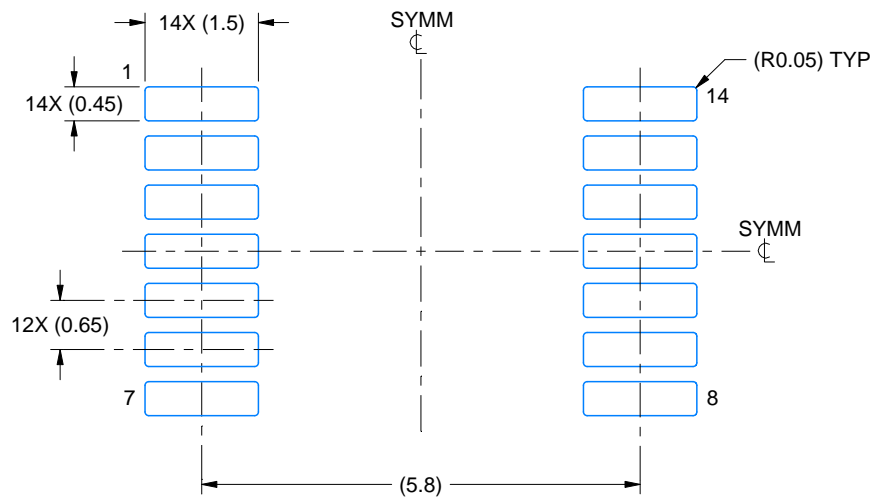


# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

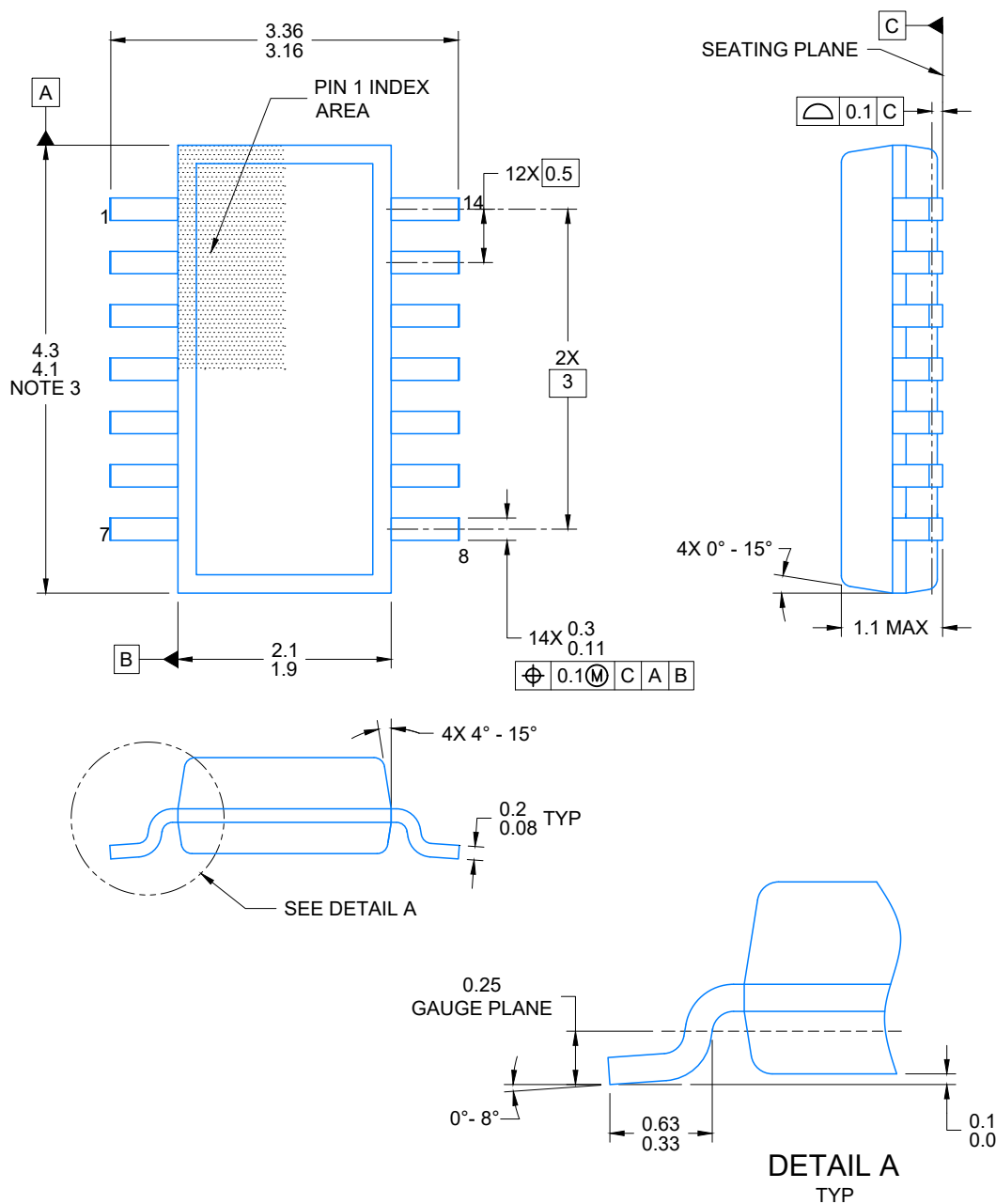


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

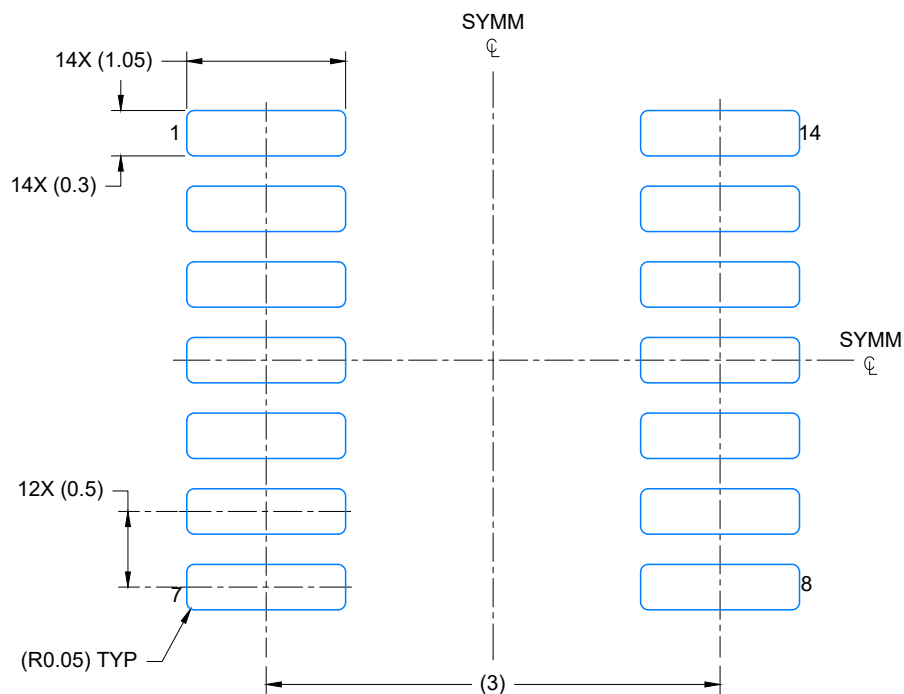


4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB





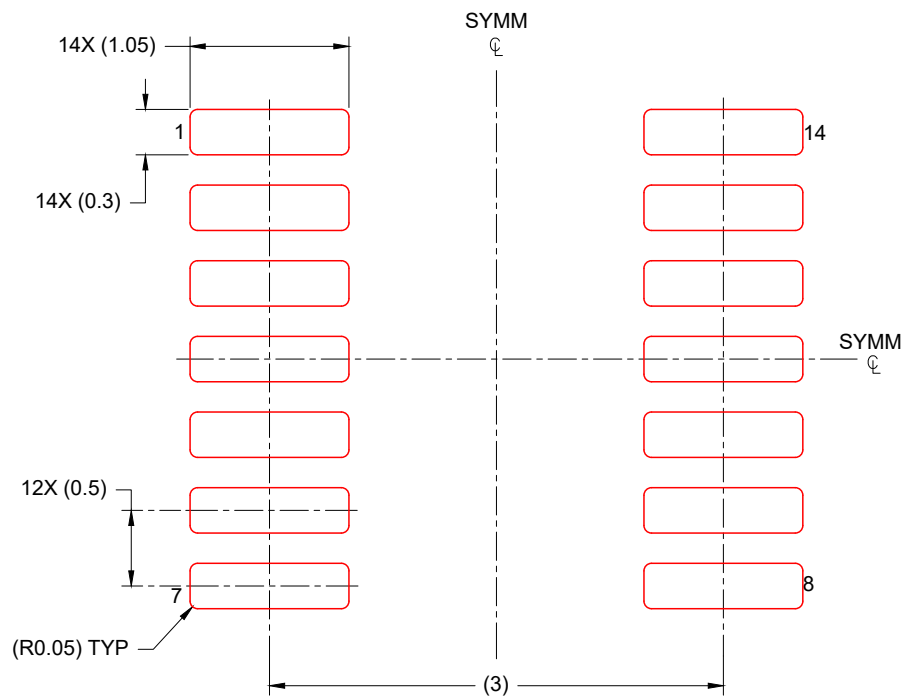
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224643/D 07/2024

## NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 20X

4224643/D 07/2024

## NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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最終更新日：2025 年 10 月