

## SNx4LVC00A クワッド、2 入力、正論理 NAND ゲート

### 1 特長

- JESD 22 を上回る ESD 保護
  - 2000V 人体モデル
  - 1000V 荷電デバイス モデル
- SN74LVC00A 動作範囲 1.65V ~ 3.6V
- SN54LVC00A 動作範囲 2V ~ 3.6V
- SNx4LVC00A  $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$  および  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$  で動作を規定
- SN54LVC00A  $-55^{\circ}\text{C} \sim +125^{\circ}\text{C}$  で動作を規定
- 5.5V までの入力電圧に対応
- 最大  $t_{pd}$  4.3ns (3.3V 時)
- $V_{OLP}$  標準値 (出力グランド バウンス)  $< 0.8\text{V}$  ( $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ )
- $V_{OHV}$  標準値 (出力  $V_{OH}$  アンダーシュート)  $> 2\text{V}$  ( $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ )
- JESD 17 準拠  
250mA 超のラッチアップ性能
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

### 2 アプリケーション

- AV レシーバ
- オーディオ ドック : ポータブル
- Blu-ray プレーヤおよびホーム シアター
- MP3 プレーヤ / レコーダ
- パーソナル デジタル アシスタント (PDA)
- 電源 : テレコム / サーバ AC/DC 電源 : シングルコントローラ : アナログおよびデジタル
- ソリッド ステート ドライブ (SSD) : クライアントおよびエンタープライズ
- テレビ : LCD、デジタル、高解像度 (HDTV)
- タブレット : エンタープライズ
- ビデオ分析 : サーバ
- ワイヤレス ヘッドセット、キーボード、マウス

### 3 概要

SN54LVC00A クワッド 2 入力正論理 NAND ゲートは 2.7V ~ 3.6V の  $V_{CC}$  で動作するように設計されており、SN74LVC00A クワッド 2 入力正論理 NAND ゲートは 1.65V ~ 3.6V の  $V_{CC}$  で動作するように設計されています。

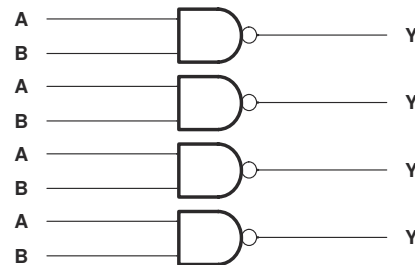
SNx4LVC00A デバイスは、ブール関数  $Y = \overline{A \cdot B}$ 、すなわち  $Y = \overline{A + B}$  を正論理で実行します。

入力は 3.3V または 5V のデバイスから駆動できます。この機能により、3.3V と 5V が混在するシステム環境での変換装置としてこのデバイスを使用できます。

#### 製品情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (3)
SNx4LVC00A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65 mm × 3.91 mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.20 mm × 5.30 mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.30 mm × 5.30 mm
	PW (TSSOP, 14)	5mm × 4.4mm	5.00 mm × 4.40 mm
	RGY (VQFN, 14)	3.5mm × 3.5mm	3.50 mm × 3.50 mm
	FK (LCCC, 20)	8.9mm × 8.9mm	8.89 mm × 8.89 mm
	J (CDIP, 14)	19.55mm × 7.9mm	19.55 mm × 6.7mm
W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm	

- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



概略回路図



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## 4 Pin Configuration and Functions

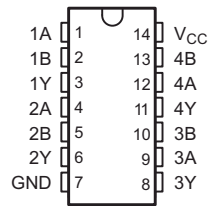
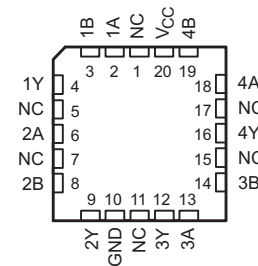


图 4-1. SN54LVC00A J or W Package; SN74LVC00A D, DB, NS, or PW Package 14-Pin CDIP, CFP SOIC, SSOP, SO, or TSSOP (Top View)



NC - No internal connection

图 4-2. SN54LVC00A FK Package 20-Pin LCCC (Top View)

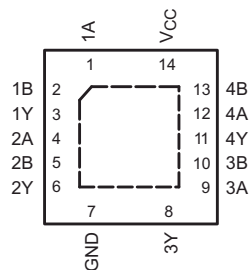


图 4-3. SN74LVC00A BQA or RGY Package 14-Pin WQFN or VQFN (Top View)

表 4-1. Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	SN74LVC00A		SN54LVC00A			
	D, DB, NS, PW	BQA, RGY	J, W	FK		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	4	4	6	I	Gate 2 input
2B	5	5	5	8	I	Gate 2 input
2Y	6	6	6	9	O	Gate 2 output
GND	7	7	7	10	I	Ground Pin
3Y	8	8	8	12	O	Gate 3 output
3A	9	9	9	13	I	Gate 3 input
3B	10	10	10	14	I	Gate 3 input
4Y	11	11	11	16	O	Gate 4 output
4A	12	12	12	18	I	Gate 4 input
4B	13	13	13	19	I	Gate 4 input
V <sub>CC</sub>	14	14	14	20	—	Positive supply
NC	—	—	—	1	—	No Connection
				5		
				7		
				11		
				15		
				17		

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	-0.5	6.5	V	
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6.5	V	
V <sub>O</sub>	Output voltage <sup>(2) (3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA	
I <sub>O</sub>	Continuous output current		±50	mA	
V <sub>CC</sub>	Continuous current through GND		±100	mA	
P <sub>tot</sub>	Power dissipation <sup>(4) (5)</sup>	T <sub>A</sub> = -40°C to +125°C	500	mW	
T <sub>J</sub>	Junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.
- (4) For the D package: above 70°C, the value of P<sub>tot</sub> derates linearly with 8 mW/K.
- (5) For the DB, NS, and PW packages: above 60°C, the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions, SN54LVC00A

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54LVC00A		UNIT	
		-55°C to +125°C			
		MIN	MAX		
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		V	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		V	
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V	-12	mA	
		V <sub>CC</sub> = 3 V	-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V	12	mA	
		V <sub>CC</sub> = 3 V	24		

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

## 5.4 Recommended Operating Conditions, SN74LVC00A

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN74LVC00A						UNIT		
		T <sub>A</sub> = 25°C		–40°C to 85°C		–40°C to 125°C				
		MIN	MAX	MIN	MAX	MIN	MAX			
V <sub>CC</sub>	Supply voltage	Operating		1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only		1.5		1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.7		1.7		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		2		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		0.7		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		0.8		0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–4		–4		–4		mA
		V <sub>CC</sub> = 2.3 V		–8		–8		–8		
		V <sub>CC</sub> = 2.7 V		–12		–12		–12		
		V <sub>CC</sub> = 3 V		–24		–24		–24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4		4		4		mA
		V <sub>CC</sub> = 2.3 V		8		8		8		
		V <sub>CC</sub> = 2.7 V		12		12		12		
		V <sub>CC</sub> = 3 V		24		24		24		

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

## 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LVC00A						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.3	127.8	140.4	123.8	150.8	92.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.6 Electrical Characteristics, SN54LVC00A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC00A		UNIT
			–55°C to +125°C		
			MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	2.7 V to 3.6 V	V <sub>CC</sub> – 0.2		V
	I <sub>OH</sub> = –12 mA	2.7 V	2.2		
	I <sub>OH</sub> = –24 mA	3 V	2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V	0.2		V
	I <sub>OL</sub> = 12 mA	2.7 V	0.4		
	I <sub>OL</sub> = 24 mA	3 V	0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V	±5		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	10		μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500		μA

## 5.7 Electrical Characteristics, SN74LVC00A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN74LVC00A						UNIT	
			T <sub>A</sub> = 25°C			–40°C to +85°C		–40°C to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2		V <sub>CC</sub> – 0.3		V
	I <sub>OH</sub> = –4 mA	1.65 V	1.29			1.2		1.05		
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			1.7		1.55		
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
I <sub>OH</sub> = –24 mA	3 V	2.3			2.2		2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.1		0.2		V
	I <sub>OL</sub> = 4 mA	1.65 V				0.24		0.45		
	I <sub>OL</sub> = 8 mA	2.3 V				0.3		0.7		
	I <sub>OL</sub> = 12 mA	2.7 V				0.4		0.6		
	I <sub>OL</sub> = 24 mA	3 V				0.55		0.8		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V				±1		±5		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V				1		10		μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V				500		500		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V				5				pF

## 5.8 Switching Characteristics, SN54LVC00A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54LVC00A		UNIT
				–55°C to +125°C		
				MIN	MAX	
t <sub>pd</sub>	A or B	Y	2.7 V	5.1		ns
			3.3 V ± 0.3 V	1	4.3	

### 5.9 Switching Characteristics, SN74LVC00A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74LVC00A						UNIT	
				T <sub>A</sub> = 25°C			–40°C to +85°C		–40°C to +125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t <sub>pd</sub>	A or B	Y	1.8 V ± 0.15 V	1	6	12	1	12.5	1	14	ns
			2.5 V ± 0.2 V	1	4.6	5.9	1	6.4	1	7.9	
			2.7 V	1	4.3	4.9	1	5.1	1	6.5	
			3.3 V ± 0.3 V	1	3.5	4.1	1	4.3	1	5.5	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V					1		1.5	ns

### 5.10 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	18	pF
			2.5 V	18	
			3.3 V	19	

### 5.11 Typical Characteristics

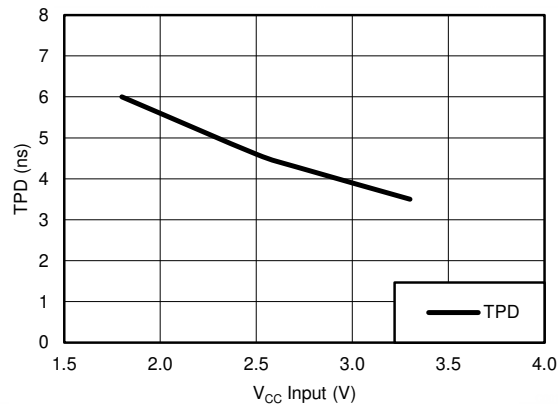
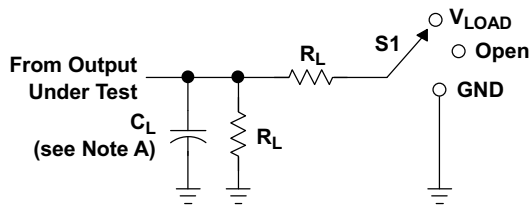


図 5-1. TPD vs V<sub>CC</sub> (T<sub>A</sub> = 25°C)

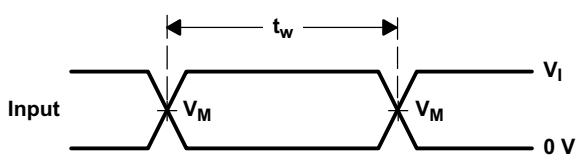
## 6 Parameter Measurement Information



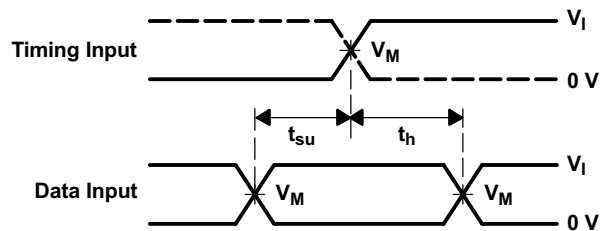
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

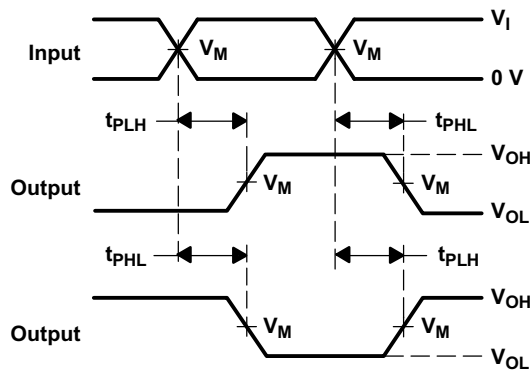
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



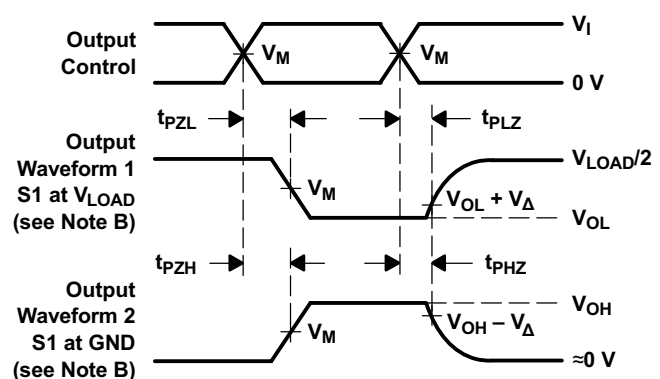
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The maximum sink and source current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

### 7.2 Functional Block Diagram



図 7-1. Logic Diagram, Each Gate (Positive Logic)

### 7.3 Feature Description

#### 7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [セクション 5.1](#) must be followed at all times.

#### 7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the [セクション 5.6](#) and [セクション 5.7](#). The worst case resistance is calculated with the maximum input voltage, given in the [セクション 5.1](#), and the maximum input leakage current, given in the [セクション 5.6](#) and [セクション 5.7](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in [セクション 5.3](#) and [セクション 5.4](#) to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

#### 7.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

#### 注意

Voltages beyond the values specified in the [セクション 5.1](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

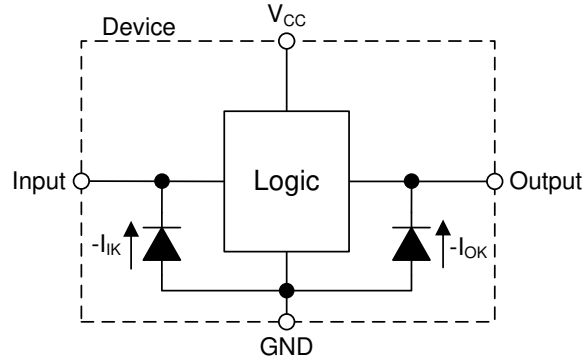


図 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

### 7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [セクション 5.1](#).

### 7.4 Device Functional Modes

表 7-1 lists the functional modes of SN54LVC00A and SN74LVC00A.

表 7-1. Function Table  
(Each Gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

SN74LVC00A is a high-drive CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to allowing the device to perform mixed-voltage input down translation. For example the A input can be 3.3 V and the B input can be 5 V, while  $V_{CC} = 2.5$  V and the device will operate properly to output a 2.5 V signal.

### 8.2 Typical Application

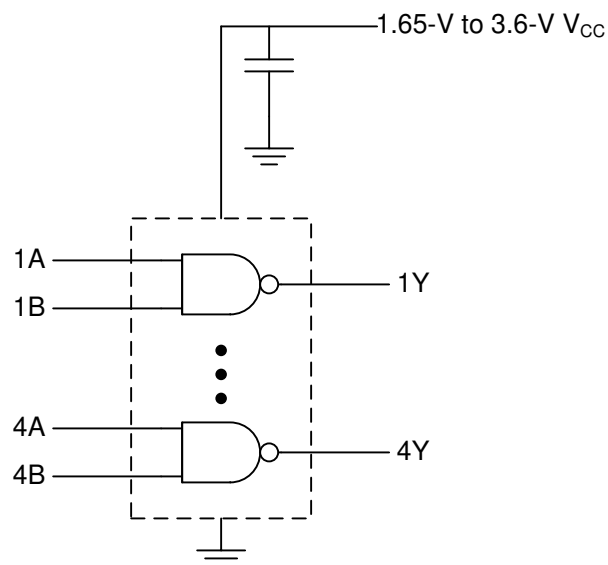


図 8-1. Typical NAND Gate Application and Supply Voltage

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [セクション 5.4](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [セクション 5.4](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommended Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above 5.5 V.

### 8.2.3 Application Curve

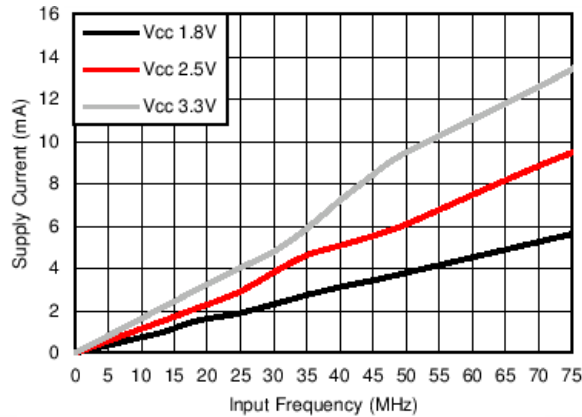


図 8-2. I<sub>CC</sub> vs Frequency

### Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [セクション 5.4](#) table.

Each V<sub>CC</sub> pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V<sub>CC</sub> pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 8.3 Layout

#### 8.3.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [セクション 8.3.2](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub>, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

#### 8.3.2 Layout Example

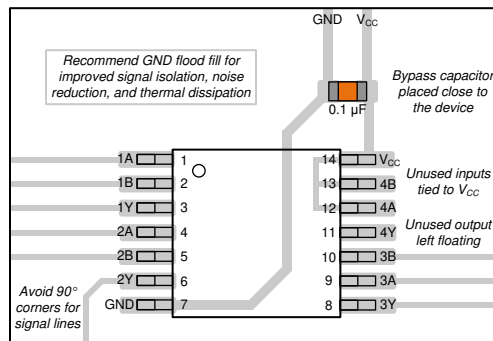


図 8-3. Layout Diagram for the SNx4LVC00A

## 9 Device and Documentation Support

### 9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC00A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LVC00A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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#### 9.3.1 Community Resources

### 9.4 Trademarks

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### 9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

#### Changes from Revision T (May 2024) to Revision U (July 2024)

Page

- Updated R $\theta$ JA values: D = 86 to 127.8, all values in °C/W.....5
- Added *Typical Characteristics* ..... 7

#### Changes from Revision S (March 2024) to Revision T (May 2024)

Page

- Updated R $\theta$ JA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for R $\theta$ JC(top), R $\theta$ JB,  $\Psi$ JT,  $\Psi$ JB, and R $\theta$ JC(bot), all values in °C/W.....5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9753301Q2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9753301Q2A SNJ54LVC 00AFK
<a href="#">5962-9753301QCA</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9753301QC A SNJ54LVC00AJ
<a href="#">5962-9753301QDA</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9753301QD A SNJ54LVC00AW
<a href="#">5962-9753301VDA</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9753301VD A SNV54LVC00AW
<a href="#">SN74LVC00ABQAR</a>	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00ABQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC00A
<a href="#">SN74LVC00AD</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00AD.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
<a href="#">SN74LVC00ADBR</a>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00ADBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00ADBR.B	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00ADBRG4	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00ADE4	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
<a href="#">SN74LVC00ADR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00ADR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00ADRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
<a href="#">SN74LVC00ADT</a>	Active	Production	SOIC (D)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00ADT.B	Active	Production	SOIC (D)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
<a href="#">SN74LVC00ANSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
SN74LVC00ANSR.B	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC00ANSRG4	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC00A
<a href="#">SN74LVC00APW</a>	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APW.B	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWE4	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWG4	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
<a href="#">SN74LVC00APWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	Call TI   Sn   Nipdau	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWRE4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
<a href="#">SN74LVC00APWRG4</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWRG4.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
<a href="#">SN74LVC00APWT</a>	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
SN74LVC00APWT.B	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC00A
<a href="#">SN74LVC00ARGYR</a>	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC00A
SN74LVC00ARGYR.A	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC00A
SN74LVC00ARGYR.B	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC00A
SN74LVC00ARGYRG4	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC00A
SN74LVC00ARGYRG4.A	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC00A
SN74LVC00ARGYRG4.B	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC00A
<a href="#">SNJ54LVC00AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9753301Q2A SNJ54LVC 00AFK
<a href="#">SNJ54LVC00AJ</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9753301QC A SNJ54LVC00AJ
<a href="#">SNJ54LVC00AW</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9753301QD A SNJ54LVC00AW

(1) **Status:** For more details on status, see our [product life cycle](#).

- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC00A, SN54LVC00A-SP, SN74LVC00A :**

- Catalog : [SN74LVC00A](#), [SN54LVC00A](#)
- Automotive : [SN74LVC00A-Q1](#), [SN74LVC00A-Q1](#)
- Enhanced Product : [SN74LVC00A-EP](#), [SN74LVC00A-EP](#)
- Military : [SN54LVC00A](#)
- Space : [SN54LVC00A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC00ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC00ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC00ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC00ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC00ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC00APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC00APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC00APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC00APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC00ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVC00ARGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC00ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC00ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVC00ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC00ADT	SOIC	D	14	250	213.0	191.0	35.0
SN74LVC00ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC00APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC00APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC00APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC00APWT	TSSOP	PW	14	250	353.0	353.0	32.0
SN74LVC00ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
SN74LVC00ARGYRG4	VQFN	RGY	14	3000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9753301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9753301QDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-9753301VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC00AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC00AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC00ADE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC00APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC00APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC00APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC00APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC00AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC00AW	W	CFP	14	25	506.98	26.16	6220	NA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

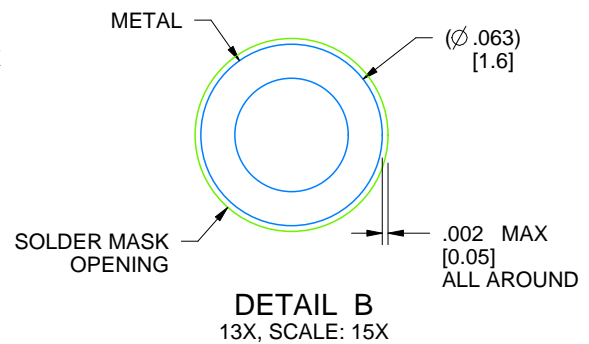
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

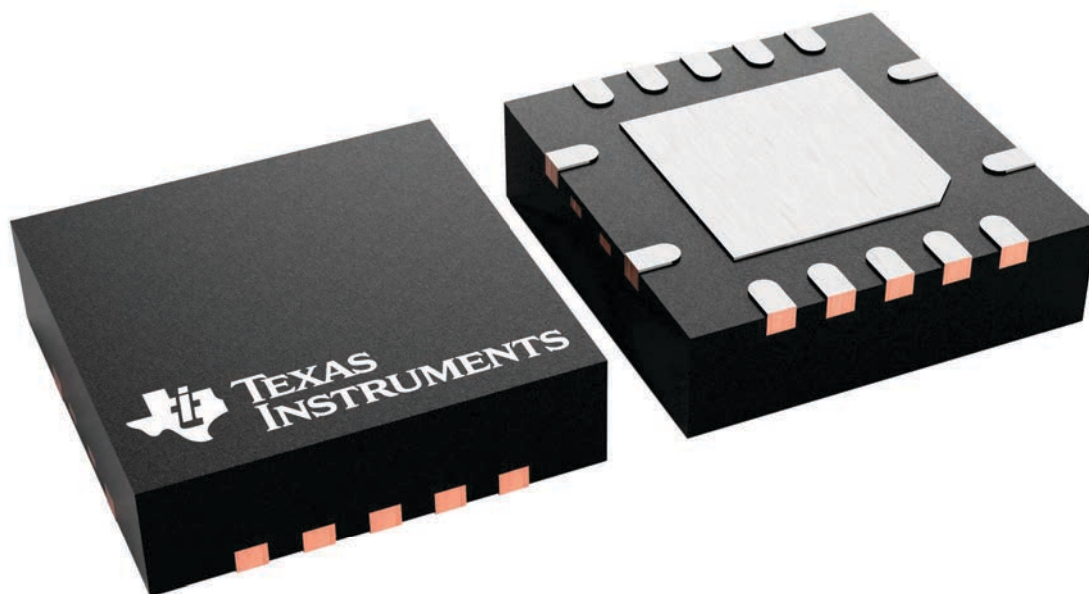
**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

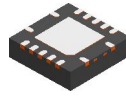
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A

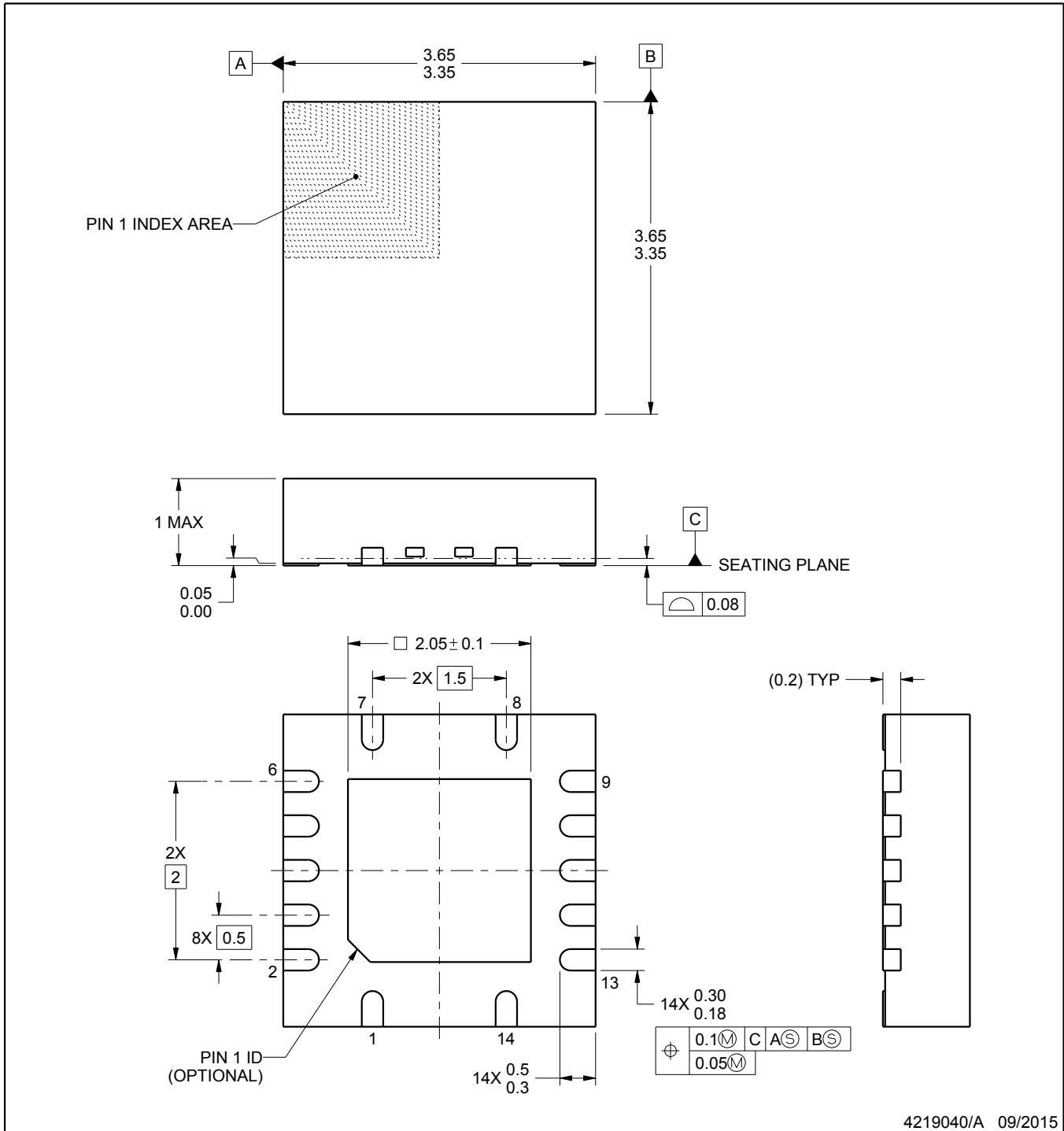
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

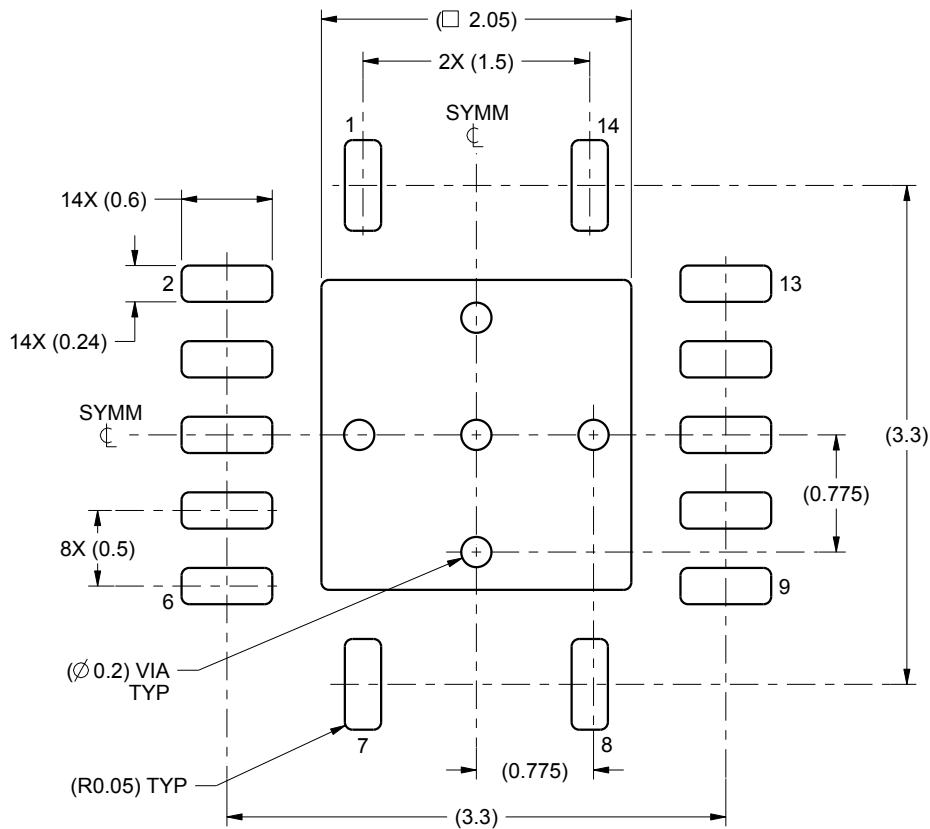
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

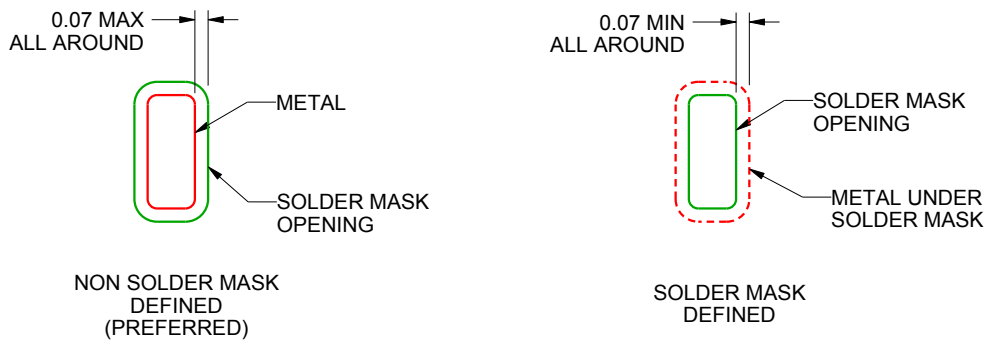
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

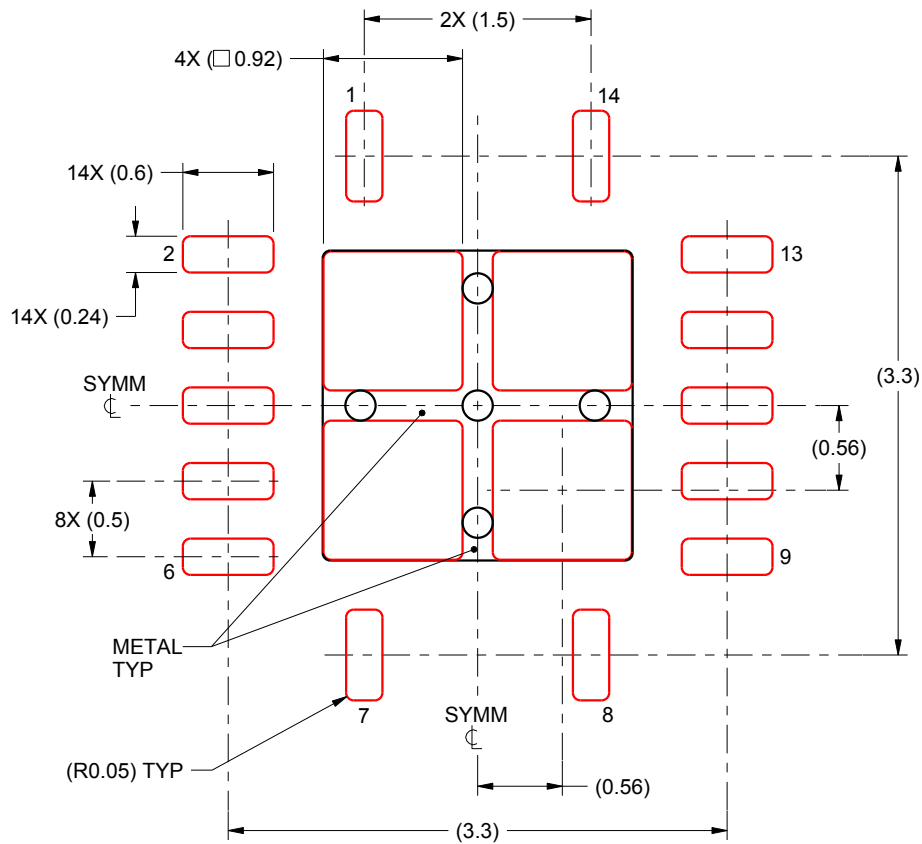
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

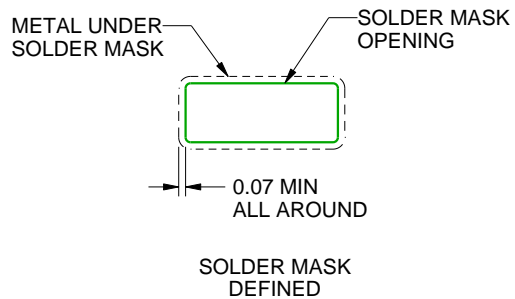
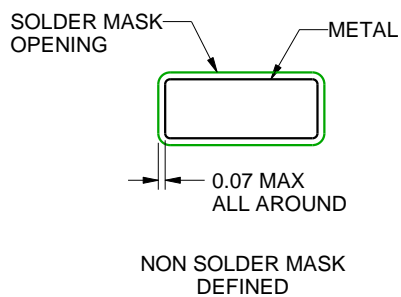
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

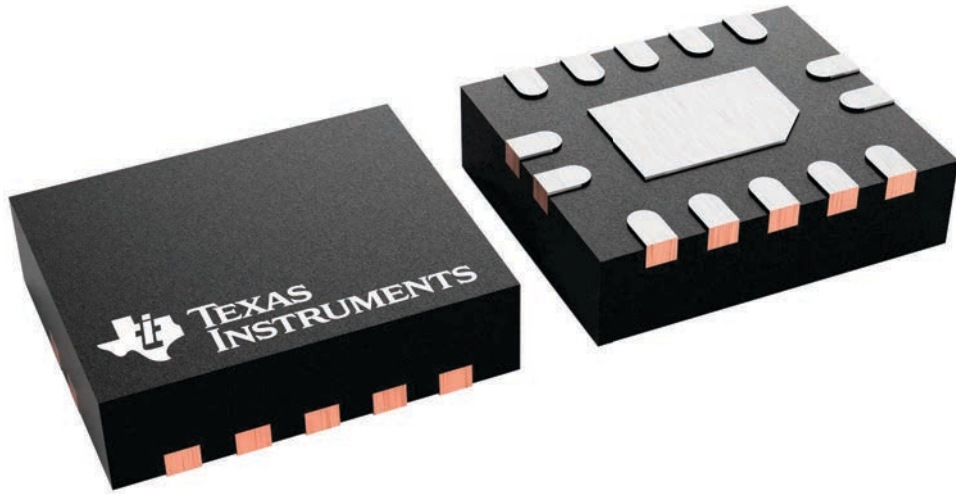
**BQA 14**

**WQFN - 0.8 mm max height**

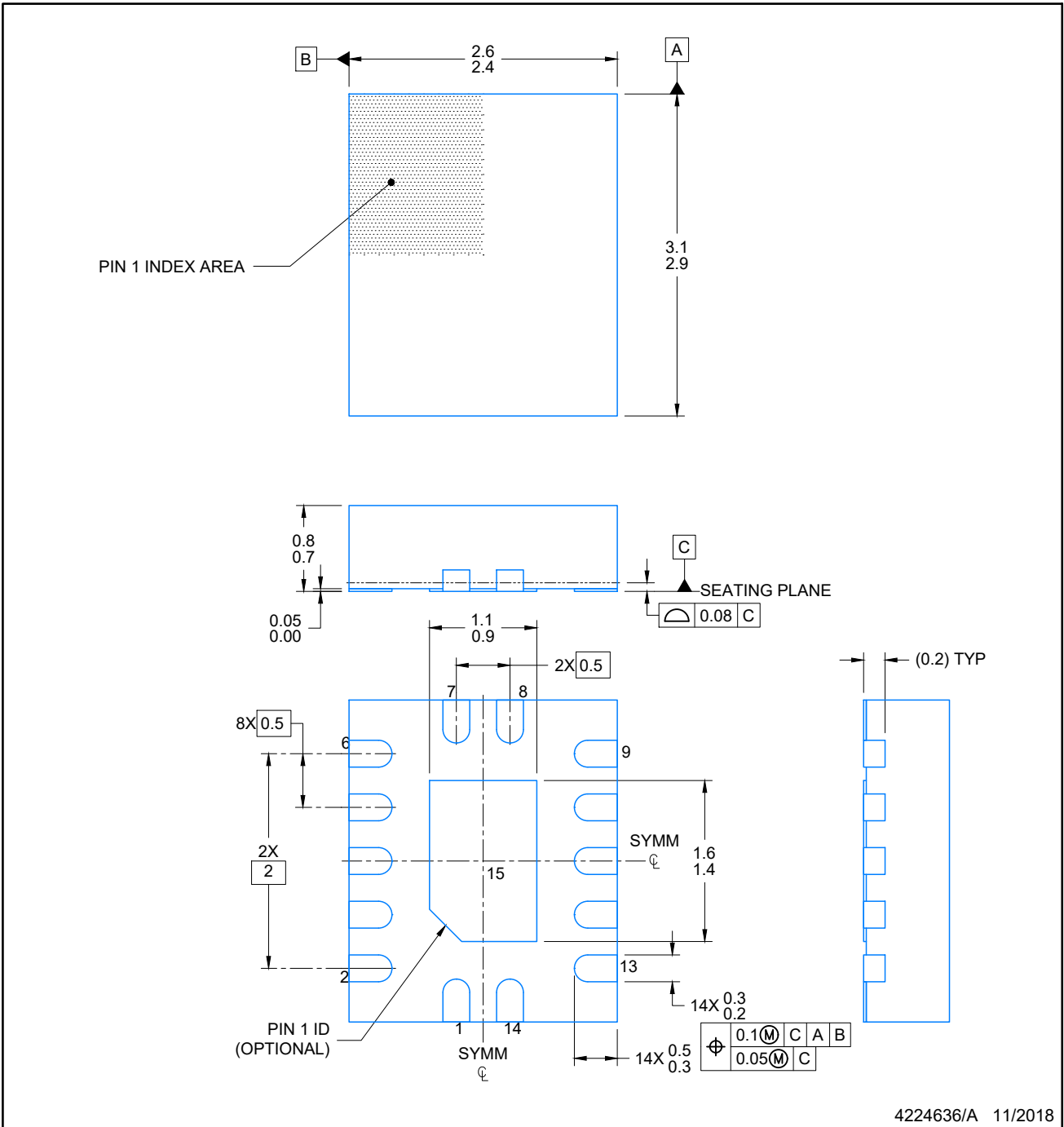
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A



NOTES:

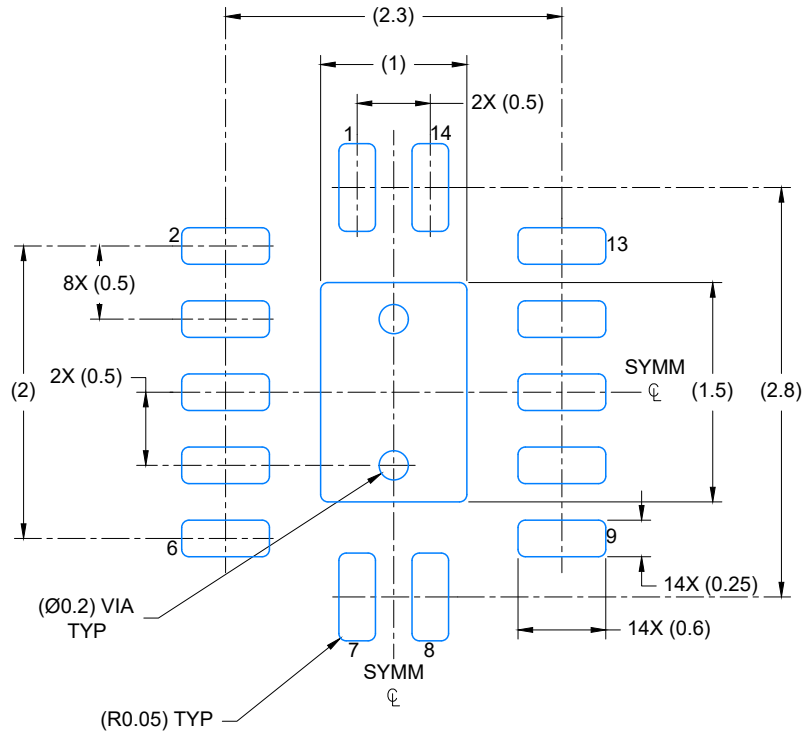
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

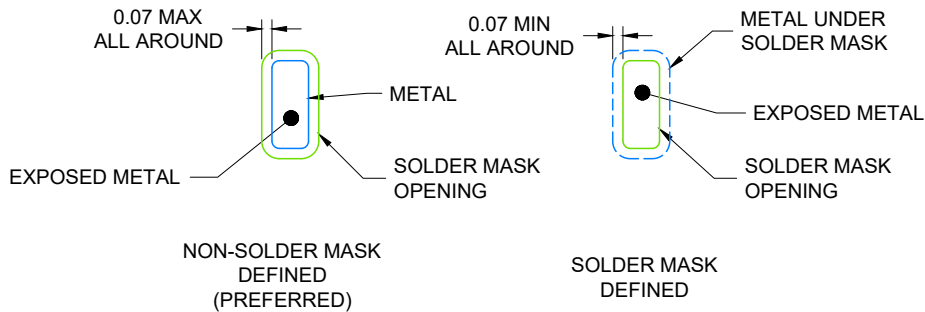
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

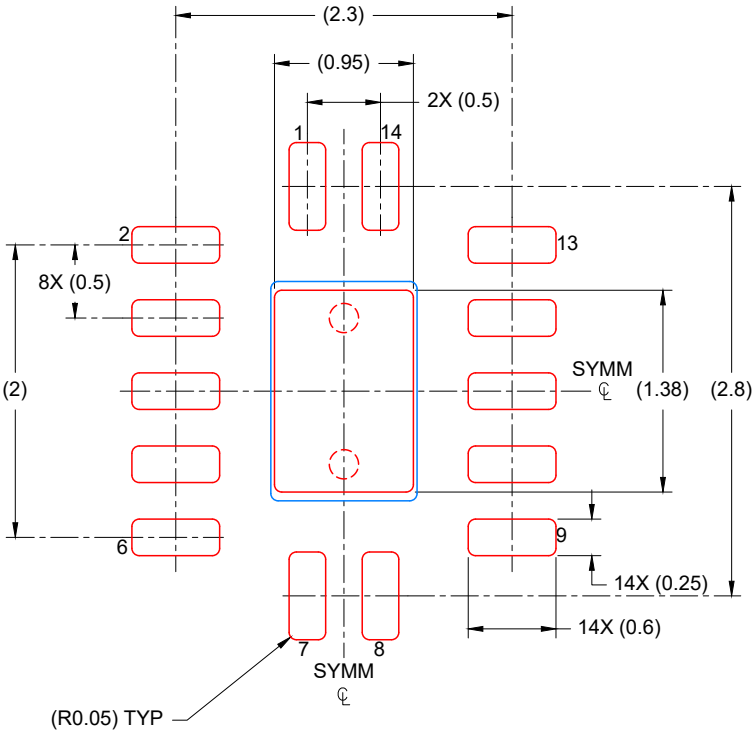
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
88% PRINTED COVERAGE BY AREA  
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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