TEXAS INSTRUMENTS
SN65220, SN65240, SN75240
JAJSLR6J – FEBRUARY 1997 – REVISED AUGUST 2022

# SNx52x0 USB ポート過渡電流サプレッサ

## 1 特長

- サブミクロンの 3V または 5V 回路をノイズ過渡から保護するように設計
- 以下を上回るポート ESD 保護性能:
  - 人体モデルで 15kV
  - マシン・モデルで 2kV
- WCSP チップ・スケール・パッケージで提供
- スタンドオフ電圧:6V (最小値)
- 低電流リーク:1µA 以下 (6V の場合)
- 低キャパシタンス:35pF (標準値)

## 2 アプリケーション

- USB フルスピード・ホスト、ハブ、ペリフェラル
- ポート

## 3 概要

SN65220 デバイスはデュアル、SN65240 および SN75240 デバイスはクワッドの単方向過渡電圧サプレッサ (TVS) です。これらのデバイスは、USB (Universal Serial Bus) ロー / フルスピード・ポートに対する電気的ノイズ過渡保護を提供します。入力容量が 35pF であるため、ハイスピード USB 2.0 アプリケーションには適していません。

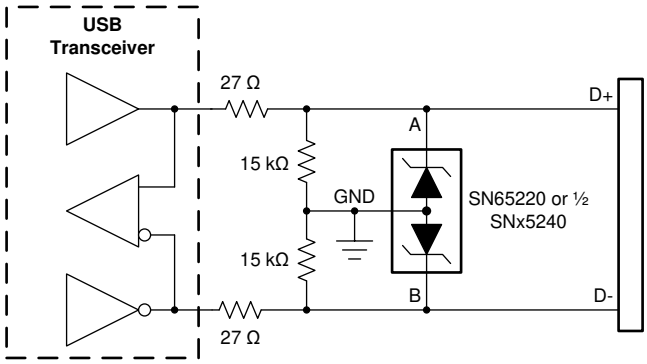
ケーブル接続されたすべての I/O は、各種ノイズ源からの電気的ノイズの過渡現象にさらされる可能性があります。このようなノイズ過渡は、十分な大きさと持続時間を持つ場合、USB トランシーバまたは USB ASIC に損傷を与える可能性があります。

SN65220、SN65240、SN75240 デバイスの ESD 性能は、IEC61000-4-2 に従ってシステム・レベルで測定されています。しかし、システム設計はこれらの試験の結果に影響を及ぼします。高水準の適合性を達成するには、入念な基板設計およびレイアウト技術が必要です。

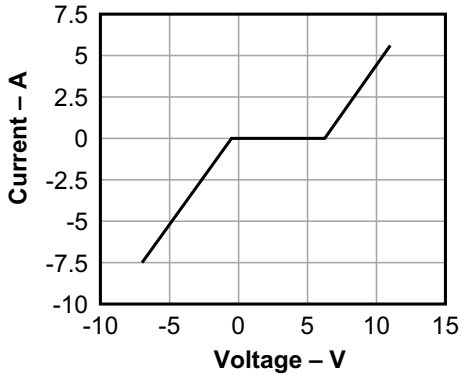
**製品情報** (1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| SN65220 | SOT-23 (6) | 2.90mm × 1.60mm |
| | DSBGA (4) | 0.925mm × 0.925mm |
| SN65240<br>SN75240 | PDIP (8) | 9.09mm × 6.35mm |
| | TSSOP (8) | 3.00mm × 4.40mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




概略回路図




TVS の電流と電圧との関係

# Table of Contents



## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision I (April 2021) to Revision J (August 2022)** — **Page**

- Updated the *SN65220*, *SN65240*, and *SN75240* suppressors in the *Device Comparison* table ... 3

**Changes from Revision H (May 2015) to Revision I (April 2021)** — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「概略回路図」の抵抗値の単位を O から Ω に更新 ... 1
- Updated the units from *O* to *Ω* in the *Typical Application Schematic for ESD Protection of USB Transceivers* figure ... 8
- Updated the units from *O* to *Ω* in the *Layout Example of a 4-Layer Board With SN65220* figure ... 10

**Changes from Revision G (August 2008) to Revision H (May 2015)** — **Page**

- 「*ピン構成および機能*」セクション、「*ESD*」表、「*熱に関する情報*」表、「*機能説明*」セクション、「*デバイスの機能モード*」、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 ... 1

## 5 Device Comparison Table

| PRODUCT | SUPPRESSORS | $T_A$ - RANGE | PACKAGE |
|---|---|---|---|
| SN65220 | 2 | –40°C to 85°C | WCSP-4 |
| | | | SOT23-6 |
| SN65240 | 4 | –40°C to 85°C | DIP-8 |
| | | | TSSOP-8 |
| SN75240 | 4 | 0°C to 70°C | DIP-8 |
| | | | TSSOP-8 |

## 6 Pin Configuration and Functions

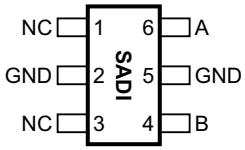



図 6-1. DBV Package, 6-Pin SOT-23 (Top View)

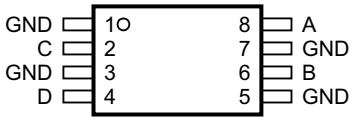



図 6-2. P, PW Package,s 8-Pin PDIP, TSSOP (Top View)

表 6-1. Pin Functions

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBV | P, PW | | |
| A | 6 | 8 | Analog input | Transient suppressor input – Line 1 |
| B | 4 | 6 | Analog input | Transient suppressor input – Line 2 |
| C | — | 2 | Analog input | Transient suppressor input – Line 3 |
| D | — | 4 | Analog input | Transient suppressor input – Line 4 |
| GND | 2, 5 | 1, 3, 5, 7 | Power | Local device ground |
| NC | 1, 3 | — | — | Internally not connected |

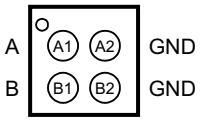



図 6-3. YZB Package, 4-Pin DSBGA (Top View)

表 6-2. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| A1 | A | Analog input | Transient suppressor input – Line 1 |
| B1 | B | Analog input | Transient suppressor input – Line 2 |
| A2, B2 | GND | Power | Local device ground |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $P_{D(peak)}$ | Peak power dissipation | | 60 | W |
| $I_{FSM}$ | Peak forward surge current | | 3 | A |
| $I_{RSM}$ | Peak reverse surge current | | –9 | A |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under セクション 7.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±15000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | SN75240 | 0 | 70 | °C |
| | | SN65220, SN65240 | –40 | 85 | |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | SN65220 | | SN65240, SN75240 | | UNIT |
|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | YZB (DSBGA) | P (PDIP) | PW (TSSOP) | |
| | | 6 PINS | 4 BALLS | 8 PINS | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 199.5 | 170 | 67.5 | 185.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 159.7 | 1.8 | 57.9 | 68.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 51.1 | 43.5 | 44.5 | 114.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 41 | 9.2 | 36.2 | 9.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 50.5 | 43.5 | 44.5 | 112.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg}$ | Leakage current | $V_I$ = 6 V at A, B, C, or D terminals | | | 1 | µA |
| $V_{(BR)}$ | Breakdown voltage | $V_I$ = 1 mA at A, B, C, or D terminals | 6.5 | 7 | 8 | V |
| $C_{IN}$ | Input capacitance to ground | $V_I$ = 0.4 sin (4E6πt) + 0.5 V | | 35 | | pF |

### 7.6 Typical Characteristics

$T_A$ = 25°C unless otherwise noted.

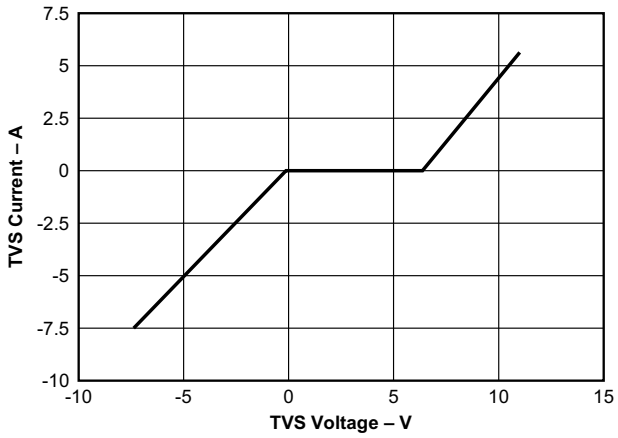



**図 7-1. Transient-Voltage-Suppressor Current vs Voltage**

## 8 Parameter Measurement Information

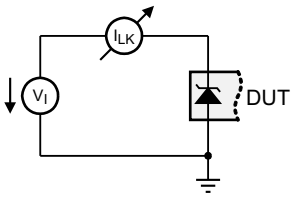



**図 8-1. Measurement of Leakage Current**

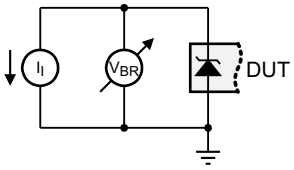



**図 8-2. Measurement of Breakdown Voltage**

# 9 Detailed Description

## 9.1 Overview

The SN65220, SN65240, and SN75240 devices integrate multiple unidirectional transient voltage suppressors (TVS). 図 9-1 shows the equivalent circuit diagram of a single TVS diode.

For positive transient voltages, only the Q1 transistor determines the switching characteristic. When the input voltage reaches the Zener voltage, $V_Z$, Zener diode D1 conducts; therefore, allowing for the base-emitter voltage, $V_{BE}$, to increase. At $V_{IN} = V_Z + V_{BE}$, the transistor starts conducting. From then on, its on-resistance decreases linearly with increasing input voltage.

For negative transient voltages, only diode D2 determines the switching characteristic. Here, switching occurs when the input voltage exceeds the diode forward voltage, $V_{FW}$.

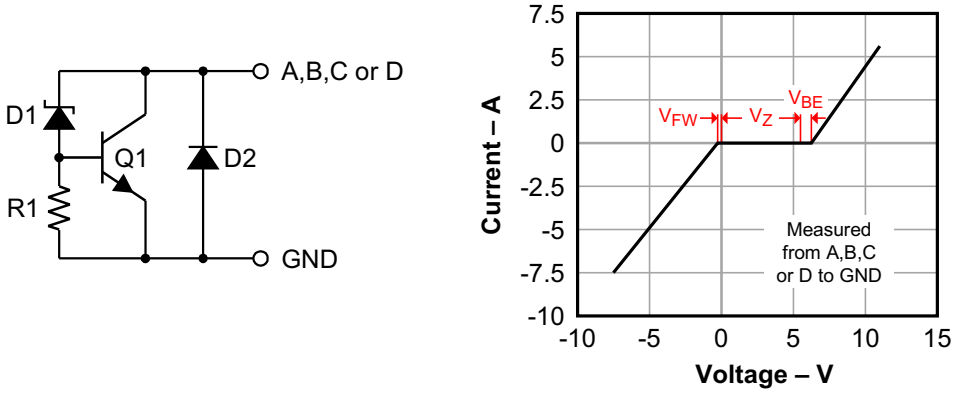
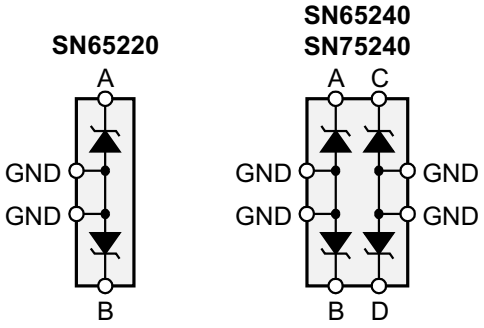



**図 9-1. TVS Structure and Current — Voltage Characteristic**

## 9.2 Functional Block Diagram



## 9.3 Feature Description

The SN65220, SN65240, and SN75240 family of unidirectional transient voltage suppressors provide transient protection to Universal Serial Bus low and full−speed ports. These TVS diodes provide a minimum breakdown voltage of 6.5-V to protect USB transceivers and USB ASICs typically implemented in 3-V or 5-V digital CMOS technology.

## 9.4 Device Functional Modes

TVS diodes possess two functional modes, a high-impedance and a conducting mode.

During normal operating conditions, that is in the absence of high voltage transients, the breakdown voltage of TVS diodes is not exceeded and the devices remain high-impedance.

In the presence of high-voltage transients the breakdown voltage is exceeded. The TVS diodes then conduct and become low-impedance. In this mode excessive transient energy is shunted directly to local circuit ground, preventing USB transceivers from electrical damage.

# 10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 10.1 Application Information

The USB has become a popular solution to connect PC peripherals. The USB allows devices to be hot-plugged in and out of the existing PC system without rebooting or turning off the PC. Because frequent human interaction with the USB system occurs as a result of its attractive hot-plugging ability, there is the possibility for large ESD strikes and damage to crucial system elements. The ESD protection included on the existing hardware is typically in the 2-kV to 4-kV range for the human body model (HBD) and 200-V to 300-V for the machine model (MM). The ESD voltage levels found in a normal USB operating environment can exceed these levels. The SN75240, SN65240, and SN65220 devices will increase the robustness of the existing USB hardware to ESD strikes common to the environment in which USB is likely to be used.

## 10.2 Typical Application

図 10-1 shows a typical USB system and application of the SN75240, SN65240, and SN65220 devices. Connections to pin A from the D+ data line, pin B from the D– data line, and the device grounds from the GND line that already exists are necessary to increase the amount of ESD protection provided to the USB port.

The design of the suppressor gives it very low maximum current leakage of 1 µA, a very low typical capacitance of 35 pF, and a standoff voltage minimum of 6 V. Because of these levels, the SN75240, SN65240, and SN65220 devices will provide added protection to the USB system hardware during ESD events without introducing the high capacitance and current leakage levels typical of external transient voltage suppressors. The addition of an SN75240, SN65240, or SN65220 device is beneficial to both full-speed and low-speed USB 1.1 bandwidth standards.

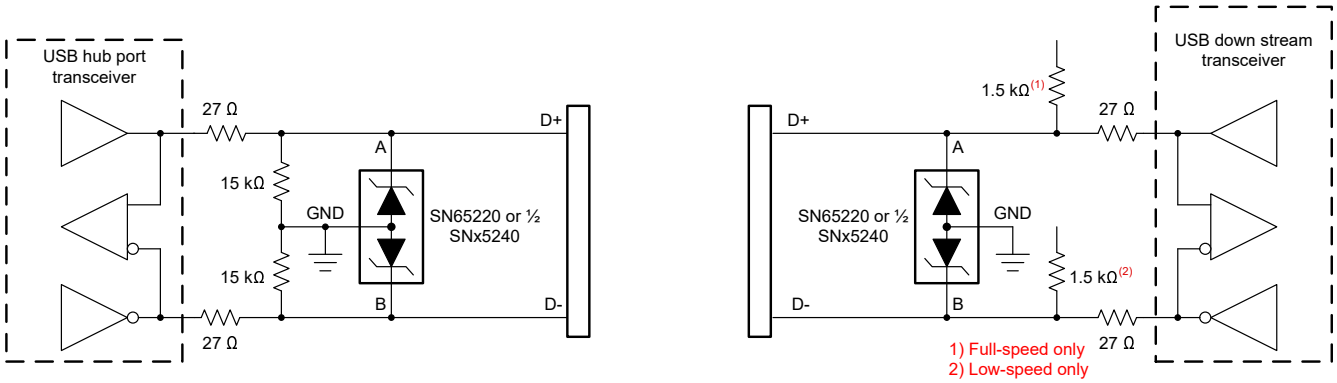



**図 10-1. Typical Application Schematic for ESD Protection of USB Transceivers**

### 10.2.1 Design Requirements

For this design example, use the parameters listed in 表 10-1 as design parameters.

**表 10-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Minimum breakdown voltage (TVS) | 6.5 V |
| Maximum supply voltage (USB transceiver) | 5.5 V |
| Typical junction capacitance (TVS) | 35 pF |
| Maximum data rate (USB transceiver) | 12 Mbps |

### 10.2.2 Detailed Design Procedure

To effectively protect USB transceivers, use TVS diodes with breakdown voltages close to 6 V, such as the SN65220, SN65240, or SN75220 devices.

Because of the TVS junction capacitance of 35 pF, apply these TVS diodes only to USB transceivers with full-speed capability that is 12 Mbps maximum.

Place the TVS diodes as close to the board connector as possible to prevent transient energies from entering further board space.

Connect the TVS diode between the data lines (D+, D–) and local circuit ground (GND).

Because noise transient represents high-speed frequencies, ensure low-inductance return paths for the transient currents by providing a solid ground plane and using two VIAs connecting the TVS terminals to ground.

### 10.2.3 Application Curve

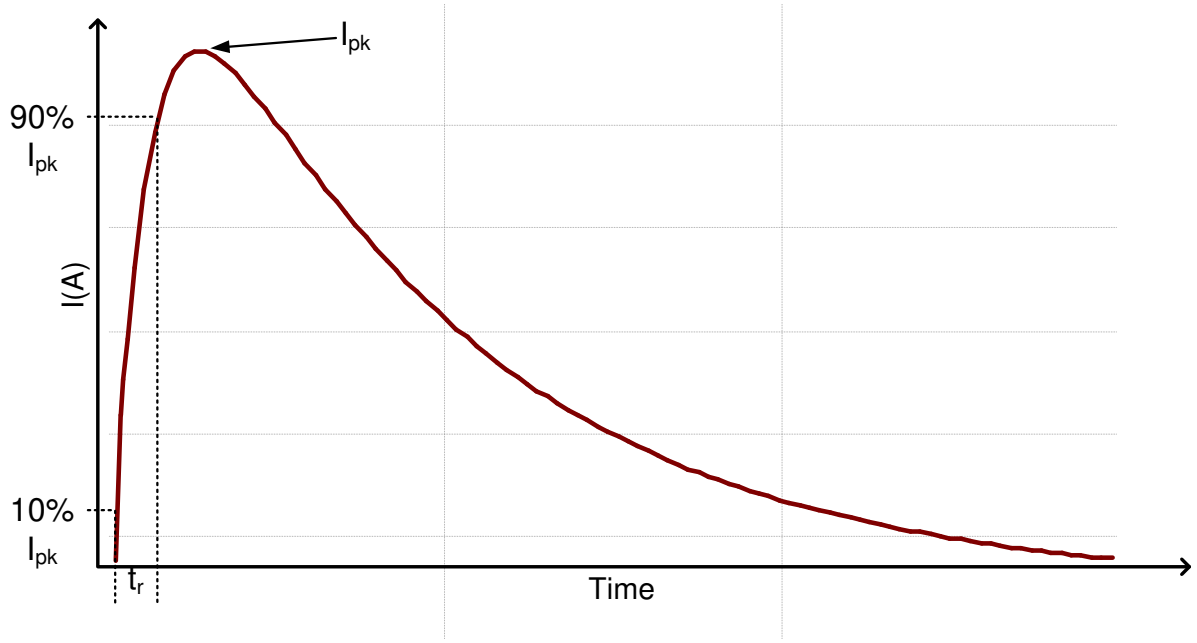



**図 10-2. HBM Curve**

# 11 Power Supply Recommendations

Unlike other semiconductor components that require a supply voltage to operate, the SN65220, SN65240, and SN75240 transient suppressors are combinations of multiple p-n diodes, activated by transient voltages. Therefore, these transient suppressors do not require external voltage supplies.

# 12 Layout

## 12.1 Layout Guidelines

The multiple ground pins provided lower the connection resistance to ground. In order to improve circuit operation, a connection to all ground pins must be provided on the system printed circuit board. Without proper device connection to ground, the speed and protection capability of the device will be degraded.

- The ground termination pads should be connected directly to a ground plane on the board for optimum performance. A single trace ground conductor will not provide an effective path for fast rise-time transient events including ESD due to parasitic inductance.
- Nominal inductive values of a PCB trace are approximately 20 nH/cm. This value may seem small, but an apparent *short length* of trace may be sufficient to produce significant L(di/dt) effects with fast rise-time ESD spikes.
- Mount the TVS as close as possible to the I/O socket to reduce radiation originating from the transient as it is routed to ground.

注

Direct connective paths of the traces are taken to the suppressor mounting pads to minimize parasitic inductance in the surge-current conductive path, thus minimizing L(di/dt) effects.

## 12.2 Layout Example

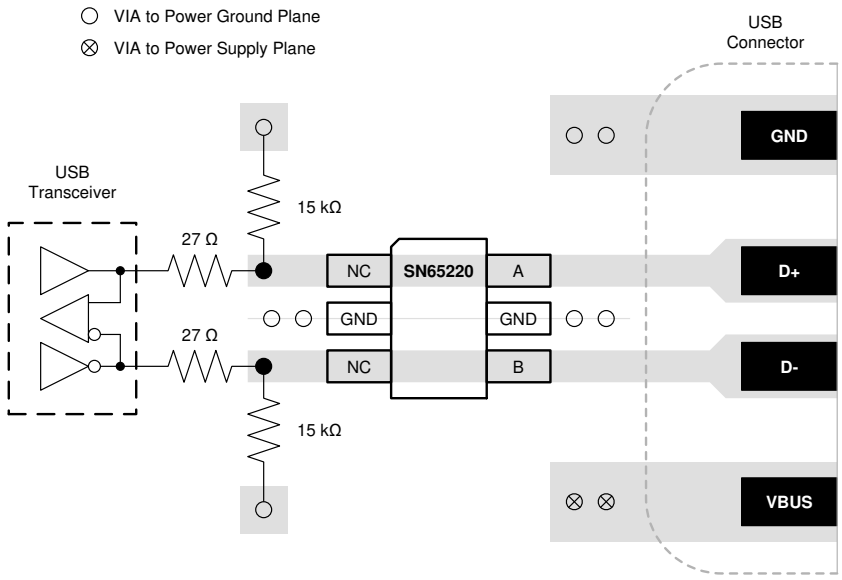



**図 12-1. Layout Example of a 4-Layer Board With SN65220**

# 13 Device and Documentation Support

## 13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65220DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SADI | Samples |
| SN65220DBVRG4 | LIFEBUY | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SADI | |
| SN65220DBVT | OBSOLETE | SOT-23 | DBV | 6 | | TBD | Call TI | Call TI | -40 to 85 | SADI | |
| SN65240P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN65240P | Samples |
| SN65240PW | OBSOLETE | TSSOP | PW | 8 | | TBD | Call TI | Call TI | -40 to 85 | A65240 | |
| SN65240PWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | A65240 | Samples |
| SN75240P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75240P | Samples |
| SN75240PW | OBSOLETE | TSSOP | PW | 8 | | TBD | Call TI | Call TI | 0 to 70 | A75240 | |
| SN75240PWR | OBSOLETE | TSSOP | PW | 8 | | TBD | Call TI | Call TI | 0 to 70 | A75240 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN65220 :**

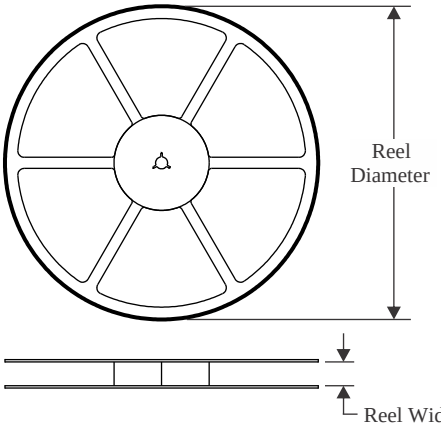
- Automotive : SN65220-Q1

NOTE: Qualified Version Definitions:

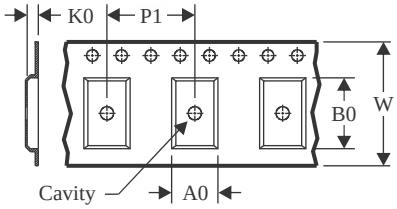
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

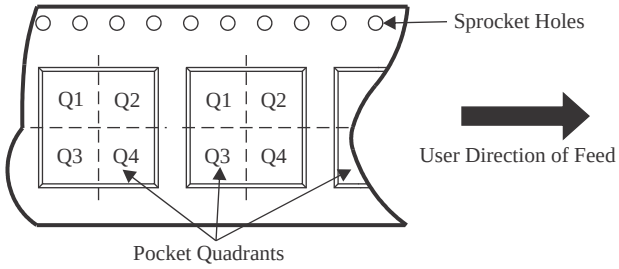



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

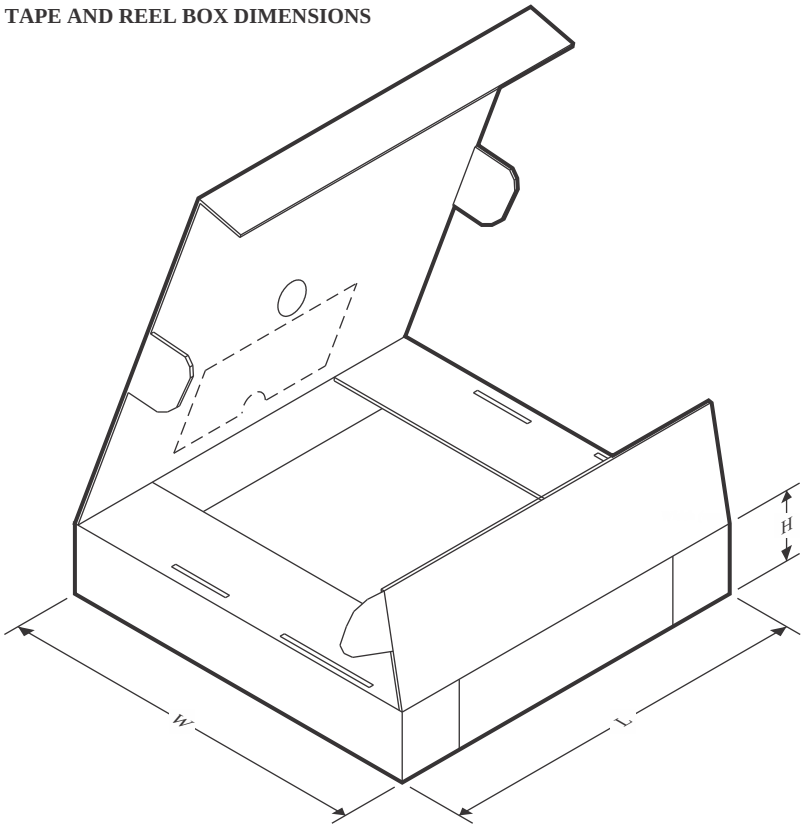
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65220DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN65220DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN65240PWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN75240PWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

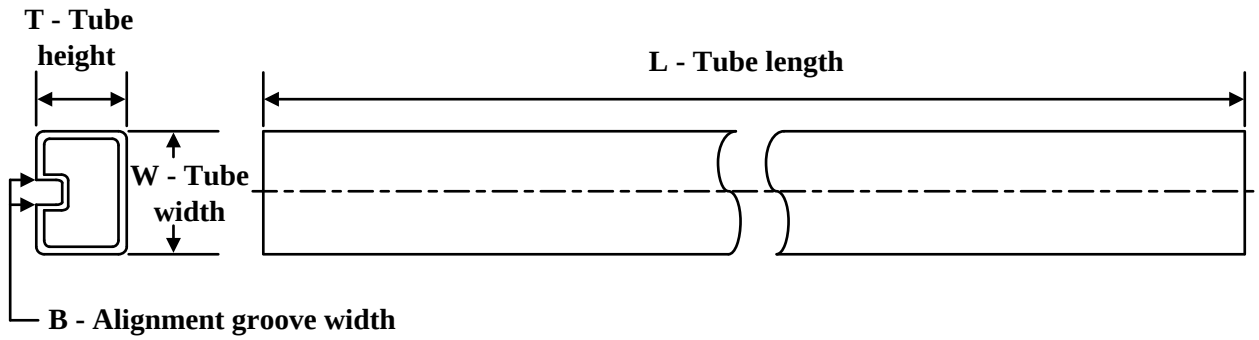
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65220DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN65220DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN65240PWR | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| SN75240PWR | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |

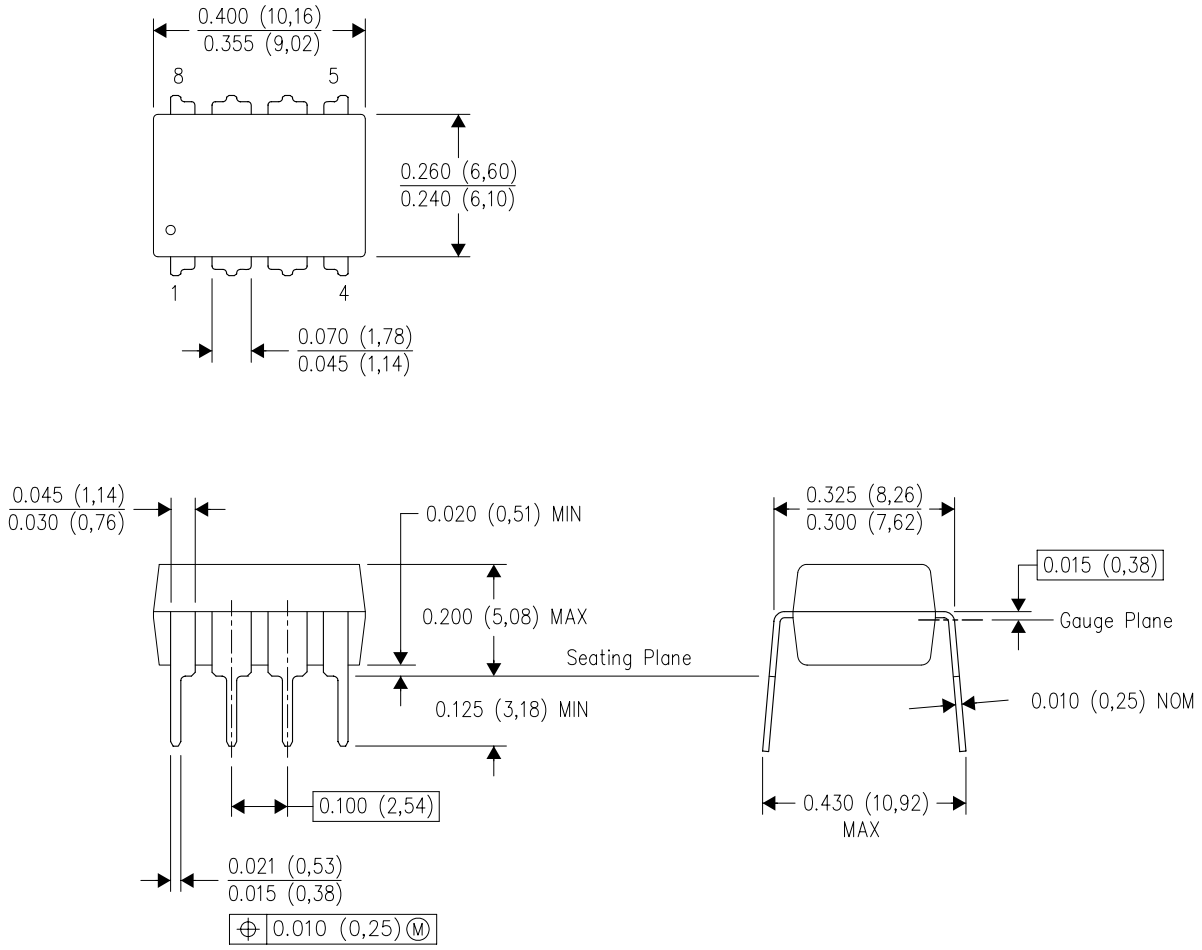
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN65240P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN65240PW | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |
| SN65240PWG4 | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |
| SN75240P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75240PW | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |
| SN75240PWG4 | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



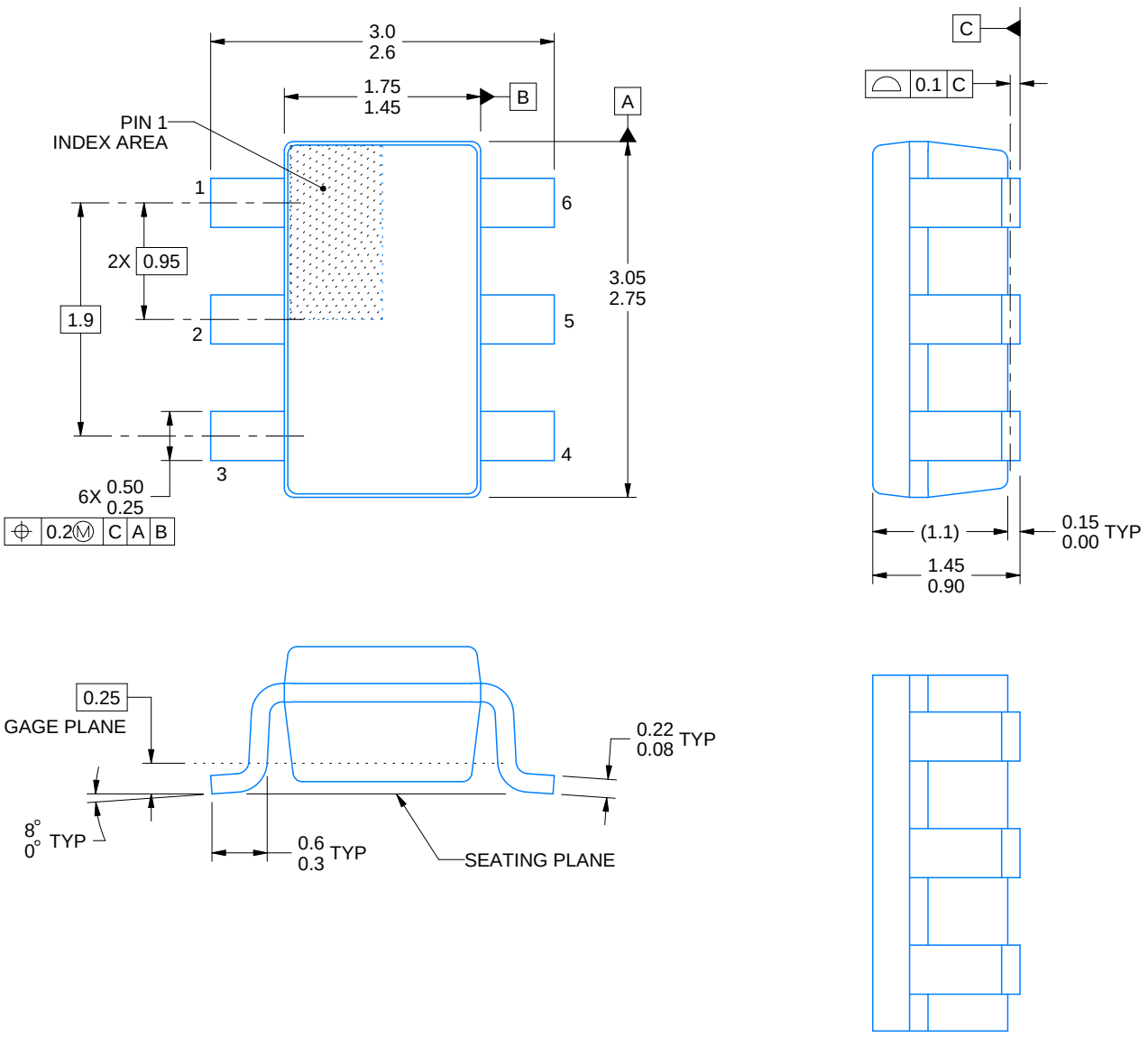

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

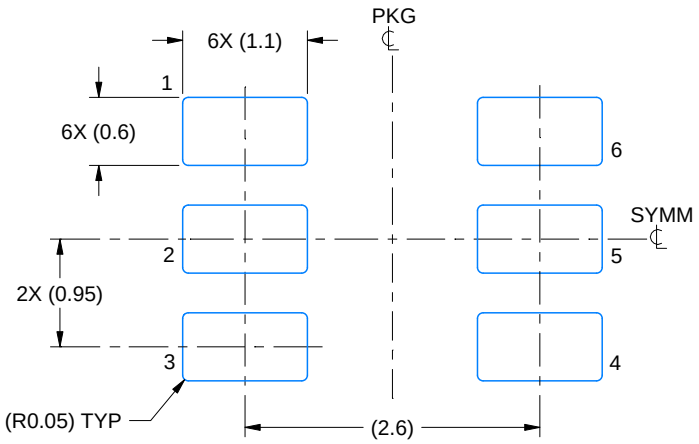



ALTERNATIVE PACKAGE SINGULATION VIEW

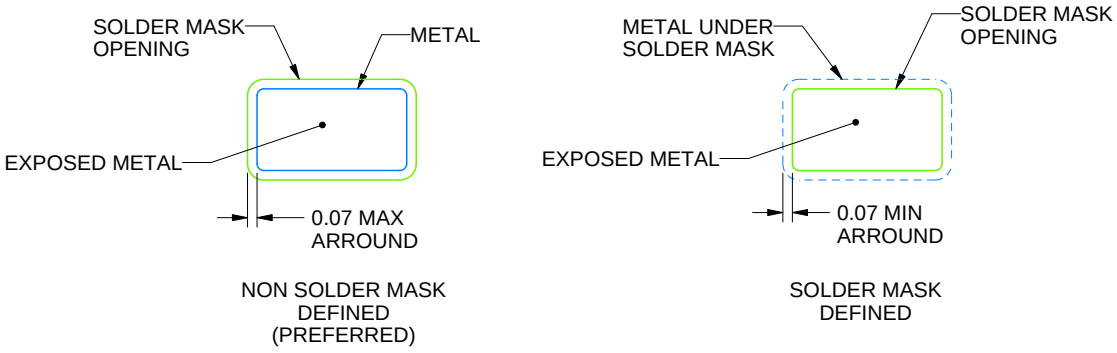
4214840/F 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

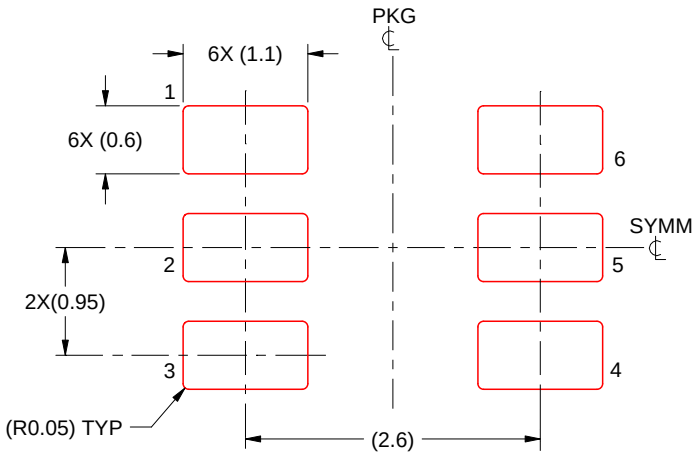



SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

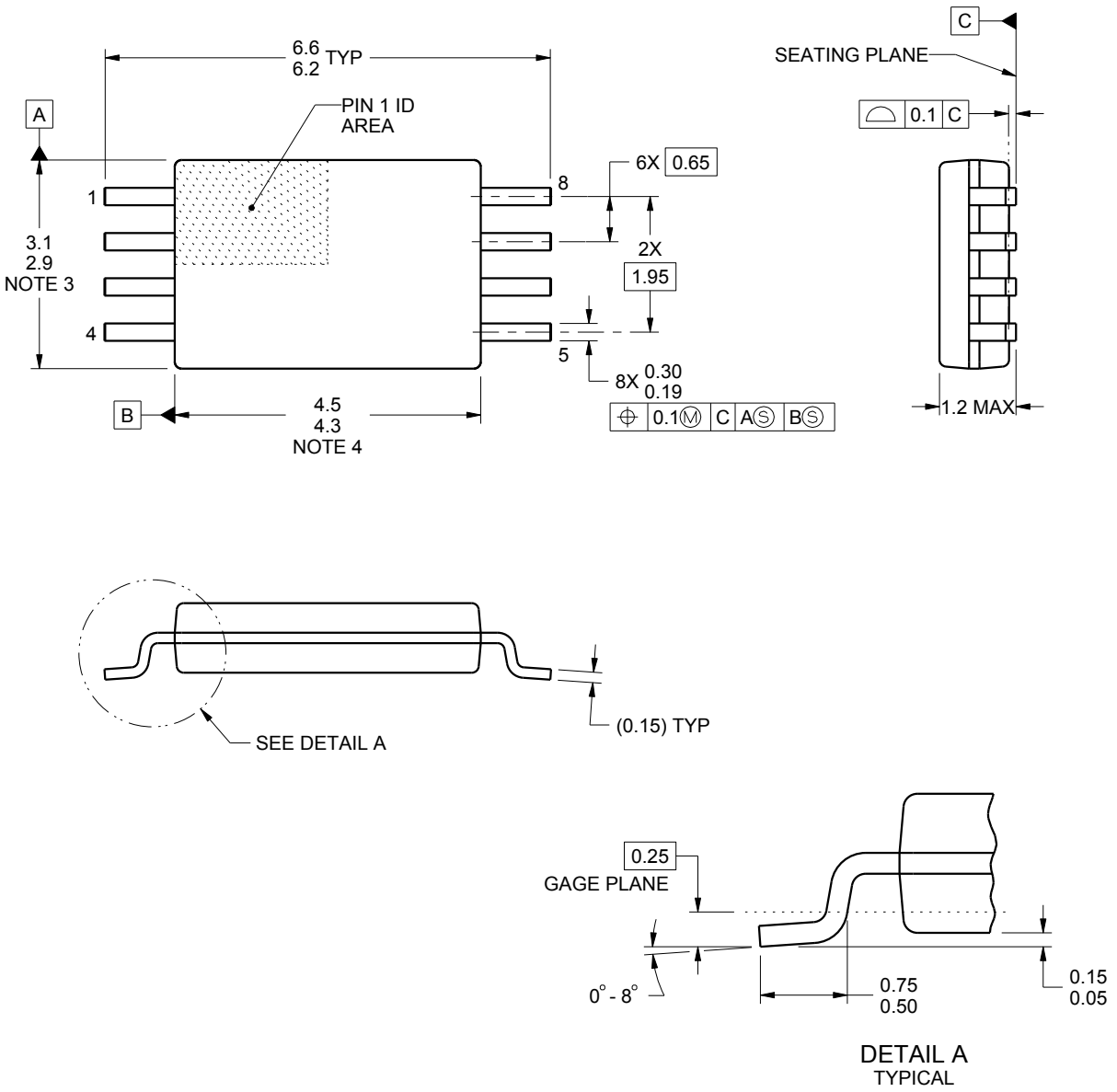
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0008A

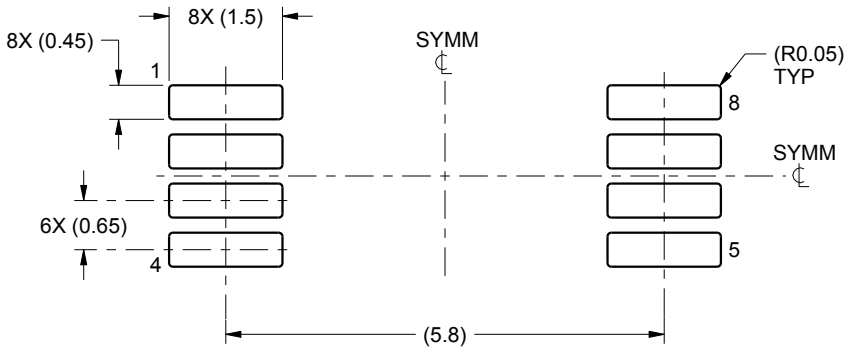
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

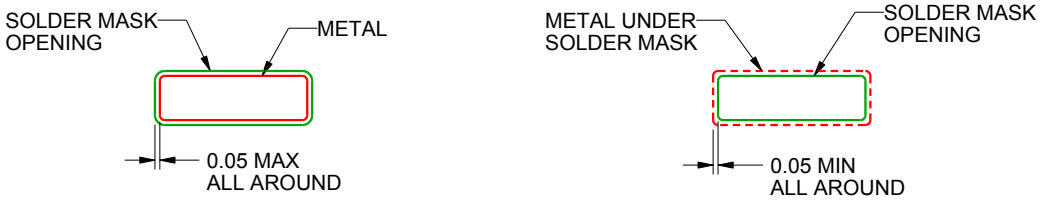



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

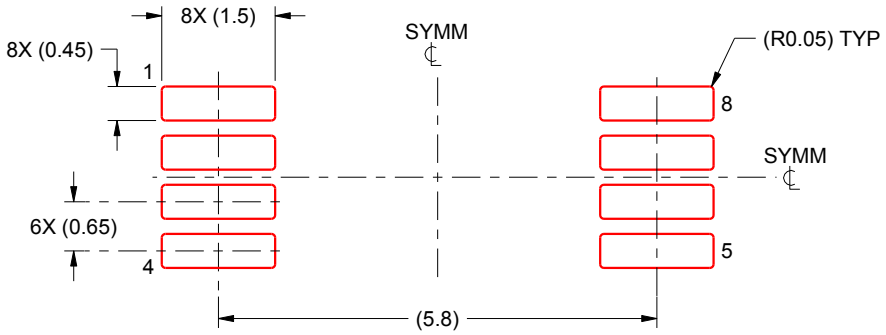



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265