TEXAS INSTRUMENTS
SN65ALS176, SN75ALS176
SN75ALS176A, SN75ALS176B
JAJSPG8I – AUGUST 1987 – REVISED JANUARY 2023

SNx5ALS176、SN75ALS176A、SN75ALS176B 差動バス・トランシーバ

1 特長

- TIA/EIA-422-B、TIA/EIA-485-A の要件以上に適合。[1] また、ITU 勧告 V.11 および X.27 に準じます
- 最大 35Mbaud のデータ・レートで動作
- 4 つのスキュー制限が利用可能：
  - SN65ALS176：15ns
  - SN75ALS176：10ns
  - SN75ALS176A：7.5ns
  - SN75ALS176B：5ns
- ノイズの多い環境での、長いバス・ラインによるマルチポイント伝送向けの設計
- 低消費電流要件：30mA 以下
- 入力 / 出力における正および負の広いバス電圧範囲
- サーマル・シャットダウン保護機能
- ドライバの正 / 負電流制限
- レシーバ入力ヒステリシス
- グリッチ・フリーのパワーアップ / パワーダウン保護機能
- レシーバの開放回路フェイルセーフ設計

2 概要

SN65ALS176 および SN75ALS176 シリーズ差動バス・トランシーバは、マルチポイント・バス伝送線路での双方向データ通信を目的として設計されています。これらのデバイスは平衡伝送線路用に設計されており、TIA/EIA-422-B、TIA/EIA-485-A、ITU 勧告 V.11 および X.27 に適合しています。

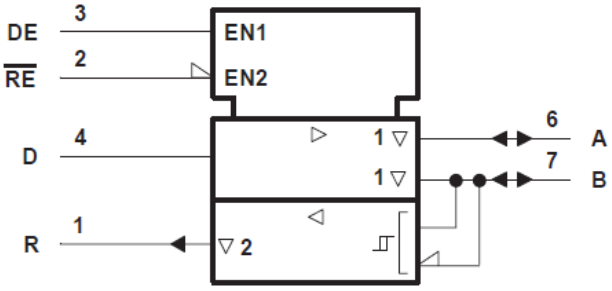
SN65ALS176 および SN75ALS176 は、3 ステートの、差動ライン・ドライバと差動入力ライン・レシーバを統合しており、このどちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力は、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディスエーブルされている場合、または V_{CC} = 0 の場合、バスへの負荷を最小化するように設計されています。このポートは広い正負の同相電圧範囲を持っているため、本デバイスはパーティライン・アプリケーションに適しています。

SN65ALS176 は -40℃ ~ 85℃で、SN75ALS176 は 0℃ ~ 70℃での動作が規定されています。

パッケージ情報

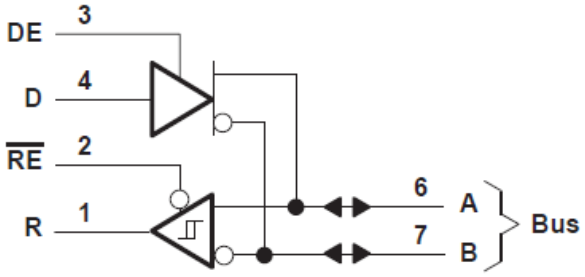
部品番号	パッケージ(1)	本体サイズ (公称)
SNx5ALS176	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm
SN75ALS176A	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm
SN75ALS176B	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



A. この記号は ANSI/IEEE Std 91-1984 と IEC Publication 617-12 に準拠しています。

論理記号



論理図 (正論理)

[1] これらのデバイスの特性は、TIA/EIA-485-A の要件を満たすかそれを上回りますが、ジェネレータ競合テスト (para.3.4.2)、およびジェネレータ電流制限 (para 3.4.3) の場合は、これはあてはまりりません。適用されるテスト電圧範囲は、SN75ALS176、SN75ALS176A、SN75ALS176B では -6V ~ 8V、SN65ALS180 では -4V ~ 8V です。

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3 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (June 2000) to Revision I (January 2023)	Page
• ドキュメントをテキサス・インスツルメンツの最新フォーマットに変更	1
• Deleted the Package thermal impedance from the *Absolute Maximum Ratings*	4
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics* graphs	9

4 Pin Configuration and Functions

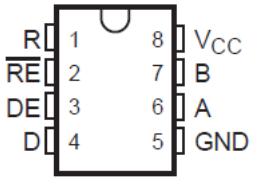


図 4-1. D or P Package (Top View)

表 4-1. Pin Functions

NO	Name	Type	Description
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	i	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Local device ground
6	A	I/O	Driver output or receiver input (complementary to B)
7	B	I/O	Driver output or receiver input (complementary to A)
8	V_{CC}	SUPPLY	4.75-V to 5.25-V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-7	12	V
V_I	Enable input voltage		5.5	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 推奨動作条件

(特に記述のない限り)

			最小値	公称値	最大値	単位
V_{CC}	電源電圧		4.75	5	5.25	V
V_I または V_{IC}	任意のバス端子での入力電圧 (個別または同相モード)				12	V
					-7	
V_{IH}	High レベル入力電圧	D、DE、および $\overline{RE}$	2			V
V_{IL}	Low レベル入力電圧	D、DE、および $\overline{RE}$			0.8	V
V_{ID}	差動入力電圧(1)				±12	V
I_{OH}	High レベル出力電流	ドライバ			-60	mA
		レシーバ			-400	µA
I_{OL}	Low レベル出力電流	ドライバ			60	mA
		レシーバ			8	
T_A	自由気流での動作温度	SN65ALS176	-40		85	℃
		SN75ALS176 シリーズ	0		70	

(1) 差動入出力バス電圧は、反転端子 B を基準とした非反転端子 A の値として測定しています。

5.3 Thermal Information

THERMAL METRIC(1)		P (PDIP) 8-Pins	D (SOIC) SN65 Devices 8-Pins	D (SOIC) SN75 Devices 8-Pin	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.7	116.7	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	54.7	56.3	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	63.4	53.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23	8.8	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.7	62.6	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω	See 図 6-1	½ V_{OD1} or 2[3]			V
		R_L = 54 Ω	See 図 6-1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See 図 6-2	1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage[4]	R_L = 54 Ω or 100 Ω	See 図 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω	See 図 6-1			3 –1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage[4]	R_L = 54 Ω or 100 Ω	See 図 6-1			±0.2	V
I_O	Output current	Outputs disabled[6]	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I= 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current[5]	V_O = –4 V	SN65ALS176			–250	mA
		V_O = –6 V	SN75ALS176			–250	
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω loadis either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of VOD and VOC, respectively, that occur when the input is changed from one logic state to the other.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3			15	ns
$t_{sk(p)}$	Pulse skew[2]	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3		0	2	ns
$t_{sk(lim)}$	Pulse skew[3]	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3			15	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3		8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω	C_L = 50 pF,	See 図 6-4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω	C_L = 50 pF,	See 図 6-5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω	C_L = 50 pF,	See 図 6-4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω	C_L = 50 pF,	See 図 6-5			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.6 Switching Characteristics - Driver

SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	'ALS176	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3	3	8	13	ns
		'ALS176A				4	7	11.5	
		'ALS176B				5	8	10	
$t_{sk(p)}$	Pulse skew(2)		R_L = 54 Ω	C_L = 50 pF,	See 図 6-3		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	'ALS176	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3			10	ns
		'ALS176A						7.5	
		'ALS176B						5	
$t_{t(OD)}$	Differential output transition time		R_L = 54 Ω	C_L = 50 pF,	See 図 6-3		8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω	C_L = 50 pF,	See 図 6-4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω	C_L = 50 pF,	See 図 6-5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω	C_L = 50 pF,	See 図 6-4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω	C_L = 50 pF,	See 図 6-5		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.7 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t(R_L = 100 Ω)	V_t(R_L = 54 W)
$\|V_{OD3}\|$	None	V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	None
I_O	$\|Ix_a\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

5.8 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA			0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+}– $V_{IT–}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See 図 6-6	I_{OH} = –400 mA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, SeeFigure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
V_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	–15		–85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.9 Switching Characteristics - Receiver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = –1.5 V to 1.5 V, See 図 6-7	C_L = 15 pF,			25	ns
$t_{sk(p)}$	Pulse skew(2)	V_{ID} = –1.5 V to 1.5 V, See 図 6-7	C_L = 15 pF,		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	R_L = 54 Ω See 図 6-3	C_L = 50 pF,			15	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See 図 6-8		11	18	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See 図 6-8		11	18	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See 図 6-8			50	ns
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See 図 6-8			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH}– t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.10 Switching Characteristics - Receiver

SN75ALS176,SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = –1.5 V to 1.5 V, See 図 6-7	C_L = 15 pF,	9	14	19	ns
		'ALS176A			10.5	14	18	
		'ALS176B			11.5	13	16.5	
$t_{sk(p)}$	Pulse skew(2)		V_{ID} = –1.5 V to 1.5 V, See 図 6-7	C_L = 15 pF,		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	'ALS176	R_L = 54 Ω See 図 6-3	C_L = 50 pF,			10	ns
		'ALS176A					7.5	
		'ALS176B					5	
t_{PZH}	Output enable time to high level		C_L = 15 pF,	See 図 6-8		7	14	ns
t_{PZL}	Output enable time to low level		C_L = 15 pF,	See 図 6-8		20	35	ns
t_{PHZ}	Output disable time from high level		C_L = 15 pF,	See 図 6-8		20	35	ns
t_{PLZ}	Output disable time from low level		C_L = 15 pF,	See 図 6-8		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.11 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

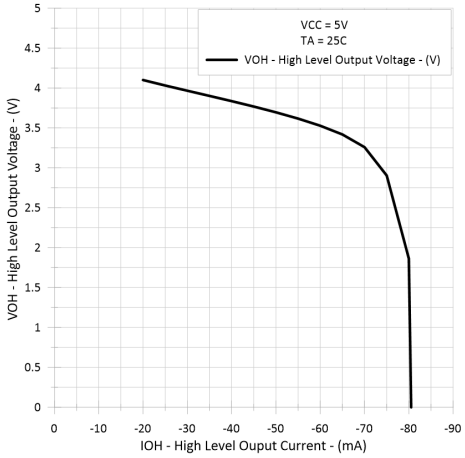


図 5-1. Driver High-LeveL Output Voltage vs High-Level Output Current

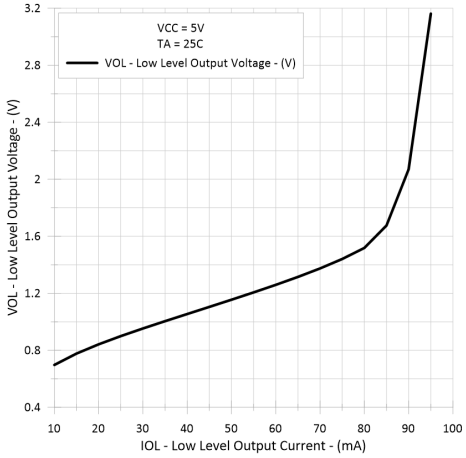


図 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

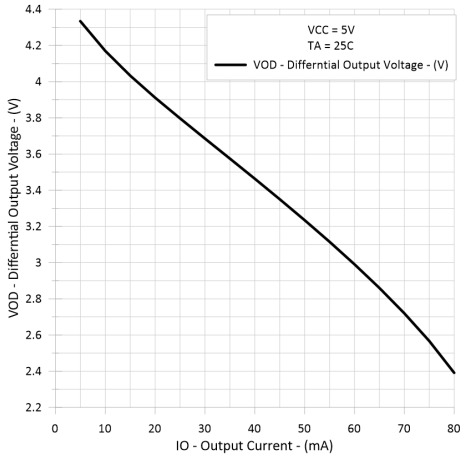


図 5-3. Driver Differential Output Voltage vs Output Current

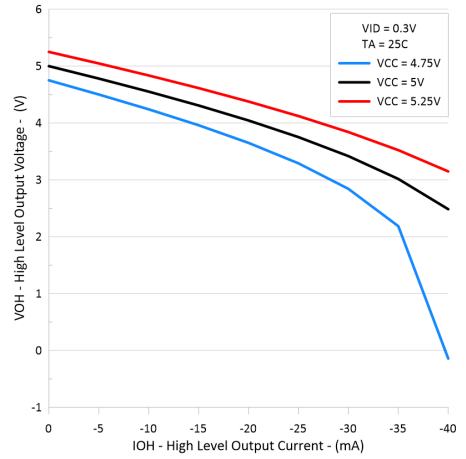


図 5-4. Receiver High-Level Output Voltage vs High-Level Output Current

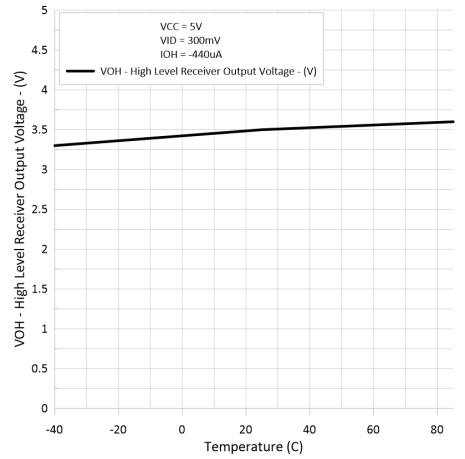


図 5-5. Receiver High-Level Output Voltage vs Free-Air Temperature

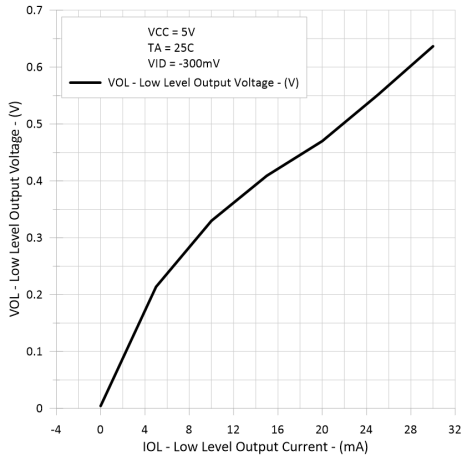


図 5-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

5.11 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

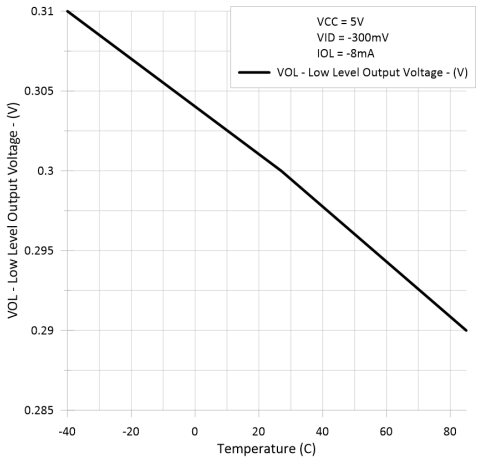


図 5-7. Receiver Low-Level Output Voltage vs Free-Air Temperature

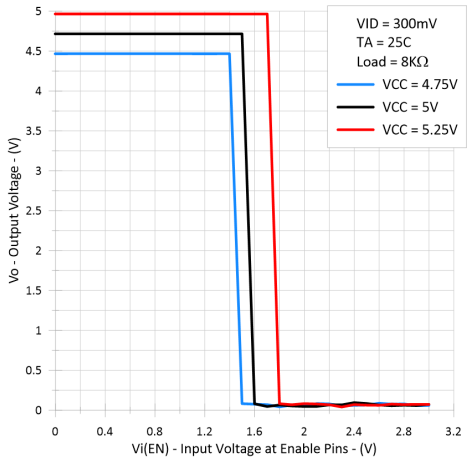


図 5-8. Receiver Output Voltage vs Enable Voltage

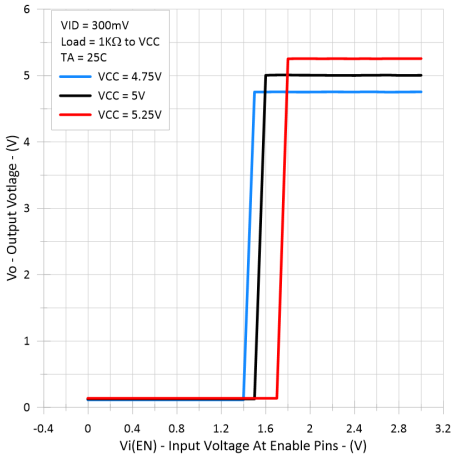


図 5-9. Receiver Output Voltage vs Enable Voltage

6 Parameter Measurement Information

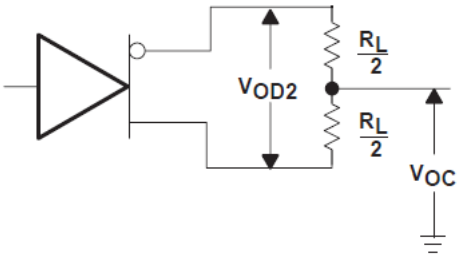


図 6-1. Driver V_{OD2} and V_{OC}

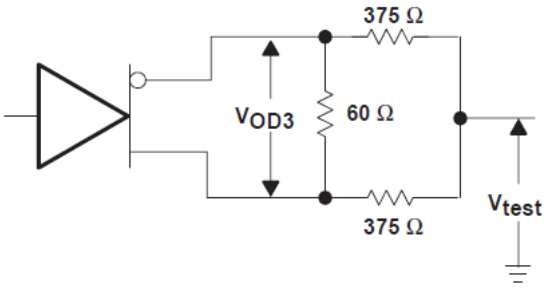
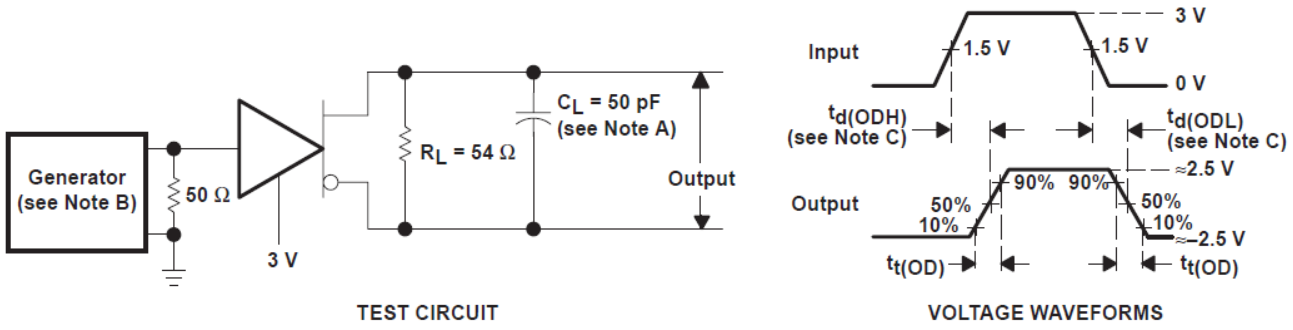


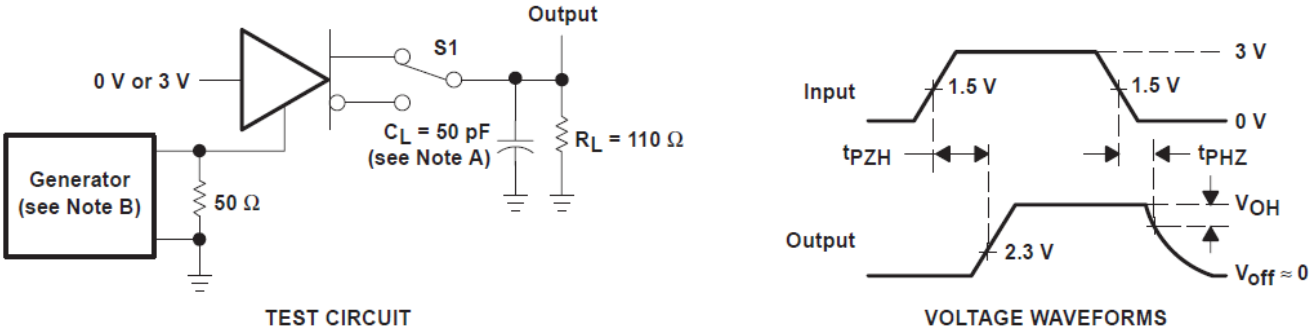
図 6-2. Driver V_{OD3}



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

図 6-3. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

図 6-4. Driver Test Circuit and Voltage Waveforms

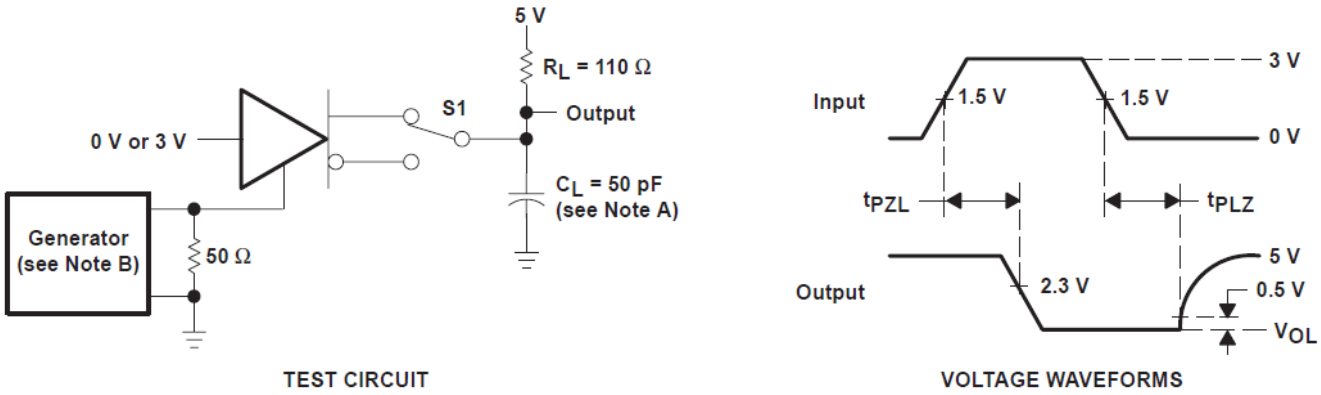


図 6-5. Driver Test Circuit and Voltage Waveforms

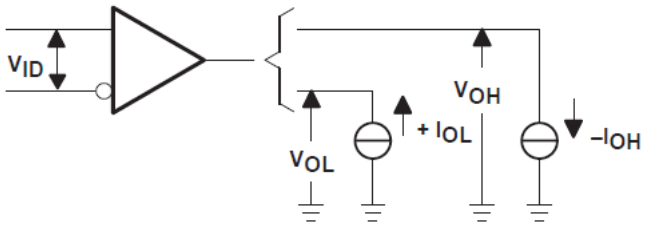
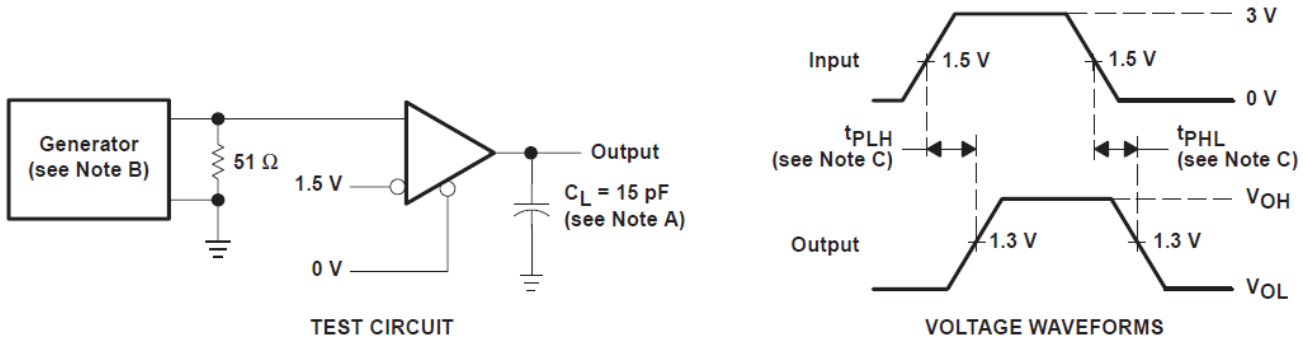


図 6-6. Receiver V_{OH} and V_{OL} Test Circuit

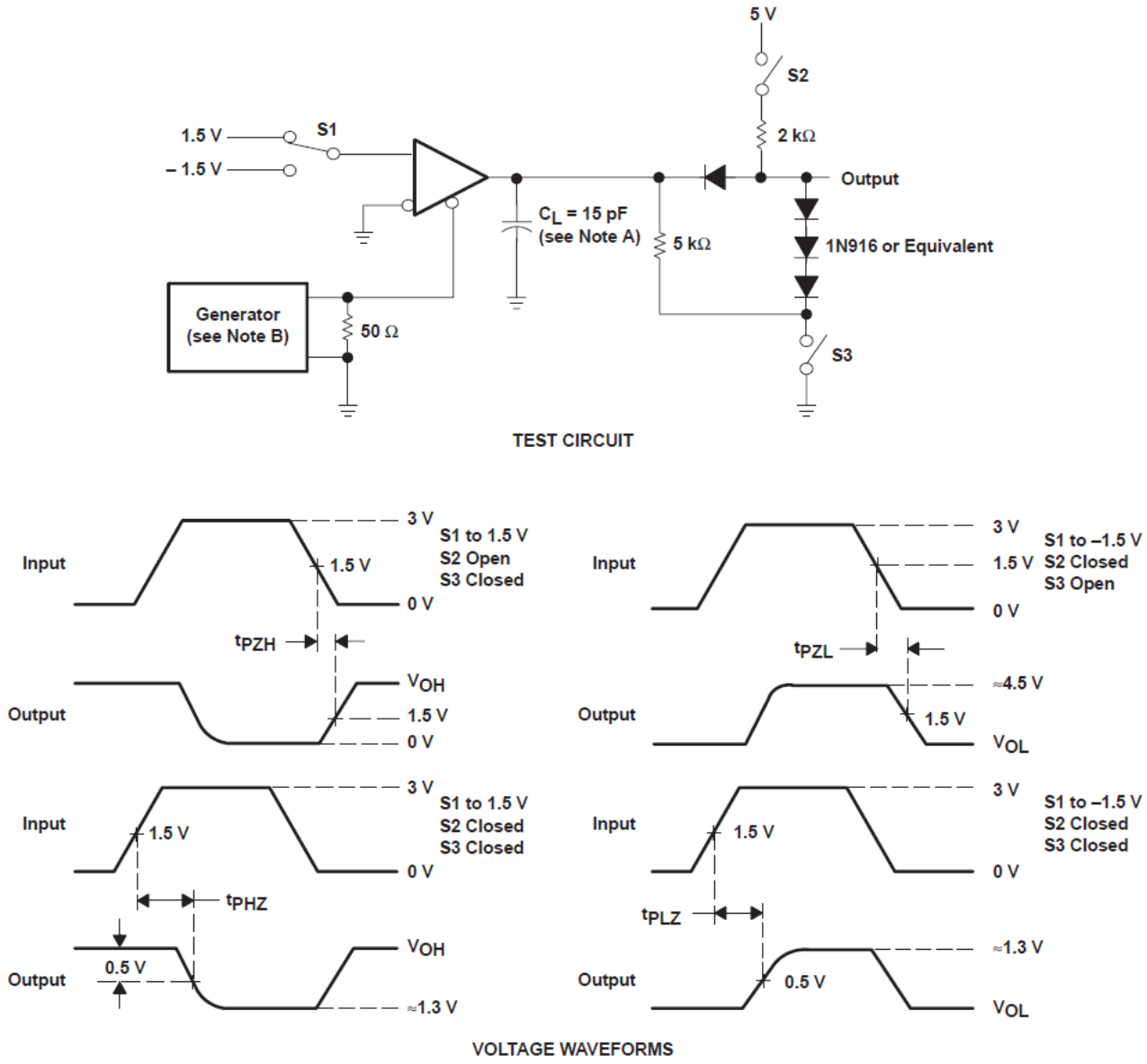


A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

C. $t_{pd} = t_{PLH}$ or t_{PHL}.

図 6-7. Receiver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

図 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

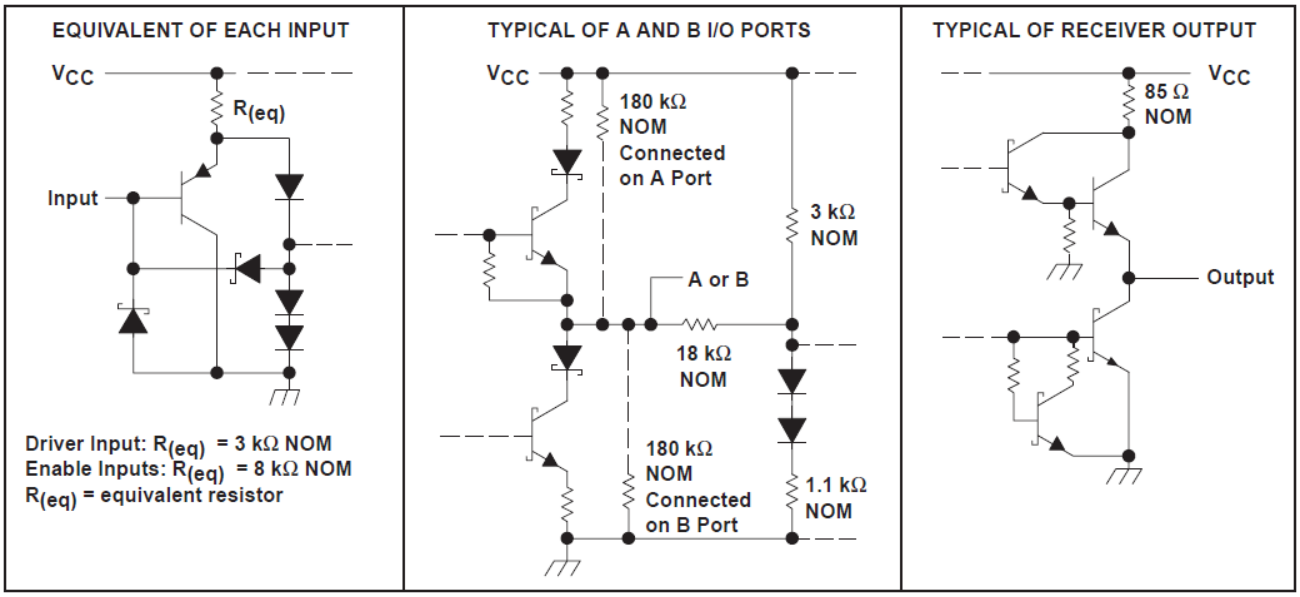


図 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Receiver(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

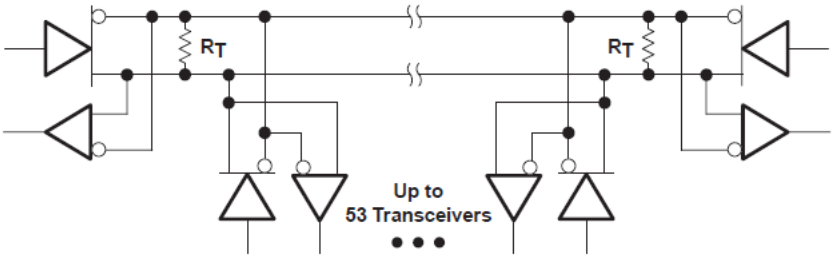
8 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.2 Typical Application



A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

図 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65ALS176D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	65A176
SN65ALS176DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65A176
SN65ALS176DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65A176
SN65ALS176DR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65A176
SN65ALS176DR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65A176
SN75ALS176AD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A
SN75ALS176AD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A
SN75ALS176ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A
SN75ALS176ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A
SN75ALS176ADRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A
SN75ALS176AP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75ALS176A
SN75ALS176AP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75ALS176A
SN75ALS176BD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	7A176B
SN75ALS176BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(75A176, 7A176B)
SN75ALS176BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(75A176, 7A176B)
SN75ALS176BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75ALS176B
SN75ALS176BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75ALS176B
SN75ALS176D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	75A176
SN75ALS176P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75ALS176
SN75ALS176P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75ALS176
SN75ALS176PE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75ALS176

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

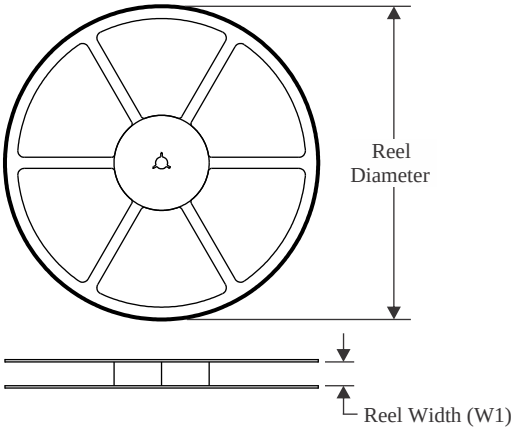
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

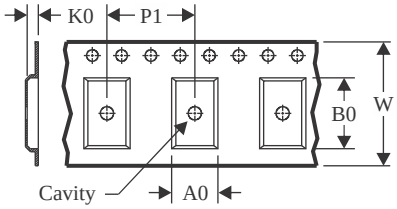
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

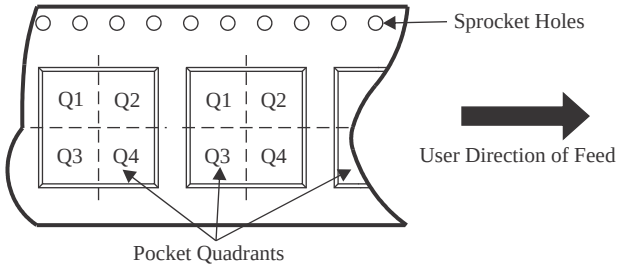


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

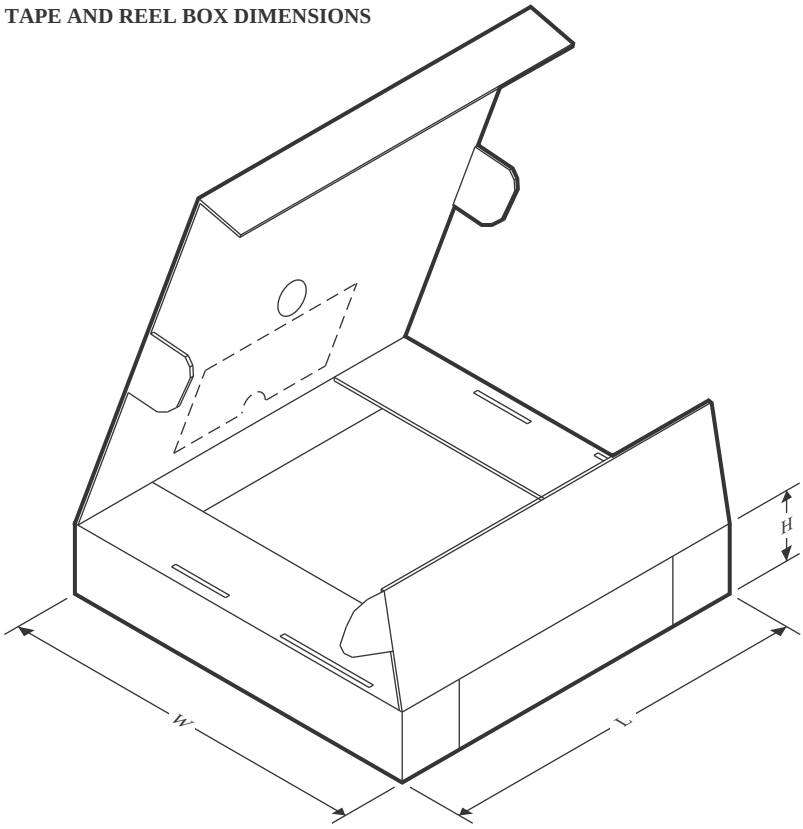
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65ALS176DR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

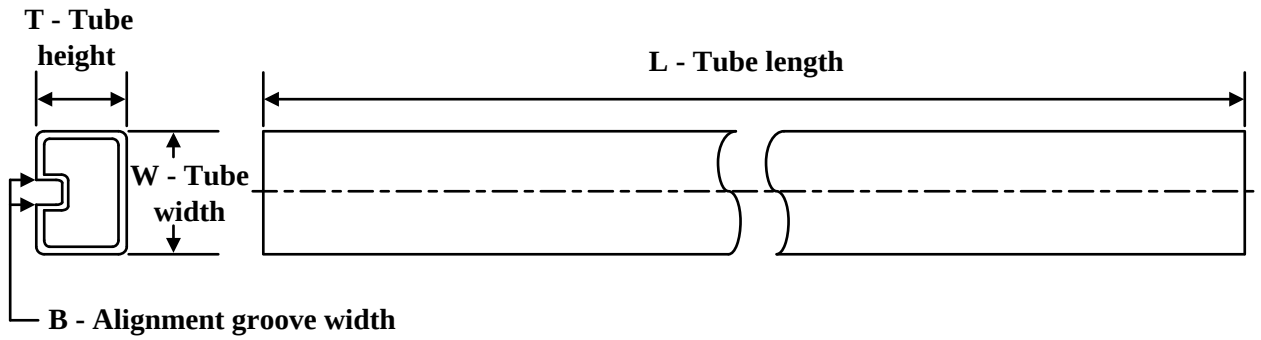
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

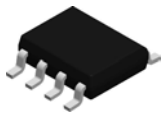
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS176DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65ALS176DR1G4	SOIC	D	8	2500	353.0	353.0	32.0
SN75ALS176ADR	SOIC	D	8	2500	353.0	353.0	32.0
SN75ALS176BDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS176AD	D	SOIC	8	75	507	8	3940	4.32
SN75ALS176AD.A	D	SOIC	8	75	507	8	3940	4.32
SN75ALS176AP	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176AP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176P	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176PE4	P	PDIP	8	50	506	13.97	11230	4.32

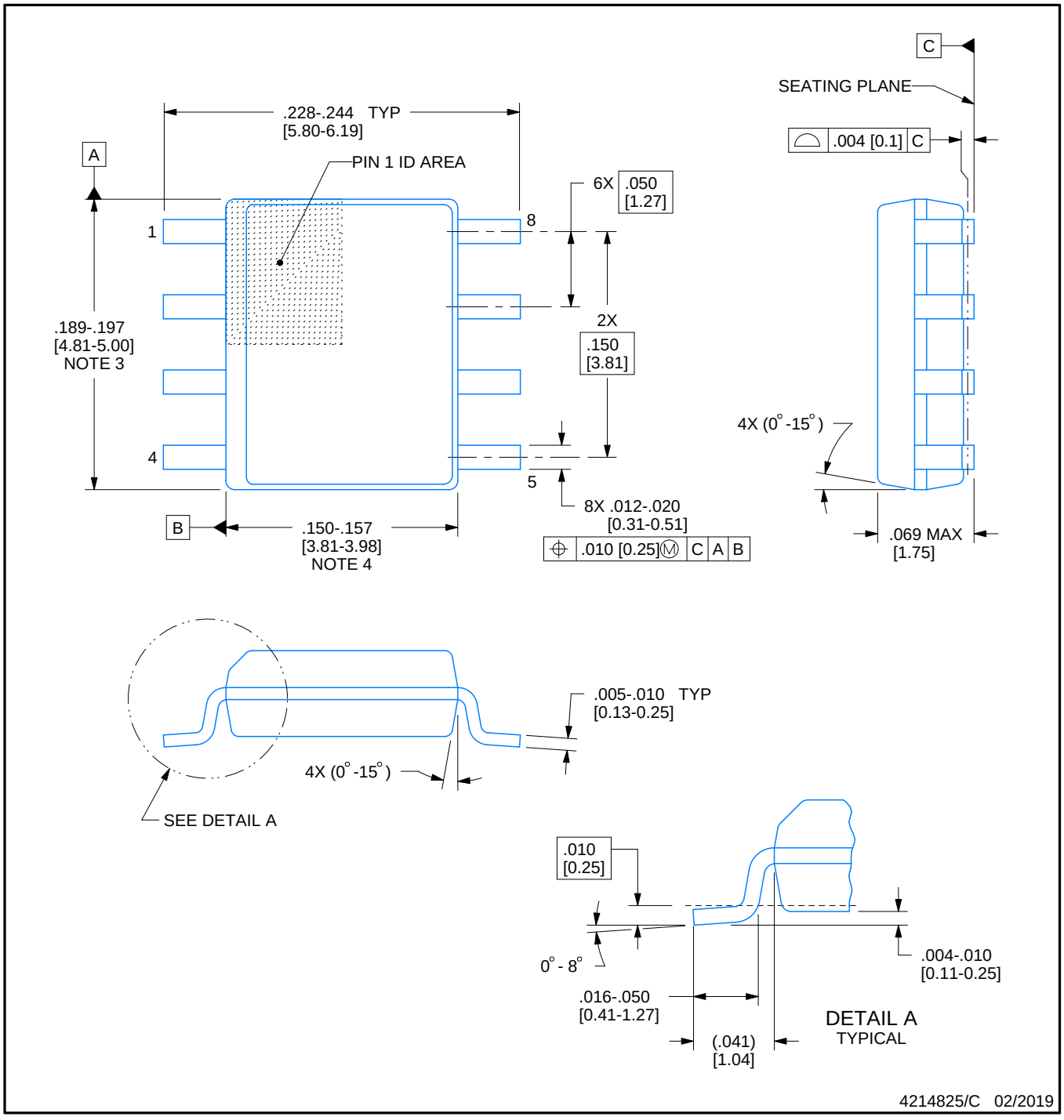


PACKAGE OUTLINE

D0008A

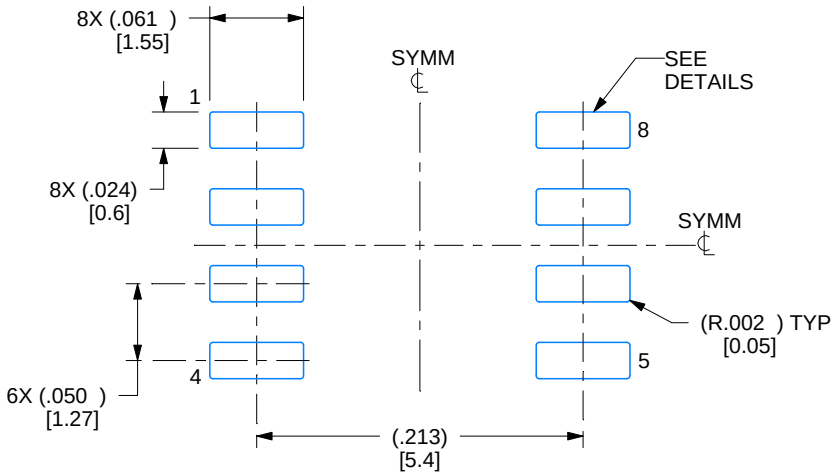
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

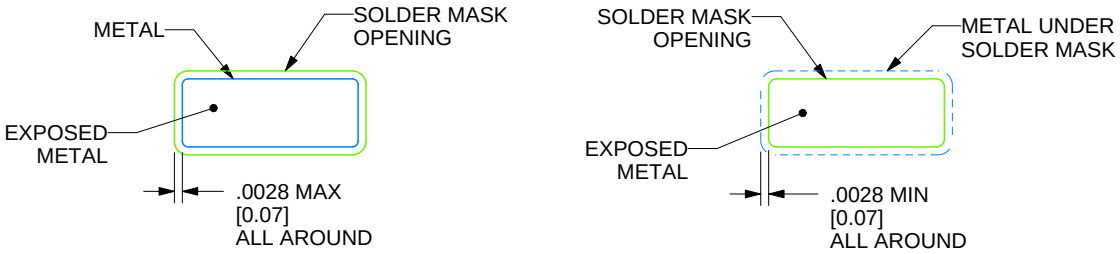


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

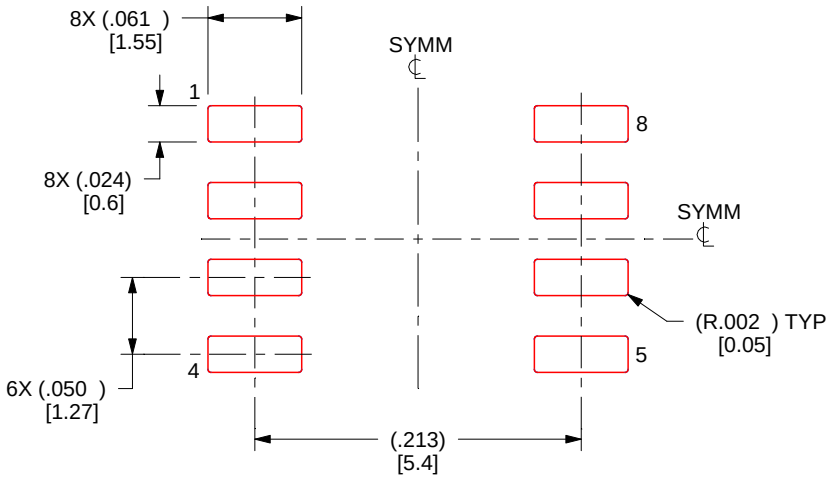
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



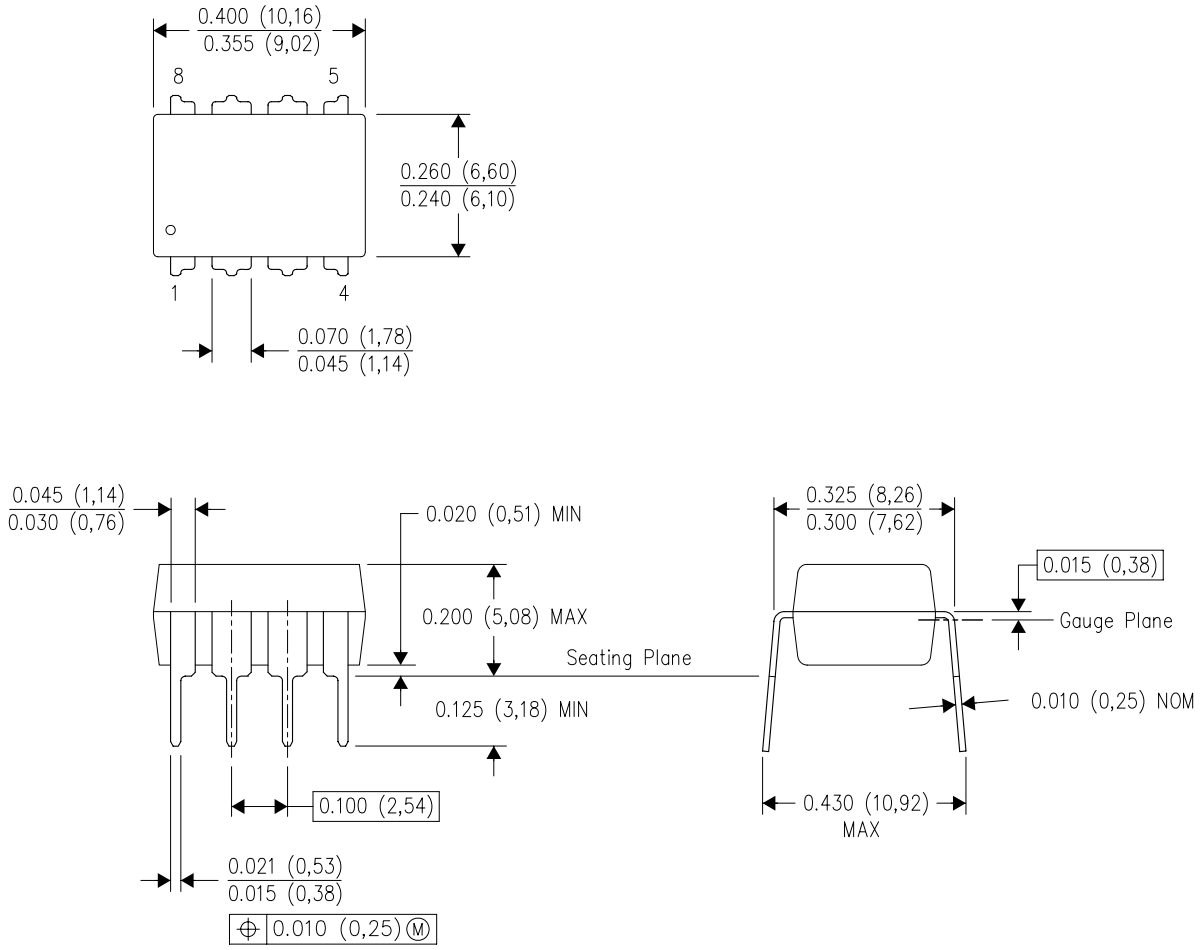
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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