

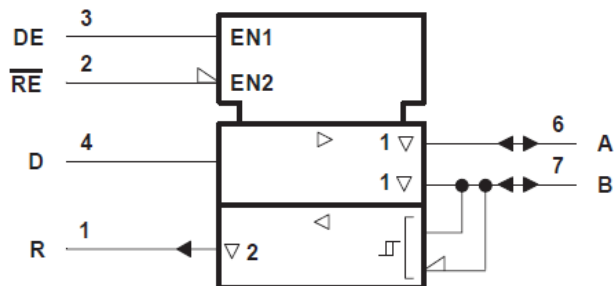
SNx5ALS176、SN75ALS176A、SN75ALS176B 差動バス・トランシーバ

1 特長

- TIA/EIA-422-B、TIA/EIA-485-A の要件以上に適合。¹ また、ITU 勧告 V.11 および X.27 に準じます
- 最大 35Mbaud のデータ・レートで動作
- 4 つのスキュー制限が利用可能：
 - SN65ALS176 : 15ns
 - SN75ALS176 : 10ns
 - SN75ALS176A : 7.5ns
 - SN75ALS176B : 5ns
- ノイズの多い環境での、長いバス・ラインによるマルチポイント伝送向けの設計
- 低消費電流要件 : 30mA 以下
- 入力 / 出力における正および負の広いバス電圧範囲
- サーマル・シャットダウン保護機能
- ドライバの正 / 負電流制限
- レシーバ入力ヒステリシス
- グリッチ・フリーのパワーアップ / パワーダウン保護機能
- レシーバの開放回路フェイルセーフ設計

2 概要

SN65ALS176 および SN75ALS176 シリーズ差動バス・トランシーバは、マルチポイント・バス伝送線路での双方向データ通信を目的として設計されています。これらのデバイスは平衡伝送線路用に設計されており、TIA/EIA-422-B、TIA/EIA-485-A、ITU 勧告 V.11 および X.27 に適合しています。



A. この記号は ANSI/IEEE Std 91-1984 と IEC Publication 617-12 に準拠しています。

論理記号

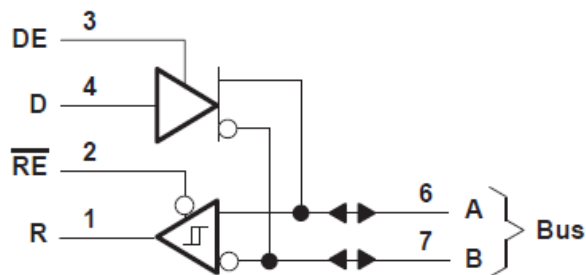
SN65ALS176 および SN75ALS176 は、3 ステートの、差動ライン・ドライバと差動入力ライン・レシーバを統合しており、このどちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディスエーブルされている場合、または $V_{CC} = 0$ の場合、バスへの負荷を最小化するように設計されています。このポートは広い正負の同相電圧範囲を持っているため、本デバイスはパーティライン・アプリケーションに適しています。

SN65ALS176 は $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ で、SN75ALS176 は $0^{\circ}\text{C} \sim 70^{\circ}\text{C}$ での動作が規定されています。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
SNx5ALS176	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm
SN75ALS176A	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm
SN75ALS176B	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

¹ これらのデバイスの特性は、TIA/EIA-485-A の要件を満たすがそれを上回りますが、ジェネレータ競合テスト (para.3.4.2)、およびジェネレータ電流制限 (para 3.4.3) の場合は、これはあてはまりません。適用されるテスト電圧範囲は、SN75ALS176、SN75ALS176A、SN75ALS176B では $-6\text{V} \sim 8\text{V}$ 、SN65ALS180 では $-4\text{V} \sim 8\text{V}$ です。



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3 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (June 2000) to Revision I (January 2023)	Page
• ドキュメントをテキサス・インスツルメンツの最新フォーマットに変更.....	1
• Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i>	4
• Added the <i>Thermal Information</i> table.....	4
• Changed the <i>Typical Characteristics</i> graphs.....	9

4 Pin Configuration and Functions

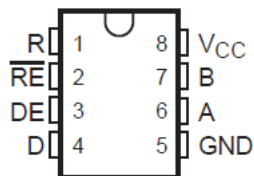


图 4-1. D or P Package (Top View)

表 4-1. Pin Functions

NO	Name	Type	Description
1	R	O	Receive data output
2	RE	I	Receiver enable, active low
3	DE	i	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Local device ground
6	A	I/O	Driver output or receiver input (complementary to B)
7	B	I/O	Driver output or receiver input (complementary to A)
8	V _{CC}	SUPPLY	4.75-V to 5.25-V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		7	V
	Voltage range at any bus terminal	-7	12	V
V _I	Enable input voltage		5.5	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 推奨動作条件

(特に記述のない限り)

			最小値	公称値	最大値	単位
V _{CC}	電源電圧		4.75	5	5.25	V
V _I または V _{IC}	任意のバス端子での入力電圧 (個別または同相モード)				12 -7	V
V _{IH}	High レベル入力電圧	D、DE、および RE	2			V
V _{IL}	Low レベル入力電圧	D、DE、および RE			0.8	V
V _{ID}	差動入力電圧 ⁽¹⁾				±12	V
I _{OH}	High レベル出力電流	ドライバ			-60	mA
		レシーバ			-400	μA
I _{OL}	Low レベル出力電流	ドライバ			60	mA
		レシーバ			8	
T _A	自由気流での動作温度	SN65ALS176	-40		85	°C
		SN75ALS176 シリーズ	0		70	

- (1) 差動入出力バス電圧は、反転端子 B を基準とした非反転端子 A の値として測定しています。

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		P (PDIP)	D (SOIC) SN65 Devices	D (SOIC) SN75 Devices	UNIT
		8-Pins	8-Pins	8-Pin	
R _{θJA}	Junction-to-ambient thermal resistance	65.7	116.7	110	°C/W
R _{θJC(top)}	Junction-to-case thermal resistance	54.7	56.3	44.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	42.1	63.4	53.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	23	8.8	4.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	41.7	62.6	52.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = –18 mA				–1.5	V
V _O	Output voltage	I _O = 0		0		6	V
V _{OD1}	Differential output voltage	I _O = 0		1.5		6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω	See Figure 6-1	½ V _{OD1} or 2 ⁽³⁾			V
		R _L = 54 Ω	See Figure 6-1	1.5	2.5	5	V
V _{OD3}	Differential output voltage	V _{test} = –7 V to 12 V,	See Figure 6-2	1.5		5	V
Δ V _{OD}	Change in magnitude of differential output voltage ⁽⁴⁾	R _L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V
V _{OC}	Common-mode output voltage	R _L = 54 Ω or 100 Ω	See Figure 6-1			3 –1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage ⁽⁴⁾	R _L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V
I _O	Output current	Outputs disabled ⁽⁶⁾	V _O = 12 V			1	mA
			V _O = –7 V			–0.8	
I _{IH}	High-level input current	V _I = 2.4 V				20	μA
I _{IL}	Low-level input current	V _I = 0.4 V				–400	μA
I _{OS}	Short-circuit output current ⁽⁵⁾	V _O = –4 V	SN65ALS176			–250	mA
		V _O = –6 V	SN75ALS176			–250	
		V _O = 0				–150	
		V _O = V _{CC}				250	
		V _O = 8 V				250	
I _{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

- (1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of VOD and VOC, respectively, that occur when the input is changed from one logic state to the other.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
t _{d(OD)}	Differential output delay time	R _L = 54 Ω	C _L = 50 pF,	See Figure 6-3			15	ns
t _{sk(p)}	Pulse skew ⁽²⁾	R _L = 54 Ω	C _L = 50 pF,	See Figure 6-3		0	2	ns
t _{sk(lim)}	Pulse skew ⁽³⁾	R _L = 54 Ω	C _L = 50 pF,	See Figure 6-3			15	ns
t _{t(OD)}	Differential output transition time	R _L = 54 Ω	C _L = 50 pF,	See Figure 6-3		8		ns
t _{PZH}	Output enable time to high level	R _L = 110 Ω	C _L = 50 pF,	See Figure 6-4			80	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω	C _L = 50 pF,	See Figure 6-5			30	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω	C _L = 50 pF,	See Figure 6-4			50	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω	C _L = 50 pF,	See Figure 6-5			30	ns

- (1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

- (2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.6 Switching Characteristics - Driver

SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	'ALS176	$R_L = 54 \Omega$	$C_L = 50 \text{ pF}$	See 6-3	3	8	13	ns
		'ALS176A				4	7	11.5	
		'ALS176B				5	8	10	
$t_{sk(p)}$	Pulse skew ⁽²⁾		$R_L = 54 \Omega$	$C_L = 50 \text{ pF}$	See 6-3		0	2	ns
$t_{sk(lim)}$	Pulse skew ⁽³⁾	'ALS176	$R_L = 54 \Omega$	$C_L = 50 \text{ pF}$	See 6-3			10	ns
		'ALS176A						7.5	
		'ALS176B						5	
$t_{i(OD)}$	Differential output transition time		$R_L = 54 \Omega$	$C_L = 50 \text{ pF}$	See 6-3		8		ns
t_{PZH}	Output enable time to high level		$R_L = 110 \Omega$	$C_L = 50 \text{ pF}$	See 6-4		23	50	ns
t_{PZL}	Output enable time to low level		$R_L = 110 \Omega$	$C_L = 50 \text{ pF}$	See 6-5		14	20	ns
t_{PHZ}	Output disable time from high level		$R_L = 110 \Omega$	$C_L = 50 \text{ pF}$	See 6-4		20	35	ns
t_{PLZ}	Output disable time from low level		$R_L = 110 \Omega$	$C_L = 50 \text{ pF}$	See 6-5		8	17	ns

- (1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.7 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$ V_{OD1} $	V_o	V_o
$ V_{OD2} $	$V_t(R_L = 100 \Omega)$	$V_t(R_L = 54 \Omega)$
$ V_{OD3} $	None	V_t (test termination measurement 2)
$\Delta V_{OD} $	$ V_t - V_t $	$ V_t - V_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - V_{os} $	$ V_{os} - V_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	None
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

5.8 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V,	I _O = –0.4 mA			0.2	V
V _{IT–}	Negative-going input threshold voltage	V _O = 0.5 V,	I _O = 8 mA	–0.2 ⁽²⁾			V
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT–})				60		mV
V _{IK}	Enable-input clamp voltage	I _I = –18 mA				–1.5	V
V _{OH}	High-level output voltage	V _{ID} = 200 mV, See Figure 6-6	I _{OH} = –400 mA,	2.7			V
V _{OL}	Low-level output voltage	V _{ID} = –200 mV, See Figure 6	I _{OL} = 8 mA,			0.45	V
I _{OZ}	High-impedance-state output current	V _O = 0.4 V to 2.4 V				±20	μA
V _I	Line input current	Other input = 0 V ⁽³⁾	V _I = 12 V			1	mA
			V _I = –7 V			–0.8	
I _{IH}	High-level-enable input current	V _{IH} = 2.7 V				20	μA
I _{IL}	Low-level-enable input current	V _{IL} = 0.4 V				–100	μA
r _I	Input resistance			12	20		kΩ
I _{OS}	Short-circuit output current	V _{ID} = 200 mV,	V _O = 0	–15		–85	mA
I _{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.9 Switching Characteristics - Receiver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t _{pd}	Propagation time	V _{ID} = –1.5 V to 1.5 V, See Figure 6-7	C _L = 15 pF,			25	ns
t _{sk(p)}	Pulse skew ⁽²⁾	V _{ID} = –1.5 V to 1.5 V, See Figure 6-7	C _L = 15 pF,		0	2	ns
t _{sk(lim)}	Pulse skew ⁽³⁾	R _L = 54 Ω See Figure 6-3	C _L = 50 pF,			15	ns
t _{PZH}	Output enable time to high level	C _L = 15 pF,	See Figure 6-8		11	18	ns
t _{PZL}	Output enable time to low level	C _L = 15 pF,	See Figure 6-8		11	18	ns
t _{PHZ}	Output disable time from high level	C _L = 15 pF,	See Figure 6-8			50	ns
t _{PLZ}	Output disable time from low level	C _L = 15 pF,	See Figure 6-8			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) Pulse skew is defined as the |t_{PLH} – t_{PHL}| of each channel of the same device.

(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.10 Switching Characteristics - Receiver

SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd}	Propagation time	'ALS176	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, See 6-7	$C_L = 15\text{ pF}$,	9	14	19	ns
		'ALS176A			10.5	14	18	
		'ALS176B			11.5	13	16.5	
$t_{sk(p)}$	Pulse skew ⁽²⁾		$V_{ID} = -1.5\text{ V to }1.5\text{ V}$, See 6-7	$C_L = 15\text{ pF}$,		0	2	ns
$t_{sk(lim)}$	Pulse skew ⁽³⁾	'ALS176	$R_L = 54\ \Omega$ See 6-3	$C_L = 50\text{ pF}$,			10	ns
		'ALS176A					7.5	
		'ALS176B					5	
t_{PZH}	Output enable time to high level		$C_L = 15\text{ pF}$,	See 6-8		7	14	ns
t_{PZL}	Output enable time to low level		$C_L = 15\text{ pF}$,	See 6-8		20	35	ns
t_{PHZ}	Output disable time from high level		$C_L = 15\text{ pF}$,	See 6-8		20	35	ns
t_{PLZ}	Output disable time from low level		$C_L = 15\text{ pF}$,	See 6-8		8	17	ns

(1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.11 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

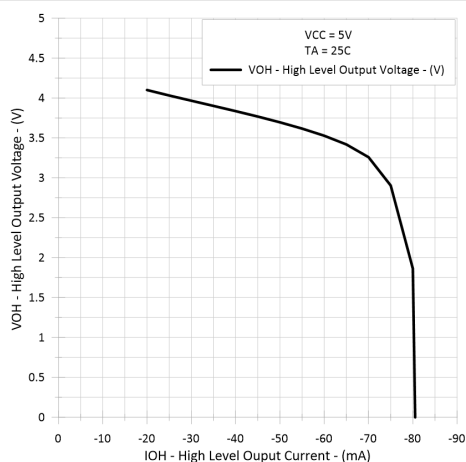


Figure 5-1. Driver High-Level Output Voltage vs High-Level Output Current

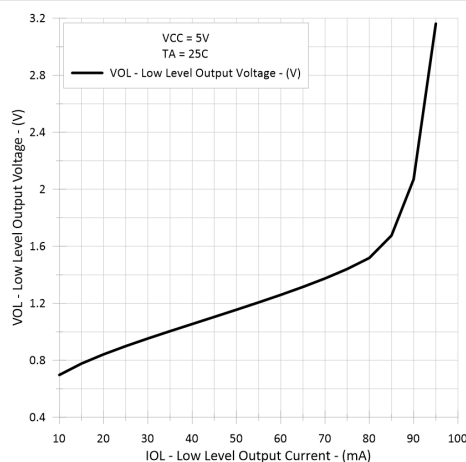


Figure 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

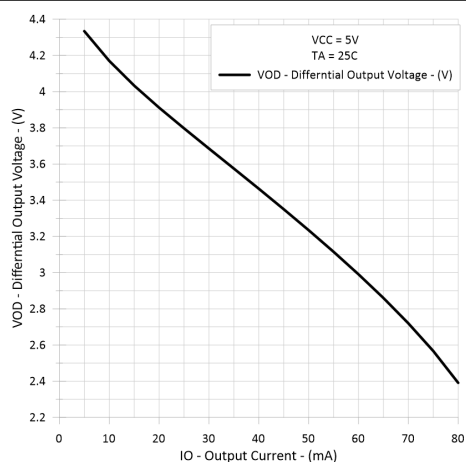


Figure 5-3. Driver Differential Output Voltage vs Output Current

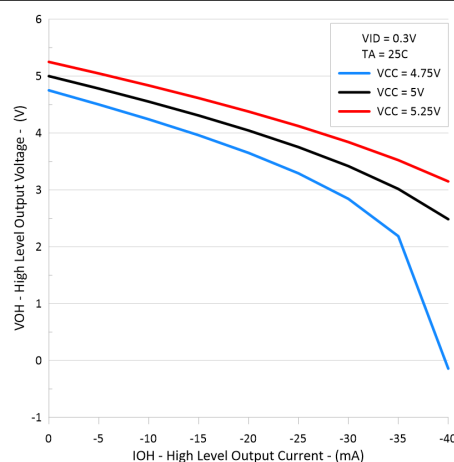


Figure 5-4. Receiver High-Level Output Voltage vs High-Level Output Current

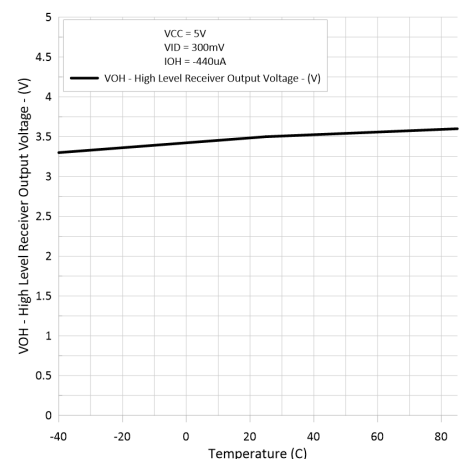


Figure 5-5. Receiver High-Level Output Voltage vs Free-Air Temperature

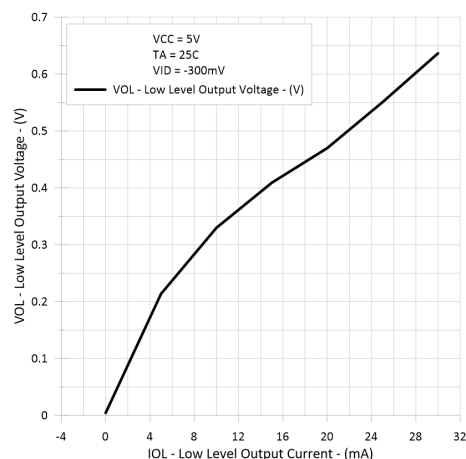
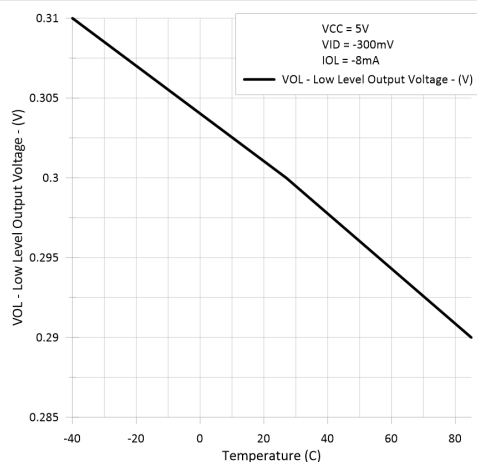


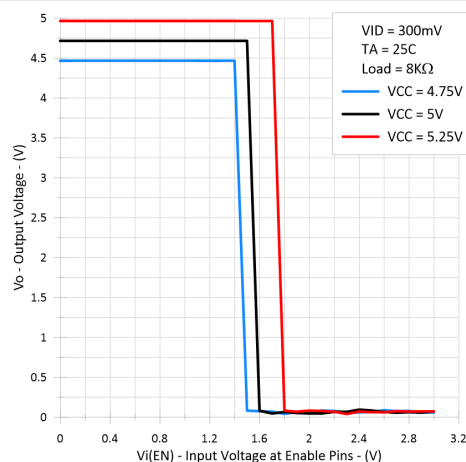
Figure 5-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

5.11 Typical Characteristics (continued)

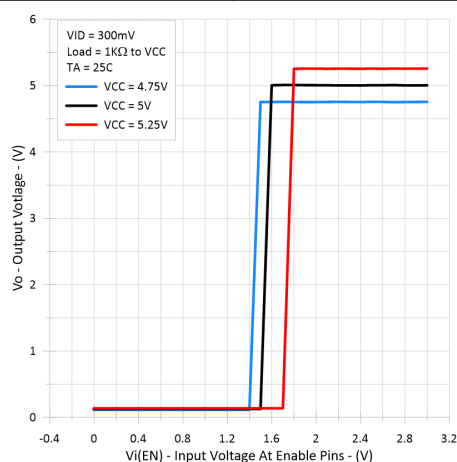
Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.



5-7. Receiver Low-Level Output Voltage vs Free-Air Temperature



5-8. Receiver Output Voltage vs Enable Voltage



5-9. Receiver Output Voltage vs Enable Voltage

6 Parameter Measurement Information

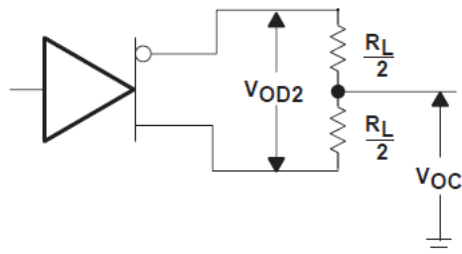


图 6-1. Driver V_{OD2} and V_{OC}

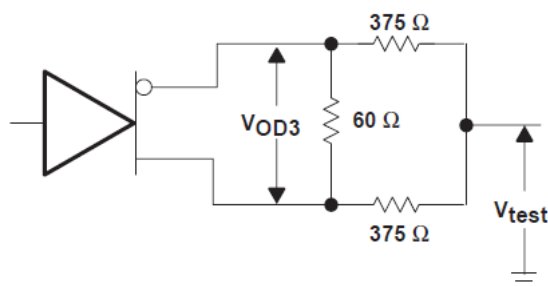
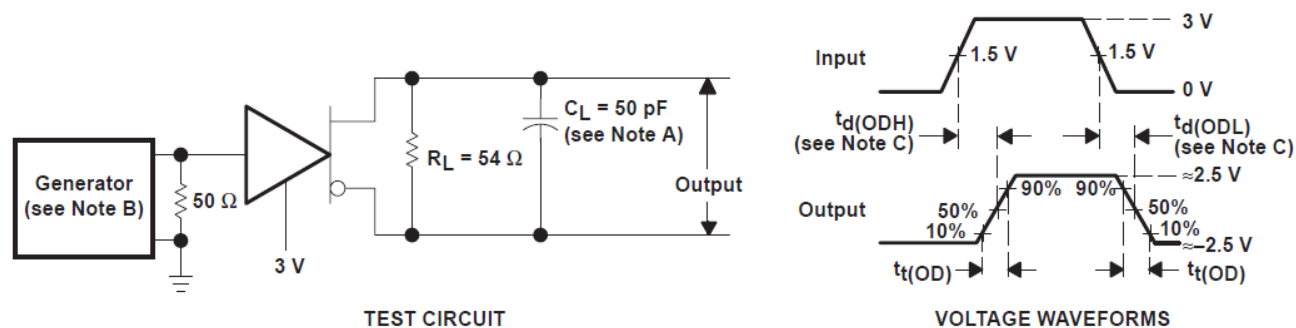
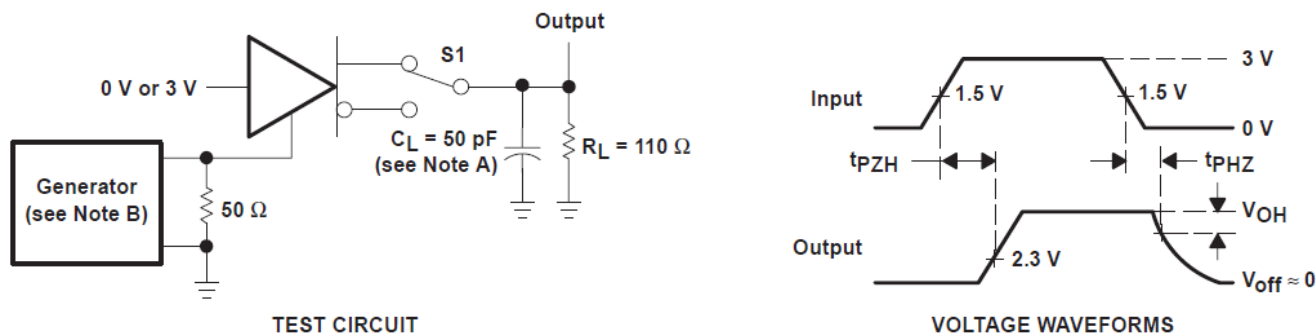


图 6-2. Driver V_{OD3}



- A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

图 6-3. Driver Test Circuit and Voltage Waveforms



- A. C_L includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

图 6-4. Driver Test Circuit and Voltage Waveforms

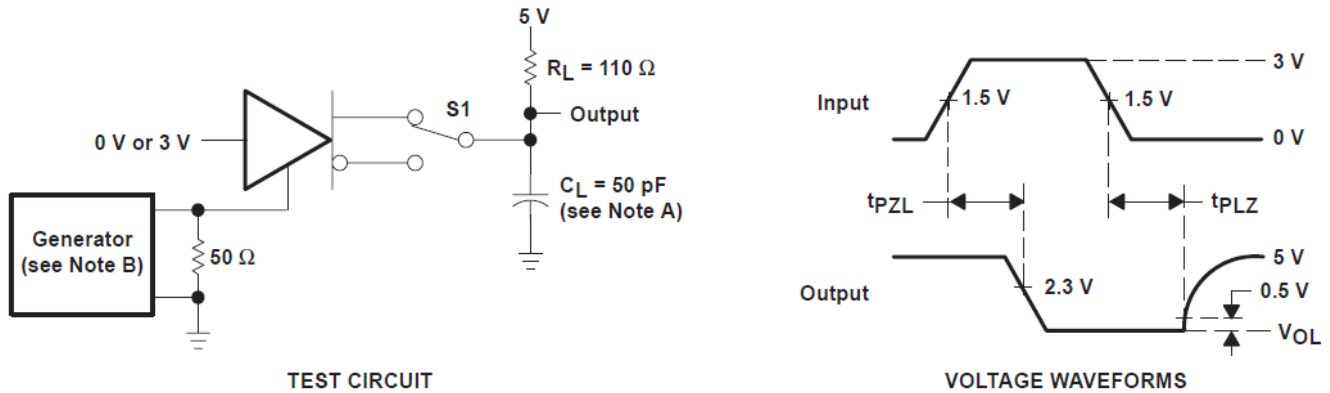


图 6-5. Driver Test Circuit and Voltage Waveforms

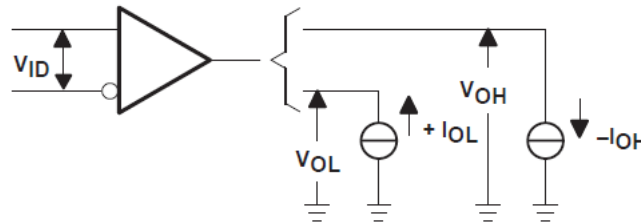
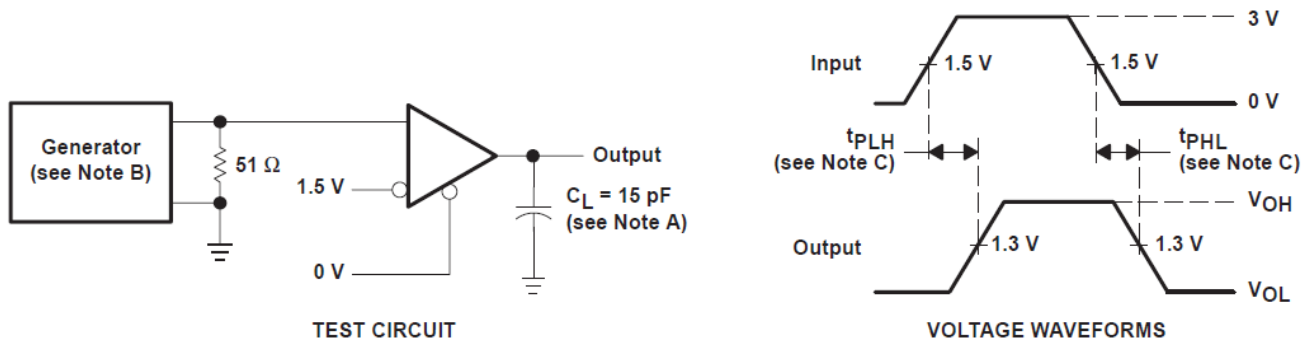
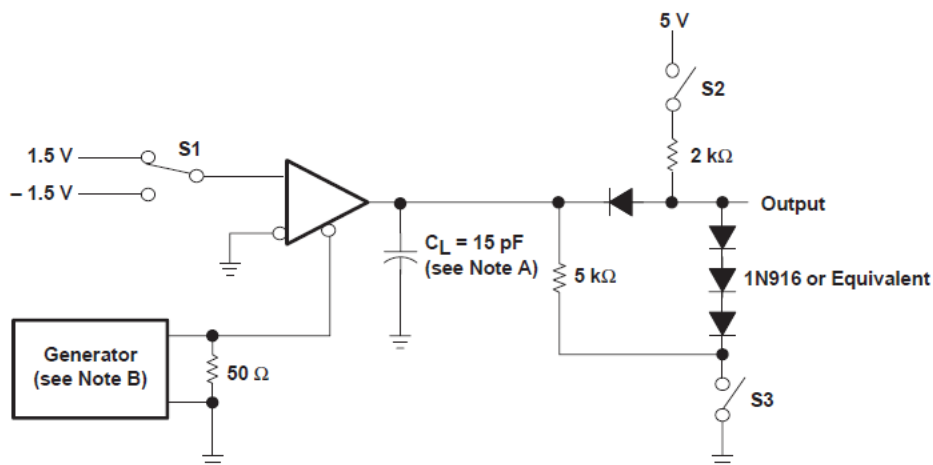


图 6-6. Receiver V_{OH} and V_{OL} Test Circuit

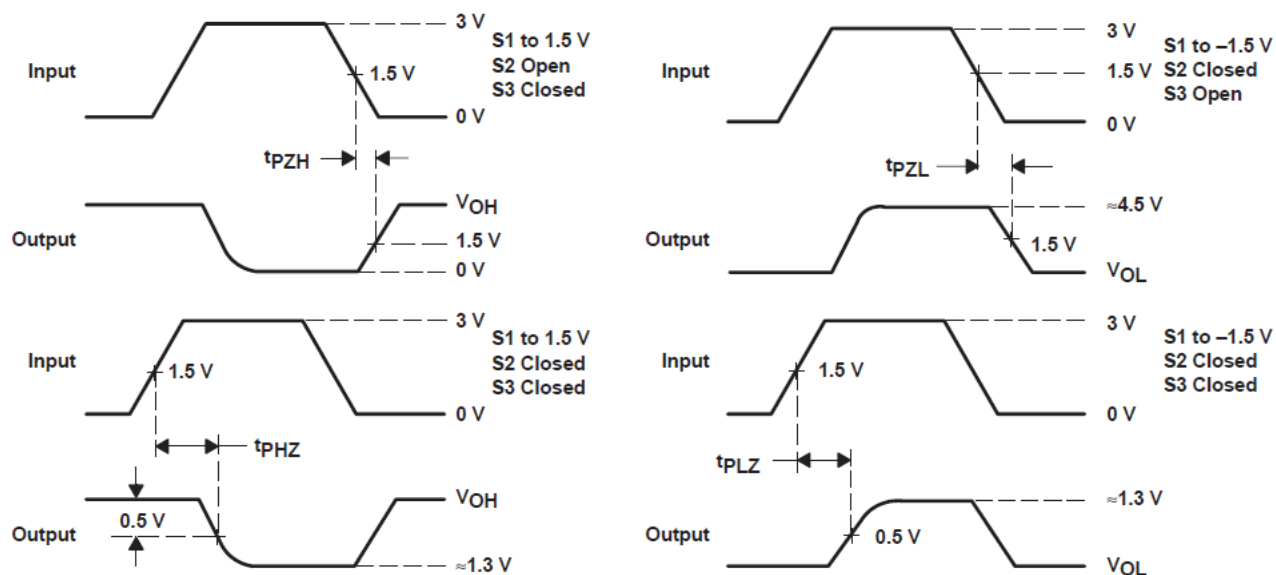


- A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 C. $t_{pd} = t_{PLH}$ or t_{PHL} .

图 6-7. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

图 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

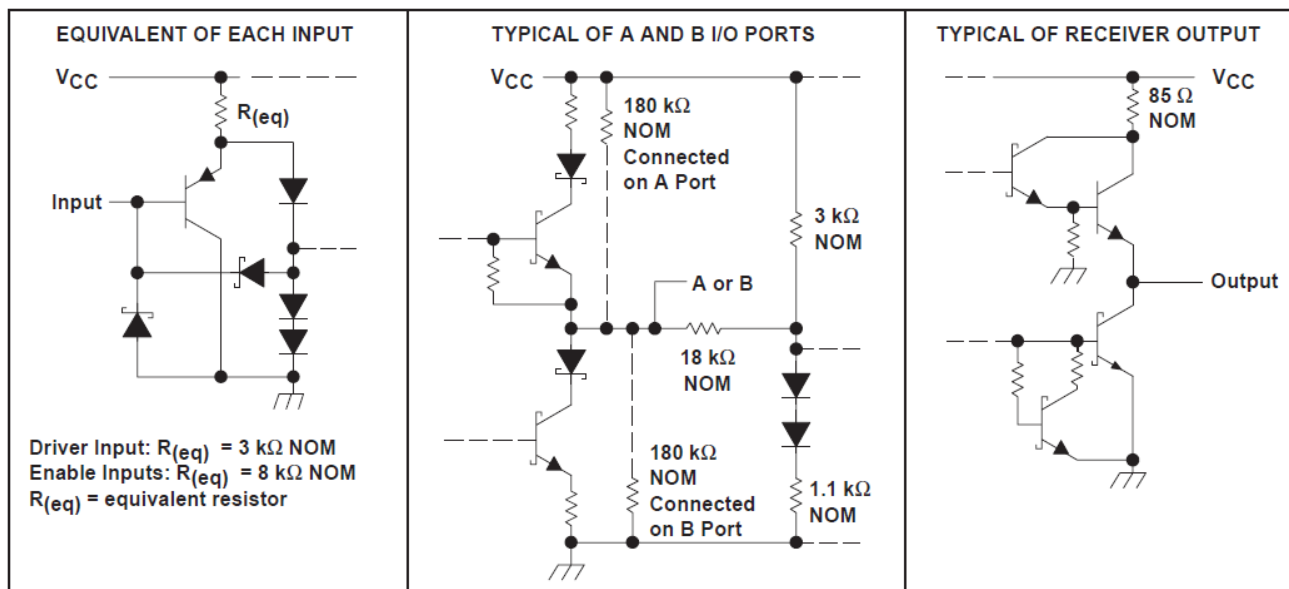


图 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver⁽¹⁾

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Receiver⁽¹⁾

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Inputs open	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

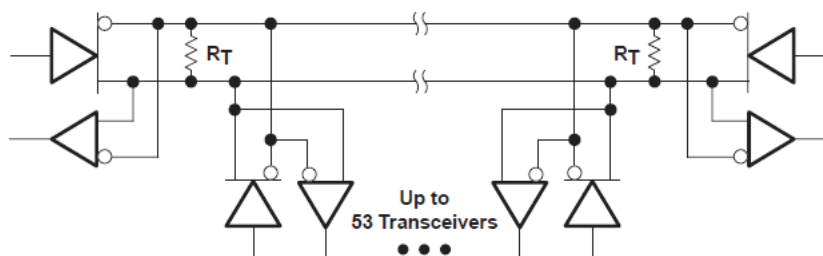
8 Application and Implementation

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8.1 Application Information

8.2 Typical Application



- A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

図 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 ドキュメントの更新通知を受け取る方法

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9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65A176	Samples
SN75ALS176AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A	Samples
SN75ALS176ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A	Samples
SN75ALS176ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7A176A	Samples
SN75ALS176AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176A	Samples
SN75ALS176BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(75A176, 7A176B)	Samples
SN75ALS176BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176B	Samples
SN75ALS176P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176	Samples
SN75ALS176PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS176	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS176DR	SOIC	D	8	2500	356.0	356.0	35.0
SN75ALS176ADR	SOIC	D	8	2500	340.5	336.1	25.0
SN75ALS176BDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS176AD	D	SOIC	8	75	507	8	3940	4.32
SN75ALS176AP	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176P	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS176PE4	P	PDIP	8	50	506	13.97	11230	4.32

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

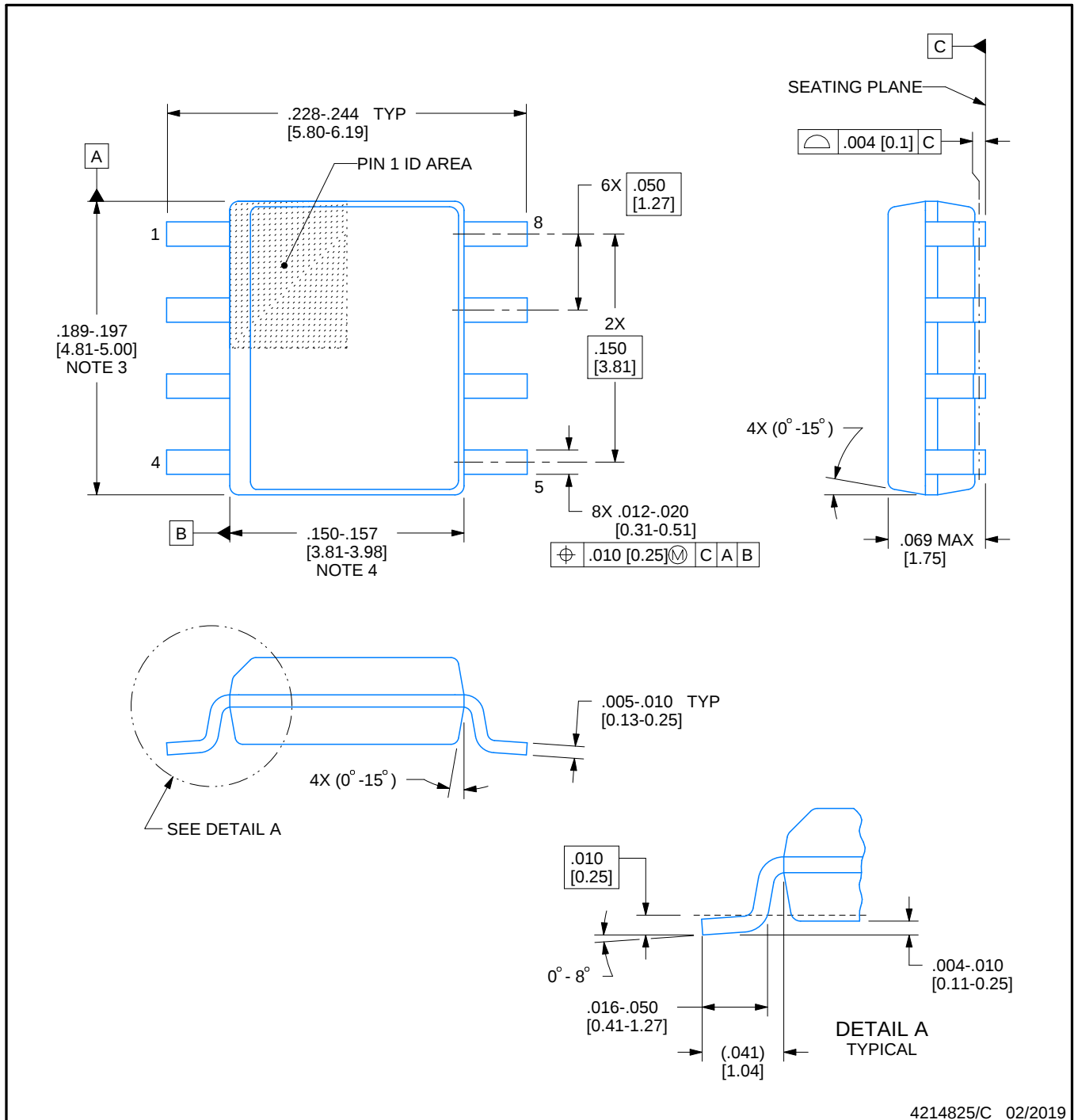


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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