SNx5ALS180 差動ドライバとレシーバのペア

1 特長

- TIA/EIA-422-B、TIA/EIA-485-A の要件を満たしているか、それを上回っています。[1] ITU 勧告 V.11 です。
- 高速の高度な低消費電力ショットキー回路
- シリアルとパラレルの両方のアプリケーションでの 25Mbaud 動作に対応
- デバイス間の低スキュー:6ns (最大)
- 小さい消費電流要件:30mA 以下
- デュアル V_{CC} およびデュアル GND を備えた個別のドライバおよびレシーバ I/O ピン
- 広い正および負の入力 / 出力バス電圧範囲
- ドライバ出力能力:±60mA
- サーマル・シャットダウン保護機能
- ドライバの正および負の電流制限
- レシーバ入力インピーダンス:12kΩ 以上
- レシーバ入力感度:最大 ±200mV
- レシーバ入力ヒステリシス:60mV (標準値)
- 単一の 5V 電源で動作
- グリッチ・フリーのパワーアップ / パワーダウン保護機能

2 概要

SN65ALS180 および SN75ALS180 差動ドライバおよびレシーバのペアは、マルチポイント・バス伝送ラインでの双方向データ通信用に設計された IC です。これらのデバイスは平衡伝送ライン用に設計されており、TIA/EIA-422-B、TIA/EIA-485-A、ITU 勧告 V.11 を満たしています。

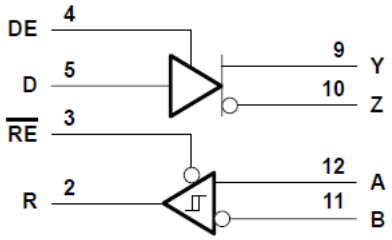
SN65ALS180 および SN75ALS180 は、3 ステート差動ライン・ドライバと差動入力ライン・レシーバを統合しており、どちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力は、自由度が増すように個別の端子に接続されており、ドライバがディセーブルされた場合、または V_{CC} = 0 の場合、バスへの負荷が最小化されるように設計されています。

これらのポートは広い正および負の同相モード電圧範囲を持っているため、本デバイスはパーティライン・アプリケーションに適しています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
SNx5ALS176	D (SOIC)	8.65mm × 3.91mm
	N (PDIP)	19.3mm × 6.35mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



論理図 (正論理)

[1] これらのデバイスは、ジェネレータ競合テスト (3.4.2 項) とジェネレータ電流制限 (3.4.3 項) を除き、TIA/EIA-485-A の要件を満たしているか、それを上回っています。適用されるテスト電圧範囲は、SN75ALS180 では -6V～8V、SN65ALS180 では -4V～8V で、

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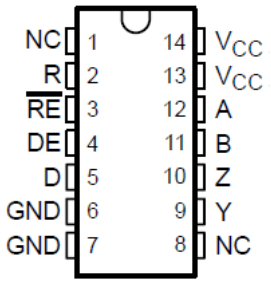
3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (April 2003) to Revision H (January 2023)	Page
• ドキュメントを最新のテキサス・インスツルメンツ・フォーマットに変更	1
• Deleted the Package thermal impedance from the *Absolute Maximum Ratings*	4
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics* graphs	8

4 Pin Configuration and Functions



NC – No internal connection

図 4-1. SN65ALS180 D Package
SN75ALS180 D or N Package
(Top View)

表 4-1. Pin Functions

NO	Name	Type	Description
1	NC	-	No Internal connection
2	R	O	Receive data output
3	$\overline{RE}$	I	Receiver enable, active low
4	DE	I	Driver enable, active high
5	D	I	Driver data input
6, 7	GND	GND	Device ground
8	NC	-	No Internal connection
9	Y	O	Digital bus output, Y (Complementary to Z)
10	Z	O	Digital bus output, Z (Complementary to Y)
11	A	I	Bus input, A (complementary to B)
12	B	I	Bus input, B (complementary to A)
13, 14	V_{CC}	SUPPLY	4.75V to 5.25V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-10	15	V
V_I	Enable input voltage		5.5	V
T_J	Operating virtual junction temperature		150	℃
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)				12	V
					–7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	SN65ALS180	–40		85	°C
		SN75ALS180	0		70	

(1) Differential-input/output bus voltage is measured at the noninverting terminal, A/Y, with respect to the inverting terminal, B/Z.

5.3 Thermal Information

THERMAL METRIC(1)		N (PDIP)	D (SOIC) (SN65 Devices)	D (SOIC) (SN75 Devices)	UNIT
		14-Pins	14-Pins	14-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	93.2	83.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	40	47.5	39.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	49.4	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	11.2	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	48.9	39.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See 図 6-1	1/2V_{OD1} or 2(3)			V
		R_L = 54 Ω	See 図 6-1	1.5	2.5	5	
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See 図 6-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(4)	R_L = 54 Ω or 100 Ω	See 図 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω	See 図 6-1			3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(4)	R_L = 54 Ω or 100 Ω	See 図 6-1			±0.2	V
I_O	Output current	Output disabled(6)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current(5)	V_O = –6 V	SN75ALS180			–250	mA
		V_O = –4 V	SN65ALS180			–250	
		V_O = 0	All			–150	
		V_O = V_{CC}	All			250	
		V_O = 8 V	All			250	
I_{CC}	Supply current	No load	Driver outputs enabled, Receiver disabled		25	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3	3	8	13	ns
	Pulse skew ($\|t_{d(ODH)} - t_{d(ODL)}\|$)	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3		1	6	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω	C_L = 50 pF,	See 図 6-3	3	8	13	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω	See 図 6-4			23	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω	See 図 6-5			19	24	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω	See 図 6-4			8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω	See 図 6-5			8	13	ns

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, Vo_b
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	$V_t(R_L = 100\ \Omega)$	$V_t(R_L = 54\ \Omega)$
$\|V_{OD3}\|$		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

5.7 Electrical Characteristics - Receivers

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+}– $V_{IT–}$)					60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 µA,	See 図 6-6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA,	See 図 6-6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	µA
I_I	Line input current	Other input = 0 V(3)	V_I = 12 V				1	mA
			V_I = –7 V				–0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	mA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					–100	mA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0		–15		–85	mA
I_{CC}	Supply current	No load	Receiver outputs enabled, Driver inputs disabled			19	30	mA
			Outputs disabled			19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.8 Switching Characteristics - Receivers

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V, See 図 6-7	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See 図 6-7	C_L = 15 pF,	9	14	19	ns
	Skew ($\lvert t_{PHL} – t_{PLH} \rvert$)	V_{ID} = –1.5 V to 1.5 V, See 図 6-7	C_L = 15 pF,		2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See 図 6-8		7	14	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See 図 6-8		7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See 図 6-8		20	35	ns
t_{PLZ}	Output disable time from low level	C_L= 15 pF,	See 図 6-8		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.9 Typical Characteristics

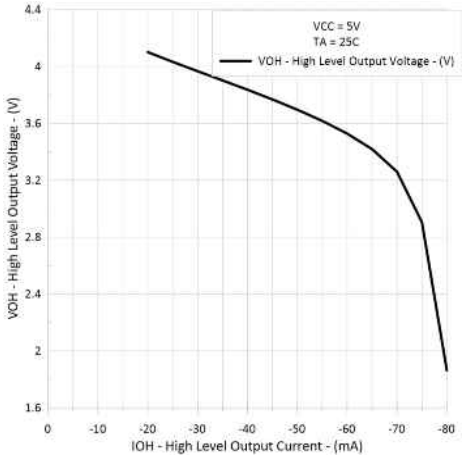


図 5-1. Drivers High-Level Output Voltage vs High-Level Output Voltage

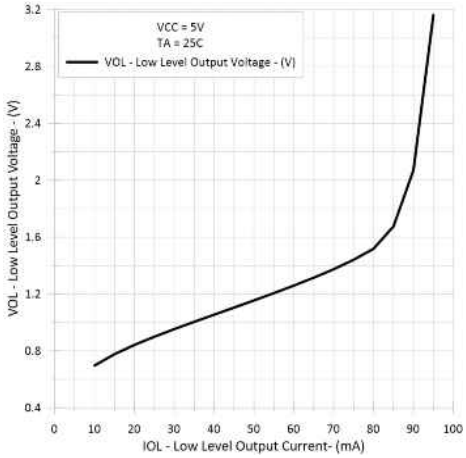


図 5-2. Drivers Low-Level Output Voltage vs Low-Level Output Current

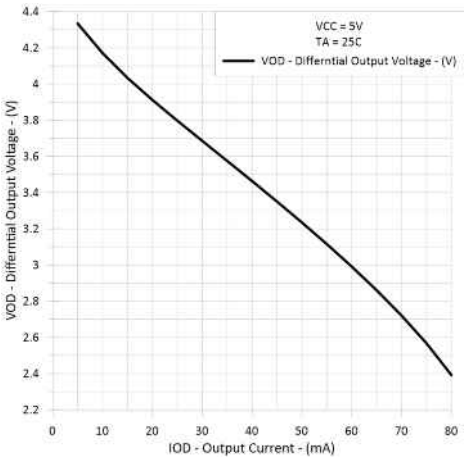


図 5-3. Drivers Differential Output Voltage vs Output Current

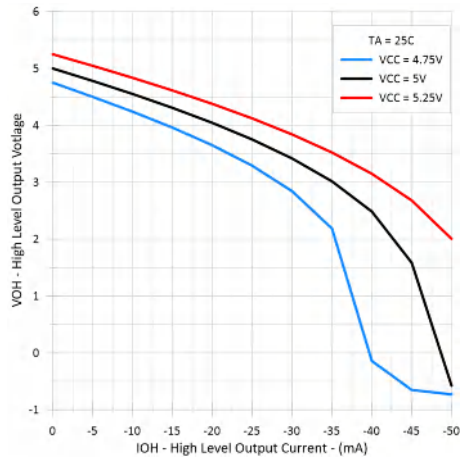


図 5-4. Receivers High-Level Output Voltage vs High-Level Output Current

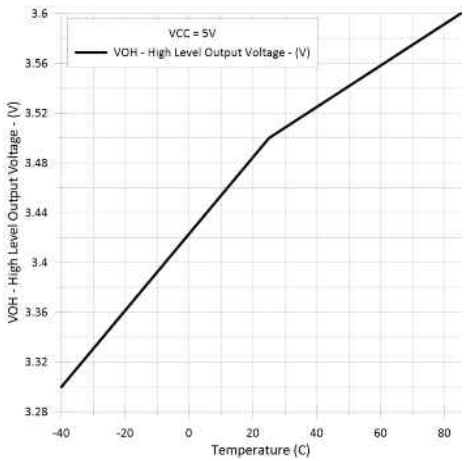


図 5-5. Receivers High-Level Output Voltage vs Free-Air Temperature

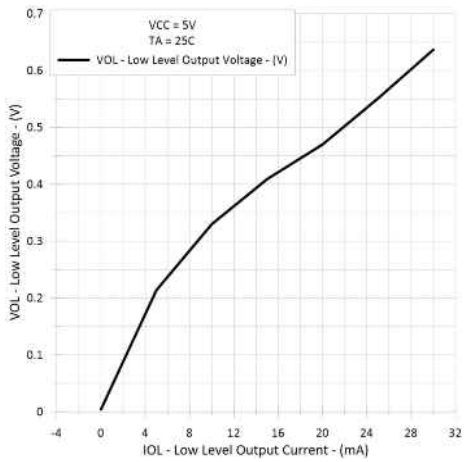


図 5-6. Receivers Low-Level Output Voltage vs Low-Level Output Current

5.9 Typical Characteristics (continued)

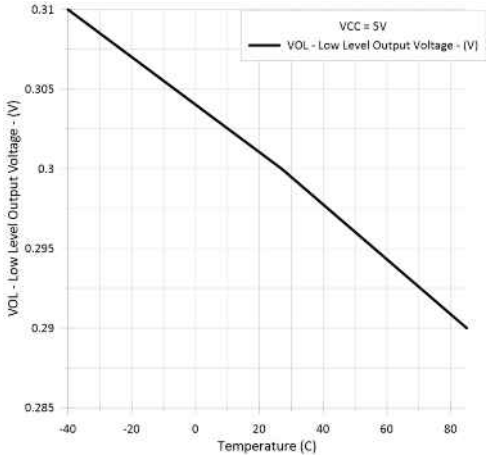


図 5-7. Receivers Low-Level Output Voltage vs Free-Air Temperature

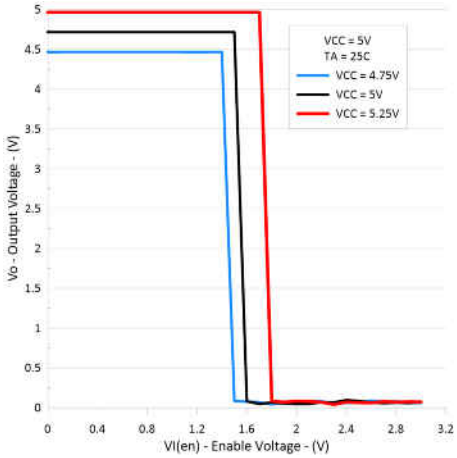


図 5-8. Receivers Output Voltage vs Enable Voltage

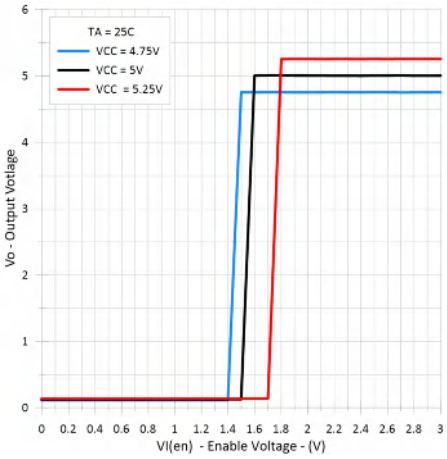


図 5-9. Receivers Output Voltage vs Enable Voltage

6 Parameter Measurement Information

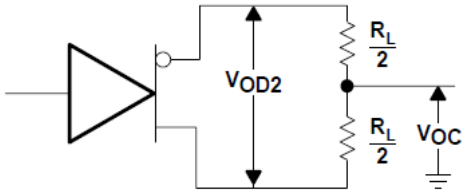


図 6-1. Driver V_{OD} and V_{OC}

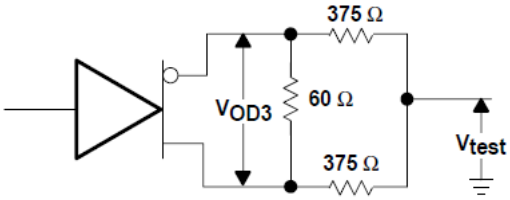
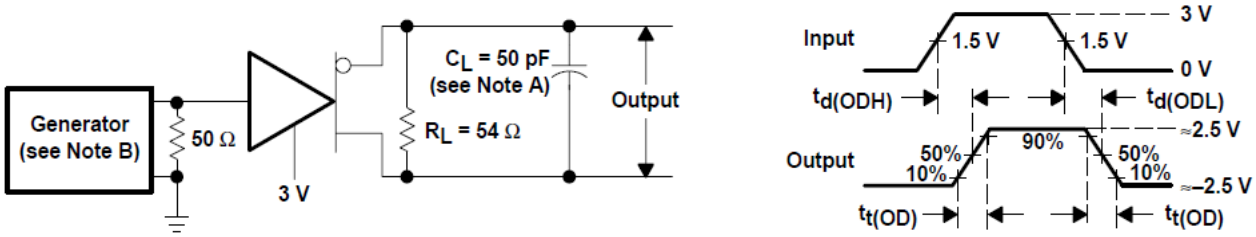
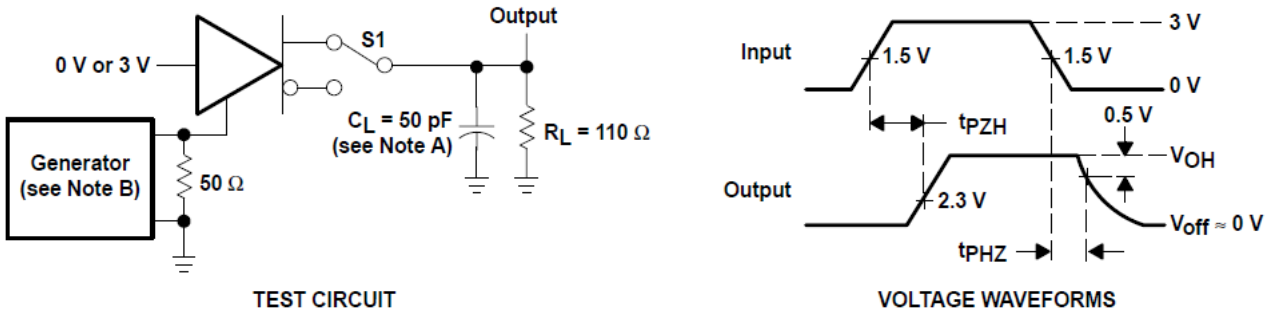


図 6-2. Driver V_{OD3}



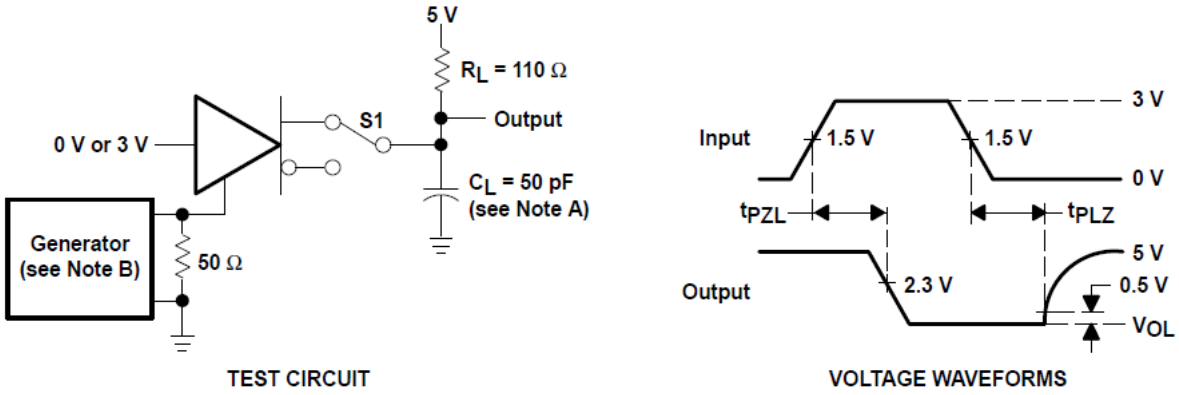
A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

図 6-3. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

図 6-4. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

図 6-5. Driver Test Circuit and Voltage Waveforms

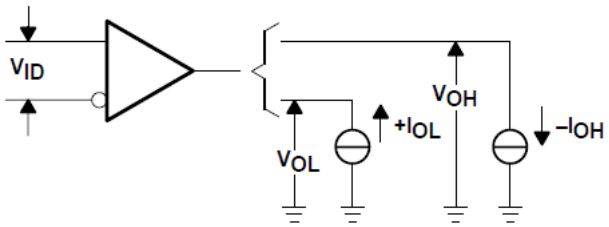
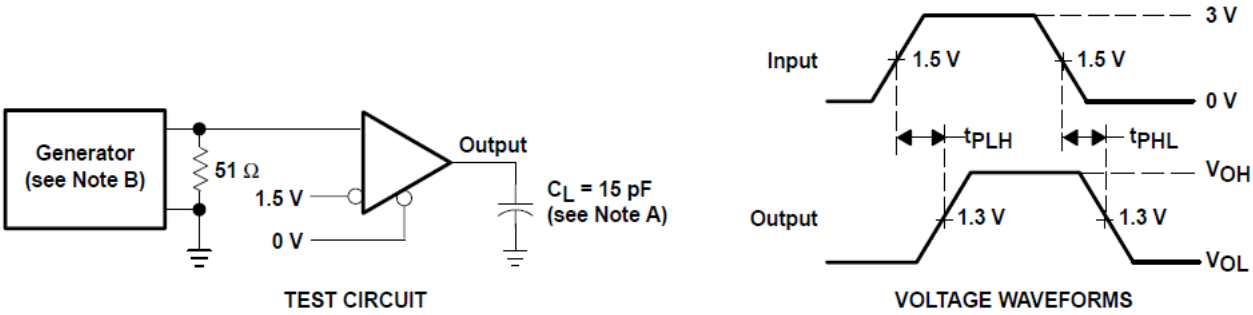
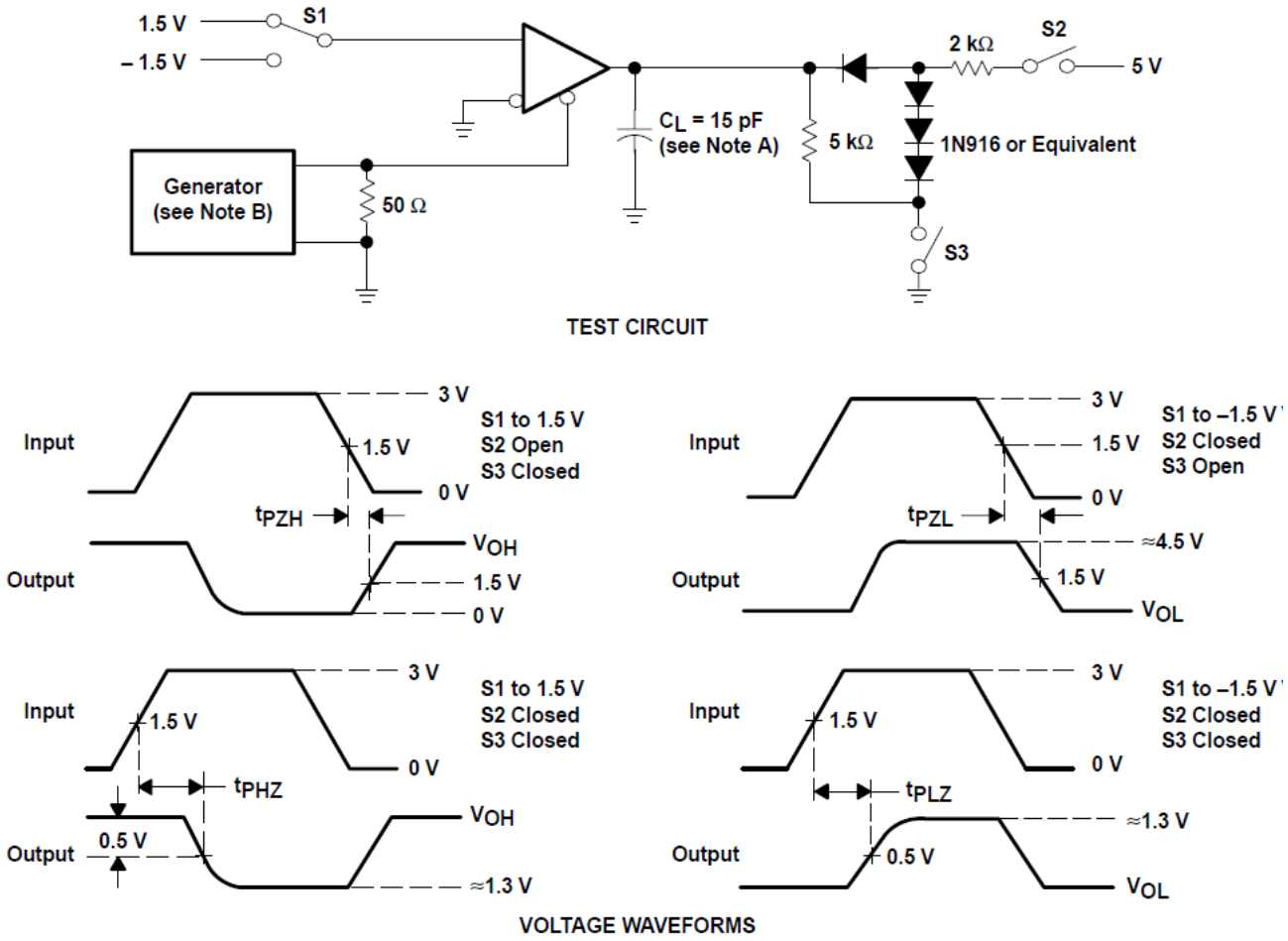


図 6-6. Receiver V_{OH} and V_{OL}



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

図 6-7. Receiver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

図 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

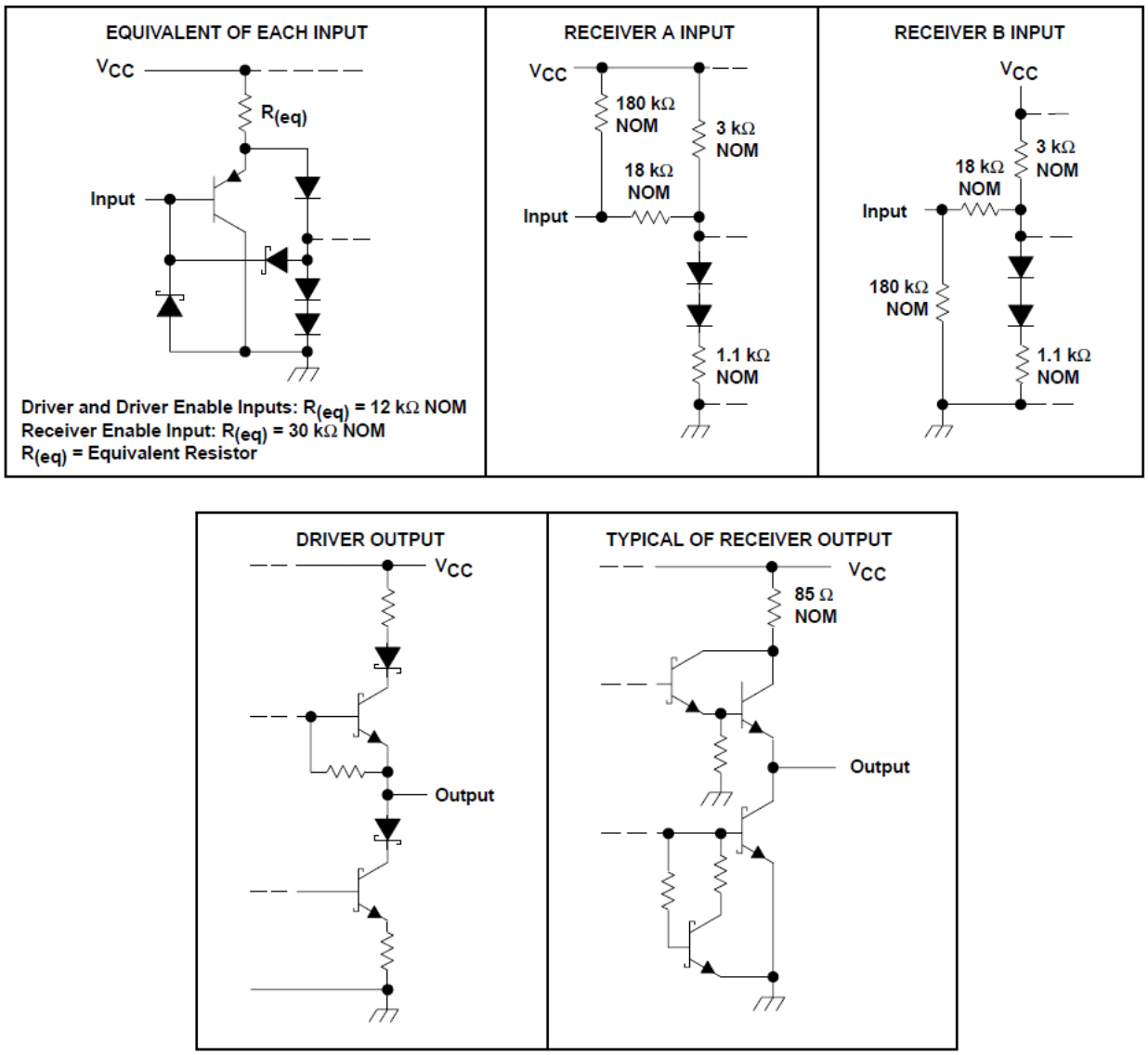


図 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 7-2. Receiver(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

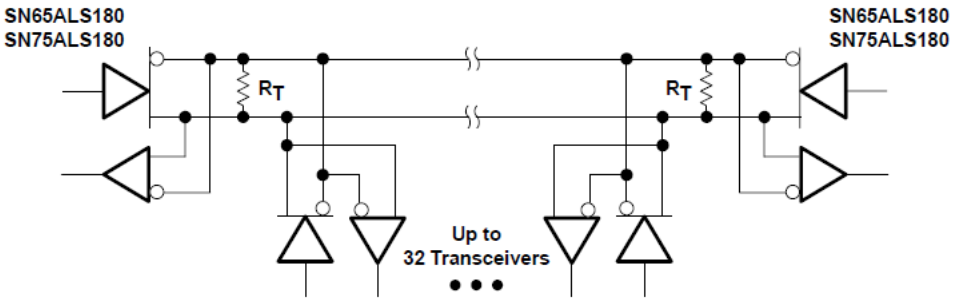
8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application



A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

図 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65ALS180D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	65ALS180
SN65ALS180DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180
SN65ALS180DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180
SN65ALS180DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180
SN75ALS180D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	75ALS180
SN75ALS180DR	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	75ALS180
SN75ALS180N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS180N
SN75ALS180N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS180N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

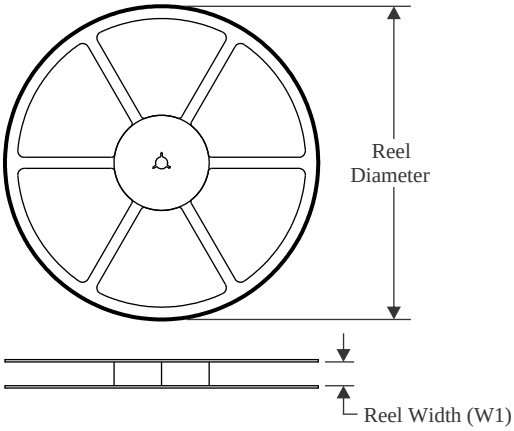
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

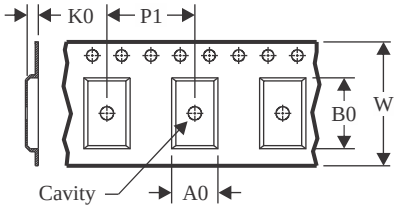
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

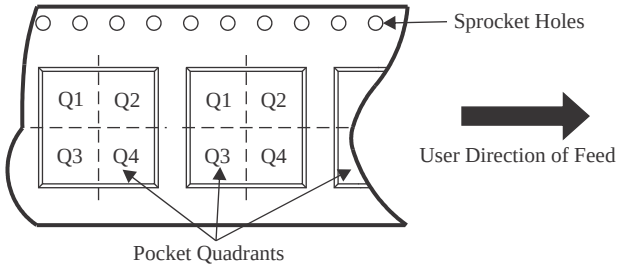


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

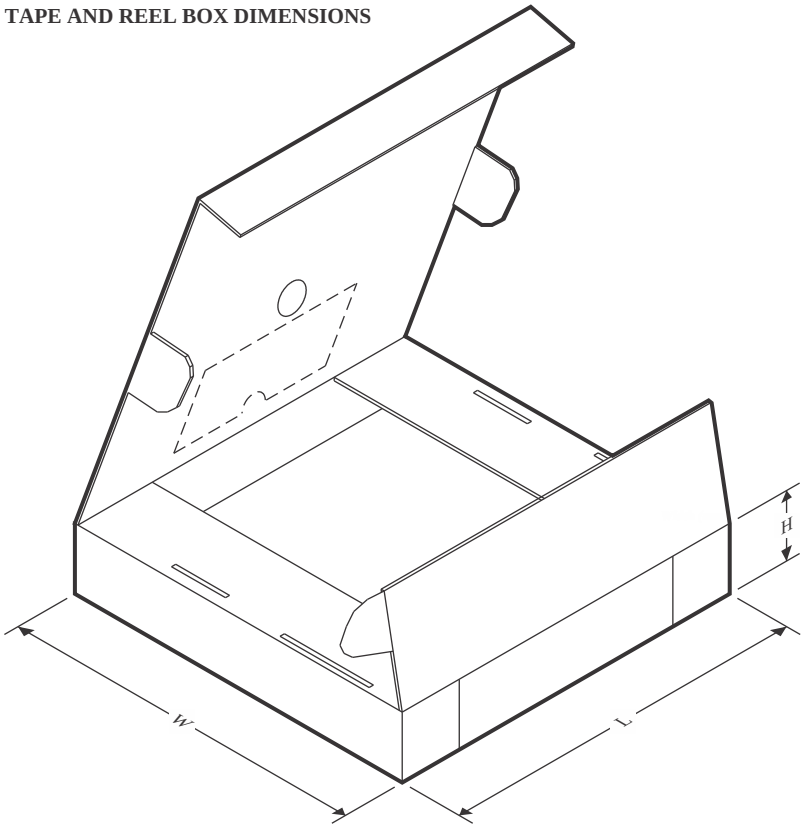
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

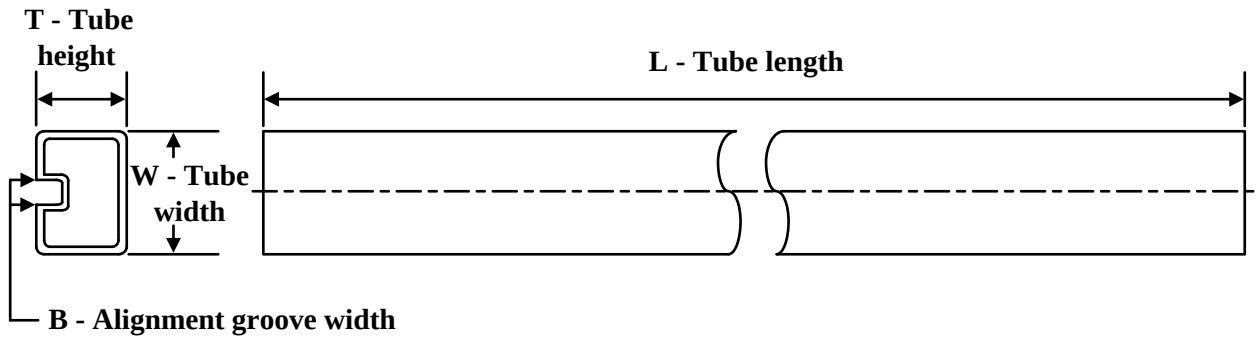
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

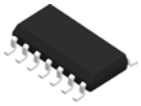
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS180DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS180N	N	PDIP	14	25	506	13.97	11230	4.32
SN75ALS180N.A	N	PDIP	14	25	506	13.97	11230	4.32

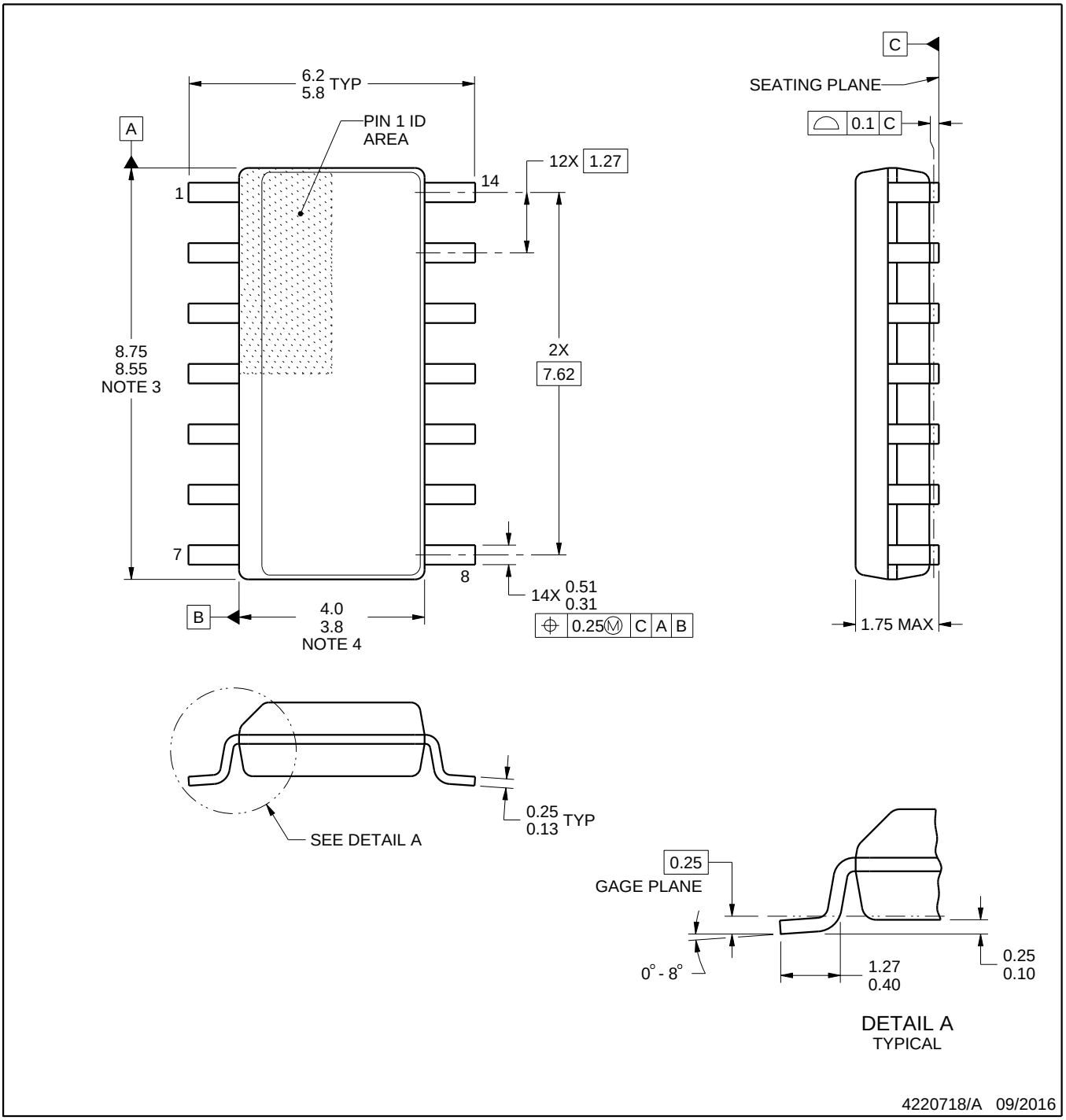


PACKAGE OUTLINE

D0014A

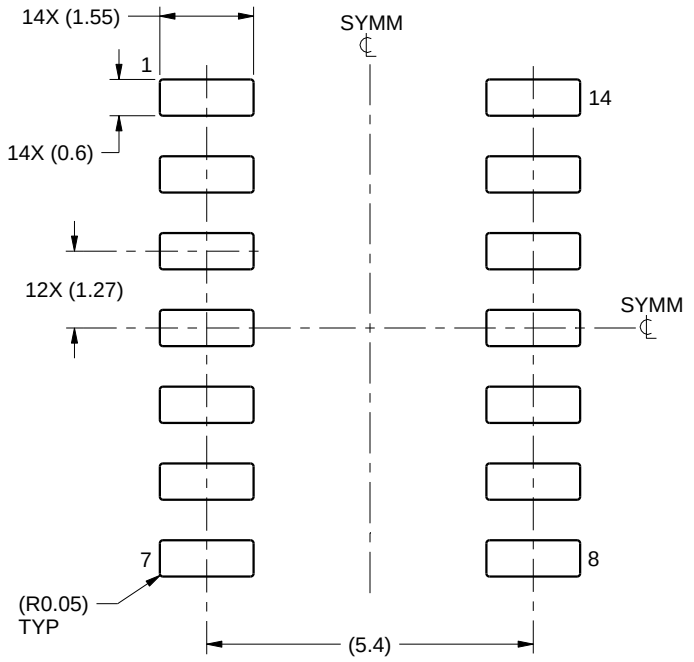
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

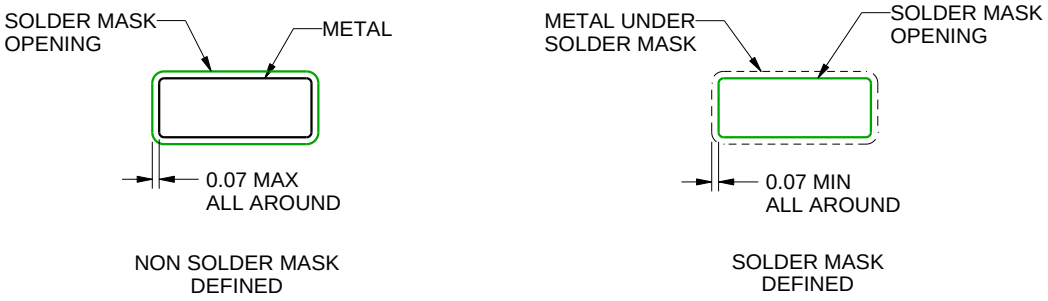


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

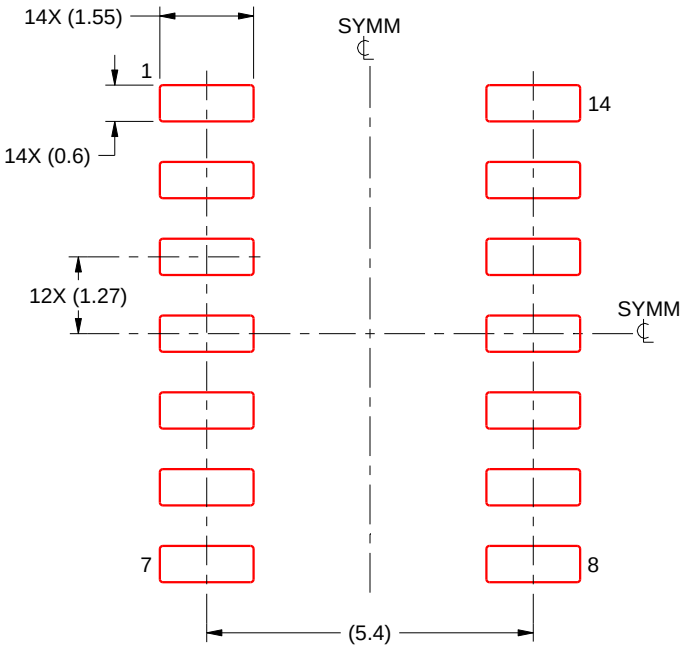
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

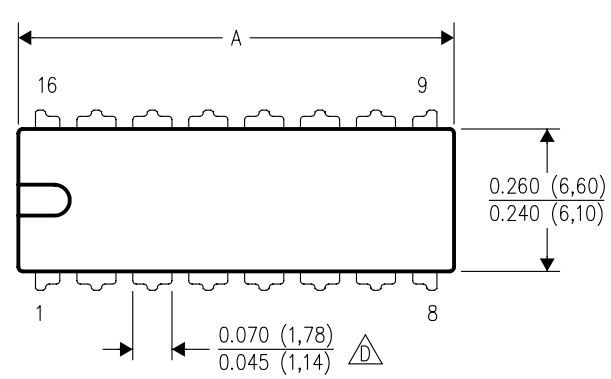
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

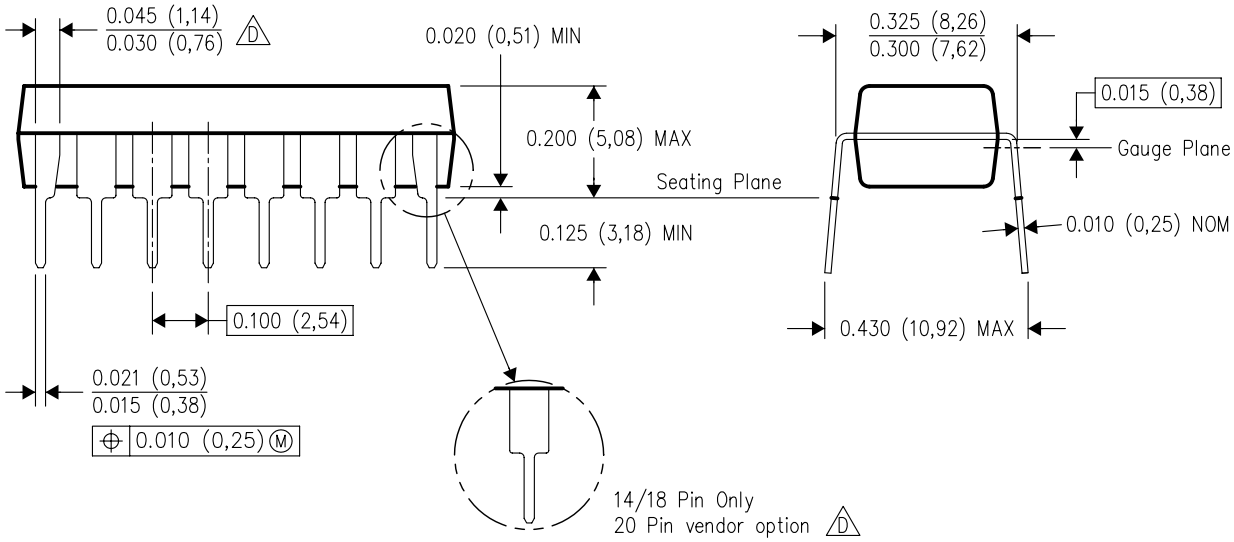
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最終更新日：2025 年 10 月