

SNx5C3243 3V~5.5V マルチチャネル RS-232 互換、ライン・ドライバ/レシーバ

1 特長

- 3V~5.5V の V_{CC} 電源で動作
- 常時アクティブの非反転レシーバ出力 (ROUT2B)
- 小さいスタンバイ電流: 1 μ A (標準値)
- 外付けコンデンサ: 4 \times 0.1 μ F
- 3.3V 電源で 5V ロジック入力を受容
- SN65C3238、SN75C3238 と組み合わせて使用可能
- 250kbit/s~1Mbit/s での動作をサポート
- 人体モデル (HBM) で ± 15 kV を超える RS-232 バス・ピン ESD 保護

2 アプリケーション

- バッテリ駆動システム
- パーソナル・エレクトロニクス
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

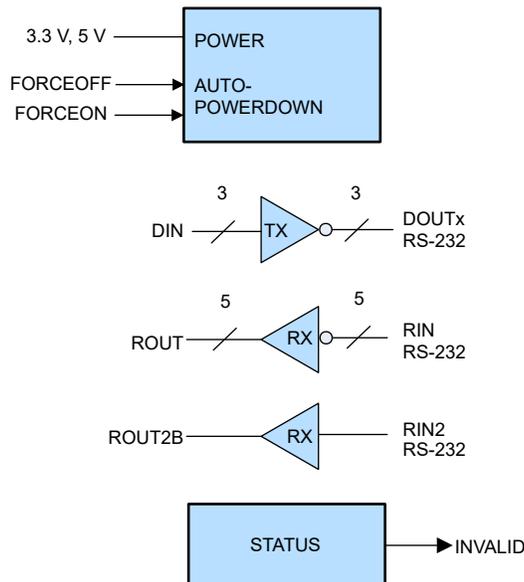
3 概要

SN65C3243 と SN75C3243 は 3 つのライン・ドライバ、5 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、 ± 15 kV のピン間 (シリアル・ポート接続ピン、GND を含む) ESD 保護機能を備えています。このデバイスは、非同期通信コントローラとシリアルポート・コネクタの間の電氣的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。さらに、このデバイスには常時アクティブな非反転出力 (ROUT2B) があり、リング・インジケータを使用するアプリケーションが、デバイスの電源がオフのときにもデータを送信できるようになっています。このデバイスは、最大 1Mbit/s のデータ信号速度、24V/ μ s~150V/ μ s の高い出力スルーレートで動作します。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN65C3243 SN75C3243	SSOP (DB)	10.2mm \times 5.30mm
	SOIC (DW)	17.9mm \times 7.50mm
	TSSOP (PW)	9.70mm \times 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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4 Revision History

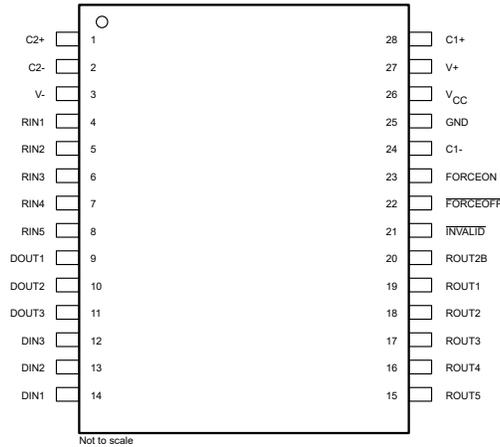
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (September 2008) to Revision I (October 2022)

Page

- 「製品情報」表、「ピン構成および機能」セクション、「ESD 定格」表、「熱に関する情報」表、「詳細説明」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加..... 1
- Changed the I_{CC} Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the *Electrical Characteristics* 5

5 Pin Configuration and Functions



**图 5-1. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP)
(Top View)**

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-	—	Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	INVALID	O	Invalid Output Pin
22	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V _{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range ⁽²⁾	-0.3	6	V	
V+	Positive-output supply voltage range ⁽²⁾	-0.3	7	V	
V-	Negative-output supply voltage range ⁽²⁾	0.3	-7	V	
V+ – V-	Supply voltage difference ⁽²⁾		13	V	
V _I	Input voltage range	Driver (FORCEOFF, FORCEON)	-0.3	6	V
		Receiver	-25	25	
V _O	Output voltage range	Driver	-13.2	13.2	V
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 on RS-232 bus pins DOUT1/2/3, RIN1/2/3/4/5 ⁽¹⁾	±15	kV

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

see [7-6](#) ⁽¹⁾

		MIN	NOM	MAX	UNIT	
Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V	
	V _{CC} = 5 V	4.5	5	5.5		
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON	V _{CC} = 3.3 V	2	V	
			V _{CC} = 5 V	2.4		
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON		0.8	V	
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON		0	5.5	V
V _I	Receiver input voltage	-25		25	V	
T _A	Operating free-air temperature	SN65C3243	-40	85	°C	
		SN75C3243	0	70		

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DB (SSOP)	DW (SOIC)	PW (TSSOP)	UNIT
		28 PINS	28 PINS	28 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	76.1	59.0	70.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	37.4	30.3	29.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.4	7.8	1.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	37.0	30.0	28.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-6](#))⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON		±0.01	±1	μA
I _{CC}	Supply current	Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V _{CC} For DB and PW package	0.3	1.2	mA
		Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V _{CC} For DW package	0.3	1	mA
		Powered off	No load, FORCEOFF = GND	1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF = V _{CC} , FORCEON = GND, All RIN are open or grounded, All DIN are grounded	1	10	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.6 Electrical Characteristics, Driver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-6](#))

PARAMETER	TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{OH}	High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4	V	
V _{OL}	Low-level output voltage	All DOUT at R _L = 3 kΩ to GND	–5	–5.4	V	
V _O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5		V	
I _{IH}	High-level input current	V _I = V _{CC}	±0.01	±1	μA	
I _{IL}	Low-level input current	V _I = GND	±0.01	±1	μA	
I _{OS}	Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V, V _O = 0 V	±35	±60	mA	
		V _{CC} = 5.5 V, V _O = 0 V	±35	±90		
r _o	Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ±2 V	300	10M	Ω	
I _{off}	Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V		±25	μA
			V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V		±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.7 Electrical Characteristics, Receiver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-6](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	µA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.8 Electrical Characteristics, Auto-Powerdown Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{T+(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}		2.7	V
V _{T-(valid)}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-2.7		V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V _{CC}	-0.3	0.3	V
V _{OH}	INVALID high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} - 0.6		V
V _{OL}	INVALID low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, FORCEOFF = V _{CC}		0.4	V

6.9 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-6](#))

PARAMETER		TEST CONDITIONS ⁽³⁾		MIN	TYP ⁽¹⁾	MAX	UNIT	
Maximum data rate (see 7-1)	R _L = 3 kΩ, One DOUT switching	C _L = 1000 pF		250		kbit/s		
		C _L = 250 pF,	V _{CC} = 3 V to 4.5 V	1000				
		C _L = 1000 pF,	V _{CC} = 4.5 V to 5.5 V	1000				
t _{sk(p)}	Pulse skew ⁽²⁾	C _L = 150 pF to 2500 pF,	R _L = 3 kΩ to 7 kΩ,	See 7-2		25	ns	
SR(tr)	Slew rate, transition region (see 7-1)	C _L = 150 pF to 1000 pF,	R _L = 3 kΩ to 7 kΩ,	V _{CC} = 3.3 V		18	150	V/μs

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
- (2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.
- (3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽³⁾		TYP ⁽¹⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See 7-3		150	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See 7-3		150	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See 7-4		200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See 7-4		200	ns
t _{sk(p)}	Pulse skew ⁽²⁾	See 7-3		50	ns

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
- (2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.
- (3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

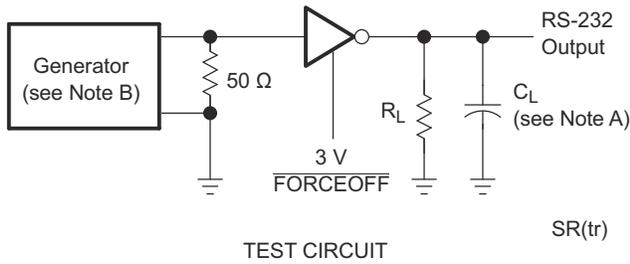
6.11 Switching Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-5](#))

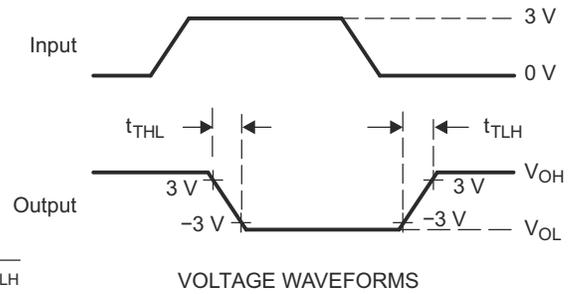
PARAMETER		TYP ⁽¹⁾	UNIT
t _{valid}	Propagation delay time, low- to high-level output	1	μs
t _{invalid}	Propagation delay time, high- to low-level output	30	μs
t _{en}	Supply enable time	100	μs

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

7 Parameter Measurement Information

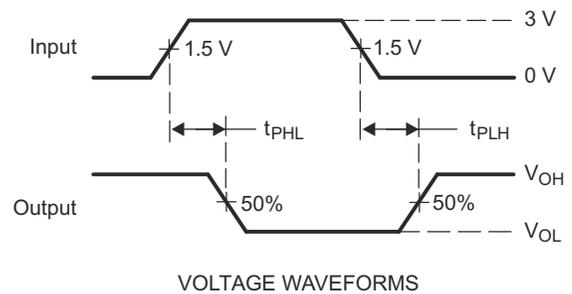
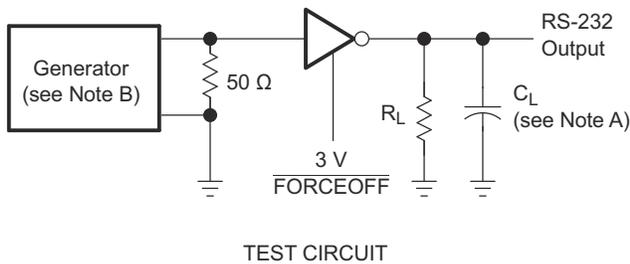


$$SR(tr) = \frac{6 V}{t_{THL} \text{ or } t_{TLH}}$$



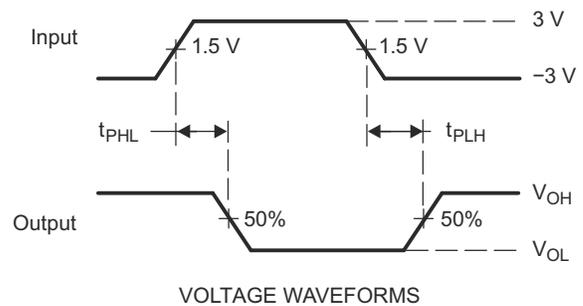
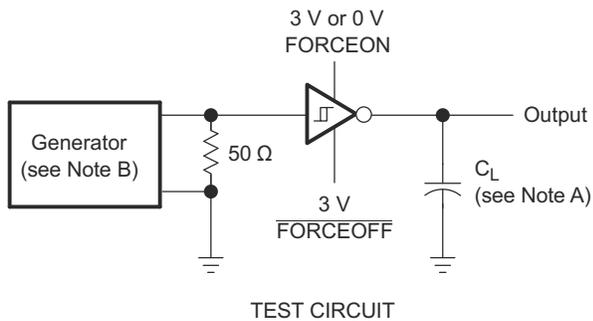
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 1 Mbits, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-1. Driver Slew Rate



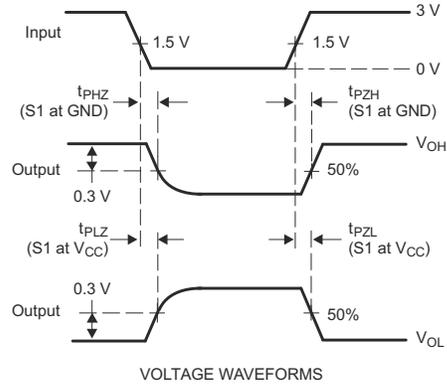
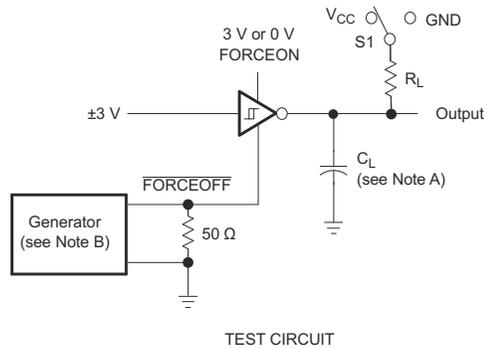
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 1 Mbits, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-2. Driver Pulse Skew



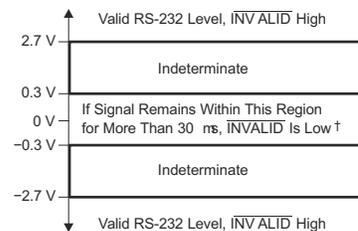
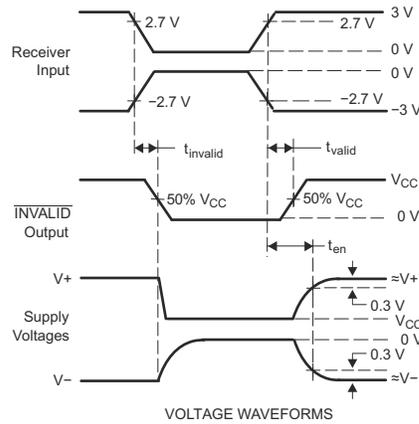
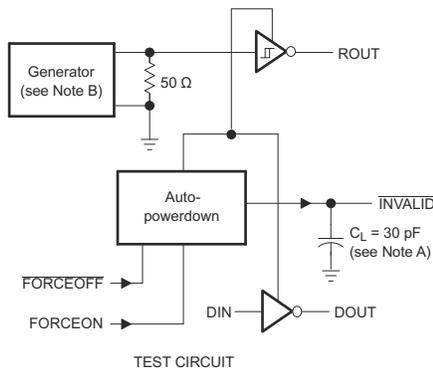
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-3. Receiver Propagation Delay Times



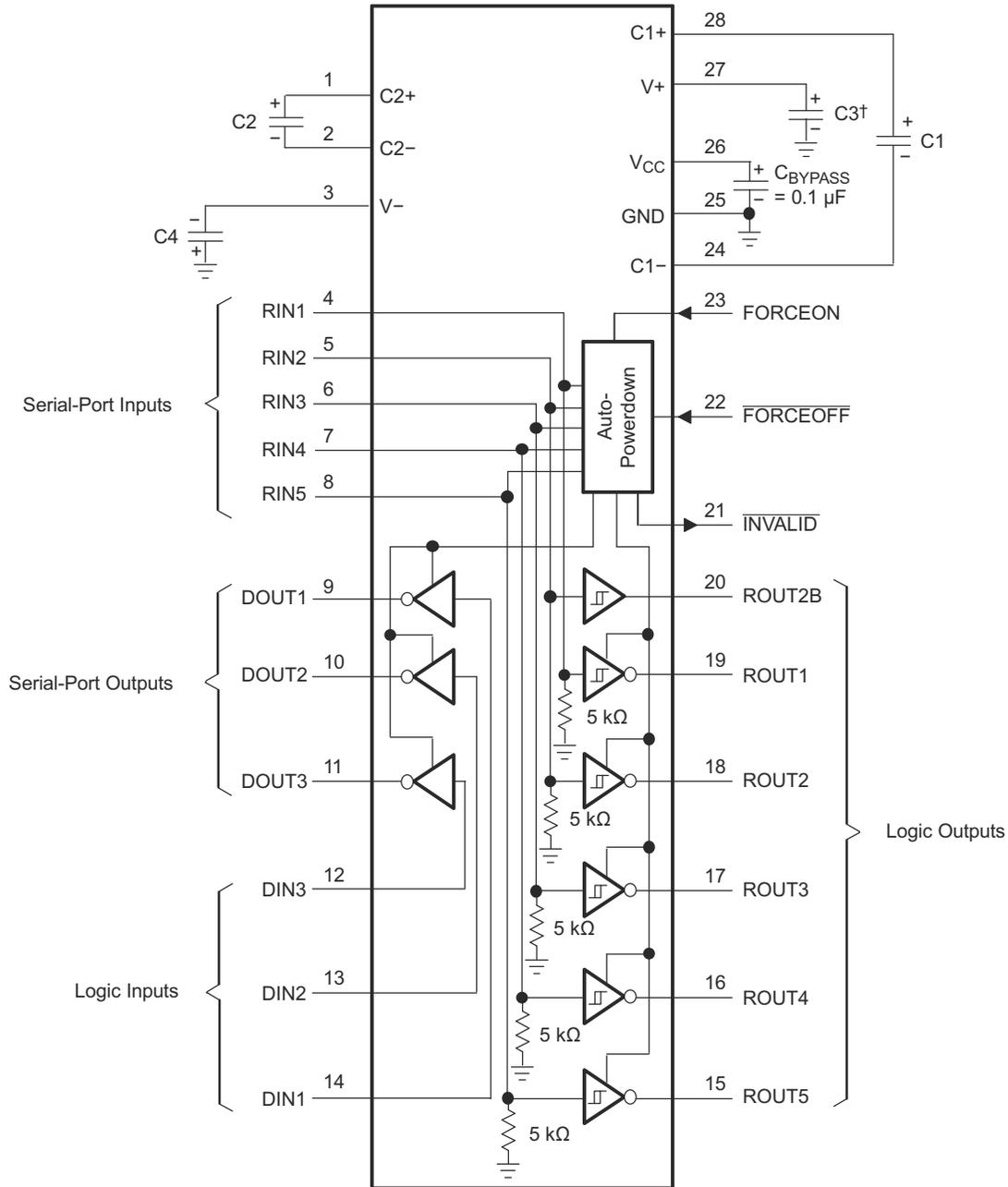
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

7-4. Receiver Enable and Disable Times



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 5 Mbits, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-5. INVALID Propagation Delay Times and Supply Enabling Time



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

图 7-6. Typical Operating Circuit and Capacitor Values

表 7-1. V_{CC} vs Capacitor Values

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

8 Detailed Description

8.1 Overview

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and FORCEOFF are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to [Figure 7-5](#) for receiver input levels.

8.2 Device Functional Modes

8.2.1 Function Tables

Each Driver, DIN⁽¹⁾

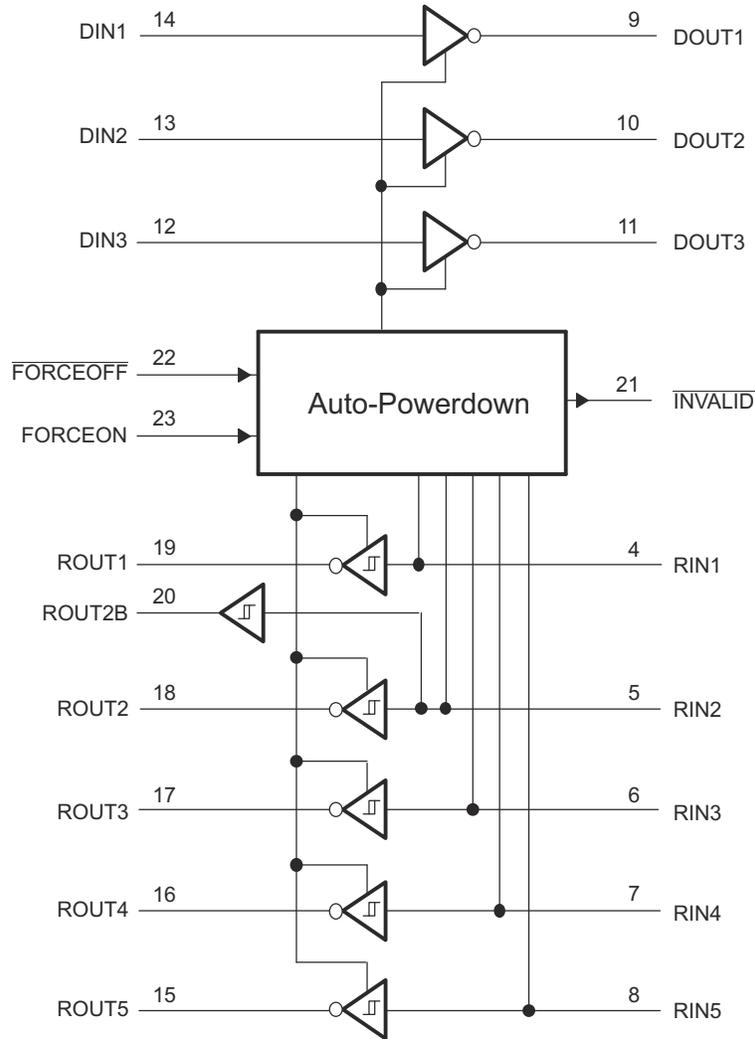
INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver, RIN⁽¹⁾

INPUTS				OUTPUTS			RECEIVER STATUS
RIN2	RIN1, RIN3–RIN5	FORCEOFF	VALID RIN RS-232 LEVEL	ROUT2B	ROUT2	ROUT1, ROUT3–5	
L	X	L	X	L	Z	Z	Powered off while ROUT2B is active
H	X	L	X	H	Z	Z	
L	L	H	YES	L	H	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	YES	L	L	L	
H	L	H	YES	H	H	H	
H	H	H	YES	H	L	L	
Open	Open	H	YES	L	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off



8-1. Logic Diagram (Positive Logic)

9 Device and Documentation Support

9.1 Device Support

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](https://www.ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3243DBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DW	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DW.A	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DWR	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243DWR.A	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243
SN65C3243PWR	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243
SN65C3243PWR.A	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243
SN75C3243DBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DW	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DW.A	Active	Production	SOIC (DW) 28	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DWR	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243DWR.A	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243
SN75C3243PW	Obsolete	Production	TSSOP (PW) 28	-	-	Call TI	Call TI	0 to 70	CA3243
SN75C3243PWR	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243
SN75C3243PWR.A	Active	Production	TSSOP (PW) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

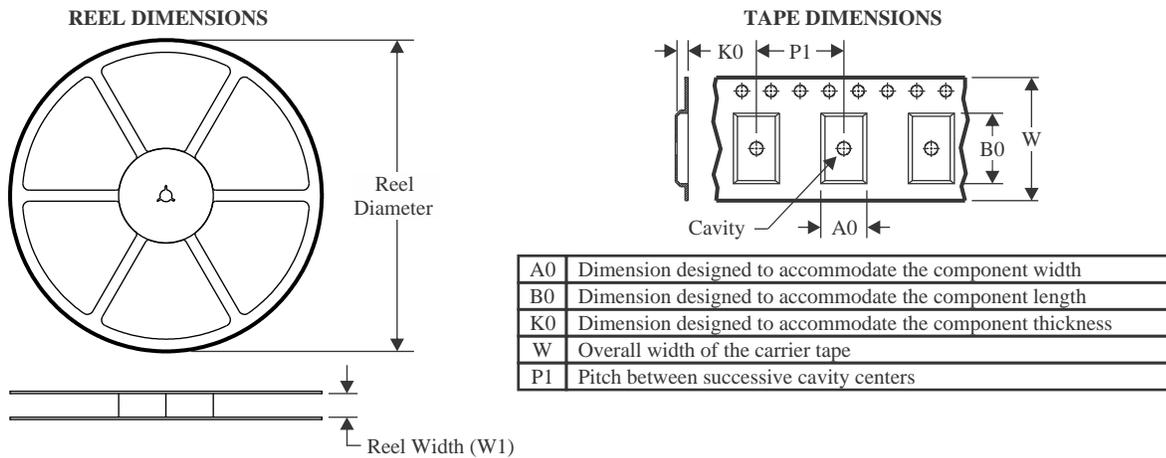
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN65C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN65C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
SN75C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN75C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN75C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3243DBR	SSOP	DB	28	2000	353.0	353.0	32.0
SN65C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN65C3243PWR	TSSOP	PW	28	2000	353.0	353.0	32.0
SN75C3243DBR	SSOP	DB	28	2000	353.0	353.0	32.0
SN75C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN75C3243PWR	TSSOP	PW	28	2000	353.0	353.0	32.0

TUBE

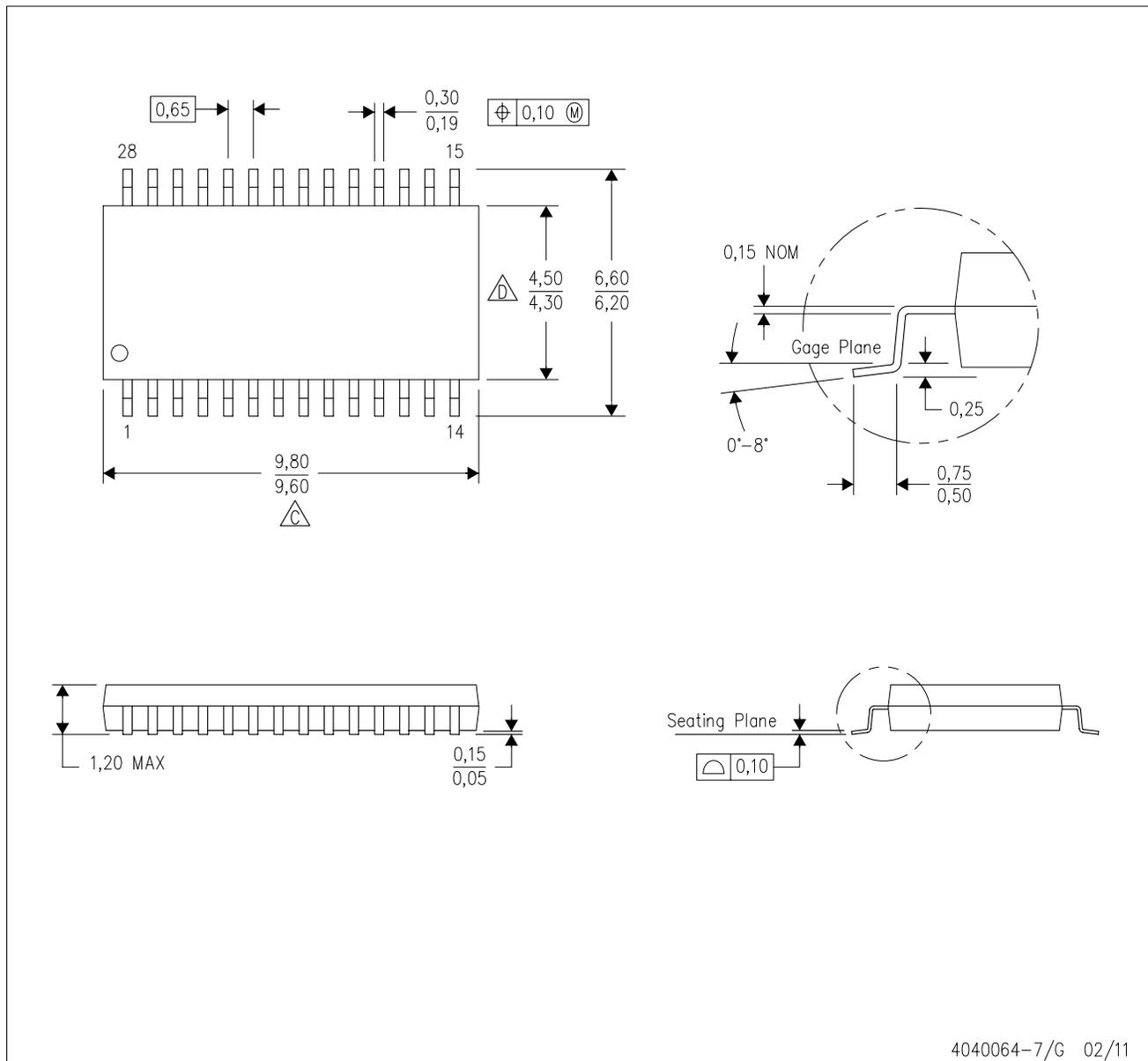

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN65C3243DW.A	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75C3243DW.A	DW	SOIC	28	20	506.98	12.7	4826	6.6

MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

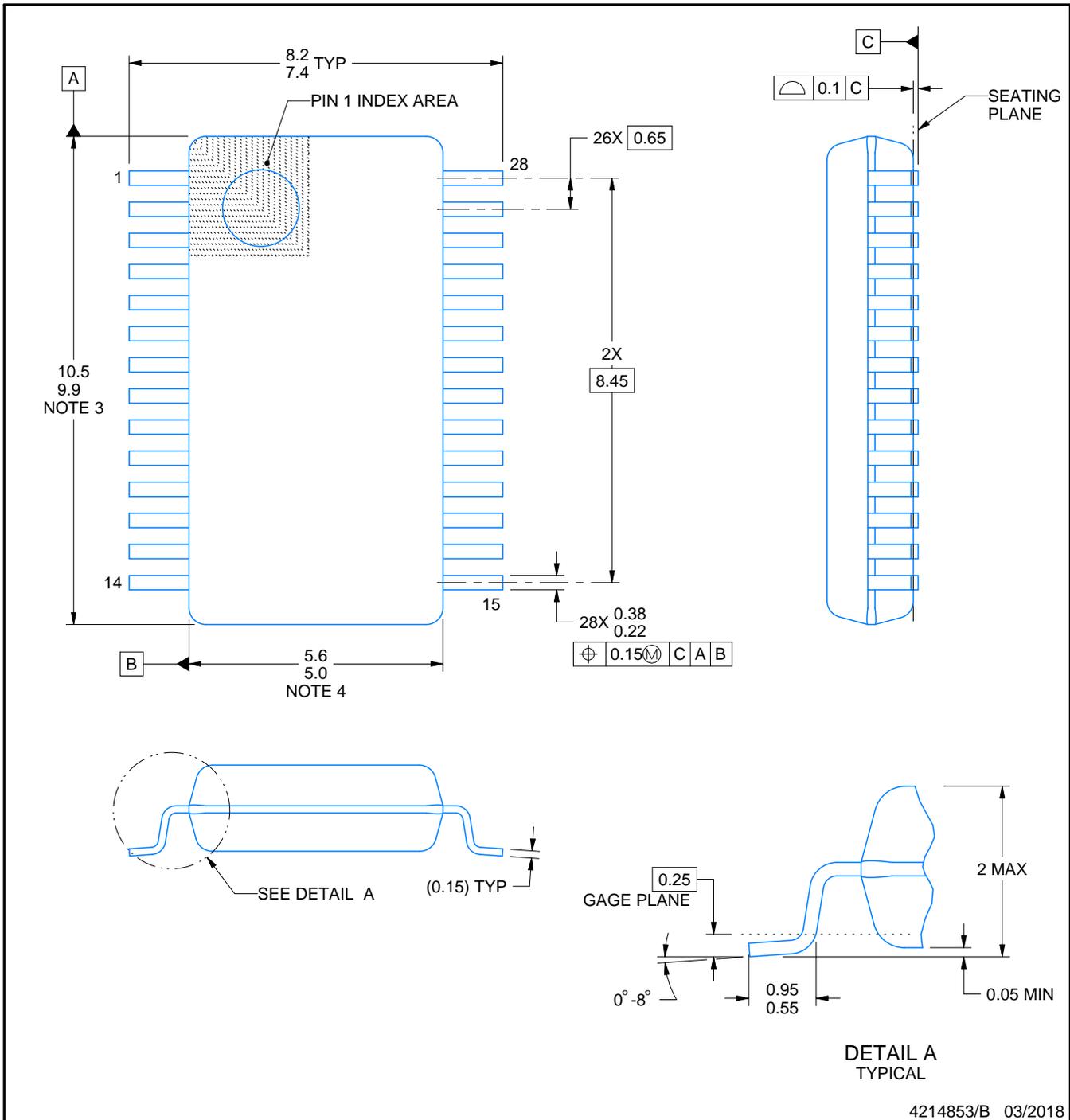
DB0028A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES:

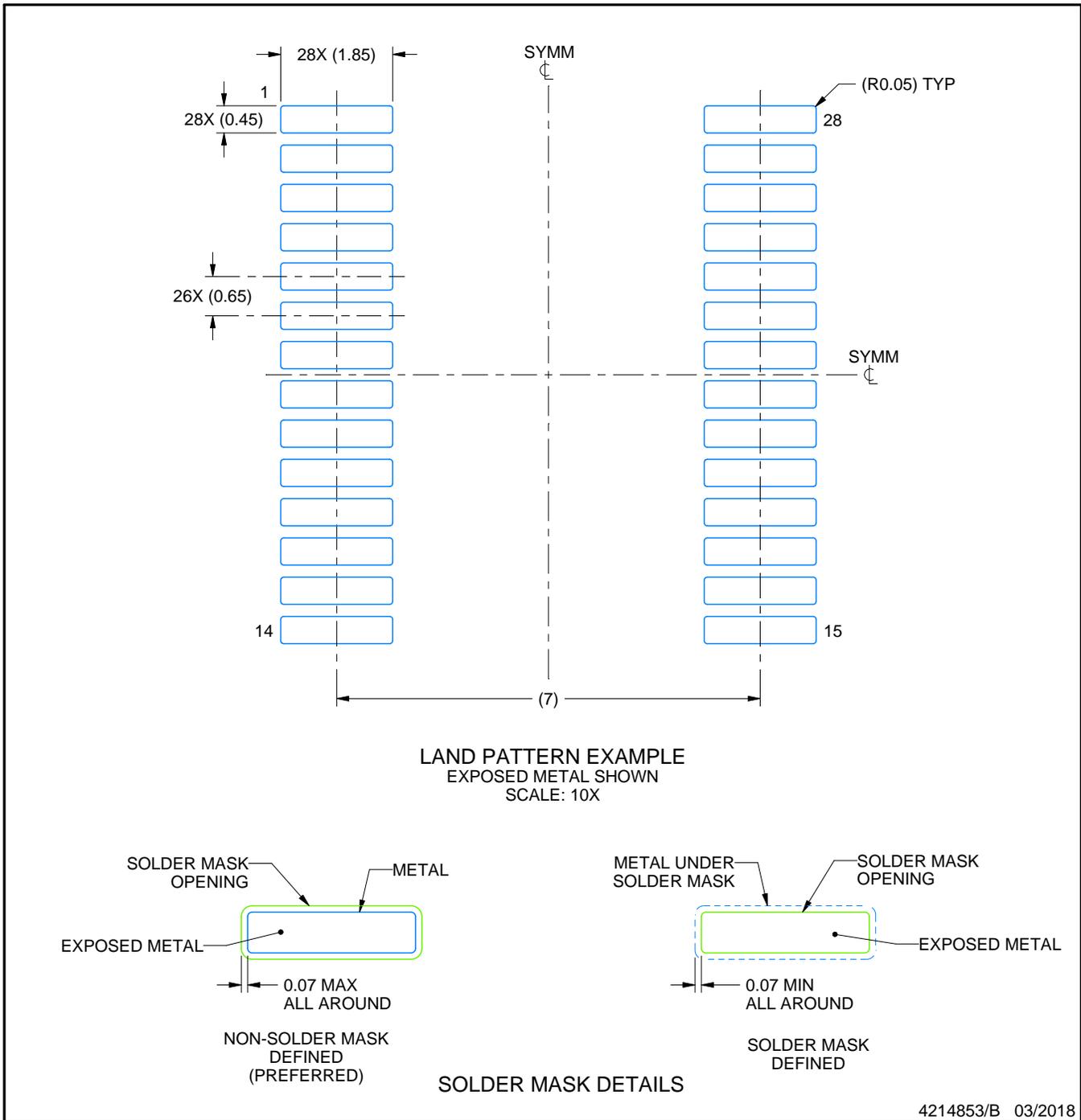
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

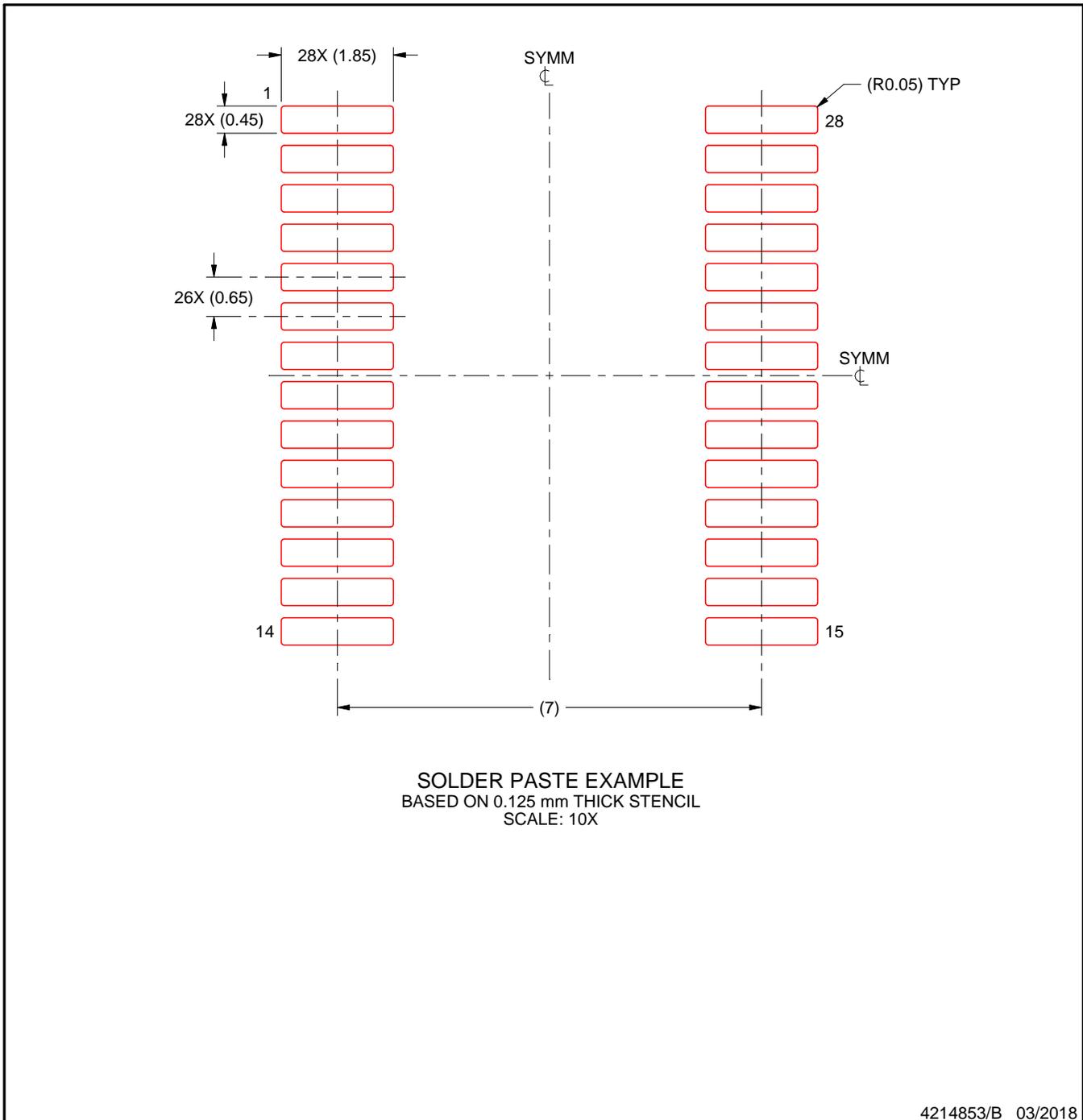
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

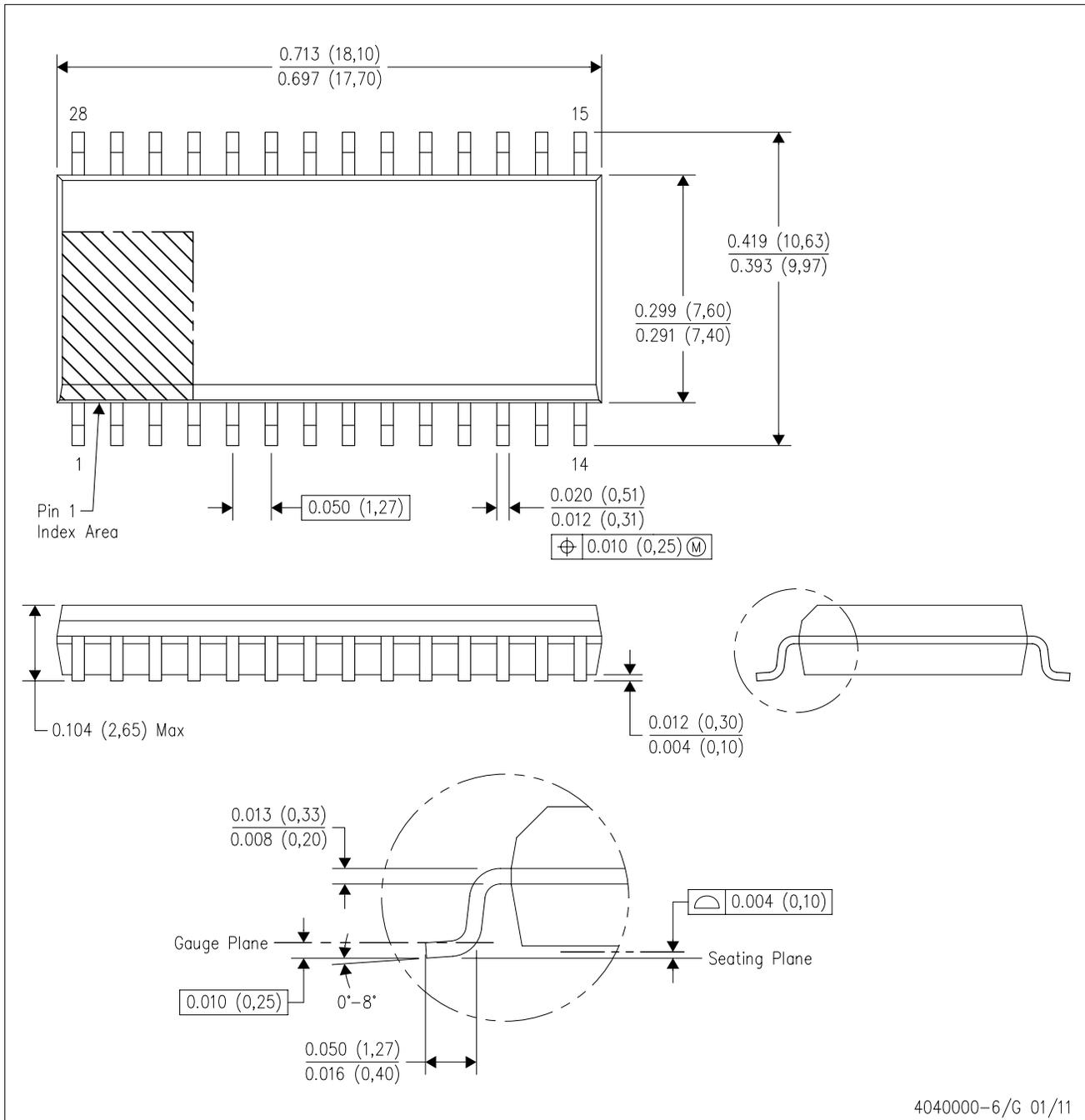


NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

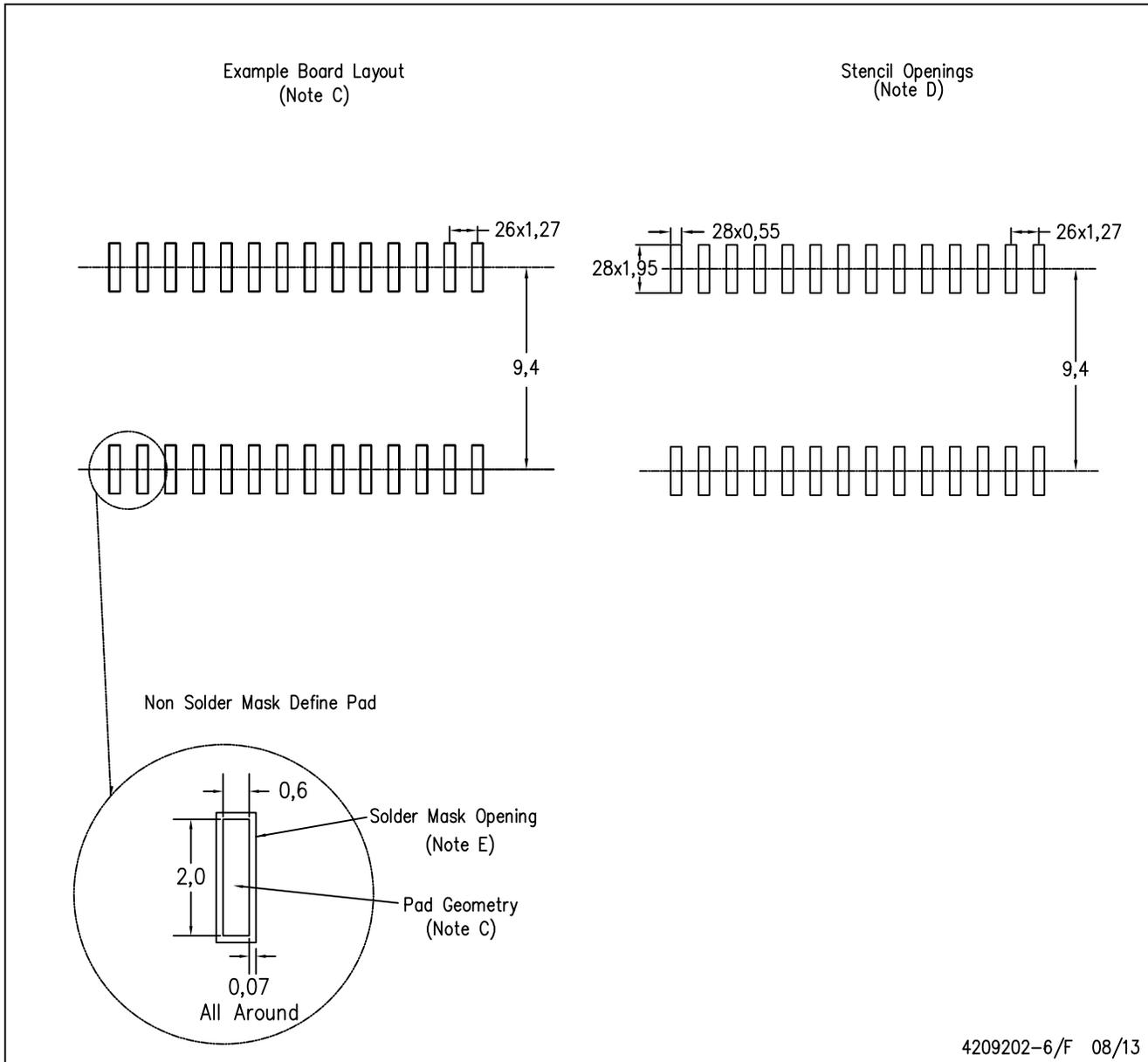


4040000-6/G 01/11

- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4209202-6/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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