

SN65HVD64 AISG® オン/オフ・キーイング同軸モデム・トランシーバ

1 特長

- 電源電圧範囲 : 3V ~ 5.5V
- 1.6V ~ 5.5V の独立したロジック電源
- レシーバ用の -15dBm ~ +5dBm のワイド入力ダイナミック・レンジ
- ドライバから同軸に供給される 0dBm ~ 6dBm の可変電力
- AISG® v2.0 および V3.0 をサポート
- 低消費電力のスタンバイ・モード
- RS-485 バス・アービトレーション用の方向制御出力
- 最大 115kbps のシグナリング・サポート
- アクティブ・バンドパス・フィルタ内蔵用の 2.176MHz の中心周波数
- 周囲温度範囲 : -40°C ~ 120°C
- 3mm × 3mm の 16 ピン VQFN パッケージ

2 アプリケーション

- AISG – アンテナ・ライン・デバイス用のインターフェイス
- タワー・マウント・アンプ (TMA)
- 一般的なモデム・インターフェイス

3 概要

SN65HVD64 トランシーバは、ロジック（ベースバンド）インターフェイスと、長い同軸メディアに適した周波数との間で信号を変調および復調し、無線機器間の有線データ転送を容易にします。

SN65HVD64 デバイスは、アンテナ・インターフェイス規格グループ v2.0 および V3.0 仕様の要件を満たすように設計された内蔵 AISG トランシーバです。

SN65HVD64 レシーバはアクティブなバンドパス・フィルタを内蔵しており、スプリアス周波数成分が存在する場合でも信号の復調を可能にします。このフィルタの中心周波数は 2.176MHz です。

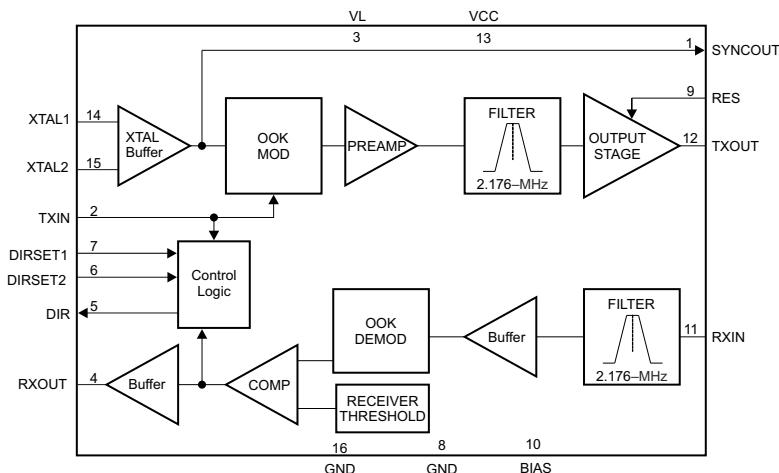
トランスマッタは、50Ω 同軸ケーブルに供給される 0dBm ~ 6dBm の可変出力電力レベルをサポートします。SN65HVD64 トランスマッタは、AISG 規格で規定されているスペクトラム放射要件に準拠しています。

方向制御出力により、RS-485 インターフェイスのバス・アービトレーションが容易になります。このデバイスには水晶用の発振器入力が内蔵されており、発振器への標準クロック入力も受け入れます。

製品情報

型番	パッケージ ⁽¹⁾ (1 ページ)	本体サイズ (公称)
SN65HVD64	VQFN (16)	3.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ブロック図



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Table of Contents

1 特長	1	8.3 Feature Description.....	14
2 アプリケーション	1	8.4 Device Functional Modes.....	15
3 概要	1	9 Application and Implementation	17
4 Revision History	2	9.1 Application Information.....	17
5 Pin Configuration and Functions	3	9.2 Typical Application.....	18
6 Specifications	4	10 Power Supply Recommendations	20
6.1 Absolute Maximum Ratings.....	4	11 Layout	21
6.2 ESD Ratings.....	4	11.1 Layout Guidelines.....	21
6.3 Recommended Operating Conditions.....	4	11.2 Layout Example.....	21
6.4 Thermal Information.....	5	12 Device and Documentation Support	22
6.5 Electrical Characteristics.....	6	12.1 Documentation Support.....	22
6.6 Switching Characteristics.....	7	12.2 Receiving Notification of Documentation Updates.....	22
6.7 Typical Characteristics.....	8	12.3 Support Resources.....	22
7 Parameter Measurement Information	11	12.4 Trademarks.....	22
8 Detailed Description	14	12.5 Electrostatic Discharge Caution.....	22
8.1 Overview.....	14	12.6 Glossary.....	22
8.2 Functional Block Diagram.....	14		

4 Revision History

DATE	REVISION	NOTES
October 2020	*	Initial release.

5 Pin Configuration and Functions

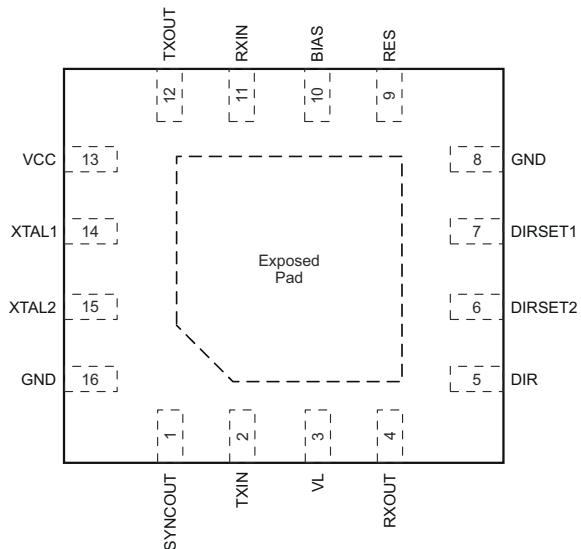


图 5-1. RGT Package, 16-Pin VQFN, Top View

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE	
BIAS	10	O	Bias voltage output for setting driver output power by external resistors
DIR	5	O	Direction control output signal for bus arbitration
DIRSET1	7	—	DIRSET1 and DIRSET2: Bits to set the duration of DIR
DIRSET2	6	—	DIRSET[2:1]: [L:L] = 9.6 kbps; [L:H] = 38.4 kbps; [H:L] = 115 kbps; [H:H] = standby mode
GND	8	—	Ground
	16		
RES	9	P	Input voltage to adjust driver output power that is set by external resistors from BIAS pin to GND
RXIN	11	I	Modulated input signal to the receiver
RXOUT	4	O	Digital data bit stream from receiver
SYNCOOUT	1	O	Open-drain output to synchronize other devices to the 4x-carrier oscillator at XTAL1 and XTAL2
TXIN	2	I	Digital data bit stream to driver
TXOUT	12	O	Modulated output signal from the driver
V _{CC}	13	P	Analog supply voltage for the device
VL	3	P	Logic supply voltage for the device
XTAL1	14	I/O	I/O pins of the crystal oscillator. Connect a 4 × f _C crystal between these pins or connect XTAL1 to an 8.704-MHz clock and connect XTAL2 to GND.
XTAL2	15		
EP	—	—	Exposed pad. Connection to ground plane is recommended for best thermal conduction.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} and VL	−0.5	6	V
Voltage at coax pins	−0.5	6	V
Voltage at logic pins	−0.3	$V_{VL} + 0.3$	V
Logic output current	−20	20	mA
TXOUT output current	Internally limited		
SYNCOUT output current	Internally limited		
Junction temperature, T_J	170		°C
Continuous total power dissipation	See the <i>Thermal Information</i>		°C
Storage temperature, T_{stg} (2)	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Applicable before the device is installed in the final product.

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000 V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
V_{CC}	3		5.5	V
V_L	1.6		5.5	V
$V_{I(pp)}$	Input signal amplitude at RXIN			1.12 Vpp
V_{IH}	High-level input voltage	70% V_L	V_L	V
		70% V_{CC}	V_{CC}	
V_{IL}	Low-level input voltage	0	30% V_L	V
		0	30% V_{CC}	
$1/t_{UI}$	9.6		115	kbps
f_{osc}	−30 ppm	8.704	30 ppm	MHz
Z_{LOAD}	Load impedance between TXOUT to RXIN			Ω
	Load impedance between RXIN and GND at f_C (channel)			Ω
R_1	Bias resistor between BIAS and RES			4.1 kΩ
R_2	Bias resistor between RES and GND			10 kΩ
R_{SYNC}	Pullup resistor between SYNCOUT and V_{CC}			1 kΩ
V_{RES}	0.7		1.5	V
C_C	Coupling capacitance between RXIN and coax (channel)			220 nF
C_{BIAS}	Capacitance between BIAS and GND			1 μF
T_A	Operating free-air temperature			−40 to 120 °C
T_J	Junction temperature			−40 to 125 °C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		VQFN	UNIT
		RGT 16 Pins	
R _{θJA}	Junction-to-ambient thermal resistance	49.4	°C/W
R _{θJCtop}	Junction-to-case (top) thermal resistance	64.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	22.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	22.9	°C/W
R _{θJCbot}	Junction-to-case (bottom) thermal resistance	25	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{CC}	Supply current	DIRSET1 = L DIRSET2 = H	TXIN = L (active)	28	33	mA
			TXIN = H (quiescent)	25	31	
			TXIN = 115 kbps, 50% duty cycle	27	33	
		DIRSET1 = H, DIRSET2 = H (standby)		12	17	
I_{VL}	Logic supply current	TXIN = H, RXIN = DC input		50		μA
PSRR	Receiver power supply rejection ratio	$V_{TXIN} = V_L$	45	60		dB
T_{SD_RISE}	Thermal shutdown rising		143	156	170	$^{\circ}C$
T_{SD_FALL}	Thermal shutdown falling		123	136	147	$^{\circ}C$
T_{SD_HYS}	Thermal shutdown hysteresis		18	20	23	$^{\circ}C$
LOGIC PINS						
V_{OH}	High-level logic output voltage (RXOUT, DIR)	$I_{OH} = -4 \text{ mA for } V_L > 2.4 \text{ V},$ $I_{OH} = -2 \text{ mA for } V_L < 2.4 \text{ V}$	90% V_{VL}			V
V_{OL}	Low-level logic output voltage (RXOUT, DIR)	$I_{OL} = 4 \text{ mA for } V_L > 2.4 \text{ V},$ $I_{OL} = 2 \text{ mA for } V_L < 2.4 \text{ V}$		10% V_{VL}		V
COAX DRIVER						
$V_{O(PP)}$	Peak-to-peak output voltage at device pin TXOUT (see FIG 7-1)	$V_{RES} = 1.5 \text{ V (Maximum setting)}$	2.24	2.5		V_{PP}
		$V_{RES} = 0.7 \text{ V (Minimum setting)}$		1.17	1.3	
$V_{O(PP)}$	Peak-to-peak voltage at coax out (see FIG 7-1)	$V_{RES} = 1.5 \text{ V}$	5	6		dBm
		$V_{RES} = 0.7 \text{ V}$		-0.6	0.3	
$V_{O(OFF)}$	Off-state output voltage	At TXOUT		1		mVpp
		At coax out		-60		dBm
	Output emissions	Coupled to coaxial cable with characteristic impedance of 50Ω , as shown in FIG 6-1 ⁽¹⁾ ⁽²⁾				N/A
f_O	Output frequency		2.176			MHz
Δf	Output frequency variation		-100	100		ppm
Z_O	Output impedance	At 100 kHz	0.03			Ω
		At 10 MHz	3.5			
$ I_{os} $	Short-circuit output current	TXOUT is also protected by a thermal shutdown circuit during short-circuit faults	300	450		mA
COAX RECEIVER						
V_{IT}	Input threshold	$f_{IN} = 2.176 \text{ MHz}$	79	112	158	mVPP
			-18	-15	-12	dBm
Z_{IN}	Input impedance	$f = f_O$	11	21		k Ω
RECEIVER FILTER						
f_{PB}	Passband	$VRXIN = 1.12VP_P$	1.1	4.17		MHz
f_{REJ}	Receiver rejection range	2.176-MHz carrier amplitude of 112.4 mV_{PP} , frequency band of spurious components with 800 mVPP allowed.	1.1	4.17		MHz
$t_{noise\ filter}$	Receiver noise filter time (slow bit rate)	DIRSET for 9.6 kbps	4			μs
	Receiver noise filter time (fast bit rate)	DIRSET for > 9.6 kbps	2			μs
XTAL AND SYNC						
I_I	Input leakage current	$XTAL1, XTAL2, 0V < V_{IN} < V_{CC}$	-15	15		μA
V_{OL}	Output low voltage	SYNCOUT, with 1-k Ω resistor from SYNCOUT to V_{CC}		0.4		V

(1) Specified by design with a recommended 470-pF capacitor between RXIN and GND. Measurements above 150 MHz are determined by setup.

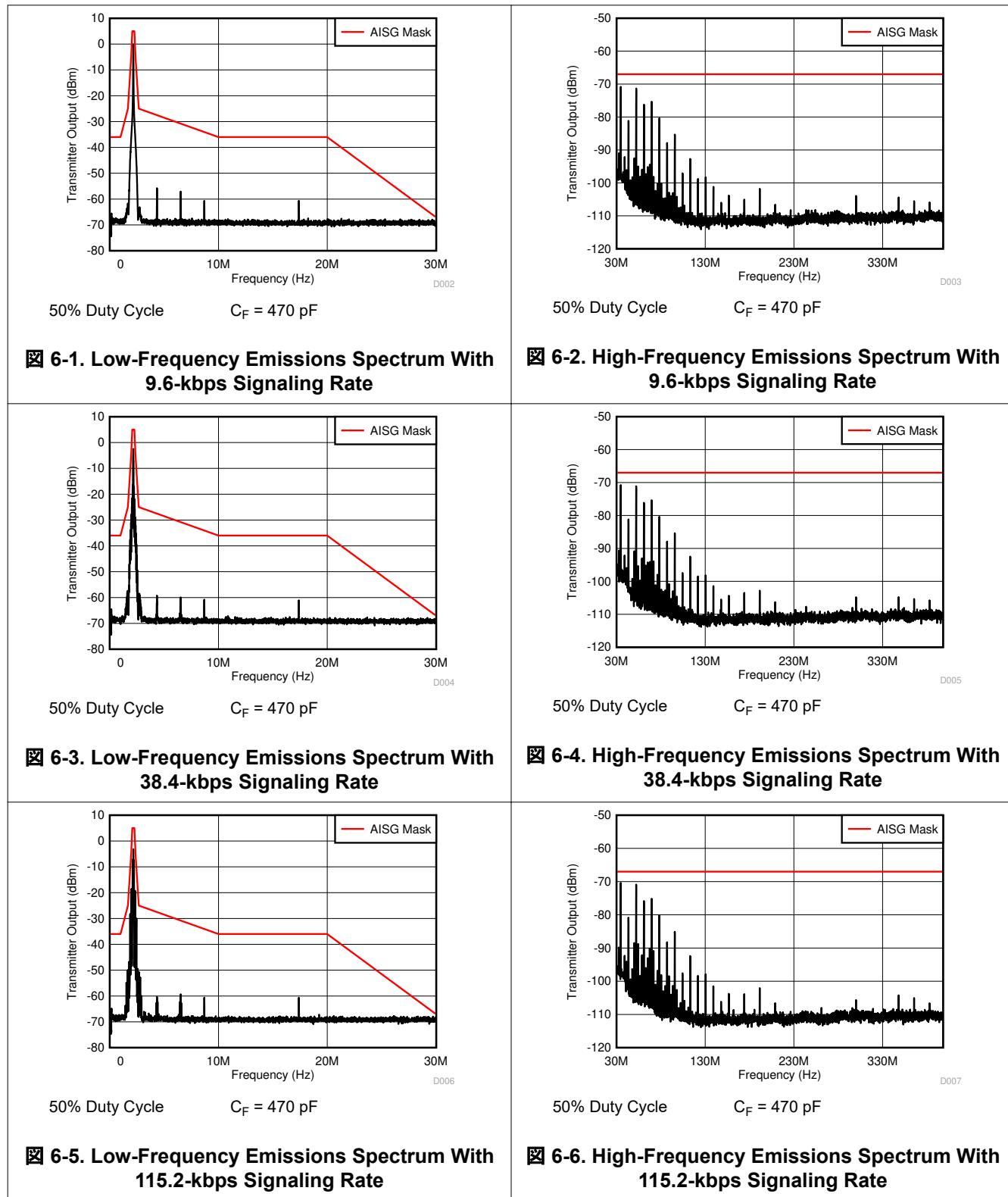
(2) Conforms to AISG spectrum emissions mask, 3GPP TS 25.461, see [FIG 7-3](#).

6.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pAQ}, t_{pQA}	Coax driver propagation delay See 图 7-1			5	μs
t_r, t_f	Coax receiver output rise/fall time $C_L = 15 \text{ pF}, R_L = 1 \text{ kΩ}$; see 图 7-1			20	ns
t_{PHL}, t_{PLH}	Receiver propagation delay See 图 7-2		5.5	11	μs
Coax receiver output duty cycle	$V_{RXIN(ON)} = 630 \text{ mVpp}, V_{RXIN(OFF)} < 5 \text{ mVpp}$, 50% duty cycle	40%	60%		
	$V_{RXIN(ON)} = 200 \text{ mVpp}, V_{RXIN(OFF)} < 5 \text{ mVpp}$, 50% duty cycle	40%	60%		
t_{DIR}	Direction control active duration DIRSET2 = GND or OPEN, DIRSET1 = GND or OPEN		1667		μs
	DIRSET2 = GND, DIRSET1 = VL		417		
	DIRSET2 = VL, DIRSET1 = VL		137		
$t_{DIRSKEW}$	Direction control skew (DIR to RXOUT)	270			ns
t_{dis}	Standby disable delay 300 mV _{PP} at 2.176 MHz on RXIN	2			ms
t_{en}	Standby enable delay 300 mV _{PP} at 2.176 MHz on RXIN	2			ms

6.7 Typical Characteristics



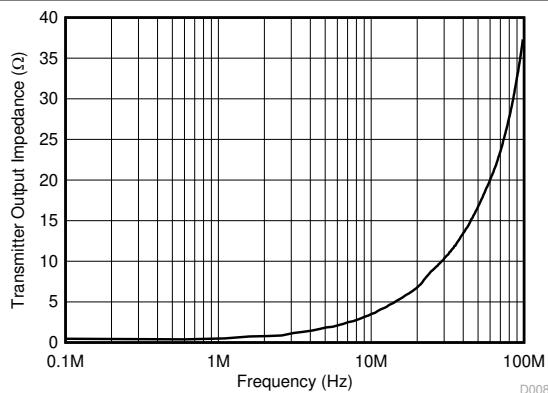


図 6-7. Transmitter Output Impedance

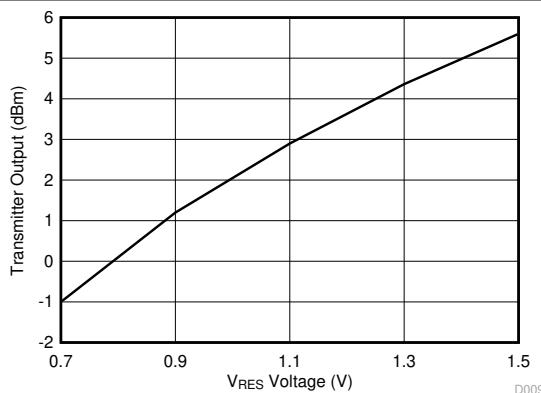
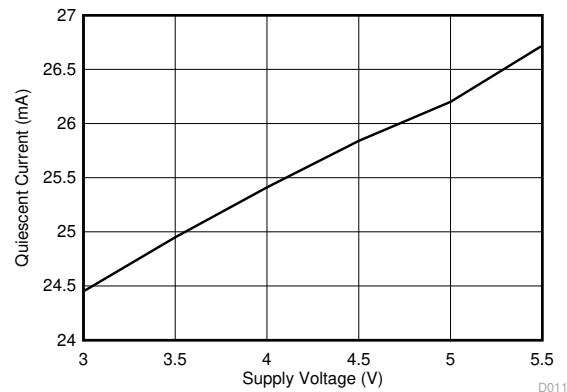


図 6-8. Transmit Power Adjustment



TXIN = VL

図 6-9. Supply Current vs Supply Voltage While Transmitting

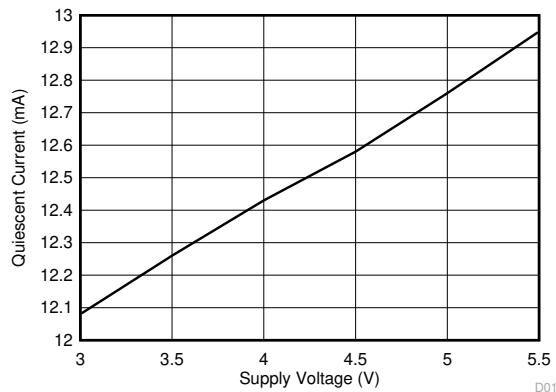


図 6-10. Supply Current vs Supply Voltage in Standby Mode

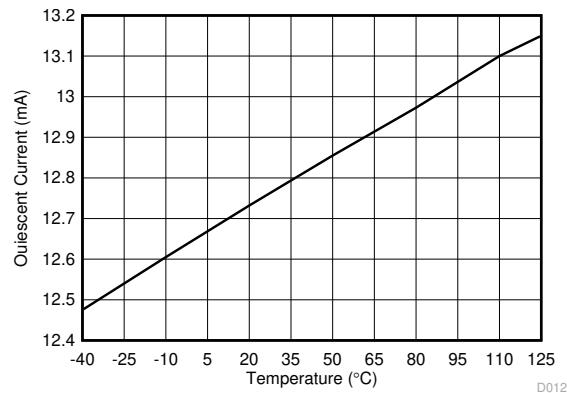


図 6-11. Supply Current vs Temperature in Standby Mode

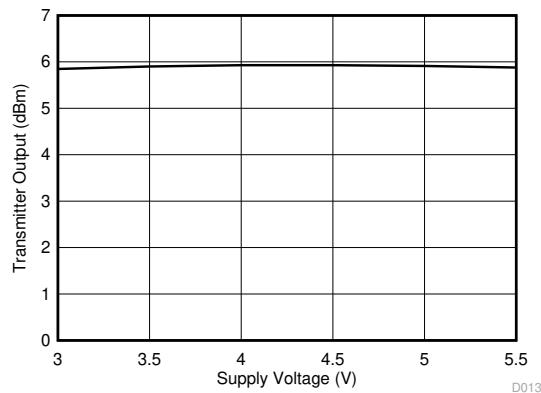


図 6-12. Transmitter Output Power vs Supply Voltage

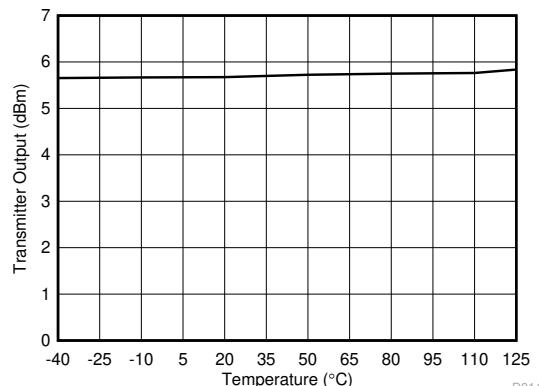


图 6-13. Transmitter Output Power vs Temperature

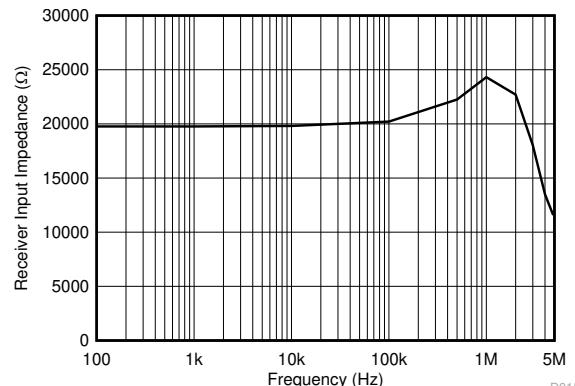


图 6-14. Receiver Input Impedance vs Frequency

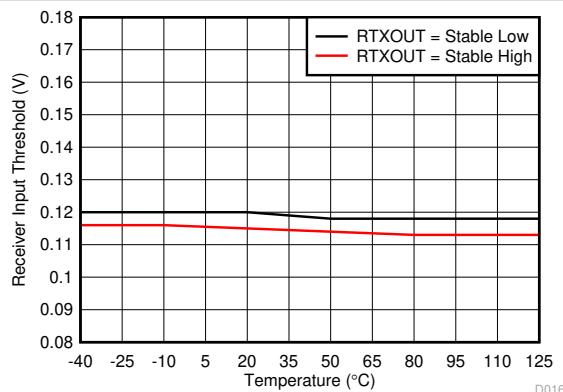


图 6-15. Receiver Input Threshold vs Temperature

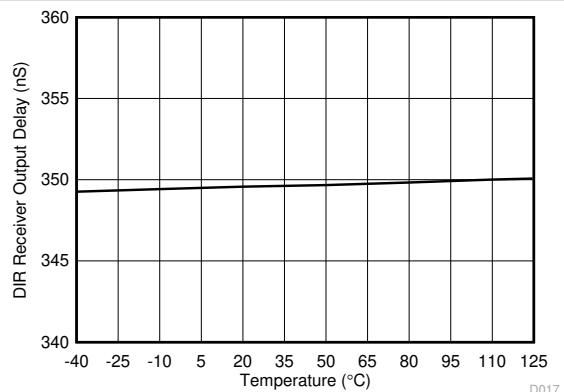


图 6-16. DIR Output Delay vs Temperature

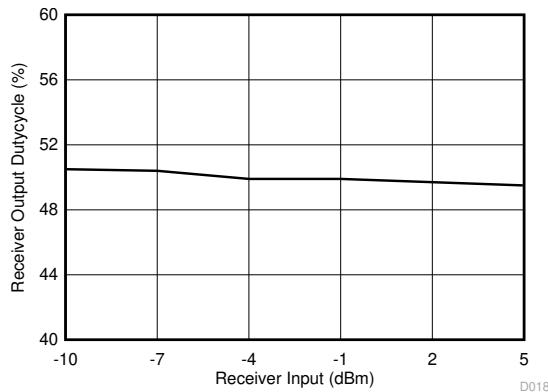


图 6-17. Receiver Duty Cycle With 9.6 kbps Signaling Rate

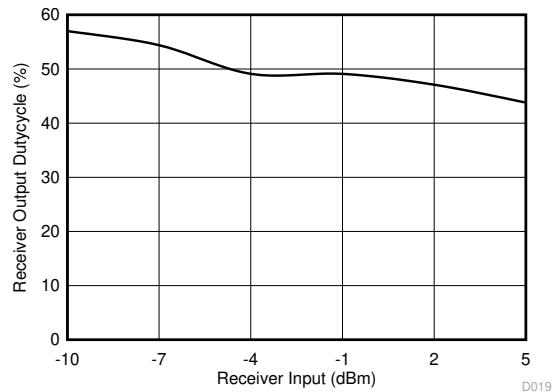


图 6-18. Receiver Duty Cycle With 115.2 kbps Signaling Rate

7 Parameter Measurement Information

Signal generator rate is 115 kbps, 50% duty cycle. Rise and fall times are less than 6 ns, and nominal output levels are 0 V and 3 V. Coupling capacitor, C_c , is 220 nF.

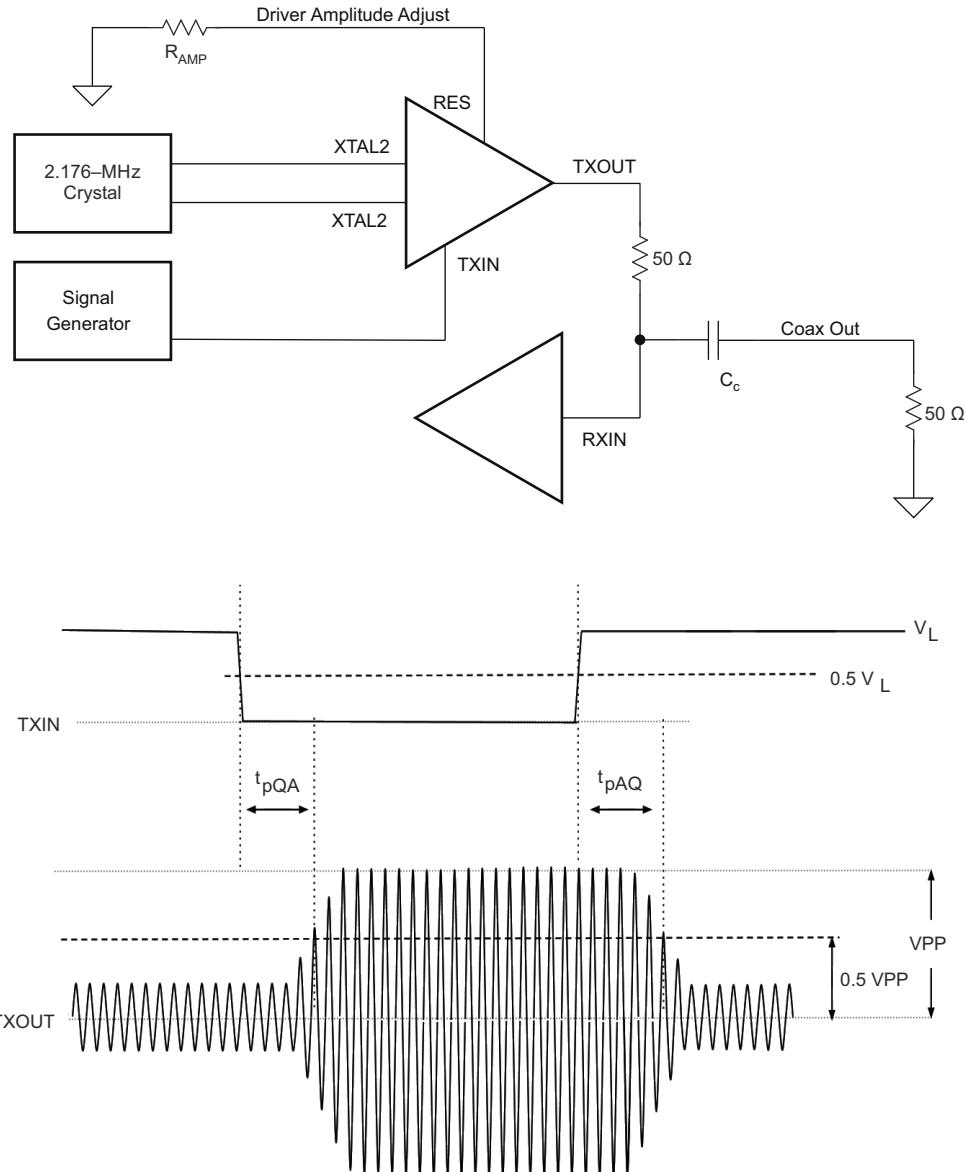


图 7-1. Measurement of Modem Driver Output Voltage With 50- Ω Loads

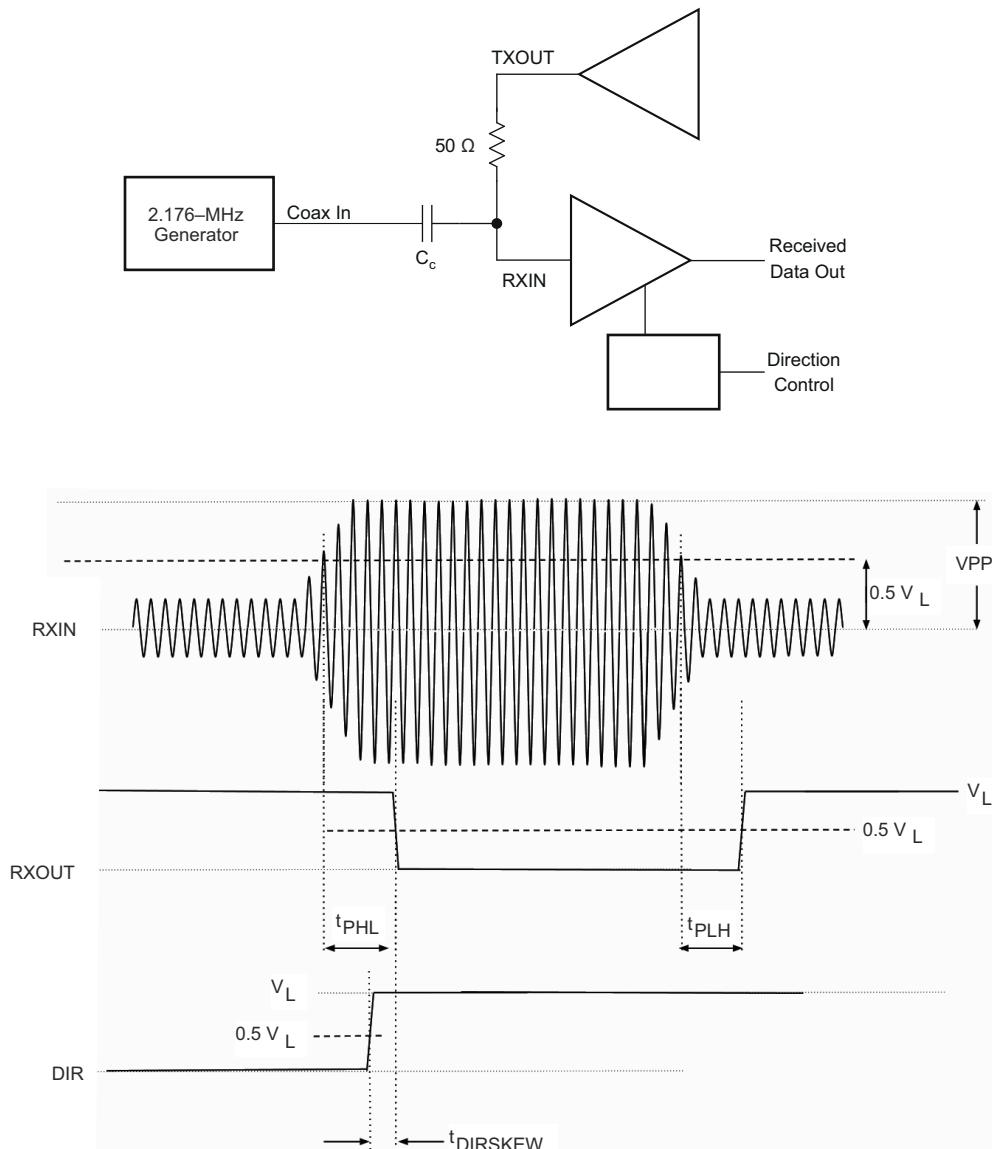
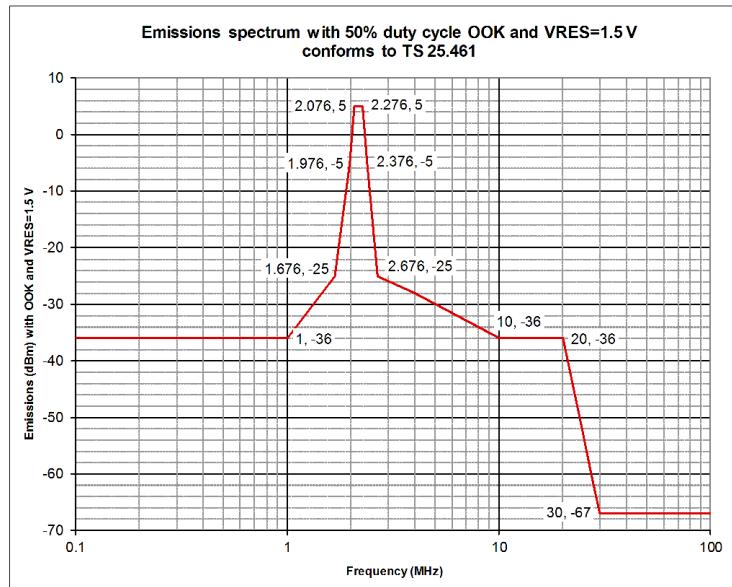


图 7-2. Measurement of Modem Receiver Propagation Delays



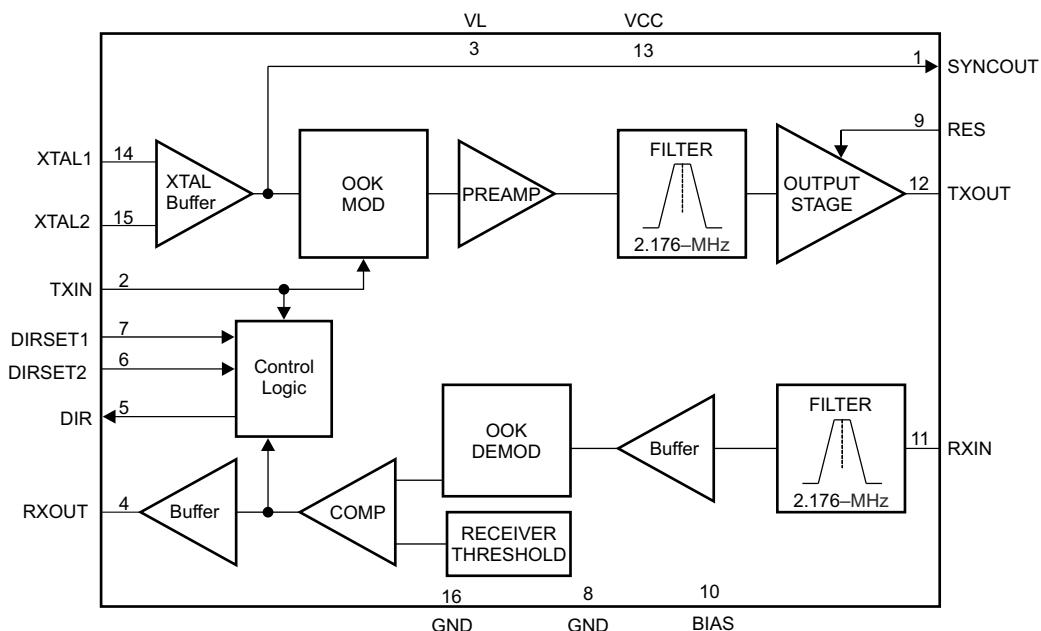
 **7-3. AISG Emissions Template**

8 Detailed Description

8.1 Overview

The SN65HVD64 transceiver modulates and demodulates signals between the logic (baseband) and a frequency suitable for long coaxial media. The SN65HVD64 device is an integrated AISG transceiver designed to meet the requirements of the Antenna Interface Standards Group v2.0 and v3.0 specification. The SN65HVD64 receiver integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176-MHz center frequency. The transmitter supports adjustable output power levels from 0 dBm to 6 dBm delivered to the 50- Ω coax cable. The SN65HVD64 transmitter is compliant with the spectrum emission requirement provided by the AISG standard. A direction control output facilitates bus arbitration for an RS-485 interface. This device integrates an oscillator input for a crystal, and also accepts standard clock inputs to the oscillator.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Coaxial Interface

The SN65HVD64 transceiver enables the transfer of data between radio equipment by modulating baseband data to a carrier frequency of 2.176 MHz (per the AISG standard). The transmitter output amplitude can be configured from 0 dBm to 6 dBm in order to communicate over a variety of different links, and the output emissions spectrum is designed to be compliant to AISG limits. The receiver features an active bandpass filter circuit that helps to separate the carrier frequency data from other spurious frequency components.

8.3.2 Reference Input

The 2.176-MHz modulation frequency is derived from an input reference that is nominally 8.704 MHz. The input reference can come either from a crystal or from an oscillator circuit with a tolerance of up to 30 ppm.

8.3.3 RS-485 Direction Control

To facilitate bus arbitration of an RS-485 interface, the SN65HVD64 provides a direction control output that can be used to control the enable/disable controls of an RS-485 transceiver. The direction control output automatically toggles based on activity present on the coaxial input interface, and has an adjustable time constant (controlled by the DIRSET1 and DIRSET2 pins) in order to accommodate various signaling rates.

8.4 Device Functional Modes

If DIRSET1 and DIRSET2 are in a logic high state, the device will be in standby mode. While in standby mode, the receiver functions normally, detecting carrier frequency activity on the RXIN pin and setting the RXOUT state. The transmitter circuits are not active in standby mode, thus the TXOUT pin is idle regardless of the logic state of TXIN. The supply current in standby mode is significantly reduced, allowing power savings when the node is not transmitting.

When not in standby mode, the default power-on state is idle. When in idle mode, RXOUT is high, and TXOUT is quiet. The device transitions to receive mode when a valid modulated signal is detected on the RXIN line or the device transitions to transmit mode when TXIN goes low. The device stays in either receive or transmit mode until DIR time-out (nominal 16 bit times) after the last activity on RXOUT or TXIN.

When in receive mode:

- RXOUT responds to all valid modulated signals on RXIN, whether from the local transmitter, a remote transmitter, or long noise burst.
- TXOUT responds to TXIN, generating 2.176-MHz signals on TXOUT when TXIN is low, and TXOUT is quiet when TXIN is high. (In normal operation, TXIN is expected to remain high when the device is in receive mode.)
- The device stays in receive mode until 16 bit times after the last rising edge on RXOUT, caused by valid modulated signal on the RXIN line.

When in transmit mode:

- RXOUT stays high, regardless of the input signal on RXIN.
- TXOUT responds to TXIN, generating 2.176-MHz signals on TXOUT when TXIN is low, and TXOUT is quiet when TXIN is high.
- The device stays in transmit mode until 16 bit times after TXIN goes high.

表 8-1 shows the driver functions. 表 8-2 shows the receiver functions. 図 8-1 shows the transitions between each state.

表 8-1. Driver Function Table

TXIN ⁽¹⁾	[DIRSET1, DIRSET2]	TXOUT	COMMENT
H	[L,L], [L,H] or [H,L]	< 1 mV _{PP} at 2.176 MHz	Driver not active
L		V _{OPP} at 2.176 MHz	Driver active
X	[H,H]	< 1 mV _{PP} at 2.176 MHz	Standby mode

(1) H = High, L = Low, X = Indeterminate

表 8-2. Receiver and DIR Function Table

RXIN ⁽¹⁾	RXOUT	DIR	COMMENT (see 図 8-1)
IDLE mode (not transmitting or receiving)			
< V _{IT} at 2.176 MHz for longer than DIR time-out	H	L	No outgoing or incoming signal
RECEIVE mode (not already transmitting)			
< V _{IT} at 2.176 MHz for less than t _{DIR} time-out	H	H	Incoming 1 bit, DIR stays HIGH for DIR time-out
> V _{IT} at 2.176 MHz for longer than t _{noise filter}	L	H	Incoming 0 bit, DIR output is HIGH
TRANSMIT mode (not already receiving)			
X	H	L	Outgoing message, DIR stays LOW for DIR time-out

(1) H = High, L = Low, X = Indeterminate

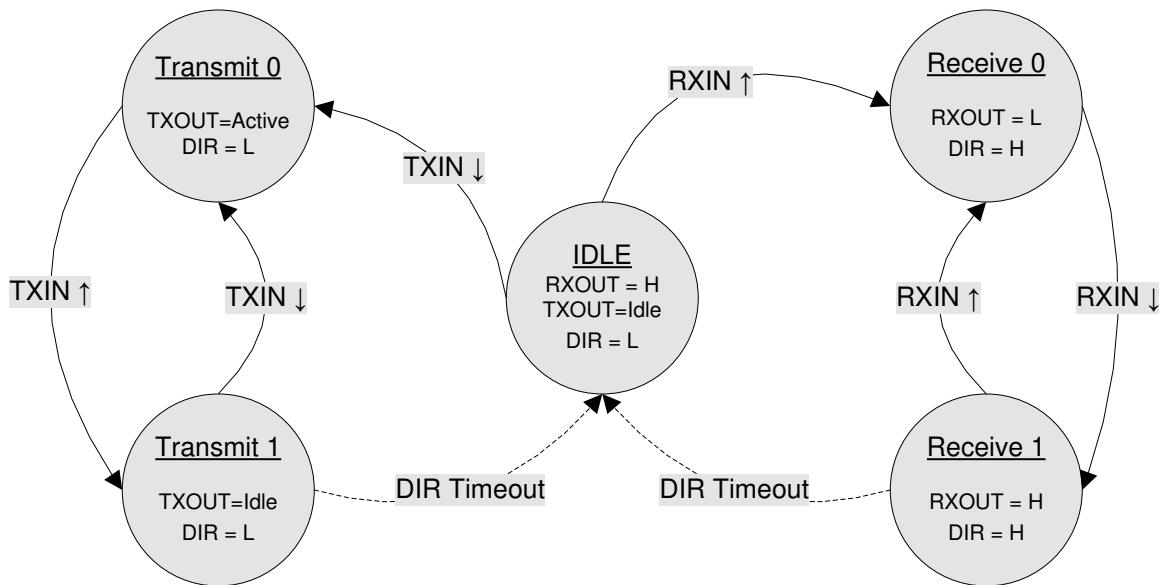


图 8-1. State Transition Diagram

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Driver Amplitude Adjust

The SN65HVD64 device can provide up to 2.5 V of peak-to-peak output signal at the TXOUT pin to compensate for potential loss within the external filter, cable, connections, and termination. External resistors are used to set the amplitude of the modulated driver output signal. Resistors connected across RES and BIAS set the output amplitude. The maximum peak-to-peak voltage at TXOUT is 2.5 V, corresponding to 6 dBm on the coaxial cable. The TXOUT voltage level can be adjusted by choice of resistors to set the voltage at the RES pin according to [式1](#):

$$V_{TXOUT} (V_{PP}) = (2.5 V_{PP} \times V_{RES} (V)) / 1.5 V V_{RES} (V) = 1.5 V \times R2 / (R1 + R2) V_{TXOUT} (V_{PP}) = 2.5 V_{PP} \times R2 / (R1 + R2) \quad (1)$$

The voltage at the RES pin should be from 0.7 V to 1.5 V. Connect RES directly to the BIAS ($R1 = 0 \Omega$) for maximum output level of 2.5 V_{PP}. This gives a minimum voltage level at TXOUT of 1.2 V_{PP}, corresponding to about 0 dBm at the coaxial cable. A 1- μ F capacitor should be connected between the BIAS pin and GND. To obtain a nominal power level of 3 dBm at the feeder cable as the AISG standard requires, use $R1 = 4.1 \text{ k}\Omega$ and $R2 = 10 \text{ k}\Omega$ that provide 1.78 V_{PP} at TXOUT.

9.1.2 Direction Control

In many applications the mast-top modem that receives data from the base distributes the received data through an RS-485 network to several mast-top devices. When the mast-top modem receives the first logic 0 bit (active modulated signal) it takes control of the mast-top RS-485 network by asserting the direction control signal. The duration of the direction control assertion should be optimized to pass a complete message of length B bits at the known signaling rate ($1/t_{BIT}$) before relinquishing control of the mast-top RS-485 network. For example, if the messages are 10 bits in length ($B=10$) and the signaling rate is 9600 bits per second ($t_{BIT} = 0.104 \text{ ms}$) then a positive pulse of duration 1.7 ms is sufficient (with margin to allow for network propagation delays) to enable the mast-top RS-485 drivers to distribute each received message. [图 9-1](#) shows the assertion of direction control.

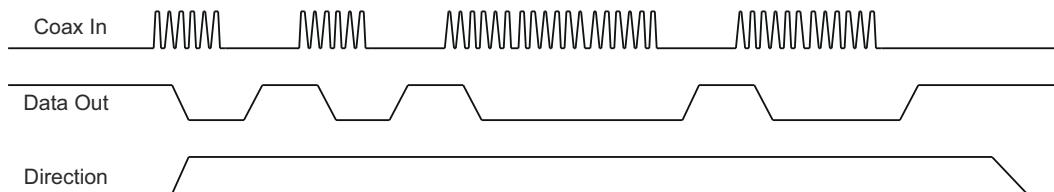


图 9-1. Assertion of Direction Control

9.1.3 Direction Control Time Constant

The time constant for the direction control function can be set by the control mode pins, DIRSET1 and DIRSET2. These pins should be set to correspond to the desired data rate. With no external connections to the control mode pins, the internal time constant is set to the maximum value, corresponding to the minimum data rate.

9.1.4 Conversion Between dBm and Peak-to-Peak Voltage

$$dBm = 20 \times \text{LOG10} [\text{Volts-pp} / \text{SQRT}(0.008 \times Z_0)] = 20 \times \text{LOG10} [\text{VPP} / 0.63] \text{ for } Z_0 = 50 \Omega \quad (2)$$

$$\text{VPP} = \text{SQRT}(0.008 \times Z_0) \times 10^{(dBm/20)} = 0.63 \times 10^{(dBm/20)} \text{ for } Z_0 = 50 \Omega \quad (3)$$

表 9-1 shows conversions between dBm and peak-to-peak voltage with a 50- Ω load, for various levels of interest including reference levels from the 3GPP TS 25.461 Technical Specification.

表 9-1. Conversions Between dBm and Peak-to-Peak Voltage

SIGNAL ON COAX	dBm	V _{PP}
Maximum Driver ON Signal	5	1.12
Nominal Driver ON Signal	3	0.89
Minimum Driver ON Signal	1	0.71
AISG Maximum Receiver Threshold	-12	0.16
Nominal Receiver Threshold	-15	0.11
Minimum Receiver Threshold	-18	0.08
Maximum Driver OFF Signal	-40	0.006

9.2 Typical Application

The AISG On-Off Keying (OOK) interface allows for command, control, and diagnostic information to be communicated between a base station and the corresponding tower-mounted antennae. 图 9-2 shows a typical application.

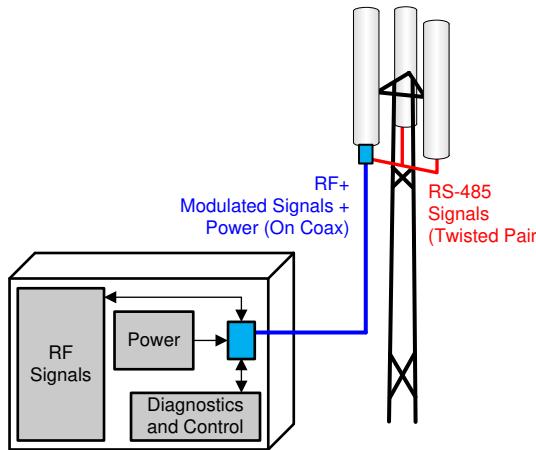


图 9-2. Typical AISG Application

9.2.1 Design Requirements

An AISG transceiver is used to convert between digital logic-level signals and RF signals. The AISG standard requires an RF carrier frequency of 2.176 MHz with 100-ppm accuracy. The output signal of the driver, when active, should be from 1 dBm to 5 dBm. The receiver must be designed such that the input threshold is from -18 dBm to -12 dBm.

9.2.2 Detailed Design Procedure

To ensure accuracy of the carrier frequency, an input reference frequency equal to four times the carrier (that is, 8.704 MHz) should be connected to the XTAL1 or XTAL2 inputs. This signal can come from a crystal (connected between XTAL1 and XTAL2) or from a PLL/clock generator circuit (connected to XTAL1 with XTAL2 grounded). The frequency accuracy must be within 100 ppm.

The driver output power level of the SN65HVD64 device can be adjusted through use of the RES pin. To align with AISG requirements, a nominal power level of 3 dBm should be configured by connecting a 4.1-k Ω resistor between RES and BIAS and a 10-k Ω resistor between RES and GND. [图 9-3](#) shows an example schematic.

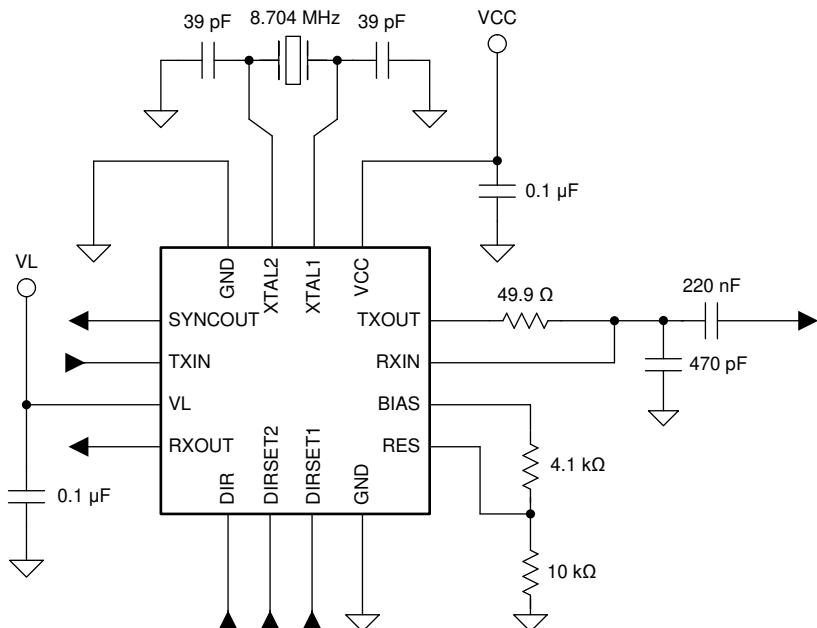


图 9-3. SN65HVD64 Schematic

9.2.3 Application Curve

[图 9-4](#) shows the application curve for the SN65HVD64 device.

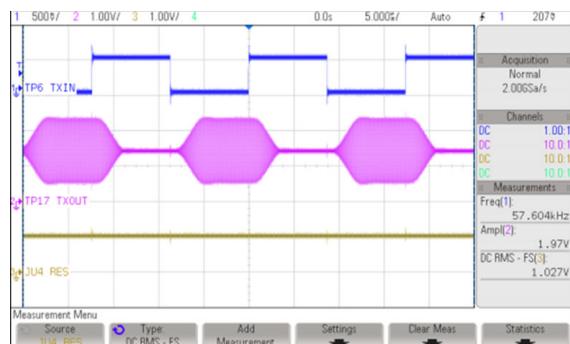


图 9-4. SN65HVD64 Application Curve

10 Power Supply Recommendations

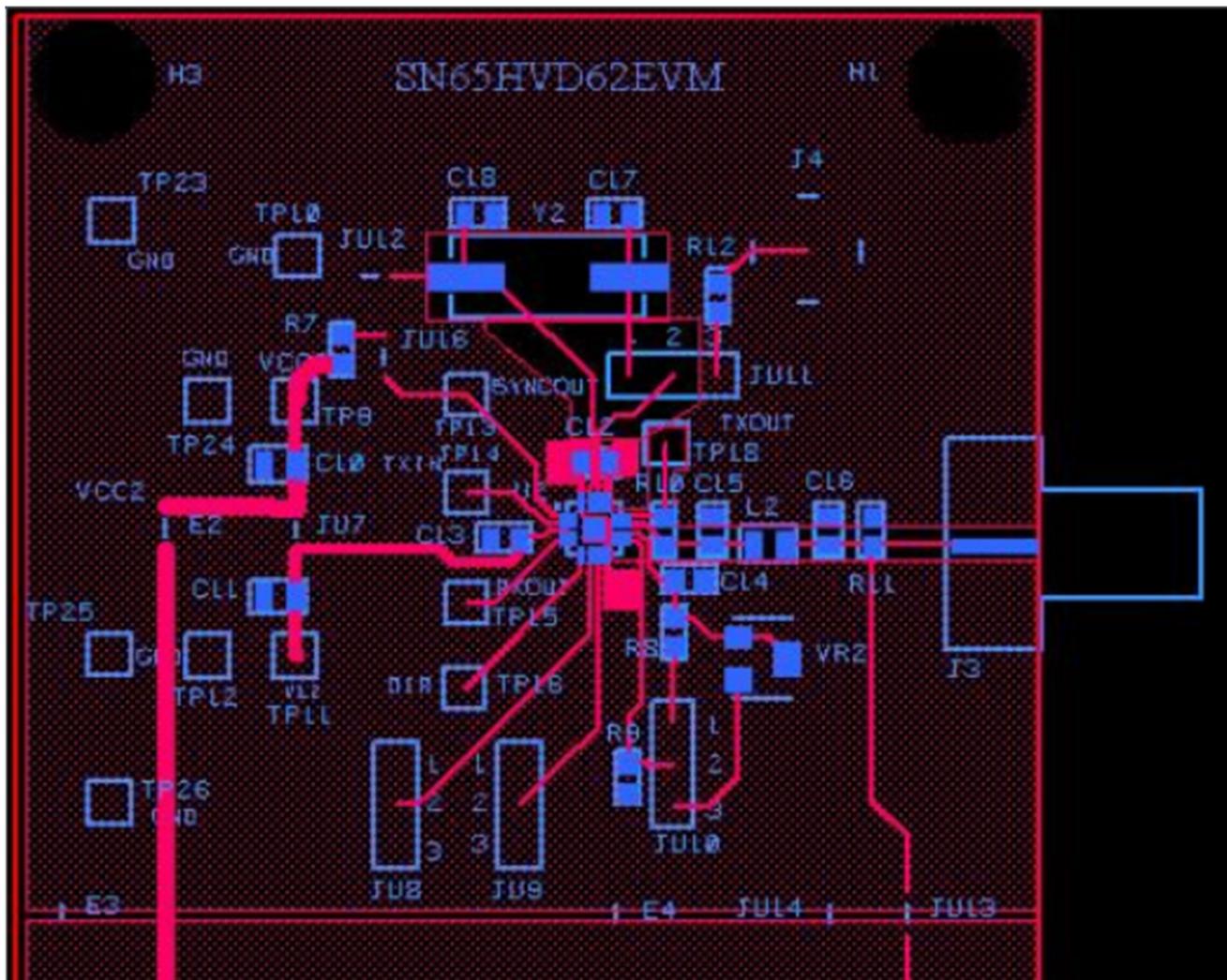
The SN65HVD64 device has two power supply pins: V_{CC} , which provides power to the analog circuitry, and VL , which is a logic supply. V_{CC} should be operated from 3 V to 5.5 V, while VL can range from 1.6 V to 5.5 V to interface to different logic levels. Power supply decoupling capacitances of at least 0.1 μ F should be placed as close as possible to each power supply pin.

11 Layout

11.1 Layout Guidelines

Best practices for high-speed PCB design should be observed because the coax interface to the SN65HVD64 device operates at RF. The RF signaling traces should have a controlled characteristic impedance that is well-matched to the coaxial line. A continuous reference plane should be used to avoid impedance discontinuities. Power and ground distribution should be done through planes rather than traces to decrease series resistance and increase the effective decoupling capacitance on the power rails.

11.2 Layout Example



11-1. SN65HVD64 Layout

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD64RGTR	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-40 to 120	HVD64
SN65HVD64RGTR.A	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 120	HVD64
SN65HVD64RGTR.B	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 120	HVD64

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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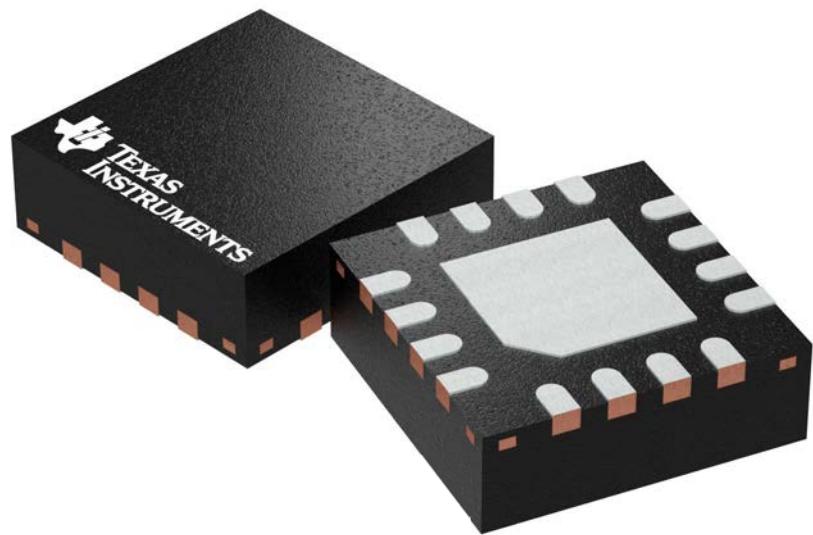
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/I

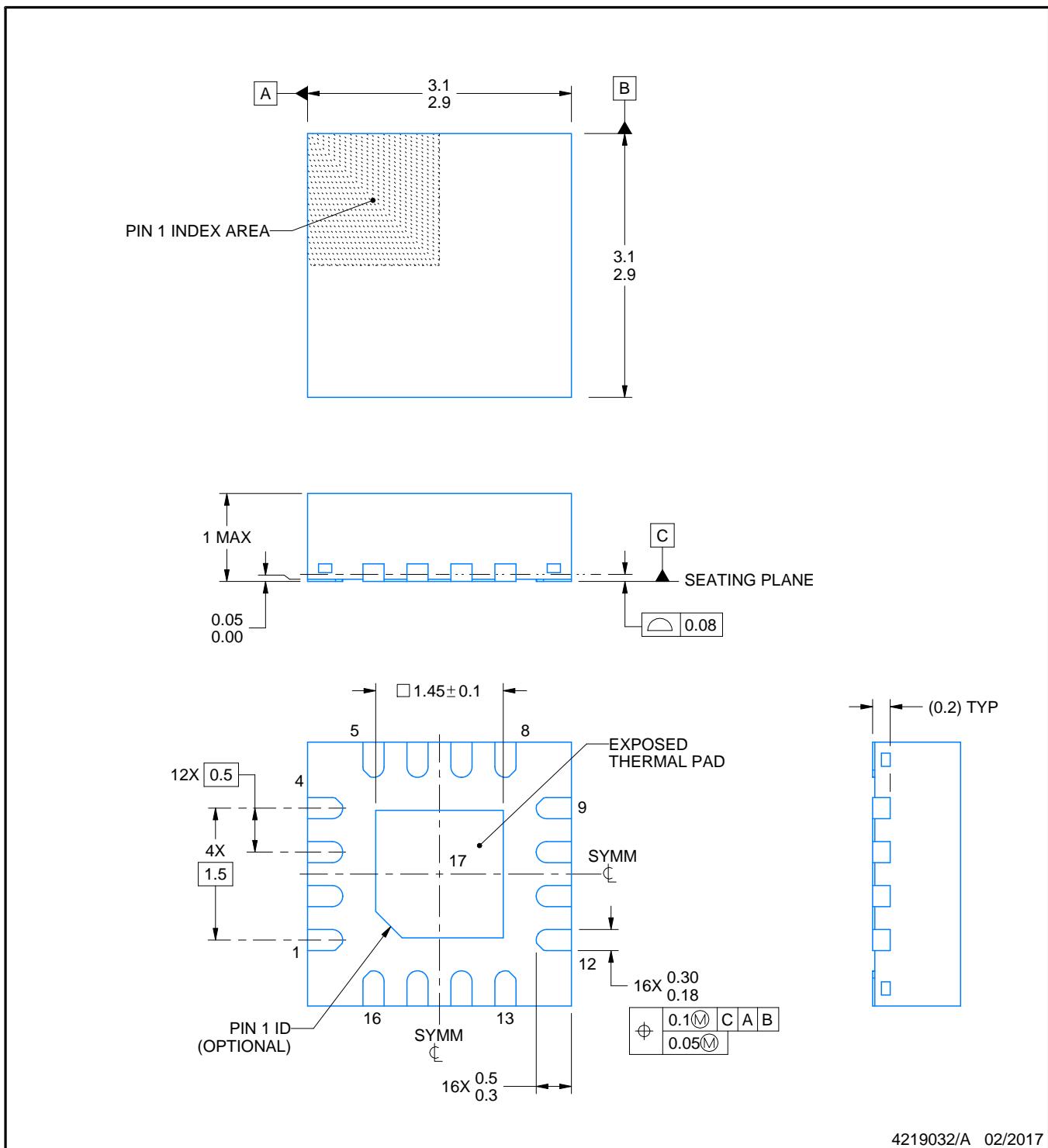
RGT0016A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219032/A 02/2017

NOTES:

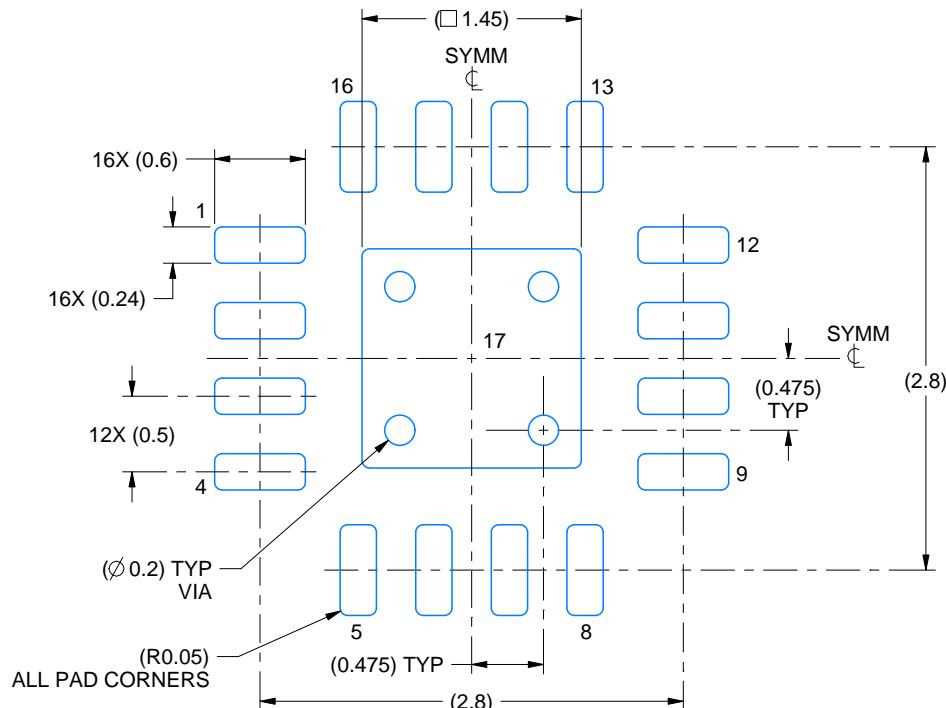
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220

EXAMPLE BOARD LAYOUT

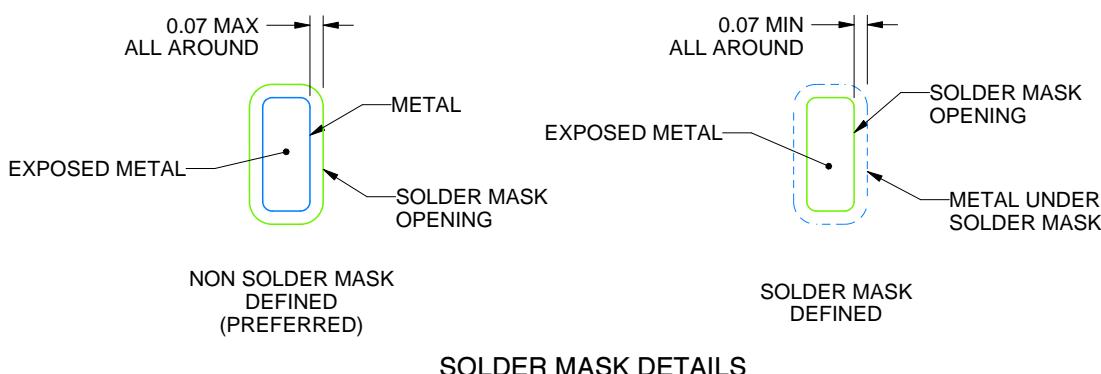
RGT0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

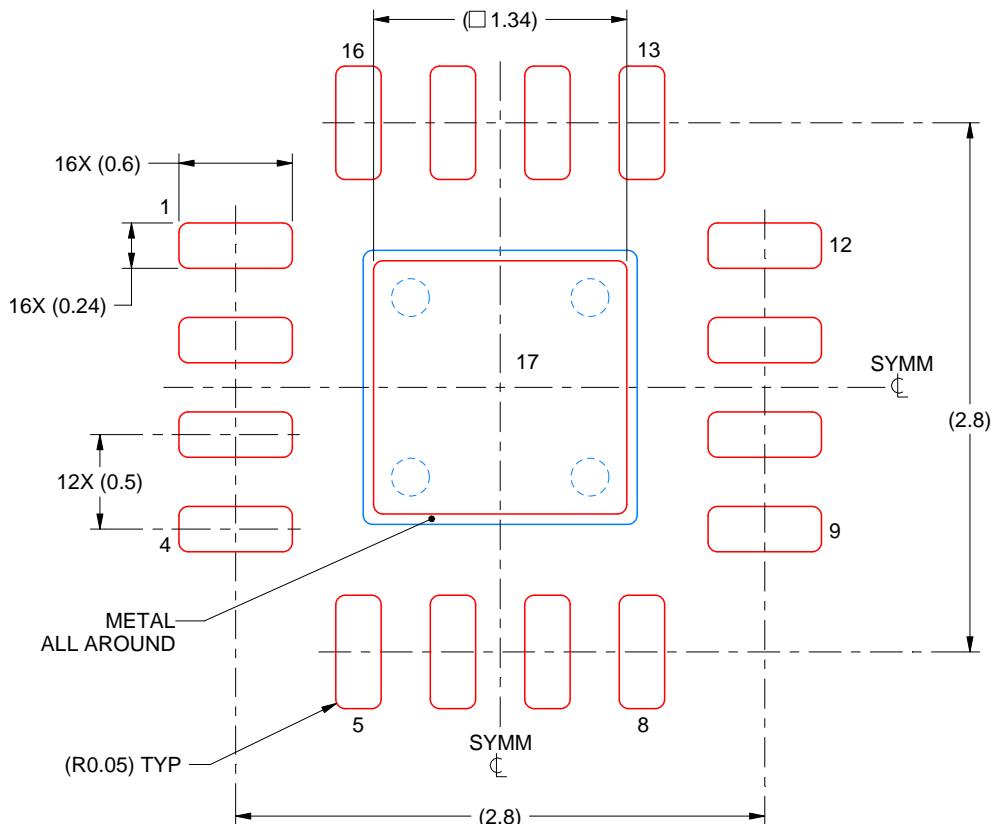
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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