- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation

- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C

- High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})

- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

SN54ABT241 . . . J OR W PACKAGE
SN74ABT241A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	20	V_{CC}
1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

SN54ABT241 . . . FK PACKAGE
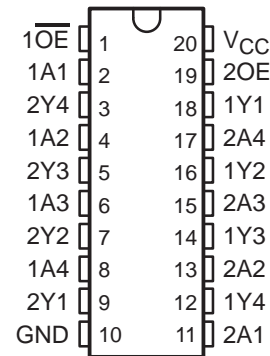**(TOP VIEW)**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT240, SN74ABT240A, and 'ABT244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs.
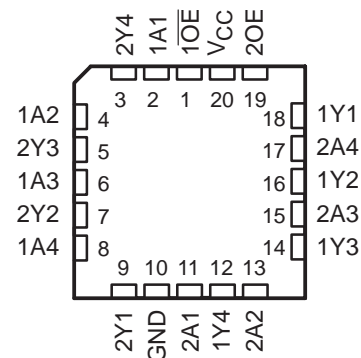
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT241A is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

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SN54ABT241, SN74ABT241A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

FUNCTION TABLES

INPUTS		OUTPUT
1OE	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†
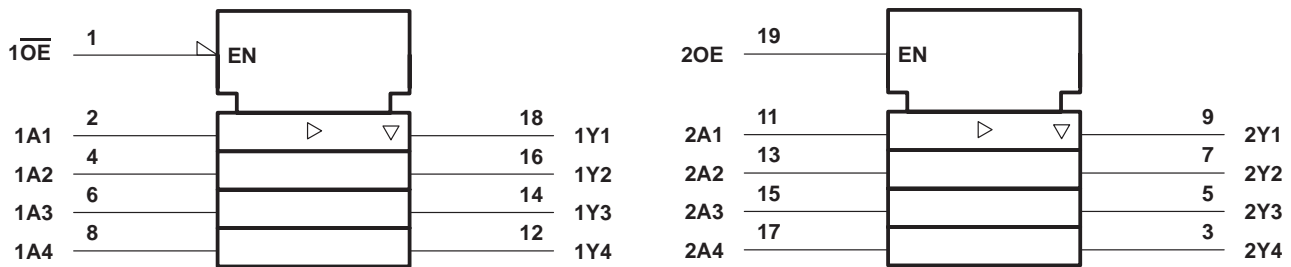
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
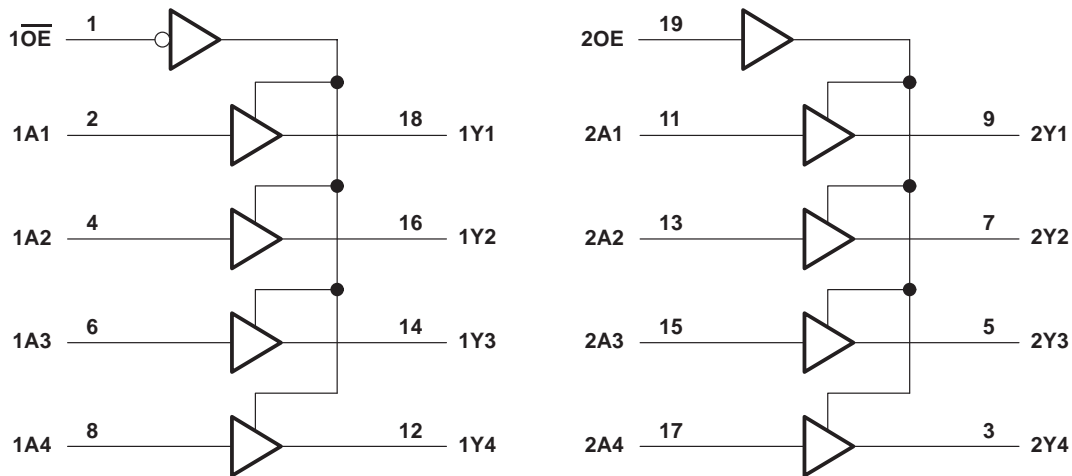Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT241 .... 96 mA
　　　　　　　　　　　　　　　　　　　　　　 SN74ABT241A .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 115°C/W
　　　　　　　　　　　　　　　　　　　　　　　　　DW package .... 97°C/W
　　　　　　　　　　　　　　　　　　　　　　　　　N package .... 67°C/W
　　　　　　　　　　　　　　　　　　　　　　　　　PW package .... 128°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT241		SN74ABT241A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$			SN54ABT241		SN74ABT241A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
	$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
	$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
		$I_{OH} = -32$ mA	2*					2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
		$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}				100						mV
I_I	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			10		10		10	µA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			−10		−10		−10	µA
I_{off}	$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O‡	$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}§	Data inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND — Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			0.05		0.05		0.05	
	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5		1.5		1.5	
C_i	$V_I = 2.5$ V or 0.5 V			4						pF
C_o	$V_O = 2.5$ V or 0.5 V			5.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT241					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.6	4.1	0.8	5.3	ns
t_{PHL}			1	2.9	4.2	0.8	5	
t_{PZH}	$\overline{OE}$ or OE	Y	1.1	4.8	6.3	1	7	ns
t_{PZL}			1.3	4.3	5.8	1	7	
t_{PHZ}	$\overline{OE}$ or OE	Y	1.1	4.6	6.1	0.8	7.9	ns
t_{PLZ}			1	3.9	5.4	0.8	6.2	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT241A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.6	4.1	1	4.6	ns
t_{PHL}			1	2.9	4.4	1	4.6	
t_{PZH}	$\overline{OE}$ or OE	Y	1.1	4.8	6.3	1.1	6.8	ns
t_{PZL}			1.3	4.3	5.8	1.3	6.8	
t_{PHZ}	$\overline{OE}$ or OE	Y	1.6	4.6	6.1	1.6	7.1	ns
t_{PLZ}			1	3.9	5.4	1	5.9	

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

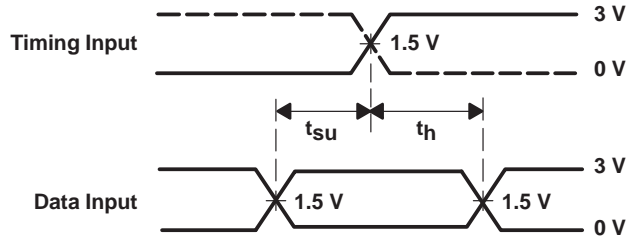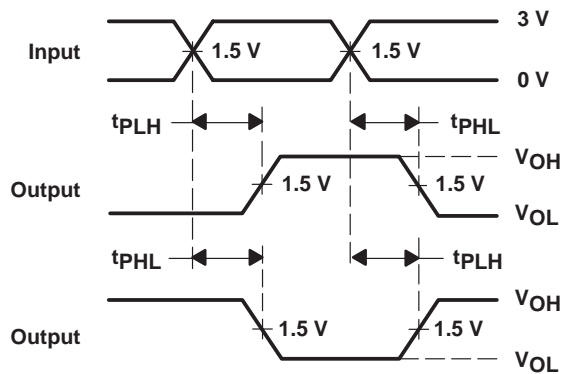| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
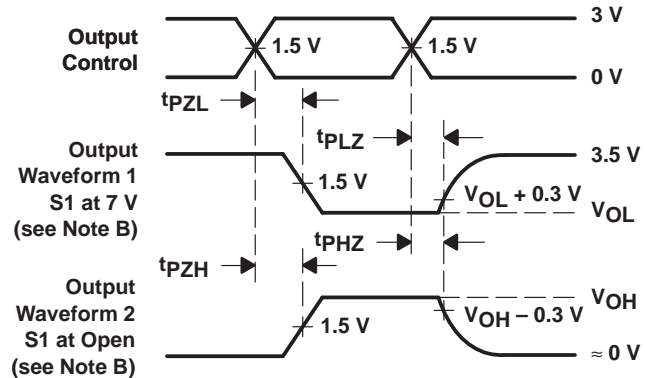
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number (1)	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9322701Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322701Q2A SNJ54ABT 241FK
5962-9322701QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322701QR A SNJ54ABT241J
5962-9322701QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322701QS A SNJ54ABT241W
SN74ABT241ADBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SN74ABT241ADBR.B	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SN74ABT241ADBRG4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SN74ABT241ADBRG4.B	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SN74ABT241ADW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT241A
SN74ABT241ADW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT241A
SN74ABT241ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT241A
SN74ABT241ADWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT241A
SN74ABT241AN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT241AN
SN74ABT241AN.B	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT241AN
SN74ABT241APW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SN74ABT241APW.B	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SN74ABT241APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SN74ABT241APWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB241A
SNJ54ABT241FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322701Q2A SNJ54ABT 241FK
SNJ54ABT241J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322701QR A SNJ54ABT241J

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ABT241W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322701QS A SNJ54ABT241W

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT241ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT241ADBRG4	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT241ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT241APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT241ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT241ADBRG4	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT241ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ABT241APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9322701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9322701QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ABT241ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT241ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT241AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT241AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT241APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74ABT241APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT241FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT241W	W	CFP	20	25	506.98	26.16	6220	NA

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.300 (7,62)
0.245 (6,22)

0.100 (2,45)
0.045 (1,14)

0.009 (0,23)
0.004 (0,10)

0.320 (8,13) MAX

1   20

0.022 (0,56)
0.015 (0,38)

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180−4/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil−Std 1835 GDFP2−F20

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

A

6.6
6.2 TYP

PIN 1 INDEX AREA

1

20

18X 0.65

6.6
6.4
NOTE 3

2X
5.85

10

11

20X 0.30
0.19

⊕ 0.1Ⓜ C A B

B

4.5
4.3
NOTE 4

C

SEATING
PLANE

⌒ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

0° -8°

DETAIL A
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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20X (1.5)

SYMM

1

20X (0.45)

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

2X 5.85

7.5 / 6.9
NOTE 3

10

11

B

5.6 / 5.0
NOTE 4

20X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

C

△ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95 / 0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

TEXAS INSTRUMENTS
www.ti.com

20X (1.85)

1

20X (0.45)

18X (0.65)

SYMM

(R0.05) TYP

20

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65) / 0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52) / 0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66) / 0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36) / 0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4229370VA\

N (R–PDIP–T**)   PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
     △C   Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
     △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

PIN 1 ID
AREA

10.63
9.97 TYP

A

1

13.0
12.6
NOTE 3

10

B

7.6
7.4
NOTE 4

20

11

18X 1.27

2X
11.43

20X 0.51
0.31

⌖ 0.25Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 TYP
0.10

0.25
GAGE PLANE

0° - 8°

1.27
0.40

0.3
0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10   11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING   METAL

METAL UNDER
SOLDER MASK   SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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