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4 Pin Configuration and Functions

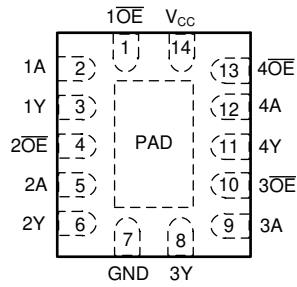


Figure 4-1. SN74AC125 BQA Package (Top View)

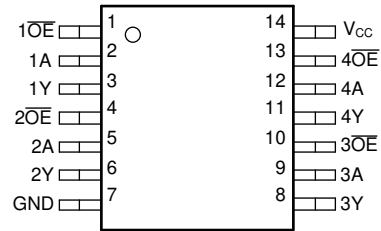


Figure 4-2. SN74AC125, PW Package (Top View)

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1OE	1	I	Channel 1, active-low output enable
1A	2	I	Channel 1, input A
1Y	3	O	Channel 1, output Y
2OE	4	I	Channel 2, active-low output enable
2A	5	I	Channel 2, input B
2Y	6	O	Channel 2, output Y
GND	7	G	Ground
3Y	8	O	Channel 3, output Y
3A	9	I	Channel 3, input A
3OE	10	I	Channel 3, active-low output enable
4Y	11	O	Channel 4, output Y
4A	12	I	Channel 4, input A
4OE	13	I	Channel 4, active-low output enable
V _{CC}	14	P	Positive supply
Thermal Pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

(2) BQA package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I	Input voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < -0.5V or V _I > V _{CC} + 0.5V		±20	mA
I _{OK}	Output clamp current	V _O < -0.5V or V _O > V _{CC} + 0.5V		±50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±50	mA
	Continuous output current through V _{CC} or GND			±200	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.5	6	V
V _{IH}	High-level input voltage	V _{CC} = 1.5V	1.2	V	
		V _{CC} = 1.8V	1.26		
		V _{CC} = 2.5V	1.75		
		V _{CC} = 3V	2.1		
		V _{CC} = 4.5V	3.15		
		V _{CC} = 6V	4.2		
V _{IL}	Low-Level input voltage	V _{CC} = 1.5V		0.3	V
		V _{CC} = 1.8V		0.54	
		V _{CC} = 2.5V		0.75	
		V _{CC} = 3V		0.9	
		V _{CC} = 4.5V		1.35	
		V _{CC} = 6V		1.8	
V _I	Input Voltage		0	V _{CC}	V
V _O	Output Voltage		0	V _{CC}	V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I _{OH}	High-level output current	V _{CC} = 1.8V		-1	mA
		V _{CC} = 2.5V		-2	
		V _{CC} = 3V		-12	
		V _{CC} = 4.5V to 6V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.8V		1	mA
		V _{CC} = 2.5V		2	
		V _{CC} = 3V		12	
		V _{CC} = 4.5V to 6V		24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.5V to 3V		50	ns/V
		V _{CC} = 3.6V to 6V		20	
T _A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
PW (TSSOP)	14	149.8	81.6	106.0	23.5	104.7	N/A	°C/W
BQA (WQFN)	14	95.2	106.6	64.8	19.8	64.6	40.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -50μA	1.5V	1.4	1.49		V
		1.8V	1.7	1.79		
		2.5V	2.4	2.49		
		3V	2.9	2.99		
		4.5V	4.4	4.49		
		6V	5.4	5.99		
	I _{OH} = -1mA	1.8V	1.44			
	I _{OH} = -2mA	2.5V	2			
	I _{OH} = -12mA	3V	2.4			
	I _{OH} = -24mA	4.5V	3.7			
	I _{OH} = -24mA	6V	4.7			
I _{OH} = -75mA	6V	3.85				

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OL}	I _{OL} = 50μA	1.5V		0.01	0.1	V
		1.8V		0.01	0.1	
		2.5V		0.01	0.1	
		3V		0.01	0.1	
		4.5V		0.01	0.1	
		6V		0.01	0.1	
	I _{OL} = 1mA	1.8V			0.36	
	I _{OL} = 2mA	2.5V			0.5	
	I _{OL} = 12mA	3V			0.5	
	I _{OL} = 24mA	4.5V			0.5	
I _{OL} = 24mA	6V			0.5		
I _{OL} = 75mA	6V			1.65		
I _I	V _I = 6V or GND	0V to 6V			±1	μA
I _{OZ}	V _O = V _{CC} or GND	6V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	6V			20	μA
C _I	V _I = V _{CC} or GND	5V		2		pF
C _O	Output disabled, V _O = V _{CC} or GND	5V		4		pF

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
C_L = 15pF							
t _{PLH}	A	Y	1.5V		13.4	20.8	ns
t _{PHL}			1.5V		12.8	19.5	
t _{PLZ}	$\overline{\text{OE}}$	Y	1.5V		9.6	14.1	ns
t _{PHZ}			1.5V		15.4	22.2	
t _{PZL}	$\overline{\text{OE}}$	Y	1.5V		13.2	20.5	ns
t _{PZH}			1.5V		15.7	23.9	
t _r		Y	1.5V		3.7	5.8	ns
t _f			1.5V		4.1	6.5	
t _{sk(o)}		Y	1.5V		0.5	1.2	ns
t _{PLH}	A	Y	1.8V		9.6	14.5	ns
t _{PHL}			1.8V		9.4	14	
t _{PLZ}	$\overline{\text{OE}}$	Y	1.8V		6.9	10	ns
t _{PHZ}			1.8V		11.6	16.2	
t _{PZL}	$\overline{\text{OE}}$	Y	1.8V		9.6	14.4	ns
t _{PZH}			1.8V		11.4	16.8	
t _r		Y	1.8V		2.8	4.4	ns
t _f			1.8V		3.1	4.7	
t _{sk(o)}		Y	1.8V		0.3	0.7	ns
t _{PLH}	A	Y	2.5V		6.2	9	ns
t _{PHL}			2.5V		6	8.7	

5.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t _{PLZ}	OE	Y	2.5V		4	5.7	ns
t _{PHZ}			2.5V		6.2	8.9	
t _{PZL}	OE	Y	2.5V		6.4	9.3	ns
t _{PZH}			2.5V		7.4	10.6	
t _r		Y	2.5V		2.2	3.5	ns
t _f			2.5V		2.1	3.2	
t _{sk(o)}		Y	2.5V		0.2	0.4	ns
t _{PLH}	A	Y	3.3V		5.1	7.4	ns
t _{PHL}			3.3V		5	7.2	
t _{PLZ}	OE	Y	3.3V		3.3	4.7	ns
t _{PHZ}			3.3V		5.2	7.4	
t _{PZL}	OE	Y	3.3V		5.3	7.6	ns
t _{PZH}			3.3V		6.2	8.5	
t _r		Y	3.3V		1.9	3	ns
t _f			3.3V		1.8	2.7	
t _{sk(o)}		Y	3.3V		0.1	0.4	ns
t _{PLH}	A	Y	5V		3.7	5.2	ns
t _{PHL}			5V		3.9	5.1	
t _{PLZ}	OE	Y	5V		2.4	3.3	ns
t _{PHZ}			5V		3.8	5.2	
t _{PZL}	OE	Y	5V		4	5.3	ns
t _{PZH}			5V		4.6	6	
t _r		Y	5V		1.4	2.2	ns
t _f			5V		1.4	2.1	
t _{sk(o)}		Y	5V		0.1	0.3	ns
t _{PLH}	A	Y	6V		3.2	4.3	ns
t _{PHL}			6V		3.3	4.3	
t _{PLZ}	OE	Y	6V		2.1	2.8	ns
t _{PHZ}			6V		3.3	4.4	
t _{PZL}	OE	Y	6V		3.3	4.4	ns
t _{PZH}			6V		3.8	5	
t _r		Y	6V		1.2	1.8	ns
t _f			6V		1.2	1.8	
t _{sk(o)}		Y	6V		0.1	0.3	ns
C_L = 50pF							
t _{PLH}	A	Y	1.5V		19	24	ns
t _{PHL}			1.5V		18.3	22.9	
t _{PLZ}	OE	Y	1.5V		13.7	18.4	ns
t _{PHZ}			1.5V		23.3	30.2	
t _{PZL}	OE	Y	1.5V		15.9	24.5	ns
t _{PZH}			1.5V		18.2	27.3	
t _r		Y	1.5V		7.5	12	ns
t _f			1.5V		7.2	11.8	

5.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t _{sk(o)}		Y	1.5V		0.5	1.1	ns
t _{PLH}	A	Y	1.8V		11.4	17.1	ns
t _{PHL}			1.8V		11.1	16.6	
t _{PLZ}	OE	Y	1.8V		10.2	13.4	ns
t _{PHZ}			1.8V		18.1	22.8	
t _{PZL}	OE	Y	1.8V		11.6	17.3	ns
t _{PZH}			1.8V		13.3	19.4	
t _r		Y	1.8V		5.6	8.9	ns
t _f			1.8V		5.5	8.6	
t _{sk(o)}		Y	1.8V		0.3	0.7	ns
t _{PLH}	A	Y	2.5V		7.5	11	ns
t _{PHL}			2.5V		7.2	10.4	
t _{PLZ}	OE	Y	2.5V		5	7.1	ns
t _{PHZ}			2.5V		8.4	11.4	
t _{PZL}	OE	Y	2.5V		7.9	11.4	ns
t _{PZH}			2.5V		8.8	12.6	
t _r		Y	2.5V		4.3	6.8	ns
t _f			2.5V		3.8	5.8	
t _{sk(o)}		Y	2.5V		0.2	0.5	ns
t _{PLH}	A	Y	3.3V		7.8	9	ns
t _{PHL}			3.3V		7.5	8.6	
t _{PLZ}	OE	Y	3.3V		4	5.6	ns
t _{PHZ}			3.3V		6.9	9.2	
t _{PZL}	OE	Y	3.3V		6.7	9.5	ns
t _{PZH}			3.3V		7.4	10.4	
t _r		Y	3.3V		3.6	5.7	ns
t _f			3.3V		3.3	4.9	
t _{sk(o)}		Y	3.3V		0.2	0.3	ns
t _{PLH}	A	Y	5V		4.7	6.5	ns
t _{PHL}			5V		4.7	6.2	
t _{PLZ}	OE	Y	5V		2.8	3.7	ns
t _{PHZ}			5V		4.7	6.4	
t _{PZL}	OE	Y	5V		5	6.7	ns
t _{PZH}			5V		5.6	7.5	
t _r		Y	5V		2.7	4.2	ns
t _f			5V		2.4	3.5	
t _{sk(o)}		Y	5V		0.1	0.3	ns
t _{PLH}	A	Y	6V		4.1	5.5	ns
t _{PHL}			6V		4	5.2	
t _{PLZ}	OE	Y	6V		2.3	3.1	ns
t _{PHZ}			6V		3.7	5	
t _{PZL}	OE	Y	6V		4.3	5.6	ns
t _{PZH}			6V		4.8	6.3	

5.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t _r		Y	6V		2.3	3.5	ns
t _f			6V		2.2	3	
t _{sk(o)}		Y	6V		0.1	0.2	ns
C_L = 150pF							
t _{PLH}	A	Y	1.5V		20.7	32	ns
t _{PHL}			1.5V		19.4	30.1	
t _{PLZ}	OE	Y	1.5V		25.4	30.6	ns
t _{PHZ}			1.5V		46	53.2	
t _{PZL}	OE	Y	1.5V		21.3	33.7	ns
t _{PZH}			1.5V		23.4	35.2	
t _r		Y	1.5V		17.9	29.5	ns
t _f			1.5V		14.9	25.6	
t _{sk(o)}		Y	1.5V		0.5	1.1	ns
t _{PLH}	A	Y	1.8V		18.7	22.8	ns
t _{PHL}			1.8V		18	21.9	
t _{PLZ}	OE	Y	1.8V		19.6	23.2	ns
t _{PHZ}			1.8V		36.2	41.2	
t _{PZL}	OE	Y	1.8V		15.7	23.7	ns
t _{PZH}			1.8V		17.3	25.2	
t _r		Y	1.8V		13.3	21.6	ns
t _f			1.8V		11.1	18.4	
t _{sk(o)}		Y	1.8V		0.3	0.7	ns
t _{PLH}	A	Y	2.5V		10.2	15	ns
t _{PHL}			2.5V		9.6	13.8	
t _{PLZ}	OE	Y	2.5V		8.3	10.4	ns
t _{PHZ}			2.5V		14.8	17.8	
t _{PZL}	OE	Y	2.5V		10.8	15.5	ns
t _{PZH}			2.5V		11.8	16.6	
t _r		Y	2.5V		9.9	16.5	ns
t _f			2.5V		7.6	12	
t _{sk(o)}		Y	2.5V		0.2	0.4	ns
t _{PLH}	A	Y	3.3V		8.7	12.6	ns
t _{PHL}			3.3V		8.2	11.5	
t _{PLZ}	OE	Y	3.3V		6.9	8.4	ns
t _{PHZ}			3.3V		12.1	14.5	
t _{PZL}	OE	Y	3.3V		9.3	12.9	ns
t _{PZH}			3.3V		10.1	13.9	
t _r		Y	3.3V		8.4	13.7	ns
t _f			3.3V		6.5	10	
t _{sk(o)}		Y	3.3V		0.2	0.3	ns
t _{PLH}	A	Y	5V		6.6	9.2	ns
t _{PHL}			5V		6.4	8.4	

5.6 Switching Characteristics (continued)

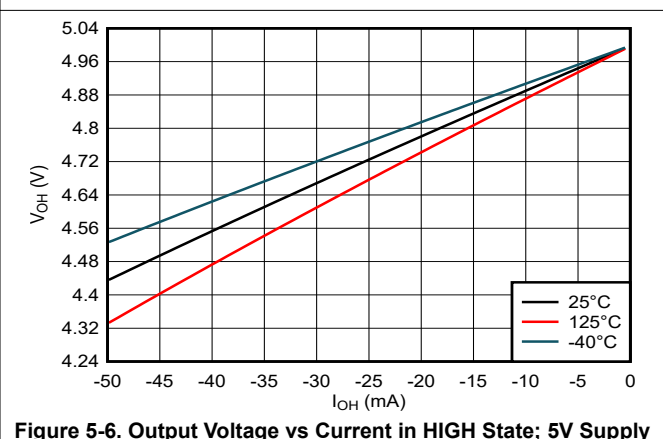
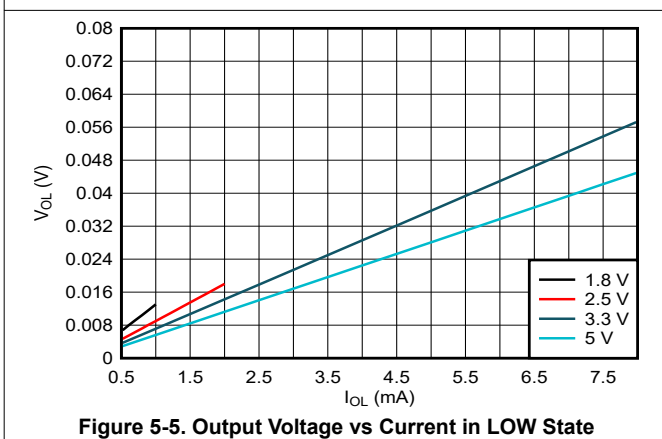
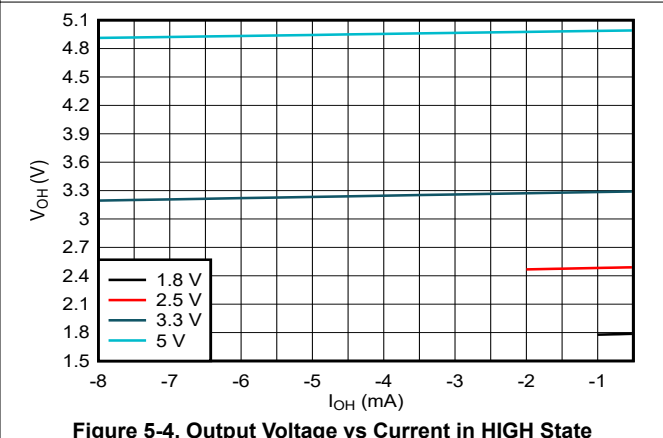
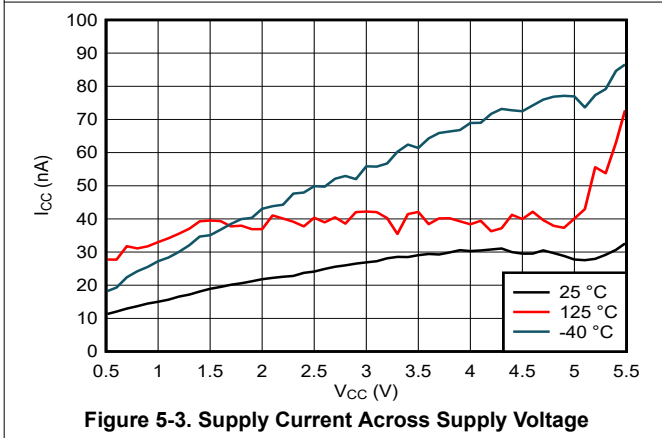
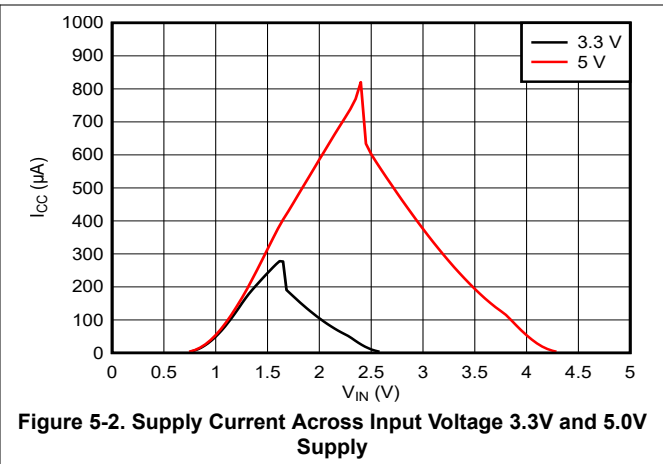
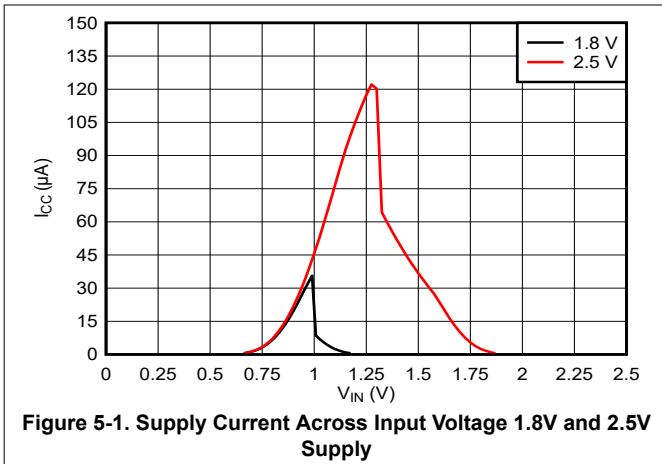
over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t _{PLZ}	OE	Y	5V	4.5	5.5	ns	
t _{PHZ}			5V	7.7	9.3		
t _{PZL}	OE	Y	5V	7.1	9.3	ns	
t _{PZH}			5V	7.8	10.3		
t _r		Y	5V	6.2	9.8	ns	
t _f			5V	5	7.2		
t _{sk(o)}		Y	5V	0.2	0.3	ns	
t _{PLH}	A	Y	6V	5.7	7.9	ns	
t _{PHL}			6V	5.5	7		
t _{PLZ}	OE	Y	6V	3.5	4.4	ns	
t _{PHZ}			6V	5.6	7		
t _{PZL}	OE	Y	6V	6	7.8	ns	
t _{PZH}			6V	6.8	8.9		
t _r		Y	6V	5.1	7.9	ns	
t _f			6V	4.4	6.2		
t _{sk(o)}		Y	6V	0.2	0.4	ns	
C _{PD} ⁽¹⁾	Any		5V	17		pF	

(1) Power dissipation capacitance is calculated using the method described in [CMOS Power Consumption and Cpd Calculation](#).

5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)



5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

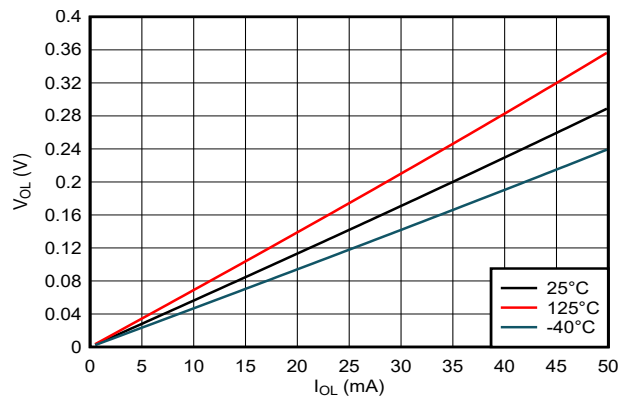


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

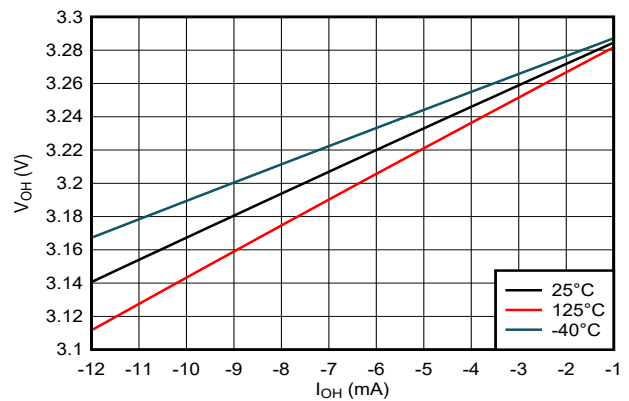


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

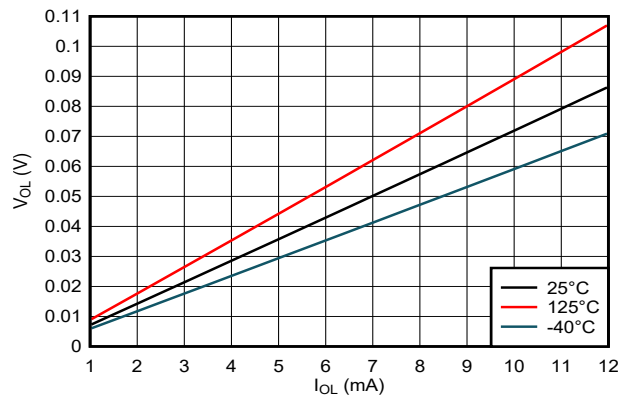


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

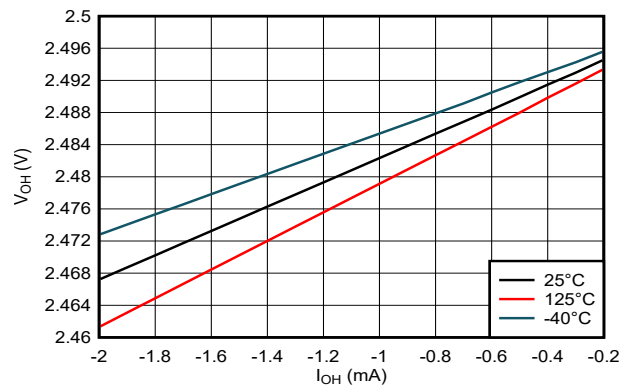


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

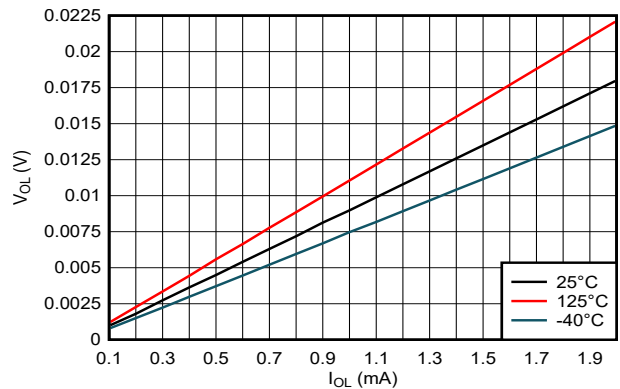


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

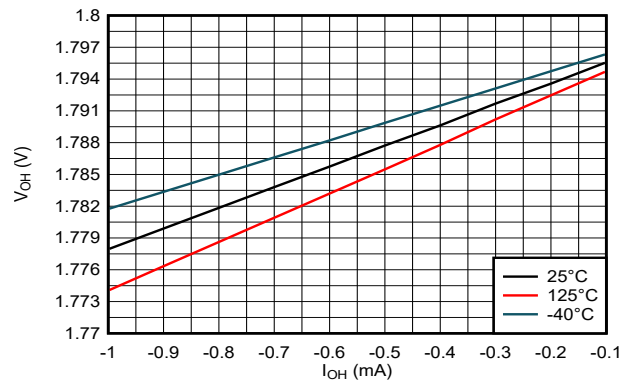


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

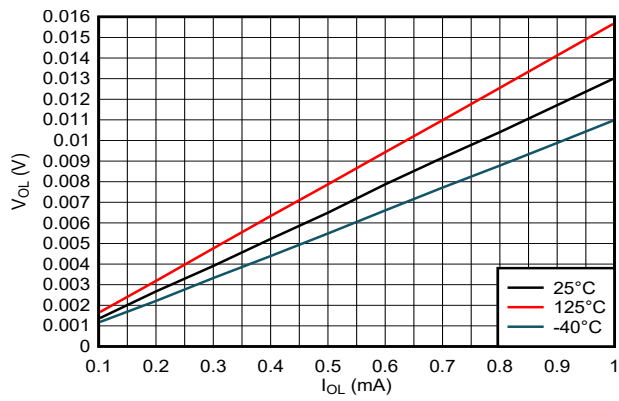


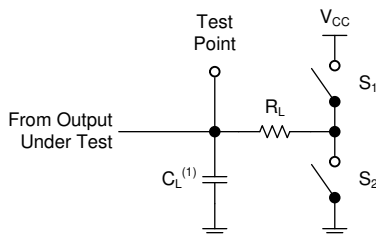
Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

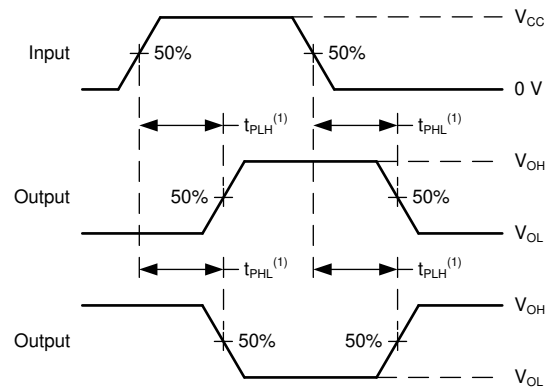
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R _L	C _L	ΔV	V _{CC}
t _{PLH} , t _{PHL}	OPEN	OPEN	—	50pF	—	ALL
t _{PLZ} , t _{PZL}	CLOSED	OPEN	500Ω	50pF	0.15V	≤ 2.5V
t _{PHZ} , t _{PZH}	OPEN	CLOSED	500Ω	50pF	0.15V	≤ 2.5V
t _{PLZ} , t _{PZL}	CLOSED	OPEN	500Ω	50pF	0.3V	> 2.5V
t _{PHZ} , t _{PZH}	OPEN	CLOSED	500Ω	50pF	0.3V	> 2.5V



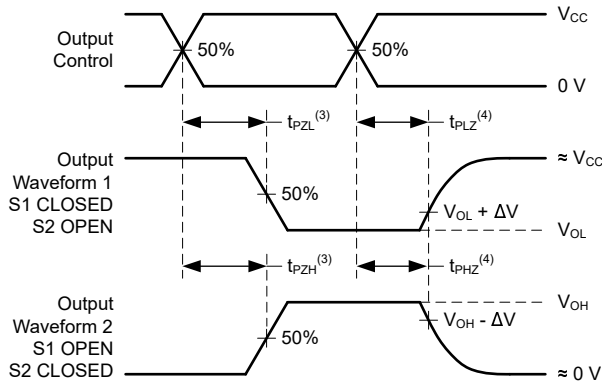
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

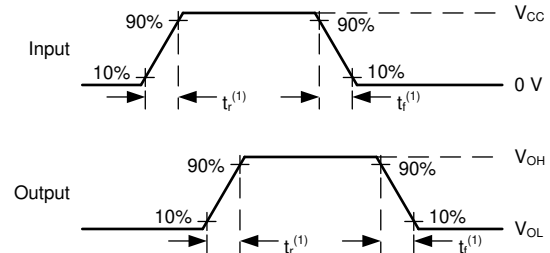
Figure 6-2. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

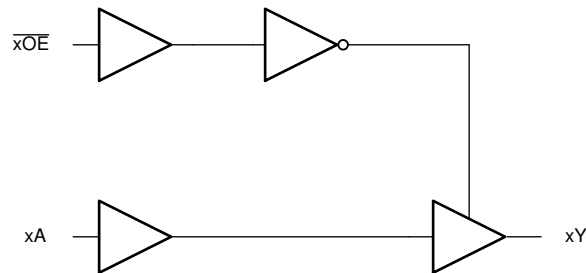
Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function $Y = A$ in positive logic. Each gate has an independent active-low output enable.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.3.3 Clamp Diode Structure

As shown in [Figure 7-1](#), the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

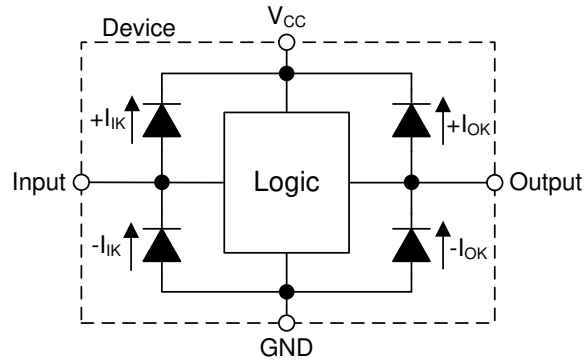


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AC125 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

8.2 Typical Application

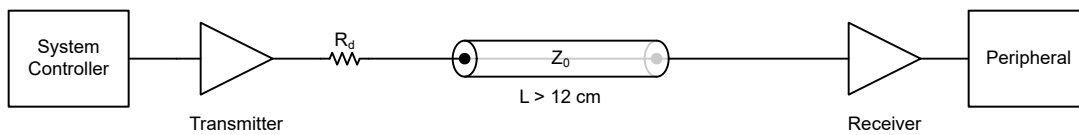


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC125 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC125 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC125 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, do not exceed 50pF.

The SN74AC125 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC125 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74AC125 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50 pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74AC125 to the receiving device.
3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

8.2.3 Application Curve

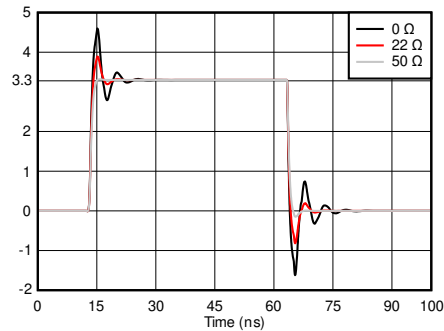


Figure 8-2. Simulated Signal Integrity at the Receiver with Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

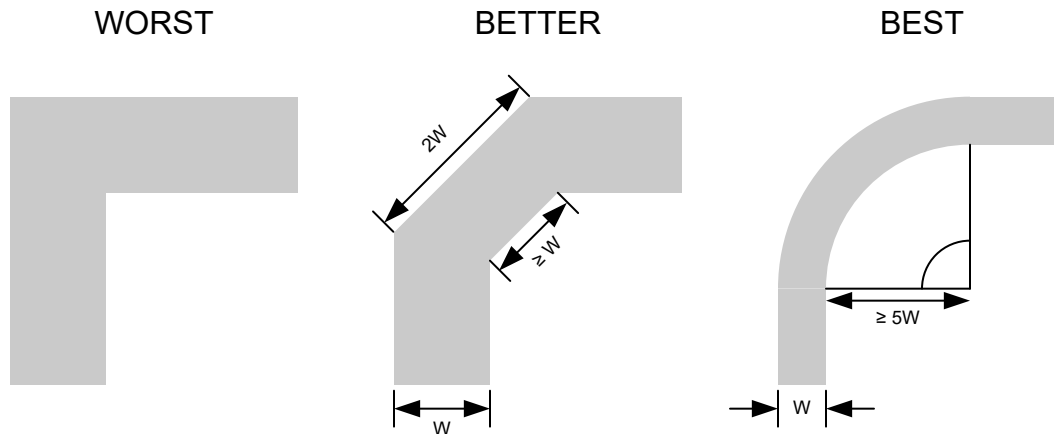


Figure 8-3. Example Trace Corners for Improved Signal Integrity

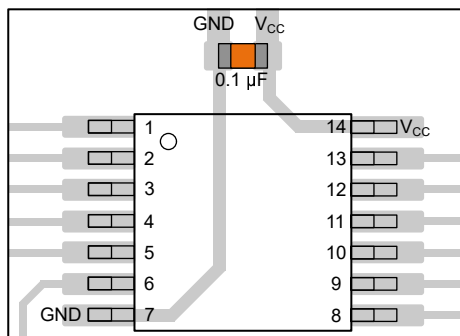


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

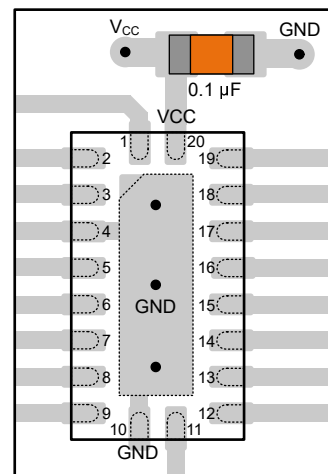


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

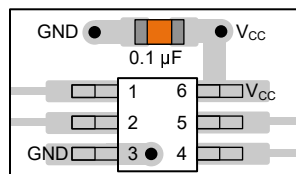


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

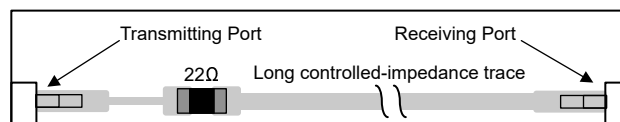


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2025) to Revision A (June 2026)	Page
• Changed title from: SN74AC125 Quadruple Non-Inverting Buffers with 3-State Outputs to: SN74AC125 Quadruple Buffer Gate With 3-State Outputs.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Last updated 10/2025