

SN74AHC08Q-Q1 車載用クワッド 2 入力正論理 AND ゲート

1 特長

- 車載アプリケーション用に認定済み
- 動作範囲: 2V ~ 5.5V V_{CC}
- EPIC™ (Enhanced-Performance Implanted CMOS) プロセス
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 概要

このデバイスはクワッド 2 入力正論理 AND ゲートであり、ブール関数 $Y = A \cdot B$ または $Y = \overline{A + B}$ を正論理で実行します。

パッケージ情報

部品番号	パッケージ ¹	パッケージ・サイズ ²
SN74AHC08Q-Q1	D (SOIC, 14)	8.65mm × 6mm
	PW (TSSOP, 14)	5.00mm × 6.4mm
	BQA (WQFN, 14)	3mm × 2.5mm

1. 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
2. パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

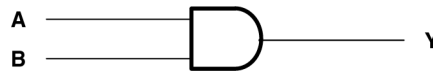


図 2-1. 論理図 (正論理)



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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (April 2008) to Revision D (June 2023)	Page
• 「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「製品情報」表に BQA パッケージを追加	1
• Updated thermal values for PW package from $R\theta_{JA} = 113$ to 147.7 , all values in $^{\circ}\text{C}/\text{W}$	5
• Added thermal value for $R\theta_{JA}$: BQA = 88.3 , all values in $^{\circ}\text{C}/\text{W}$	5

4 Pin Configuration and Functions

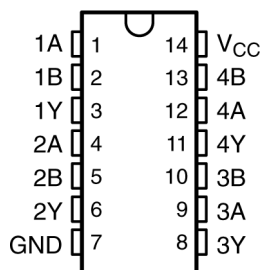


図 4-1. D or PW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V _{CC}	14	—	Positive Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ¹	Input voltage range	-0.5	7	V
V _O ¹	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current (V _I < 0)		-20	mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{CC})		±20	mA
I _O	Continuous output current (V _O = 0 to V _{CC})		±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge Human body model (HBM), per AEC Q100-002 ¹	±2000	V

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 3 V	2.1	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 3 V	0.9	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	mA
		V _{CC} = 3.3 V ± 0.3 V	-4	mA
		V _{CC} = 5 V ± 0.5 V	-8	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	mA
		V _{CC} = 3.3 V ± 0.3 V	4	mA
		V _{CC} = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V
		V _{CC} = 5 V ± 0.5 V	20	
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHC08Q-Q1			UNIT
	D (SOIC)	PW (TSSOP)	BQA (WQFN)	
	14 PINS	14 PINS	14 PINS	
R _{θJA} Junction-to-ambient thermal resistance	86	147.7	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#)

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C TO 125°C		T _A = –40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA		2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = –4 mA		3 V	2.58			2.48		2.48		
	I _{OH} = –8 mA		4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA		2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA		3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA		4.5 V			0.36		0.5		0.44	
I _I	A or B inputs	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20		20	μA
C _i		V _I = V _{CC} or GND	5 V		4	10					pF

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			T _A = –40°C TO 125°C		T _A = –40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF		6.2	8.8	1	10.5	1	10.5	ns
t _{PHL}					6.2	8.8	1	10.5	1	10.5	
t _{PLH}	A or B	Y	C _L = 50 pF		8.7	12.3	1	14	1	14	ns
t _{PHL}					8.7	12.3	1	14	1	14	

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$		4.3	5.9	1	7	1	7	ns
t_{PHL}					4.3	5.9	1	7	1	7	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$		5.8	7.9	1	9	1	9	ns
t_{PHL}					5.8	7.9	1	9	1	9	

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ¹

PARAMETER		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

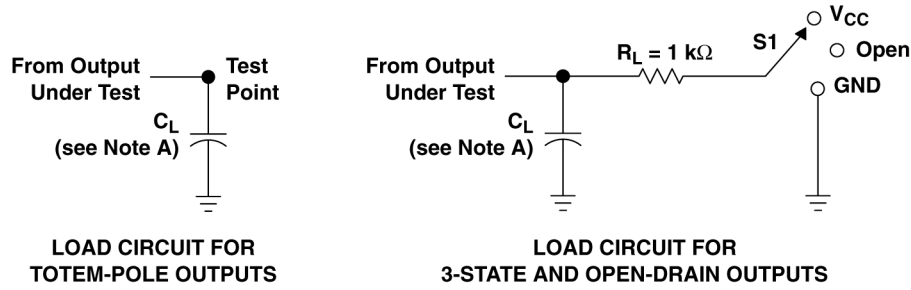
(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

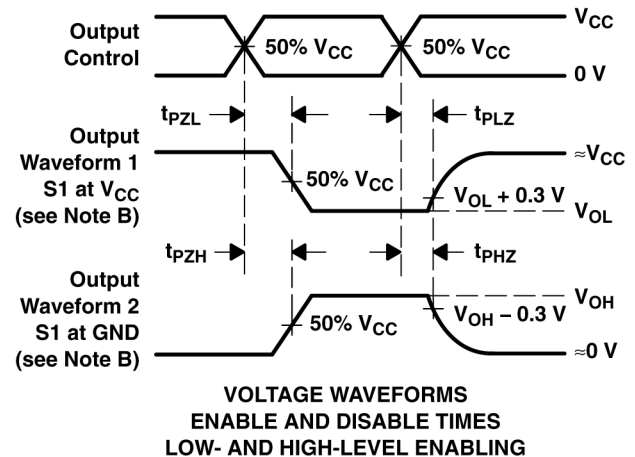
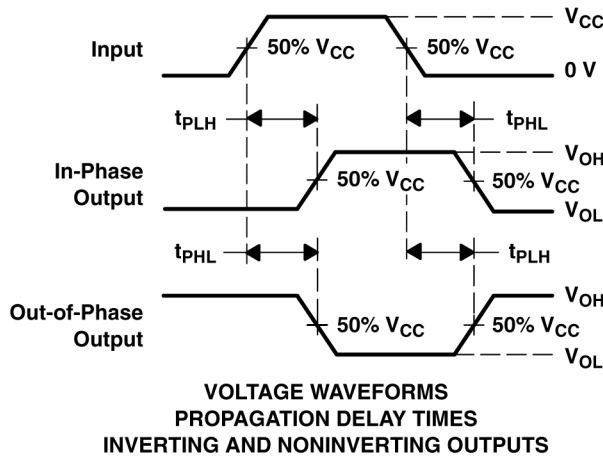
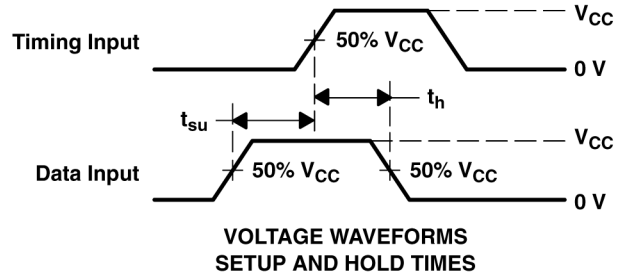
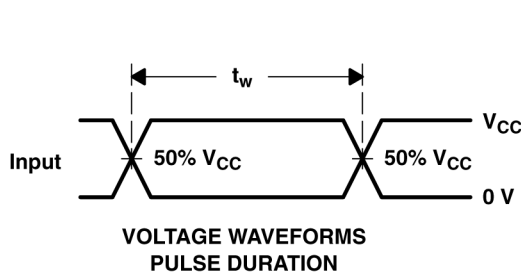
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	18	pF

6 Parameter Measurement Information



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



- A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
D. The outputs are measured one at a time, with one input transition per measurement.

6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

7 Detailed Description

7.1 Functional Block Diagram



图 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

表 7-1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC08Q-Q1	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC08QDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		AHC08Q	Samples
SN74AHC08QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08Q	Samples
SN74AHC08QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08Q	Samples
SN74AHC08QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08Q	Samples
SN74AHC08QWBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

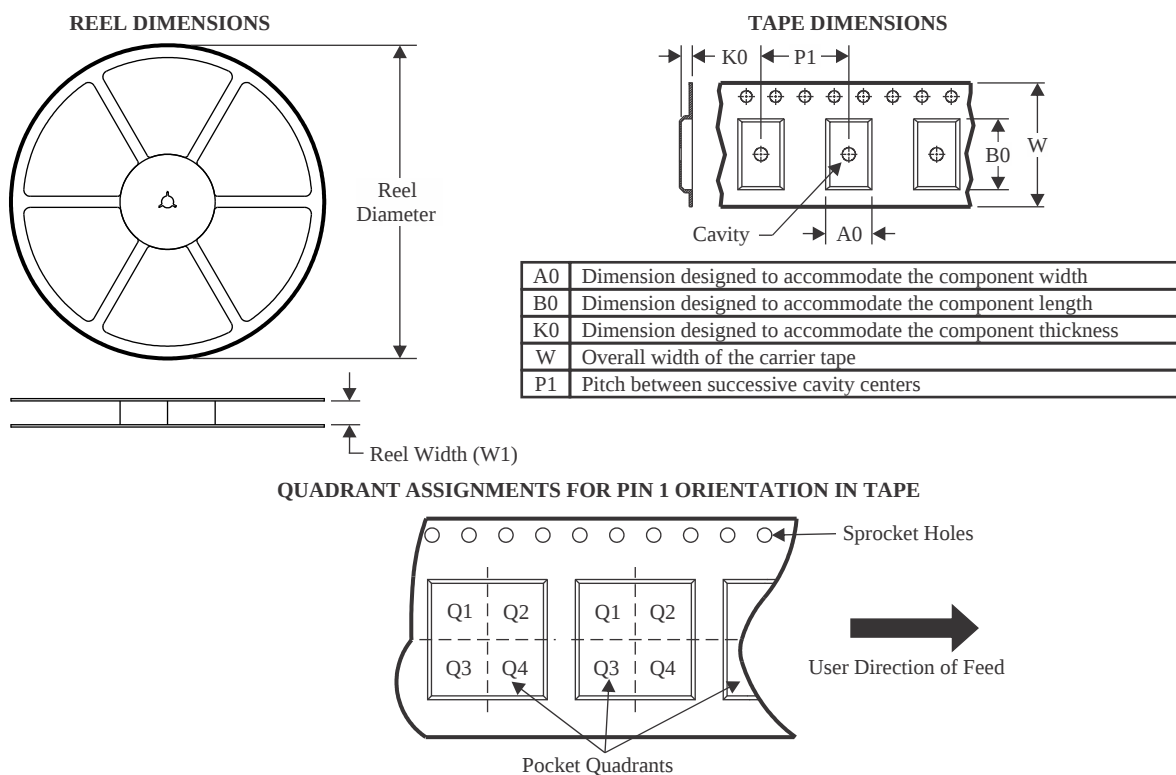
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

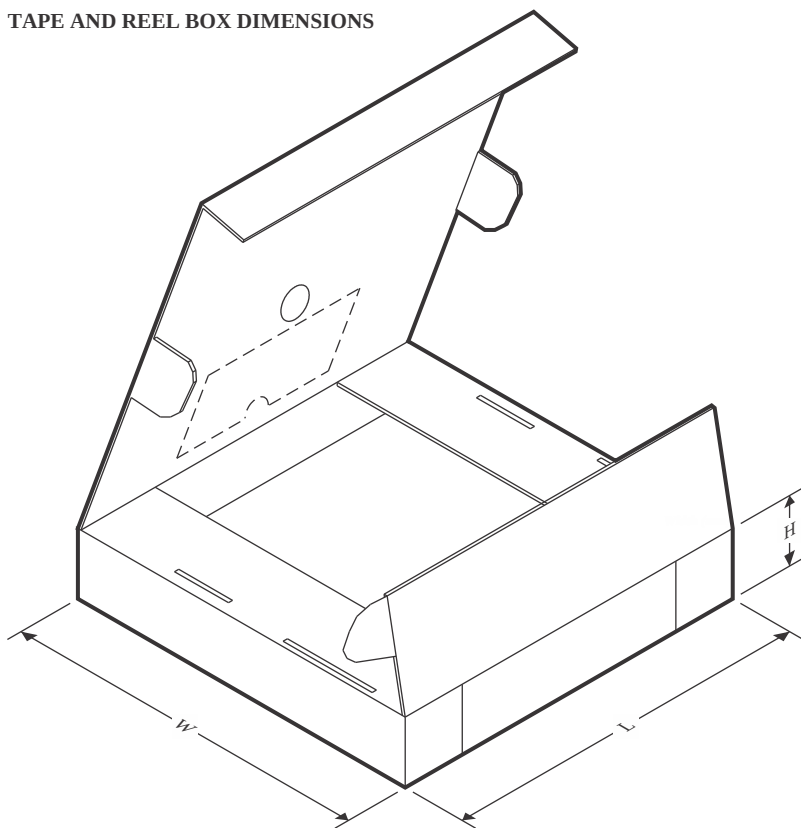
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC08QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

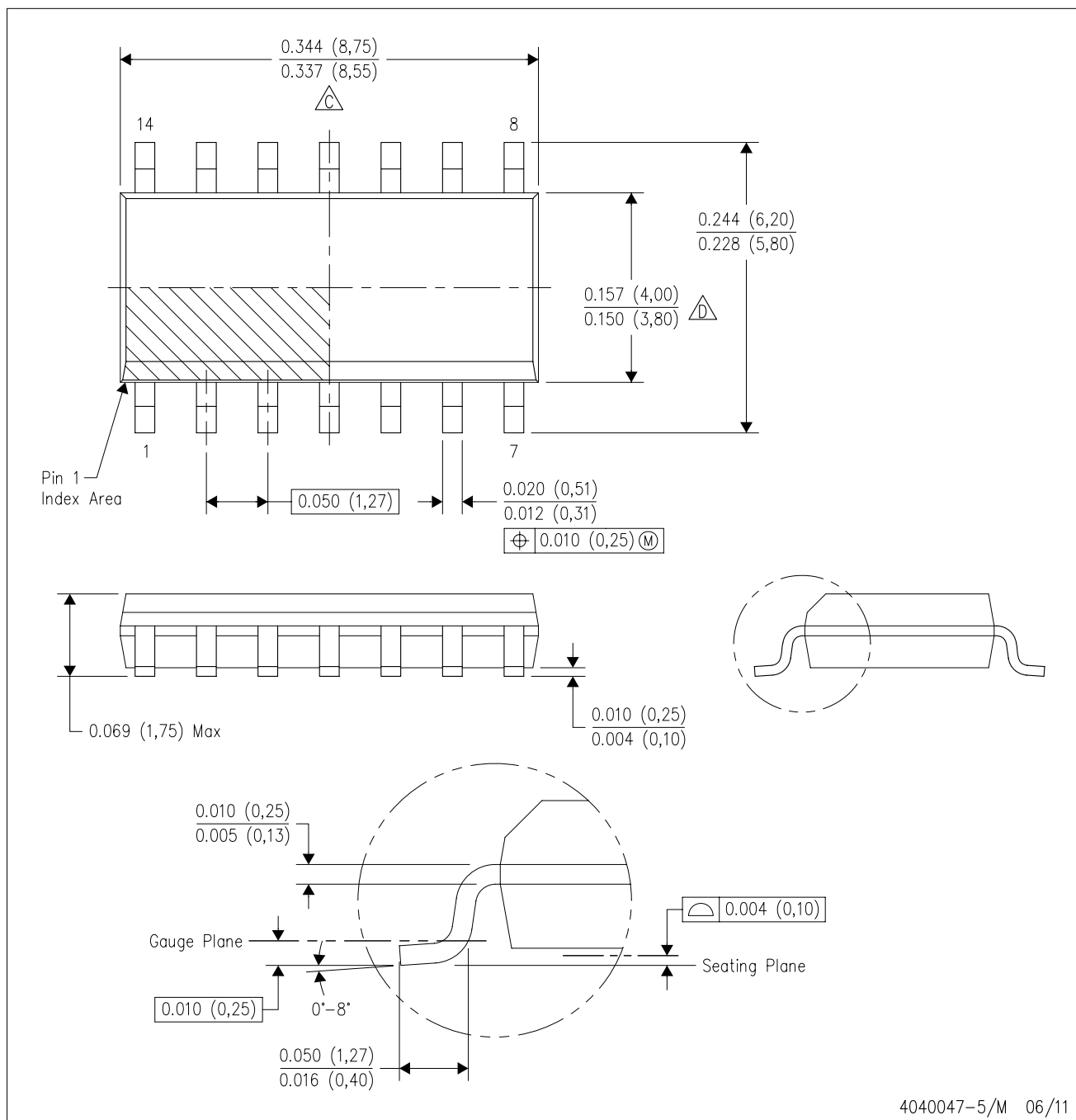


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC08QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC08QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC08QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



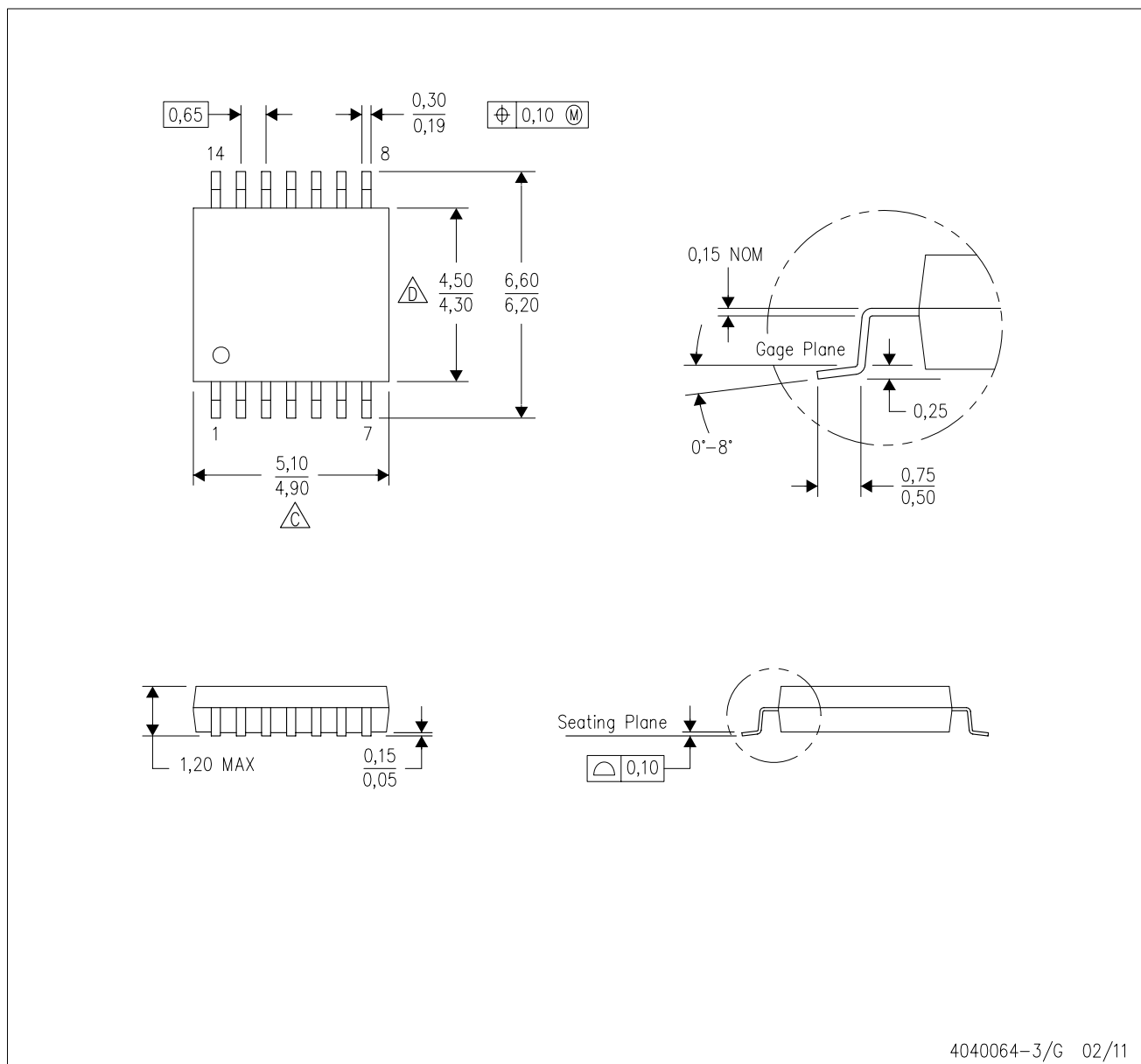
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

GENERIC PACKAGE VIEW

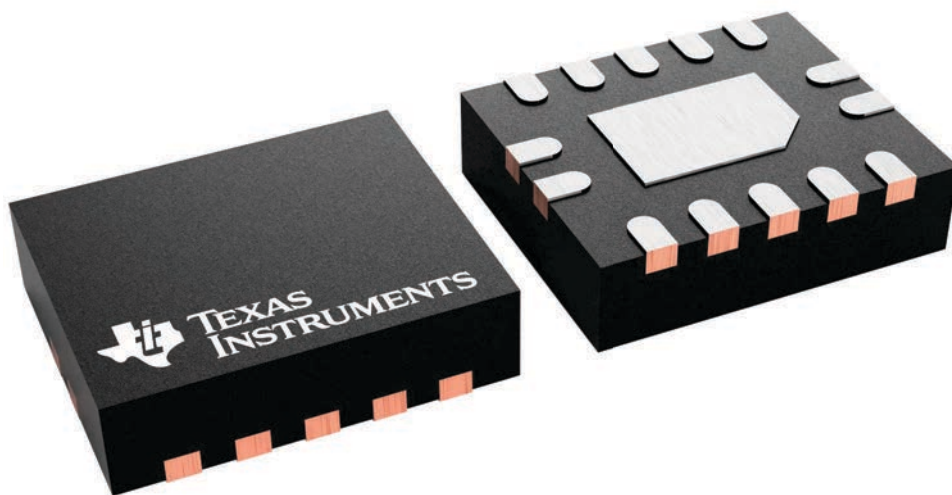
BQA 14

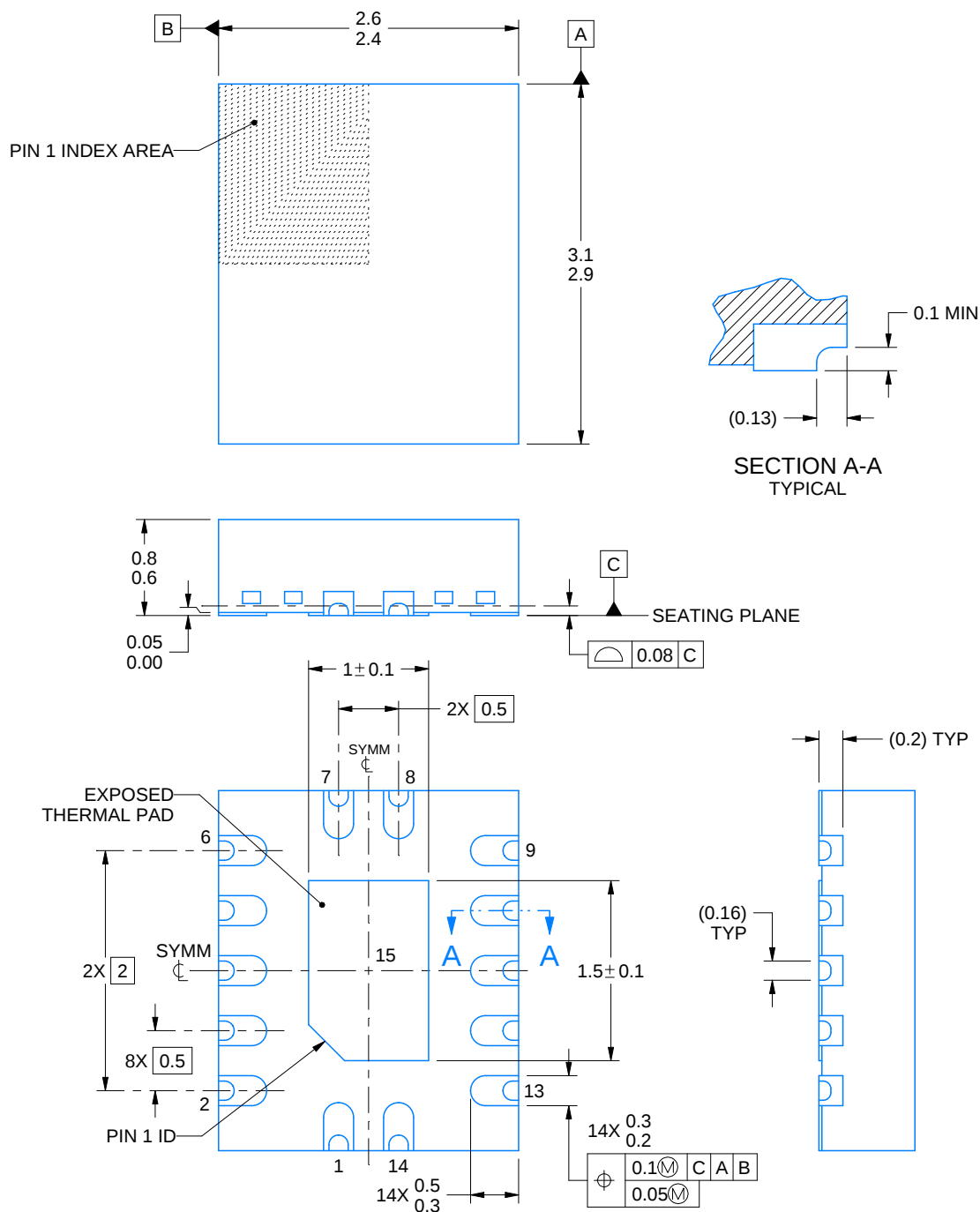
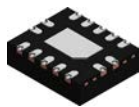
WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4227062/B 09/2021

NOTES:

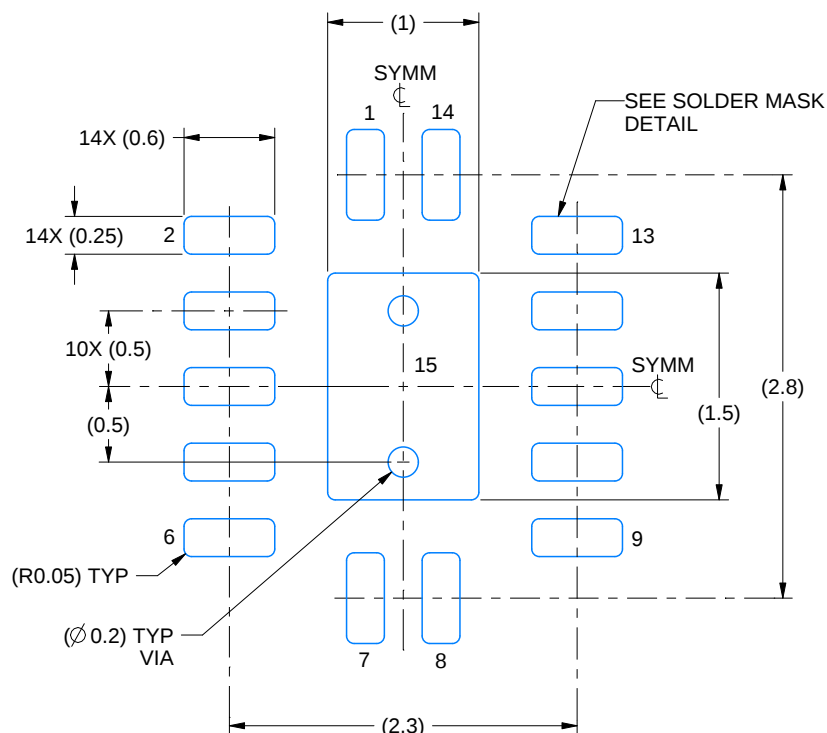
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

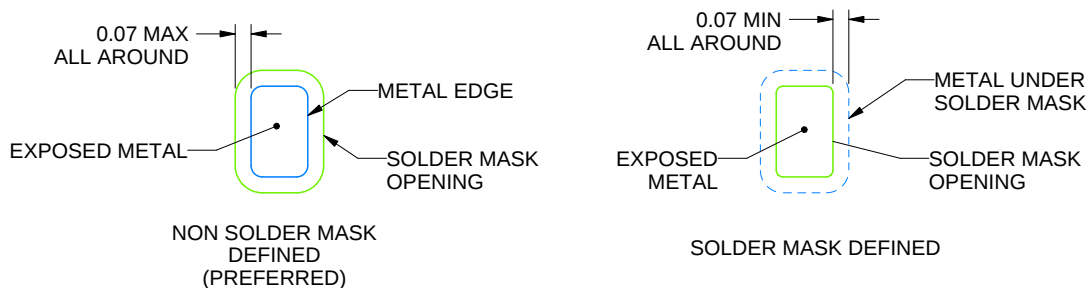
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

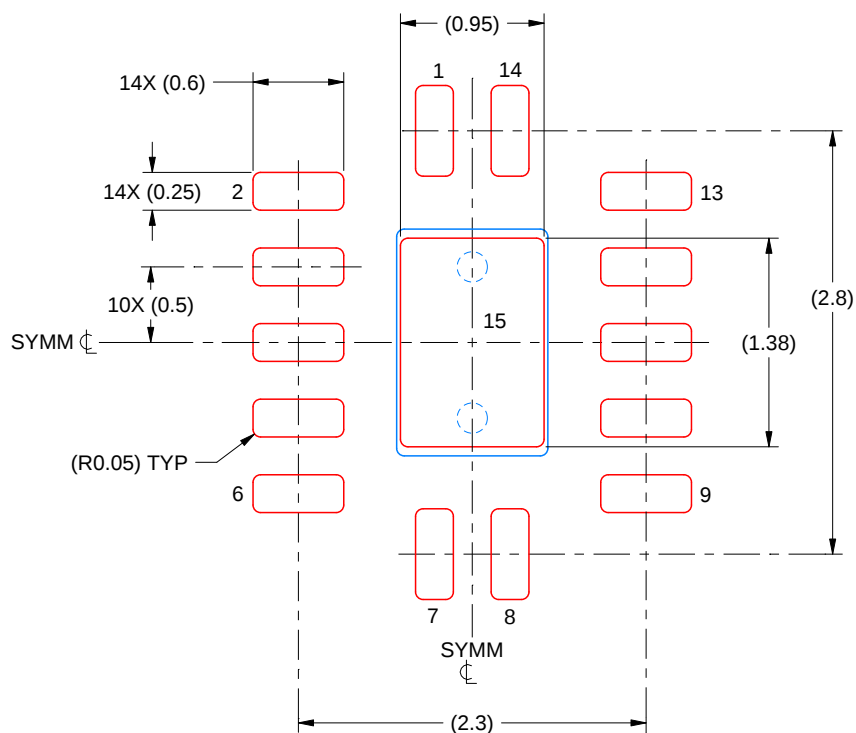
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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