

## SN74AHC1G04 シングル・インバータ・ゲート

### 1 特長

- 動作範囲：2V～5.5V
- 最大  $t_{pd}$  6.5ns (5V 時)
- 低消費電力、最大  $I_{CC}$  10 $\mu$ A
- $\pm 8$ mA の出力駆動能力 (5V 時)
- 全入力でのシュミット・トリガ・アクションにより、低速の入力立ち上がり / 立ち下がり時間を許容
- JESD 17 準拠で 250mA 超のラッチアップ性能

### 2 アプリケーション

- カメラ
- e メーター
- イーサネット・スイッチ
- インフォテインメント

### 3 説明

SN74AHC1G04 には 1 つのインバータ・ゲートが搭載されています。このデバイスは、ブール関数  $Y = \bar{A}$  を実行します。

#### パッケージ情報

| 部品番号        | パッケージ (1)       | パッケージ・サイズ (2)   | 本体サイズ (3)     |
|-------------|-----------------|-----------------|---------------|
| SN74AHC1G04 | DBV (SOT-23、5)  | 2.8mm × 2.8mm   | 2.9mm × 1.6mm |
|             | DCK (SC-70、5)   | 2.00mm × 1.25mm | 2mm × 1.25mm  |
|             | DRL (SOT-553、5) | 1.6mm × 1.6mm   | 1.6mm × 1.2mm |

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。
- 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



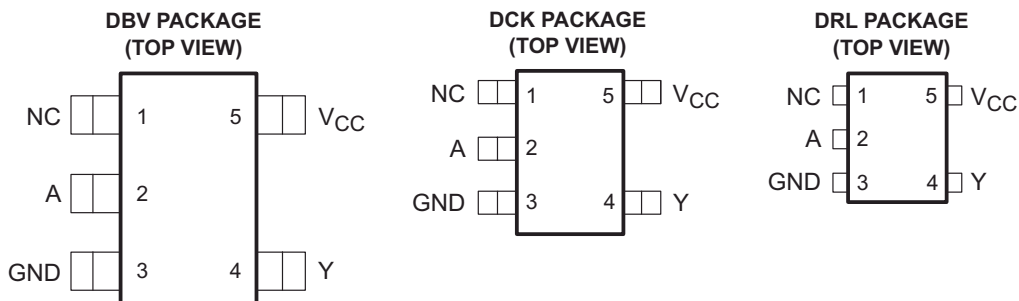
概略回路図



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## 4 Pin Configuration and Functions



NC – No internal connection  
See mechanical drawings for dimensions.

**表 4-1. Pin Functions**

| PIN |                 | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----|-----------------|---------------------|---------------|
| NO. | NAME            |                     |               |
| 1   | NC              | —                   | No Connection |
| 2   | A               | I                   | Input A       |
| 3   | GND             | —                   | Ground Pin    |
| 4   | Y               | O                   | Output Y      |
| 5   | V <sub>CC</sub> | —                   | Power Pin     |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                        | MIN                                                    | MAX                   | UNIT   |
|------------------|--------------------------------------------------------|--------------------------------------------------------|-----------------------|--------|
| V <sub>CC</sub>  | Supply voltage range                                   | –0.5                                                   | 7                     | V      |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                     | –0.5                                                   | 7                     | V      |
| V <sub>O</sub>   | Output voltage range <sup>(2)</sup>                    | –0.5                                                   | V <sub>CC</sub> + 0.5 | V      |
| I <sub>IK</sub>  | Input clamp current                                    | V <sub>I</sub> < 0                                     |                       | –20 mA |
| I <sub>OK</sub>  | Output clamp current                                   | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |                       | ±20 mA |
| I <sub>O</sub>   | Continuous output current                              | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |                       | ±25 mA |
|                  | Continuous current through each V <sub>CC</sub> or GND |                                                        |                       | ±50 mA |
| T <sub>stg</sub> | Storage temperature range                              | –65                                                    | 150                   | °C     |
| T <sub>J</sub>   | Junction temperature                                   |                                                        | 150                   | °C     |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [セクション 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|                    |                         | VALUE                                                                                    | UNIT  |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±3500 |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    | MIN                             | MAX             | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------------|------|
| V <sub>CC</sub> | Supply voltage                     | 2                               | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V           | 1.5             | V    |
|                 |                                    | V <sub>CC</sub> = 3 V           | 2.1             |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V         | 3.85            |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V           | 0.5             | V    |
|                 |                                    | V <sub>CC</sub> = 3 V           | 0.9             |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V         | 1.65            |      |
| V <sub>IH</sub> | Input voltage                      | 0                               | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     | 0                               | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V           | –50             | μA   |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V | –4              | mA   |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | –8              |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V           | 50              | μA   |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V | 4               | mA   |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | 8               |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 3.3 V ± 0.3 V | 100             | ns/V |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | 20              |      |

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                               | MIN | MAX | UNIT |
|-----------------------------------------------|-----|-----|------|
| T <sub>A</sub> Operating free-air temperature | –40 | 125 | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74AHC1G04 |       |       | UNIT |
|-------------------------------|----------------------------------------------|-------------|-------|-------|------|
|                               |                                              | DBV         | DCK   | DRL   |      |
|                               |                                              | 5 PINS      |       |       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 278         | 289.2 | 328.7 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 180.5       | 205.8 | 105.1 |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 184.4       | 176.2 | 150.3 |      |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 115.4       | 117.6 | 6.9   |      |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 183.4       | 175.1 | 148.4 |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bot) thermal resistance    | N/A         | N/A   | N/A   |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | –40°C to 85°C |      | –40°C to 125°C |      | UNIT |
|-------------------------------------------|-------------------------------------------------------------|-----------------|-----------------------|-----|------|---------------|------|----------------|------|------|
|                                           |                                                             |                 | MIN                   | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |      |
| V <sub>OH</sub> High level output voltage | I <sub>OH</sub> = –50 μA                                    | 2 V             | 1.9                   | 2   |      | 1.9           |      | 1.9            |      | V    |
|                                           |                                                             | 3 V             | 2.9                   | 3   |      | 2.9           |      | 2.9            |      |      |
|                                           |                                                             | 4.5 V           | 4.4                   | 4.5 |      | 4.4           |      | 4.4            |      |      |
|                                           | I <sub>OH</sub> = –4 mA                                     | 3 V             | 2.58                  |     |      | 2.48          |      | 2.48           |      |      |
|                                           |                                                             | 4.5 V           | 3.94                  |     |      | 3.8           |      | 3.8            |      |      |
| V <sub>OL</sub> Low level output voltage  | I <sub>OH</sub> = 50 μA                                     | 2 V             |                       |     | 0.1  |               | 0.1  |                | 0.1  | V    |
|                                           |                                                             | 3 V             |                       |     | 0.1  |               | 0.1  |                | 0.1  |      |
|                                           |                                                             | 4.5 V           |                       |     | 0.1  |               | 0.1  |                | 0.1  |      |
|                                           | I <sub>OL</sub> = 4 mA                                      | 3 V             |                       |     | 0.36 |               | 0.44 |                | 0.44 |      |
|                                           |                                                             | 4.5 V           |                       |     | 0.36 |               | 0.44 |                | 0.44 |      |
| I <sub>I</sub> Input leakage current      | V <sub>I</sub> = 5.5 V or GND                               | 0 V to 5.5 V    |                       |     | ±0.1 |               | ±1   |                | ±1   | μA   |
| I <sub>CC</sub> Supply current            | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |     | 1    |               | 10   |                | 10   | μA   |
| C <sub>i</sub> Input Capacitance V        | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 2   | 10   |               | 10   |                | 10   | pF   |

## 5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | OUTPUT<br>CAPACITANCE | $T_A = 25^\circ\text{C}$ |     |      | $-40^\circ\text{C to } 85^\circ\text{C}$ |     | $-40^\circ\text{C to } 125^\circ\text{C}$ |     | UNIT |
|-----------|-----------------|----------------|-----------------------|--------------------------|-----|------|------------------------------------------|-----|-------------------------------------------|-----|------|
|           |                 |                |                       | MIN                      | TYP | MAX  | MIN                                      | MAX | MIN                                       | MAX |      |
| $t_{PLH}$ | A               | Y              | $C_L = 15\text{ pF}$  |                          | 5   | 7.1  | 1                                        | 8.5 | 1                                         | 9.5 | ns   |
| $t_{PHL}$ |                 |                |                       |                          | 5   | 7.1  | 1                                        | 8.5 | 1                                         | 9.5 |      |
| $t_{PLH}$ | A               | Y              | $C_L = 50\text{ pF}$  |                          | 7.5 | 10.6 | 1                                        | 12  | 1                                         | 13  | ns   |
| $t_{PHL}$ |                 |                |                       |                          | 7.5 | 10.6 | 1                                        | 12  | 1                                         | 13  |      |

## 5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | OUTPUT<br>CAPACITANCE | $T_A = 25^\circ\text{C}$ |     |     | $-40^\circ\text{C to } 85^\circ\text{C}$ |     | $-40^\circ\text{C to } 125^\circ\text{C}$ |     | UNIT |
|-----------|-----------------|----------------|-----------------------|--------------------------|-----|-----|------------------------------------------|-----|-------------------------------------------|-----|------|
|           |                 |                |                       | MIN                      | TYP | MAX | MIN                                      | MAX | MIN                                       | MAX |      |
| $t_{PLH}$ | A               | Y              | $C_L = 15\text{ pF}$  |                          | 3.8 | 5.5 | 1                                        | 6.5 | 1                                         | 7   | ns   |
| $t_{PHL}$ |                 |                |                       |                          | 3.8 | 5.5 | 1                                        | 6.5 | 1                                         | 7   |      |
| $t_{PLH}$ | A               | Y              | $C_L = 50\text{ pF}$  |                          | 5.3 | 7.5 | 1                                        | 6.5 | 1                                         | 7   | ns   |
| $t_{PHL}$ |                 |                |                       |                          | 5.3 | 7.5 | 1                                        | 6.5 | 1                                         | 7   |      |

## 5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS |                    | TYP | UNIT |
|-----------|-------------------------------|-----------------|--------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | No load,        | $f = 1\text{ MHz}$ | 12  | pF   |

## 5.9 Typical Characteristics

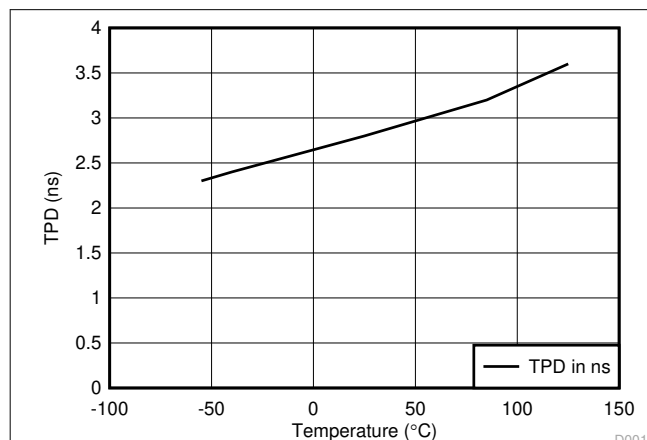


图 5-1. TPD vs Temperature at 5 V

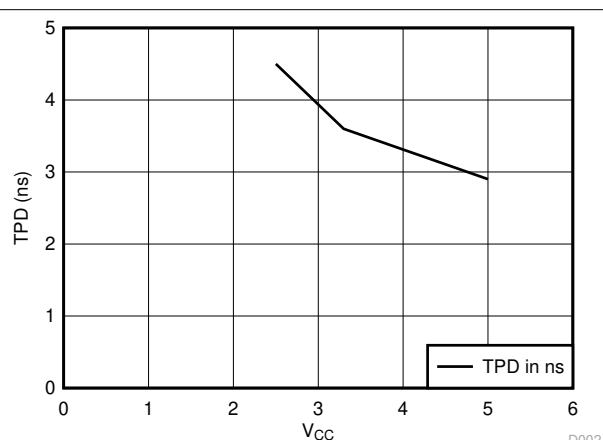
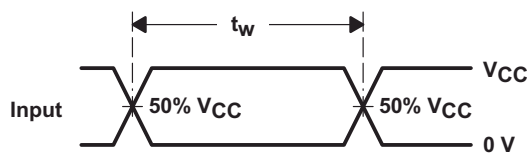
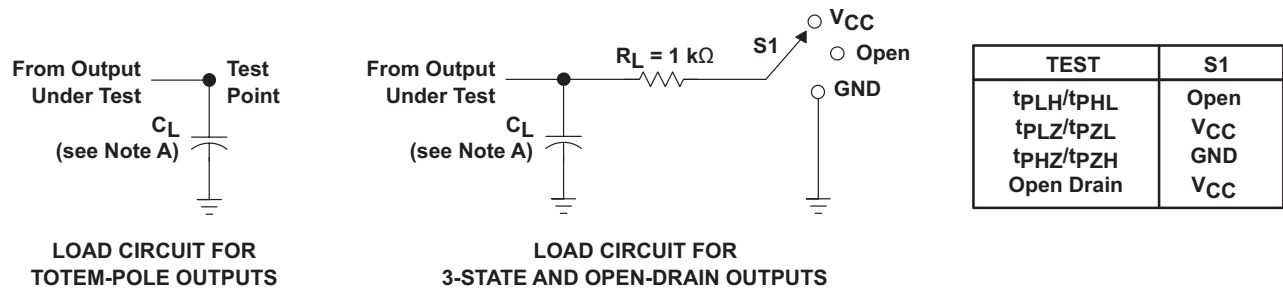
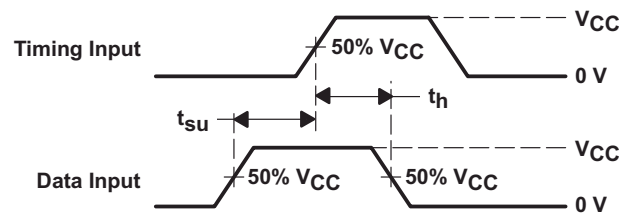


图 5-2. TPD vs  $V_{CC}$  at  $25^\circ\text{C}$

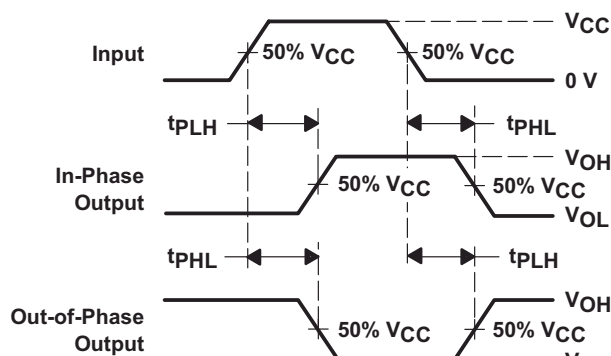
## 6 Parameter Measurement Information



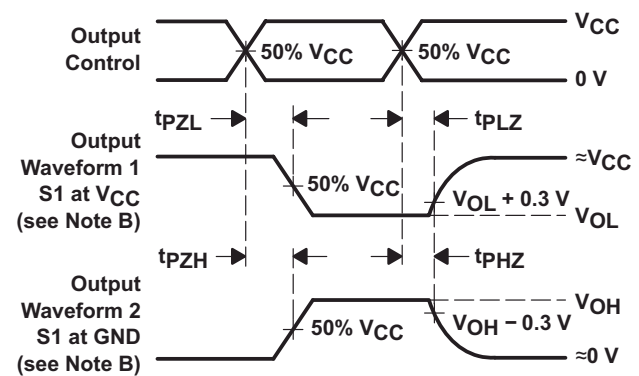
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**图 6-1. Load Circuit And Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

The SN74AHC1G04 device contains one inverter gate. The device performs the Boolean function  $Y = \bar{A}$ .

This single gate inverter has Schmitt-Trigger action on its input, allowing for slower rise and fall times and some noise rejection. This is not a true Schmitt-Trigger, so there is a limit on rise and fall times.

### 7.2 Functional Block Diagram



図 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- Lower drive
  - This will produce slower edges and help prevent ringing on outputs

### 7.4 Device Functional Modes

表 7-1. Function Table

| INPUT <sup>(1)</sup><br>A | OUTPUT <sup>(2)</sup><br>Y |
|---------------------------|----------------------------|
| H                         | L                          |
| L                         | H                          |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State



## 8 Application and Implementation

### 注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツはその正確性も完全性も保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

SN74AHC1G04 is a low-drive CMOS device that can be used for a multitude of inverting buffer type functions. It can produce 8 mA of drive current at 5 V, making it Ideal for driving multiple outputs and good for low-noise applications. The inputs are 5.5-V tolerant, allowing it to translate down to  $V_{CC}$ .

### 8.2 Typical Application

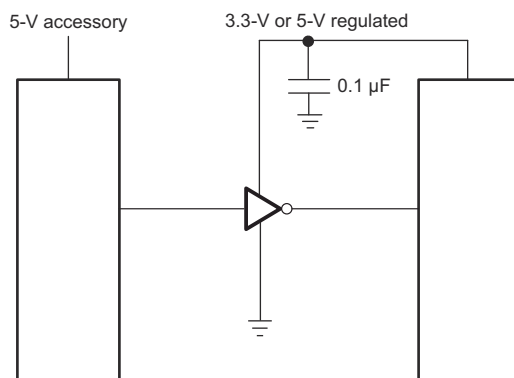


図 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [セクション 5.3](#) table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [セクション 5.3](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## 8.2.3 Application Curves

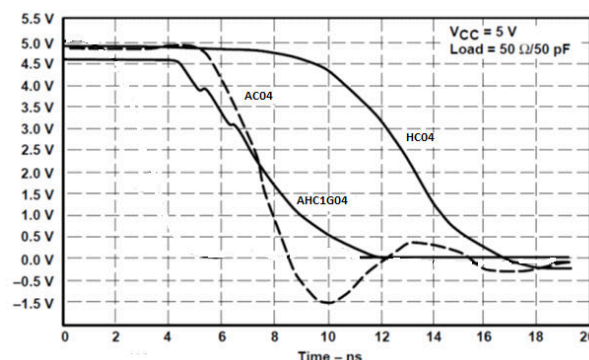


図 8-2. Typical Application Curve

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [セクション 5.3](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [図 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 8.4.2 Layout Example

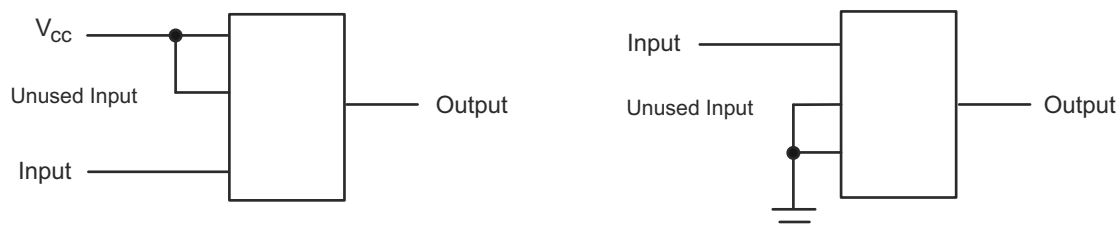


図 8-3. Layout Diagram

## 9 Device and Documentation Support

### 9.1 Documentation Support (Analog)

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。  
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

**テキサス・インスツルメンツ E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.  
すべての商標は、それぞれの所有者に帰属します。

### 9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

**テキサス・インスツルメンツ用語集** この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

| Changes from Revision U (October 2023) to Revision V (February 2024)                                                                                                                                     | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Updated thermal values for DBV package from RθJA = 231.3 to 278, RθJC(top) = 119.9 to 180.5, RθJB = 60.6 to 184.4, ΨJT = 17.8 to 115.4, ΨJB = 60.1 to 183.4, RθJC(bot) = N/A, all values in °C/W ..... | 5    |

| Changes from Revision T (January 2016) to Revision U (October 2023)                                                                                                                                  | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新 .....                                                                                                                                                                | 1    |
| • Updated thermal values for DCK package from RθJA = 287.6 to 289.2, RθJC(top) = 97.7 to 205.8, RθJB = 65 to 176.2, ΨJT = 2 to 117.6, ΨJB = 64.2 to 175.1, RθJC(bot) = N/A, all values in °C/W ..... | 5    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                        |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------------------------|
| <a href="#">SN74AHC1G04DBVR</a>   | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (38CH, 3BUF, A043, A04G, A04J, A04L, A04S) |
| SN74AHC1G04DBVR.A                 | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (38CH, 3BUF, A043, A04G, A04J, A04L, A04S) |
| SN74AHC1G04DBVRE4                 | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | A04G                                       |
| <a href="#">SN74AHC1G04DBVRG4</a> | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | A04G                                       |
| SN74AHC1G04DBVRG4.A               | Active        | Production           | SOT-23 (DBV)   5  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | A04G                                       |
| <a href="#">SN74AHC1G04DBVT</a>   | Obsolete      | Production           | SOT-23 (DBV)   5  | -                     | -           | Call TI                              | Call TI                           | -40 to 125   | (A043, A04G, A04J, A04S)                   |
| <a href="#">SN74AHC1G04DBVTG4</a> | Active        | Production           | SOT-23 (DBV)   5  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | A04G                                       |
| SN74AHC1G04DBVTG4.A               | Active        | Production           | SOT-23 (DBV)   5  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | A04G                                       |
| <a href="#">SN74AHC1G04DCK3</a>   | Obsolete      | Production           | SC70 (DCK)   5    | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | ACY                                        |
| <a href="#">SN74AHC1G04DCKR</a>   | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (1R6, AC3, ACG, ACJ, ACL, ACS)             |
| SN74AHC1G04DCKR.A                 | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | (1R6, AC3, ACG, ACJ, ACL, ACS)             |
| SN74AHC1G04DCKRE4                 | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC3                                        |
| <a href="#">SN74AHC1G04DCKRG4</a> | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC3                                        |
| SN74AHC1G04DCKRG4.A               | Active        | Production           | SC70 (DCK)   5    | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC3                                        |
| <a href="#">SN74AHC1G04DCKT</a>   | Obsolete      | Production           | SC70 (DCK)   5    | -                     | -           | Call TI                              | Call TI                           | -40 to 125   | (AC3, ACG, ACJ, ACS)                       |
| <a href="#">SN74AHC1G04DCKTG4</a> | Active        | Production           | SC70 (DCK)   5    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC3                                        |
| SN74AHC1G04DCKTG4.A               | Active        | Production           | SC70 (DCK)   5    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC3                                        |
| <a href="#">SN74AHC1G04DRLR</a>   | Active        | Production           | SOT-5X3 (DRL)   5 | 4000   LARGE T&R      | Yes         | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM                | -40 to 125   | (ACB, ACS)                                 |
| SN74AHC1G04DRLR.A                 | Active        | Production           | SOT-5X3 (DRL)   5 | 4000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | (ACB, ACS)                                 |
| SN74AHC1G04DRLRG4                 | Active        | Production           | SOT-5X3 (DRL)   5 | 4000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | (ACB, ACS)                                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN74AHC1G04 :

- Automotive : [SN74AHC1G04-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC1G04DBVR   | SOT-23       | DBV             | 5    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DBVTG4 | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DCKR   | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DCKR   | SC70         | DCK             | 5    | 3000 | 180.0              | 8.4                | 2.3     | 2.55    | 1.2     | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DCKRG4 | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DCKTG4 | SC70         | DCK             | 5    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 180.0              | 8.4                | 1.98    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |
| SN74AHC1G04DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 180.0              | 9.5                | 1.78    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |

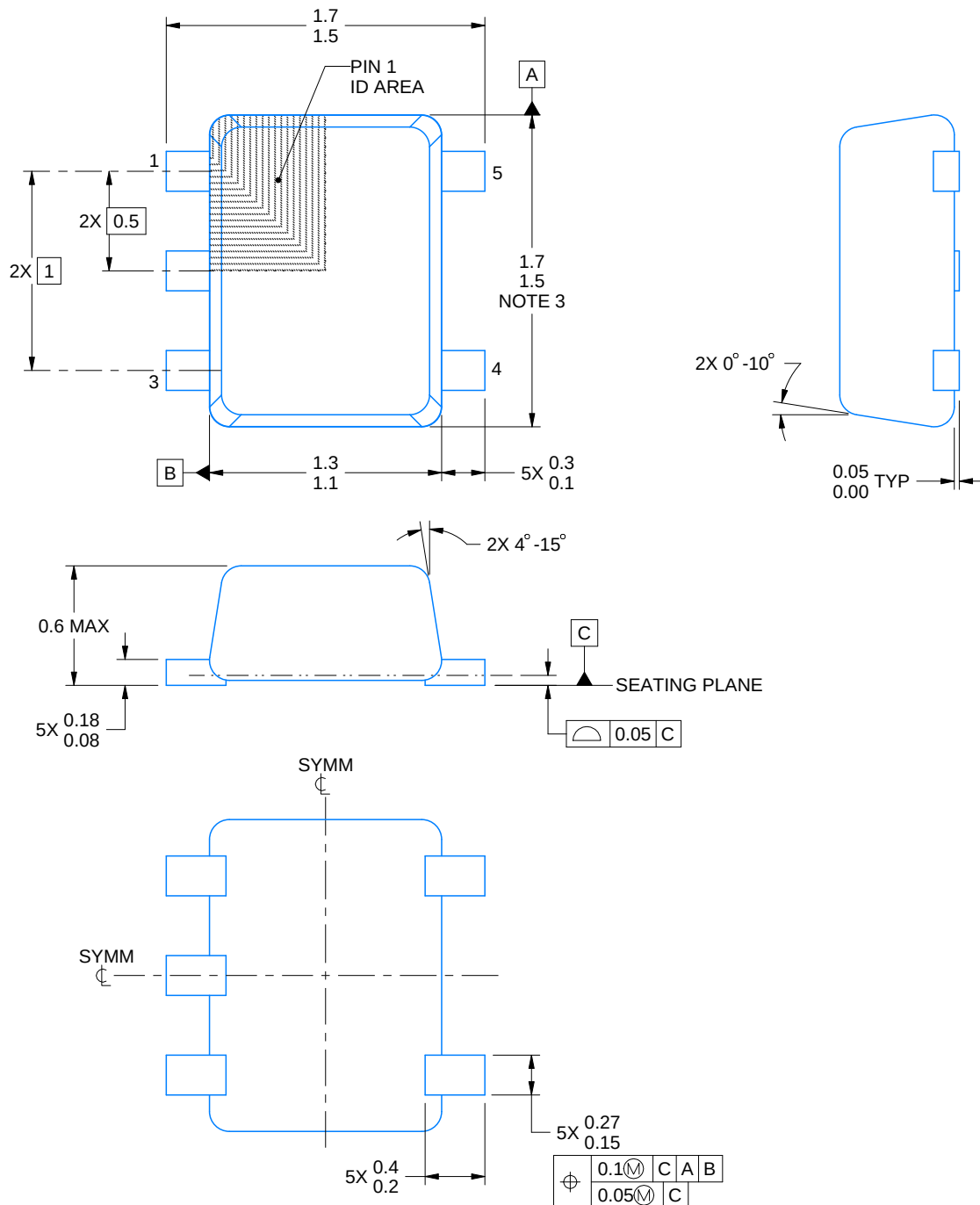
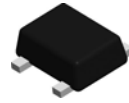
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC1G04DBVR   | SOT-23       | DBV             | 5    | 3000 | 208.0       | 191.0      | 35.0        |
| SN74AHC1G04DBVR   | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHC1G04DBVR   | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHC1G04DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G04DBVTG4 | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G04DCKR   | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G04DCKR   | SC70         | DCK             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74AHC1G04DCKRG4 | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74AHC1G04DCKTG4 | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74AHC1G04DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 202.0       | 201.0      | 28.0        |
| SN74AHC1G04DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 184.0       | 184.0      | 19.0        |





4220753/E 11/2024

## NOTES:

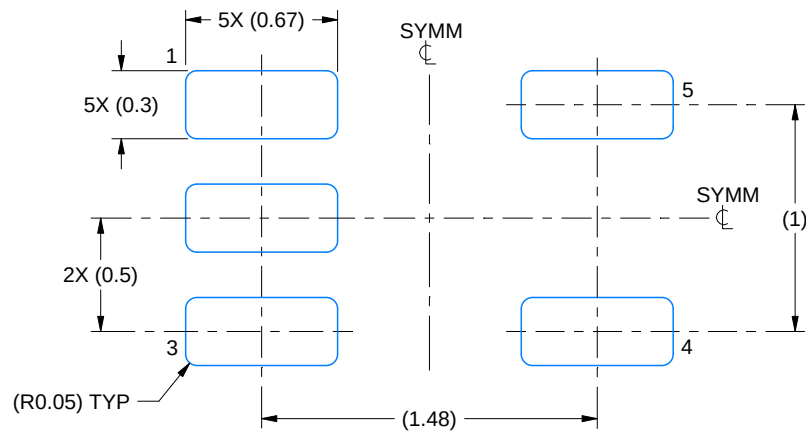
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

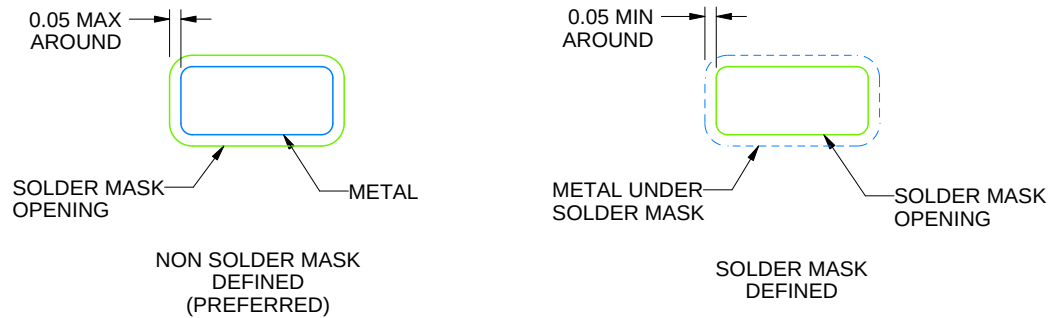
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

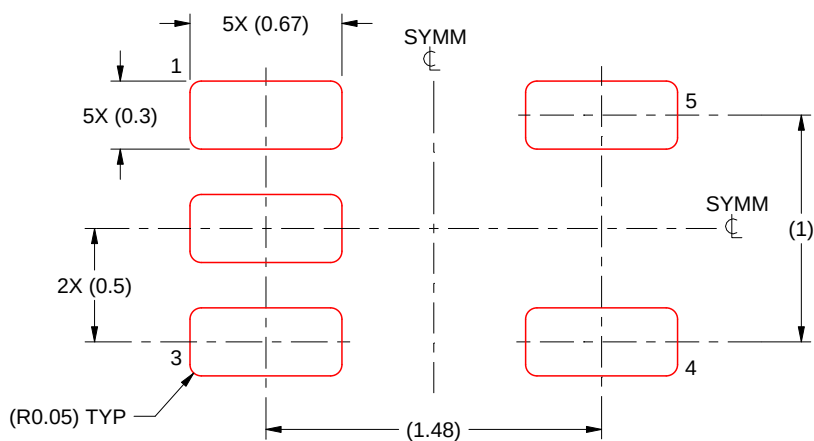
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

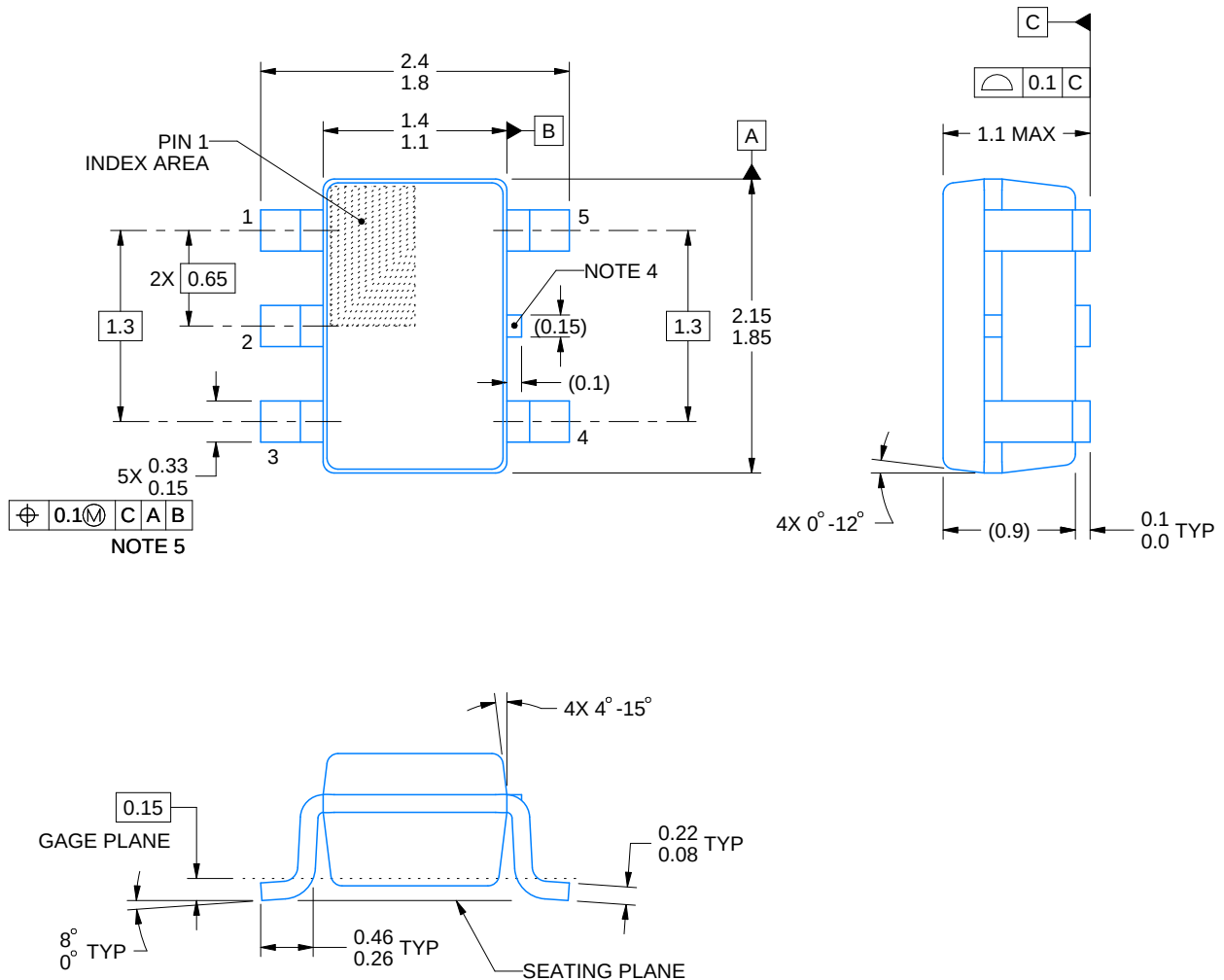


SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4214834/G 11/2024

## NOTES:

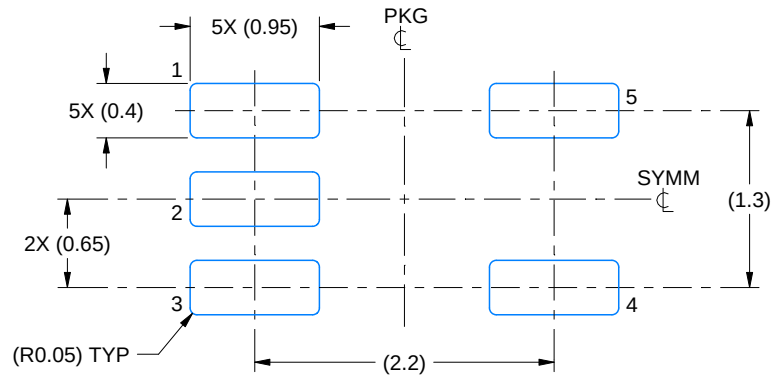
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

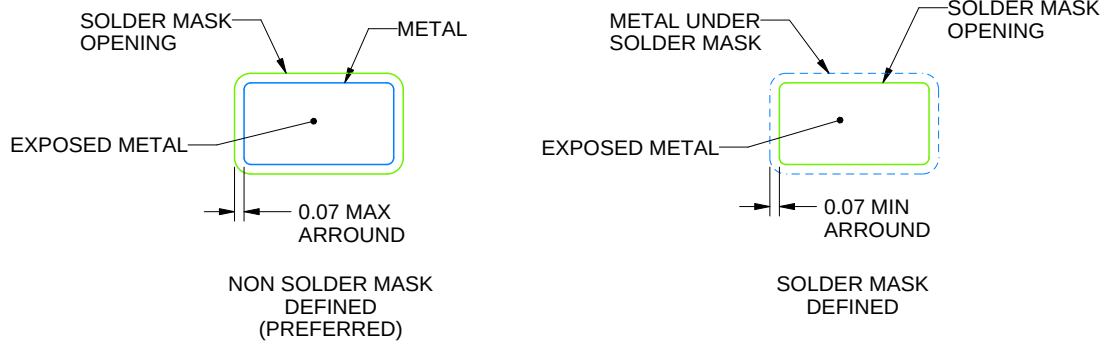
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

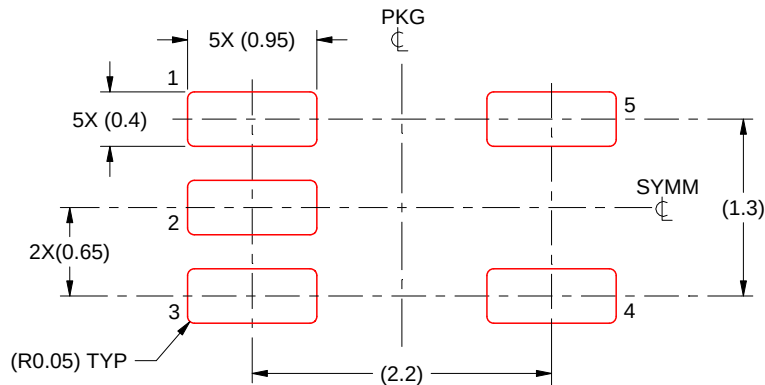


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

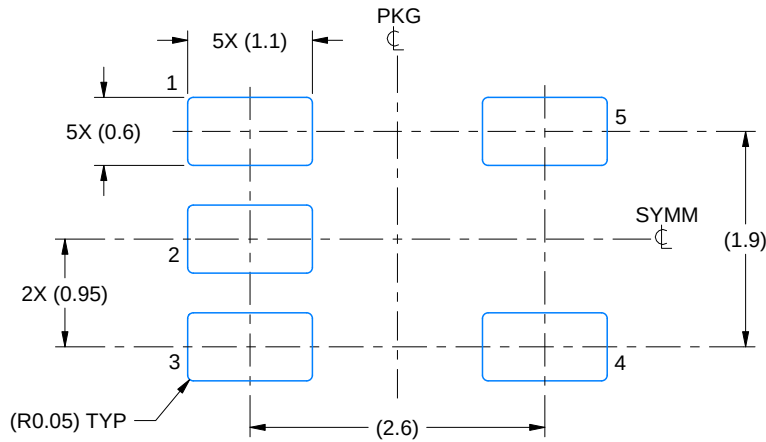


# EXAMPLE BOARD LAYOUT

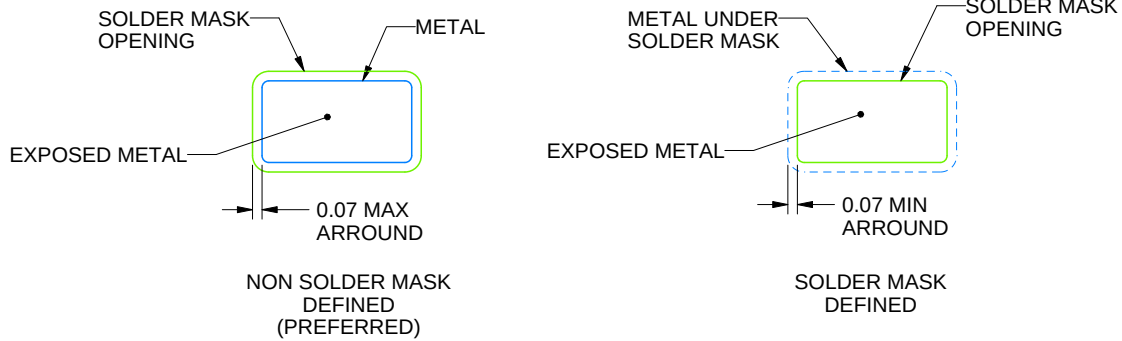
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

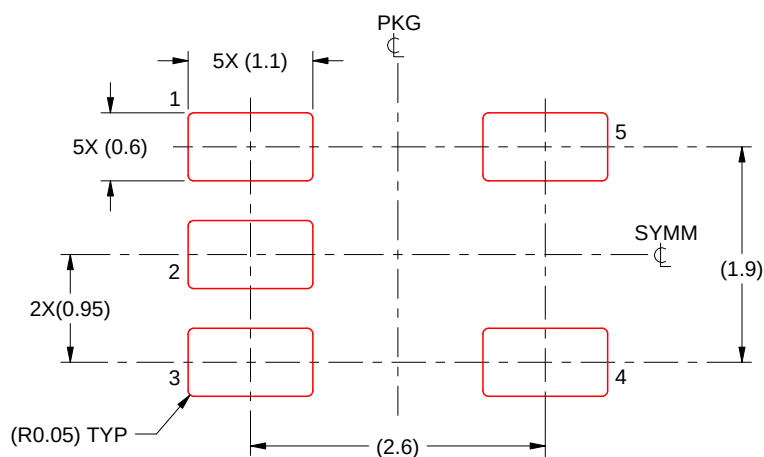
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



**DBV0005A**

## SOT-23 - 1.45 mm max height

## SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月