

SN74AHCT594 出力レジスタ搭載、8ビットシフトレジスタ

1 特長

- 入力は TTL 電圧互換
- 8ビット、シリアル入力、パラレル出力、ストレージ付きシフトレジスタ
- シフトおよびストレージレジスタの独立した直接オーバーライドクリア
- シフトレジスタとストレージレジスタにそれぞれ独立したクロック
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
 - ±3500V 人体モデル
 - ±200V マシンモデル

2 アプリケーション

- ネットワークスイッチ
- 電カインフラストラクチャ
- PC、ノート PC
- 健康管理およびフィットネス / ウェアラブル
- 試験および測定機器

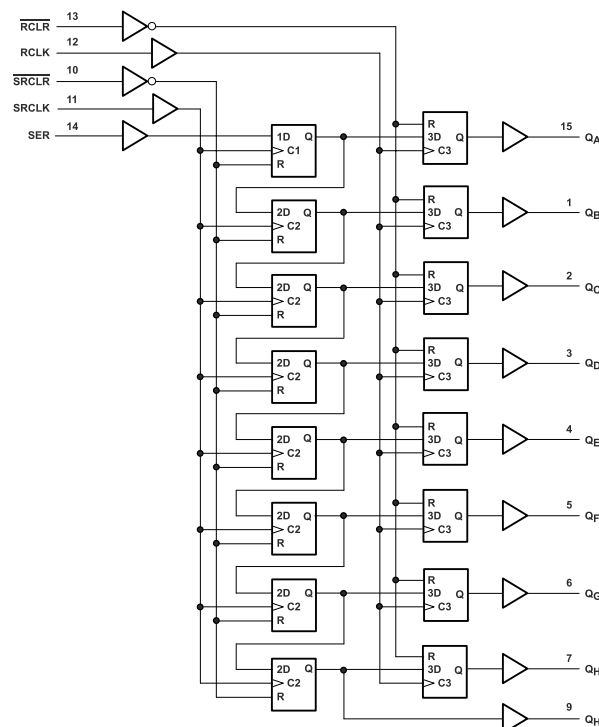
3 概要

SN74AHCT594 デバイスには 8 ビットのシリアル イン / パラレル アウトのシフトレジスタが搭載されており、8 ビットの D タイプ ストレージレジスタヘデータを供給します。

パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)	本体サイズ (3)
SN74AHCT594	N (PDIP, 16)	19.3mm × 9.4mm	19.32mm × 6.35mm
	DB (SSOP, 16)	6.2mm × 7.8mm	6.20mm × 5.30mm
	PW (TSSOP, 16)	5mm × 6.4mm	5.00mm × 4.40mm
	NS (SOP, 16)	10.2mm × 7.8mm	10.20mm × 5.30mm
	D (SOIC, 16)	9.9mm × 6mm	9.90mm × 3.90mm

- (1) 詳細については、[セクション 11](#) を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



概略回路図

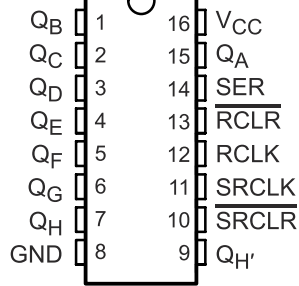


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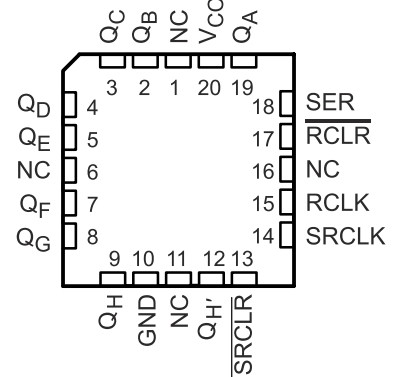
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4 Pin Configuration and Functions

SN54AHCT594 . . . J OR W PACKAGE
 SN74AHCT594 . . . D, DB, N, NS, OR PW PACKAGE
 (TOP VIEW)



SN54AHCT594 . . . FK PACKAGE
 (TOP VIEW)



NC – No internal connection

✎ 4-1.

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	Q _B	O	Output B
2	Q _C	O	Output C
3	Q _D	O	Output D
4	Q _E	O	Output E
5	Q _F	O	Output F
6	Q _G	O	Output G
7	Q _H	O	Output H
8	GND	—	Ground Pin
9	Q _H '	I	QH inverted
10	SRCLR	I	Serial Clear
11	SRCLK	I	Serial Clock
12	RCLK	I	Storage Clock
13	RCLR	I	Storage Clear
14	SER	I	Serial Input
15	Q _A	O	Output A
16	V _{CC}	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±75	mA
T _{stg}	Storage Temperature Range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [セクション 5.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74AHCT594		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-8	mA
I _{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise and fall time		20	ns/V
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHCT594					UNIT
	D	DB	N	NS	PW	
	16 PINS					
R _{θJA} Junction-to-ambient thermal resistance	93.8	129.6	47.5	79.1	135.9	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	54.7	90	34.9	35.4	70.3	
R _{θJB} Junction-to-board thermal resistance	50.9	92.7	27.5	39.9	81.3	
ψ _{JT} Junction-to-top characterization parameter	20.8	46.1	19.8	5.4	22.5	
ψ _{JB} Junction-to-board characterization parameter	50.7	91.7	27.4	39.5	80.8	
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = –8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5V			0.1		0.1	0.1	V	
	I _{OL} = 8 mA			0.36		0.44		0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 ⁽¹⁾	±1 ⁽¹⁾	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20	20	μA	
ΔI _{CC} ⁽²⁾	One input at 3.5 V, Other inputs at V _{CC} or GND	5.5 V			2		2.2	2.2	mA	
C _i	V _I = V _{CC} or GND	5 V		2	10		10	10	pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		T _A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	RCLK or SRCLK high or low	5		5.5		6.5	ns
		RCLR or SRCLR low	5.2		5.5		6	
t _{su}	Setup time	SER before SRCLK↑	3		3		3.5	ns
		SRCLK↑ before RCLK↑ ⁽¹⁾	5		5		5.5	
		SRCLR low before RCLK↑	5		5		5.5	
		SRCLR high (inactive) before SRCLK↑	2.9		3.3		4	
		RCLR high (inactive) before RCLK↑	3.4		3.8		4.5	
t _h	Hold time	SER after SRCLK↑	2		2		2.5	ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	135 ⁽¹⁾	170 ⁽¹⁾		115		115	MHz	
			C _L = 50 pF	120	140		95		95		
t _{PLH}	RCLK	Q _A – Q _H	C _L = 15 pF		3.3 ⁽¹⁾	6.2 ⁽¹⁾	1	6.5	1	7.5	ns
t _{PHL}					3.7 ⁽¹⁾	6.5 ⁽¹⁾	1	6.9	1	7.8	
t _{PLH}	SRCLK	Q _{H'}	C _L = 15 pF		3.7 ⁽¹⁾	6.8 ⁽¹⁾	1	7.2	1	8	ns
t _{PHL}					4.1 ⁽¹⁾	7.2 ⁽¹⁾	1	7.6	1	8.5	
t _{PLH}	RCLR	Q _A – Q _H	C _L = 15 pF		4.5 ⁽¹⁾	7.6 ⁽¹⁾	1	8.2	1	9.5	ns
t _{PHL}					4.1 ⁽¹⁾	7.1 ⁽¹⁾	1	7.6	1	8.5	
t _{PLH}	RCLK	Q _A – Q _H	C _L = 50 pF		4.9	7.8	1	8.3	1	9.5	ns
t _{PHL}					5.8	8.9	1	9.7	1	10.5	
t _{PLH}	SRCLK	Q _{H'}	C _L = 50 pF		5.5	8.6	1	9.7	1	10	ns
t _{PHL}					6	9.2	1	10.1	1	11	
t _{PLH}	RCLR	Q _A – Q _H	C _L = 50 pF		6.6	10	1	10.7	1	11.5	ns
t _{PHL}					6	9.2	1	10.1	1	11	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C⁽¹⁾

PARAMETER		SN74AHCT594			UNIT
		MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		1		V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		–0.6		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3.8		V
V _{IH(D)}	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	112	pF

5.10 Typical Characteristics

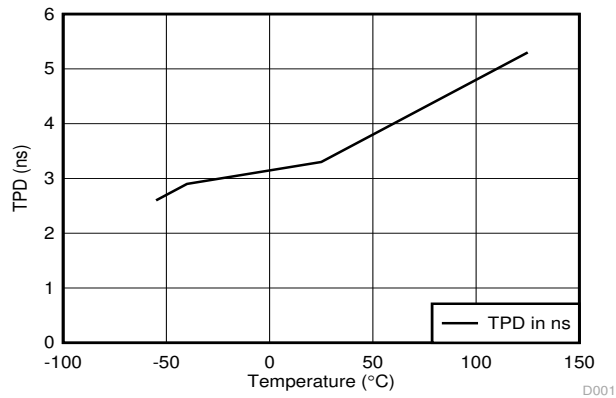
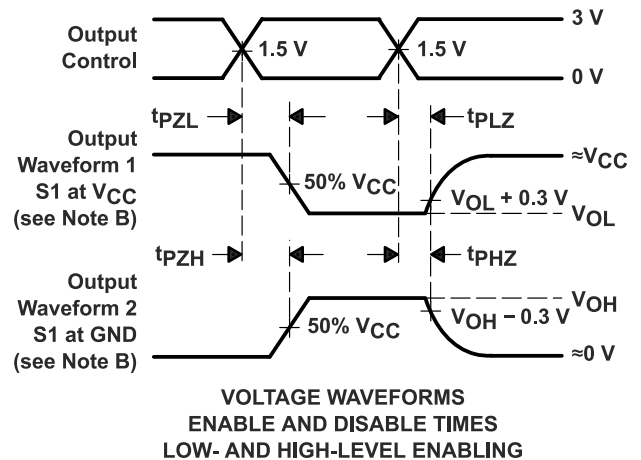
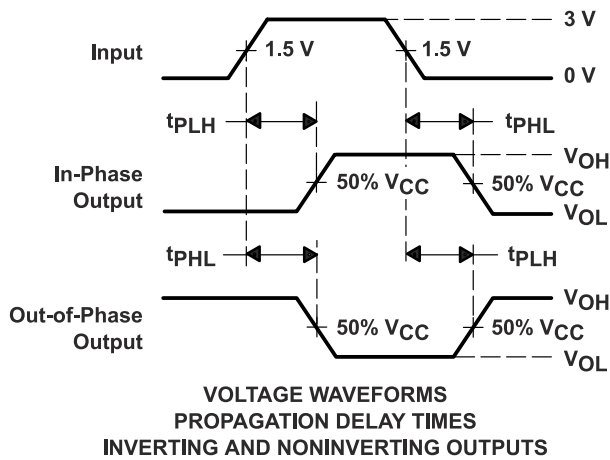
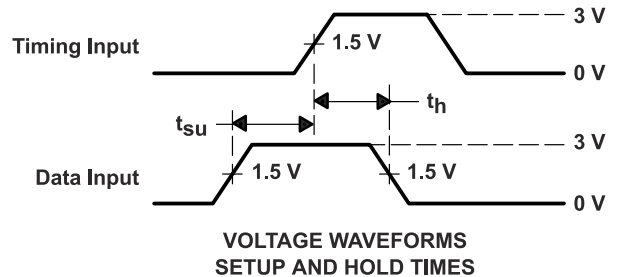
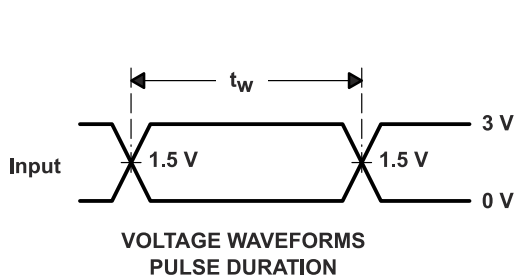
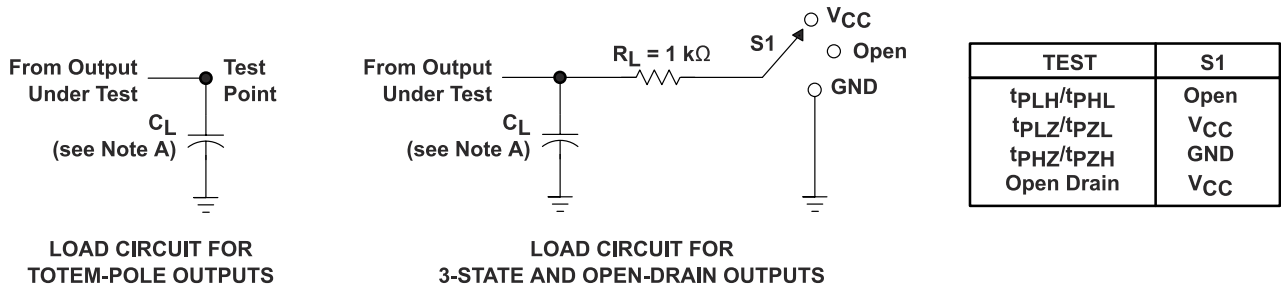


図 5-1. TPD vs Temperature

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

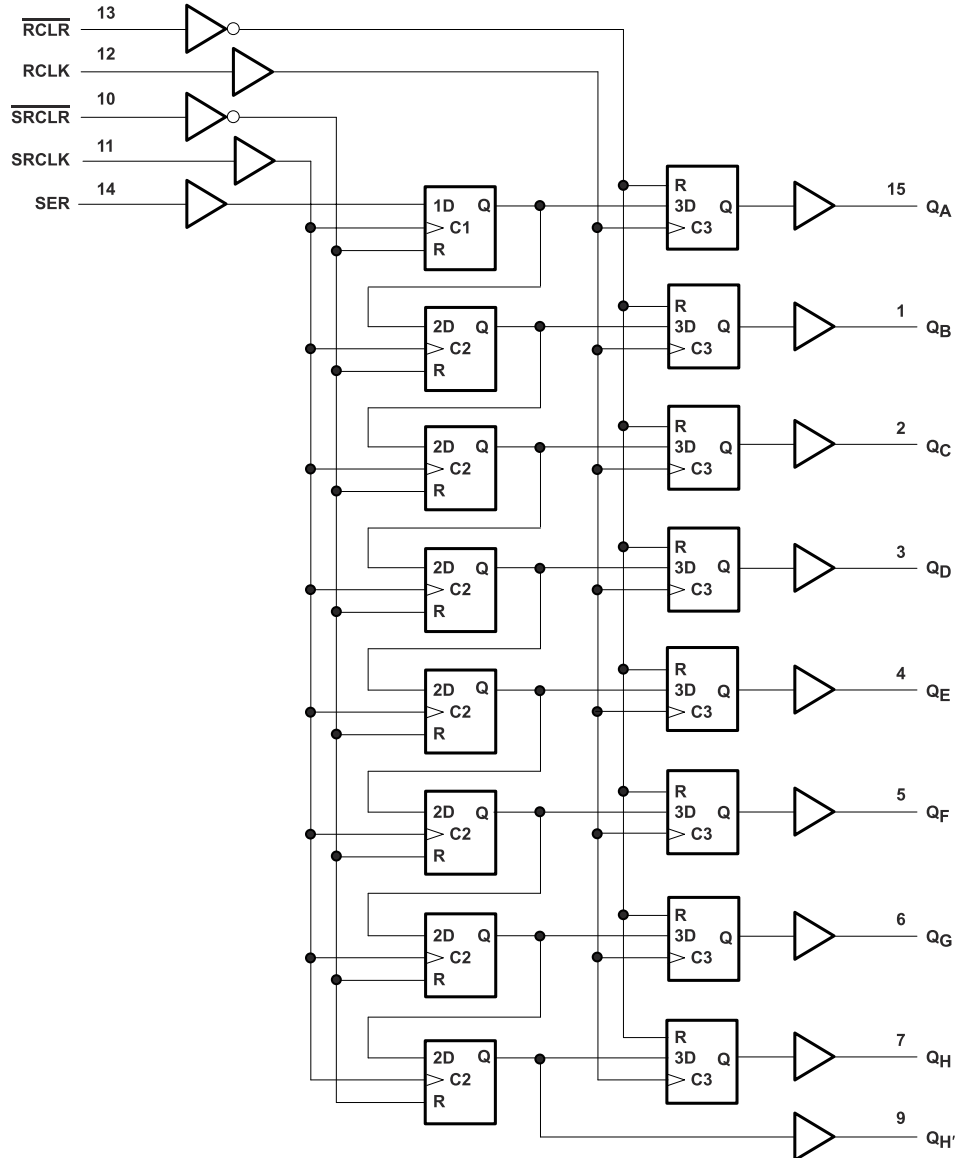
7 Detailed Description

7.1 Overview

The 'AHCT594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{\text{SRCLR}}$, $\overline{\text{RCLR}}$) inputs are provided on both the shift and storage registers. A serial (Q_H') output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

7.2 Functional Block Diagram



7.3 Feature Description

- V_{CC} is optimized at 5 V
- Allow Up voltage translation from 3.3 V to 5 V
 - Inputs accept V_{IH} levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-Voltage compatible

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift-register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift-register data is stored in the storage register.
X	X	X	↓	H	Storage-register state is not changed.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

SN74AHCT594 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of $0.8\text{ V }V_{IL}$ and $2\text{ V }V_{IH}$. This feature makes it ideal for translating up from 3.3 V to 5 V. [図 8-2](#) shows this type of translation.

8.2 Typical Application

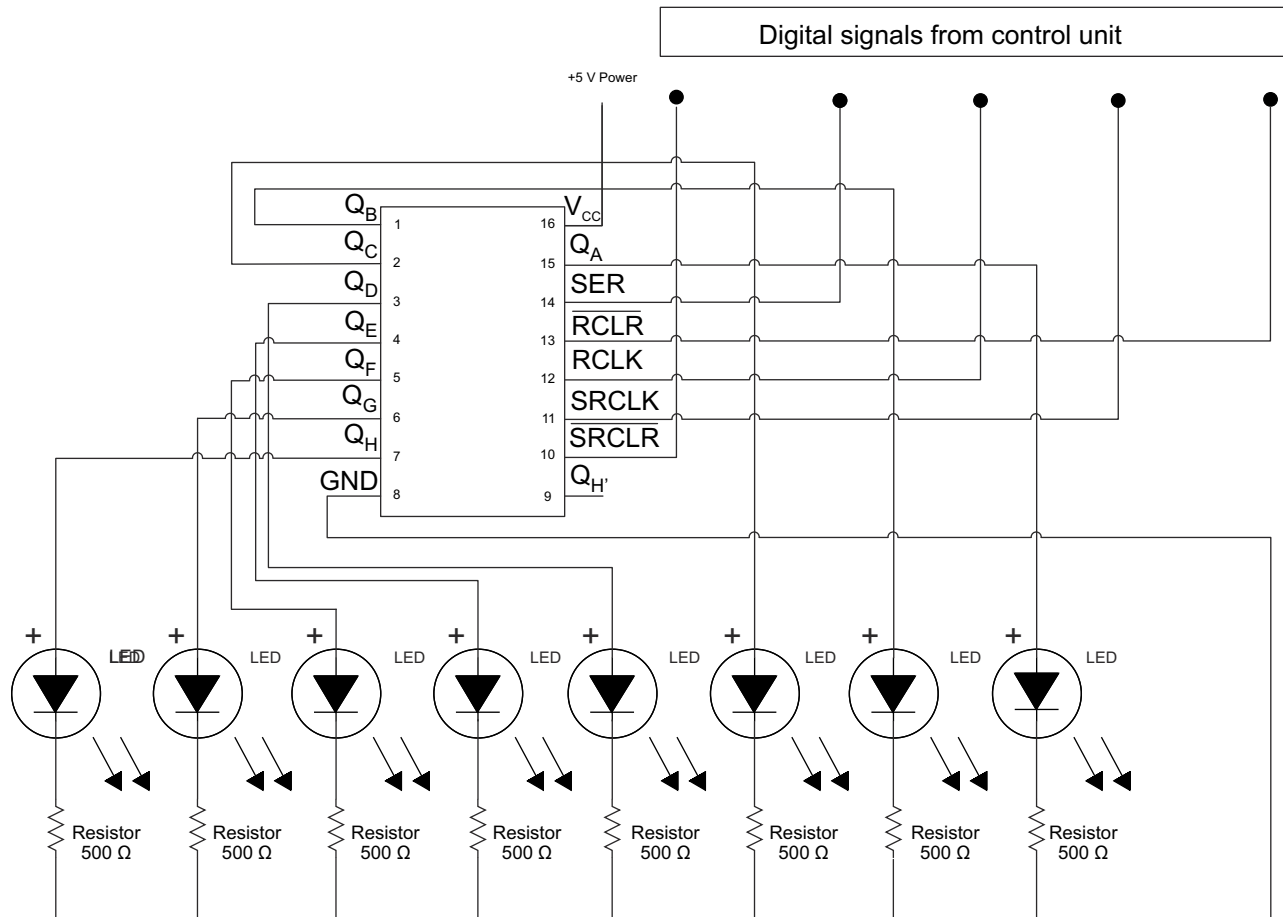


図 8-1. Application Schematic

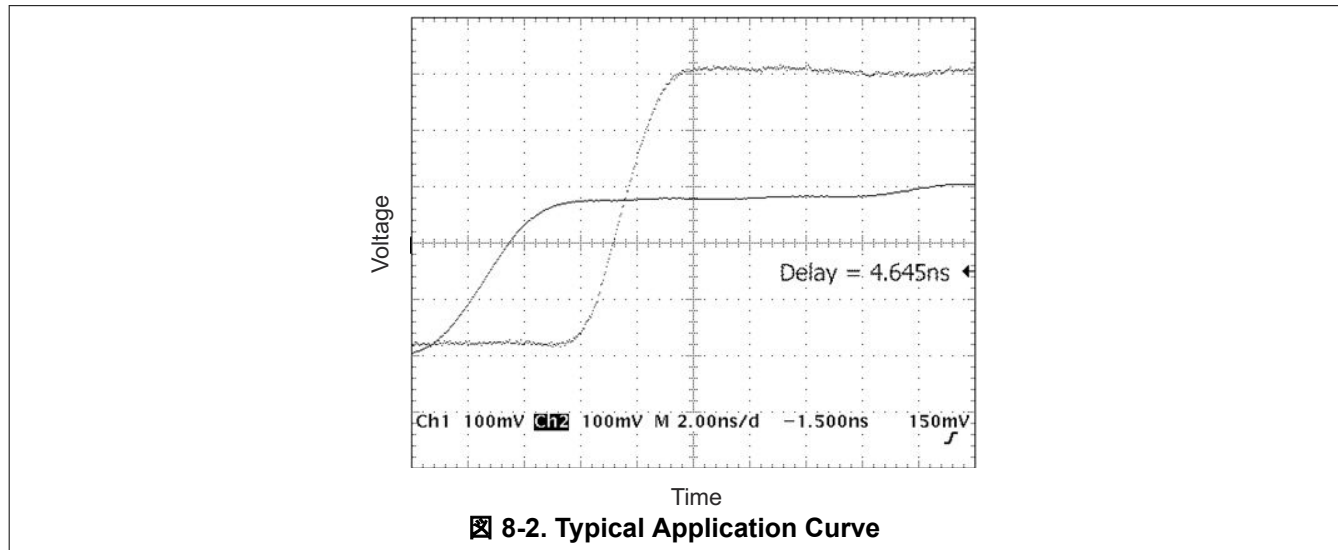
8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input conditions
 - Rise time and fall time specs see ($\Delta t/\Delta V$) in [セクション 5.3](#) table.
 - Specified High and low levels. See (V_{IH} and V_{IL}) in [セクション 5.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommend output conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part
 - Outputs should not be pulled above V_{CC}

8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [セクション 5.3](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [図 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

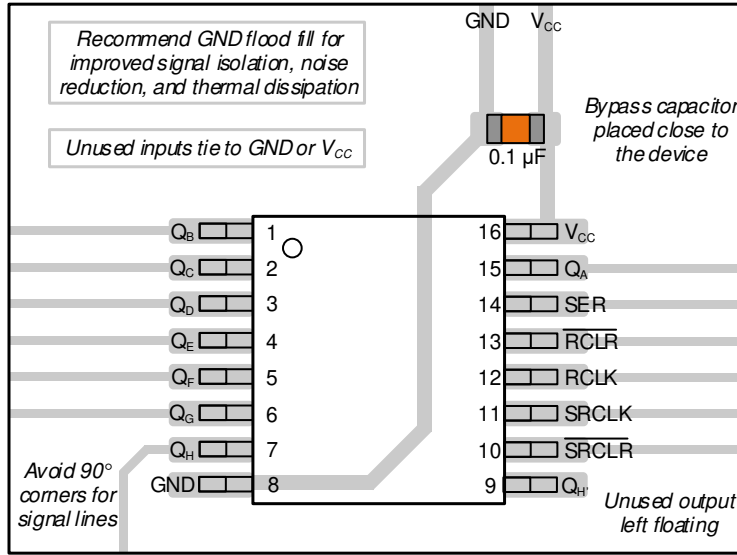


図 8-3. Example Layout for the SN74AHCT594

9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT594	Click here	Click here	Click here	Click here	Click here

9.2 Trademarks

すべての商標は、それぞれの所有者に帰属します。

9.3 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.4 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision J (April 2024) to Revision K (July 2024)	Page
<ul style="list-style-type: none"> Updated thermal values for D package from RθJA = 80.2 to 93.8, RθJC(top) = 39.1 to 54.7, RθJB = 27.7 to 50.9, ΨJT = 9.9 to 20.8, ΨJB = 37.4 to 50.7, RθJC(bot) = N/A, all values in °C/W 	5

Changes from Revision I (December 2014) to Revision J (April 2024)	Page
<ul style="list-style-type: none"> データシート全体にわたってマシン モデルについての記述を削除し、データシートの構造レイアウトを現在の標準に更新 	1
<ul style="list-style-type: none"> Updated RθJA values: DB = 97.5 to 129.6, PW = 105.7 to 135.9; Updated DB and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W 	5
<ul style="list-style-type: none"> Updated layout image 	13

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHCT594D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 125	AHCT594
SN74AHCT594DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB594
SN74AHCT594DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB594
SN74AHCT594DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT594
SN74AHCT594DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT594
SN74AHCT594N	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT594N
SN74AHCT594N.A	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT594N
SN74AHCT594NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT594
SN74AHCT594NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT594
SN74AHCT594PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HB594
SN74AHCT594PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB594

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHCT594 :

- Automotive : [SN74AHCT594-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

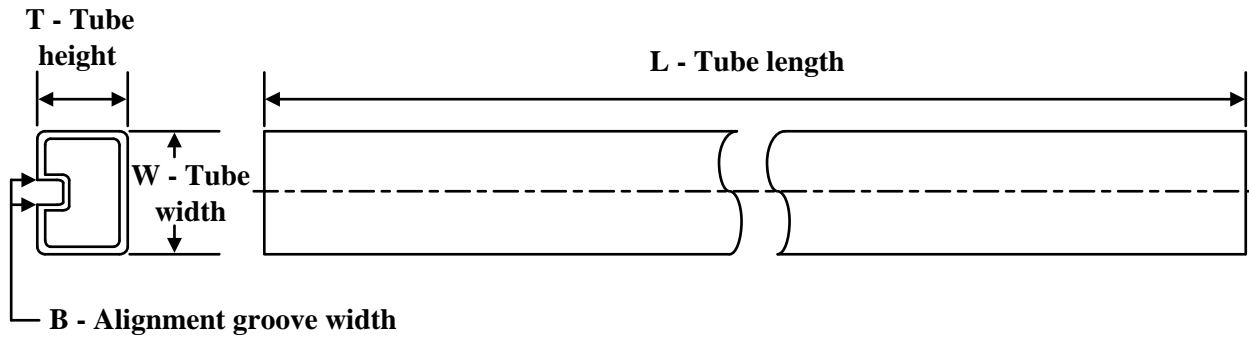
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT594DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT594DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHCT594NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHCT594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



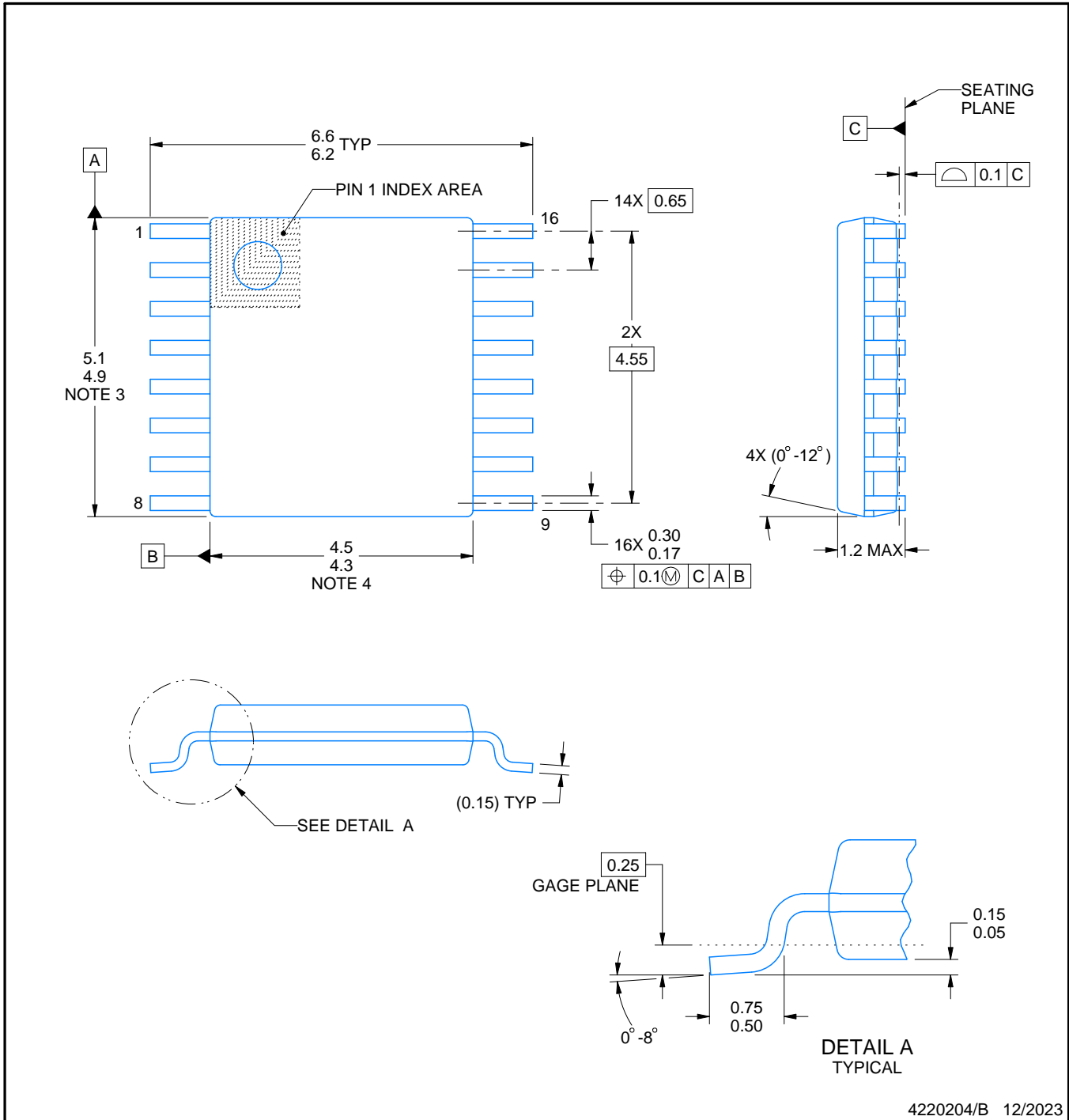
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT594DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHCT594DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT594DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT594NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74AHCT594PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT594N.A	N	PDIP	16	25	506	13.97	11230	4.32



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

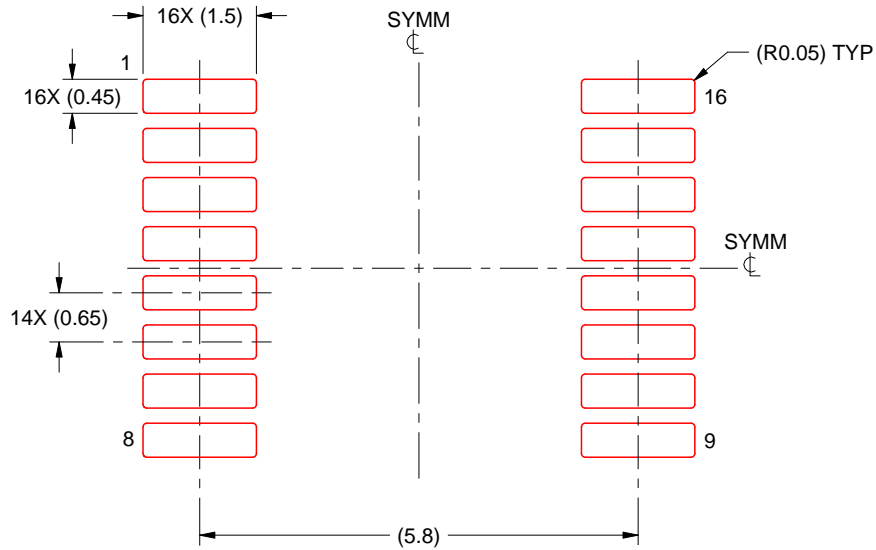
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

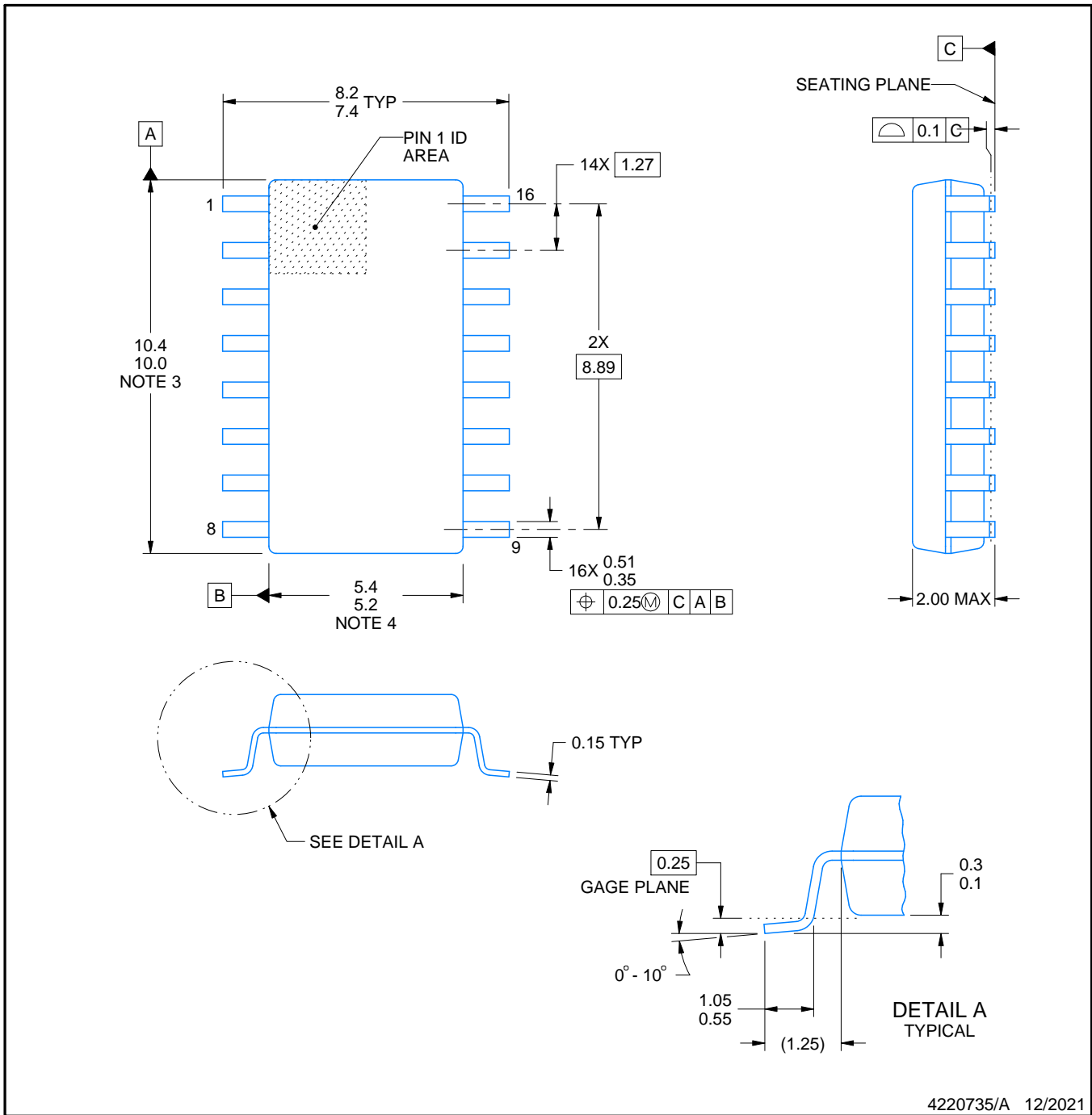


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

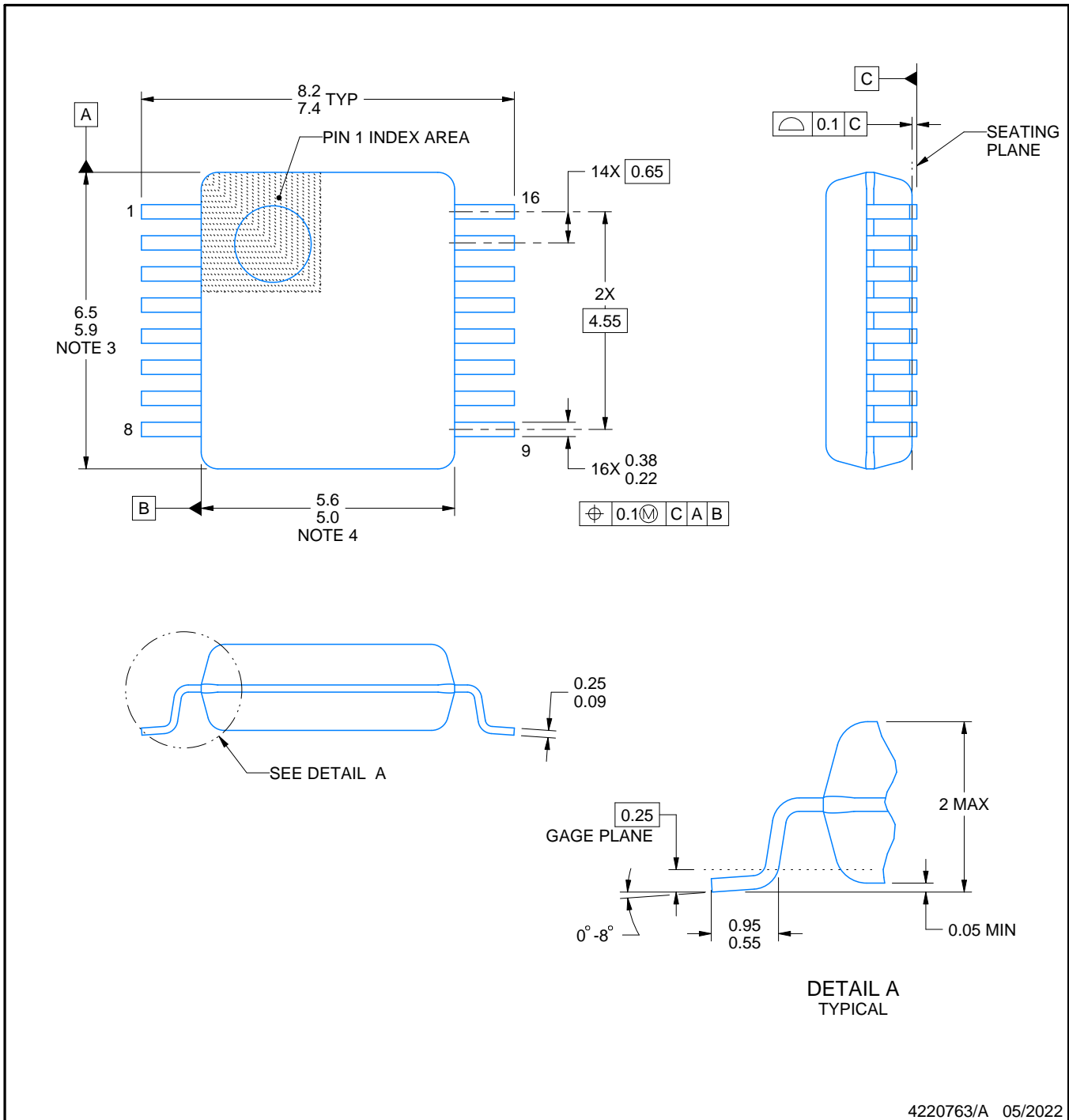
DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

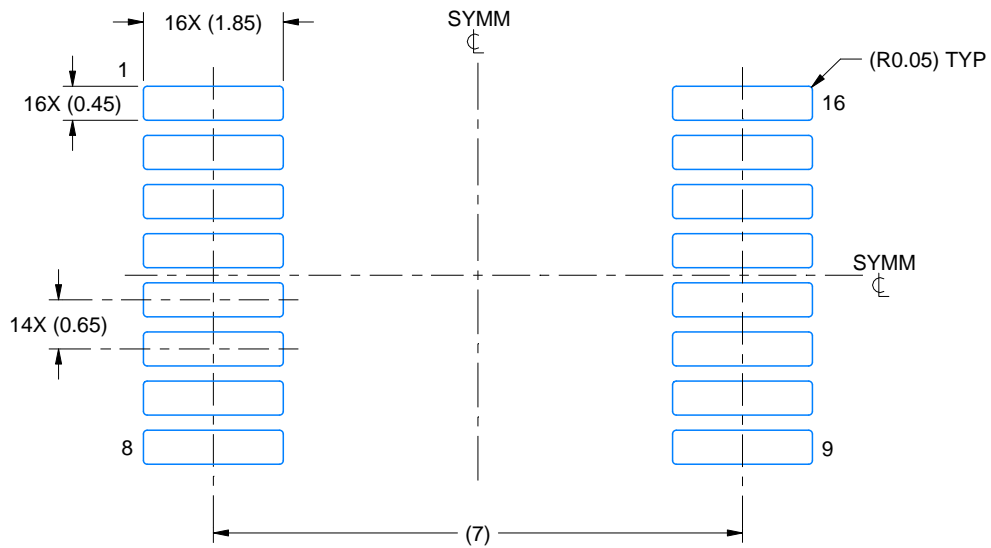
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

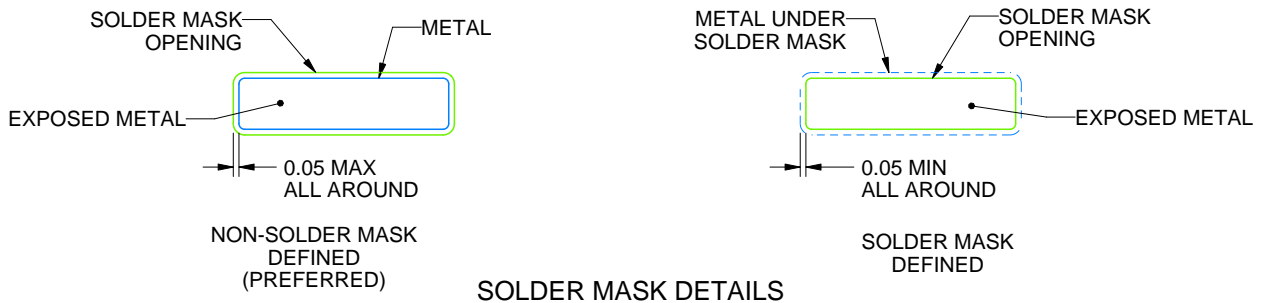
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

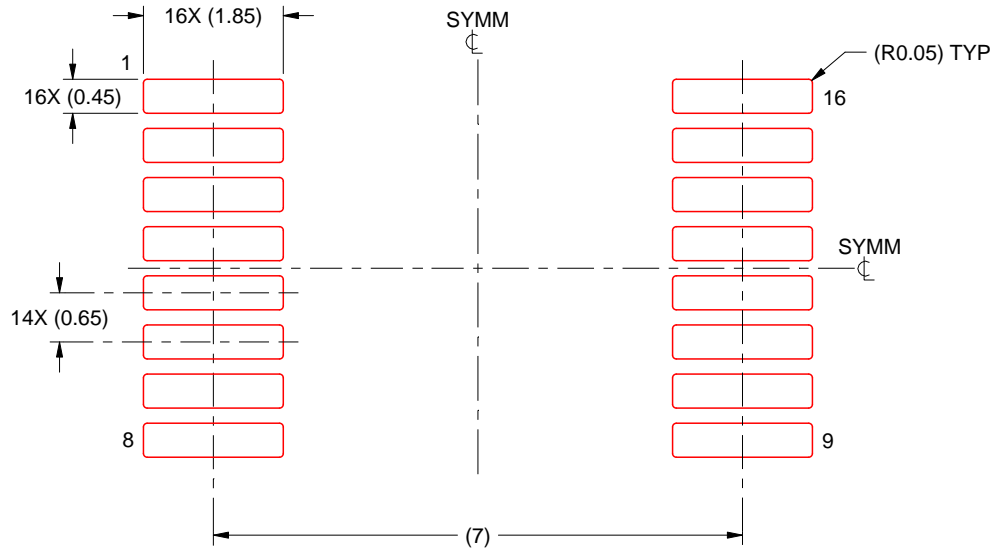
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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