

# SNx4HC257、SNx4HC258 3 ステート出力、クワッド、2 ライン入力 1 ライン出力、データ・セクタ / マルチプレクサ

## 1 特長

- 幅広い動作電圧範囲: 2V~6V
- 大電流反転出力は最大 15 個の LSTTL 負荷を駆動可能
- 低消費電力、最大  $I_{CC}$  80 $\mu$ A
- HC257:  $t_{pd} = 9$ ns (標準値)
- HC258:  $t_{pd} = 12$ ns (標準値)
- 5V で  $\pm 6$ mA の出力駆動能力
- 低い入力電流: 最大 1 $\mu$ A
- 高性能システムの複数のソースからバス・インターフェイスを提供

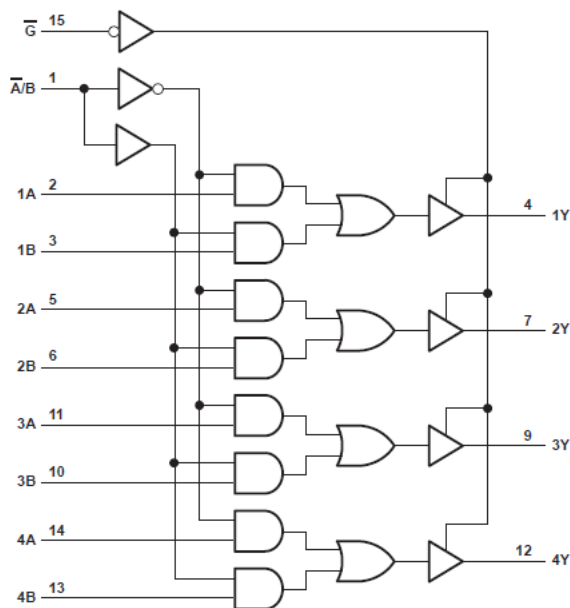
## 2 概要

SNx4HC257 および 258 は、2 つのデータ源の 1 つを選択するための 4 つのデータ・セクタ / マルチプレクサを内蔵しています。すべてのチャンネルは、同じアドレス選択 ( $\bar{A}/B$ ) 入力とアクティブ LOW のストロブ ( $\bar{G}$ ) 入力により制御されます。 $\bar{G}$  ピンが HIGH レベルになると、すべての出力が強制的に高インピーダンス状態になります。257 は非反転出力であり、258 は反転出力です。

### デバイス情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
SN74HC257D	SOIC (16)	9.90mm × 3.90mm
SN74HC257N	PDIP (16)	19.31mm × 6.35mm
SN74HC257NS	SO (16)	6.20mm × 5.30mm
SN74HC257PW	TSSOP (16)	5.00mm × 4.40mm
SN74HC258D	SOIC (16)	9.90mm × 3.90mm
SN74HC258N	PDIP (16)	19.31mm × 6.35mm
SN74HC258NS	SO (16)	6.20mm × 5.30mm
SN74HC258PW	TSSOP (16)	5.00mm × 4.40mm
SN54HC257J	CDIP (16)	24.38mm × 6.92mm
SNJ54HC257FK	LCCC (20)	8.89mm × 8.45mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ここに示すピン番号は D、J、N、NS、PW の各パッケージのものであります。

### SN74HC257 の機能ブロック図



## Table of Contents

<b>1 特長</b> .....	1	7.2 Functional Block Diagram.....	9
<b>2 概要</b> .....	1	7.3 Device Functional Modes.....	10
<b>3 Revision History</b> .....	2	<b>8 Power Supply Recommendations</b> .....	11
<b>4 Pin Configuration and Functions</b> .....	3	<b>9 Layout</b> .....	11
<b>5 Specifications</b> .....	4	9.1 Layout Guidelines.....	11
5.1 Absolute Maximum Ratings.....	4	<b>10 Device and Documentation Support</b> .....	12
5.2 Recommended Operating Conditions <sup>(1)</sup> .....	4	10.1 Documentation Support.....	12
5.3 Thermal Information.....	4	10.2 Receiving Notification of Documentation Updates..	12
5.4 Electrical Characteristics.....	5	10.3 サポート・リソース.....	12
5.5 Switching Characteristics.....	6	10.4 Trademarks.....	12
5.6 Operating Characteristics.....	7	10.5 Electrostatic Discharge Caution.....	12
<b>6 Parameter Measurement Information</b> .....	8	10.6 Glossary.....	12
<b>7 Detailed Description</b> .....	9	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	12
7.1 Overview.....	9		

### 3 Revision History

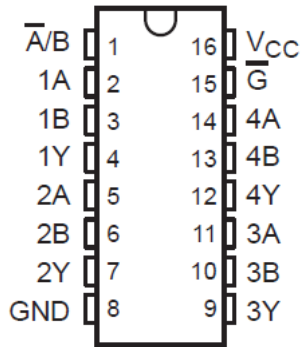
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

#### Changes from Revision B (September 2003) to Revision C (March 2022)

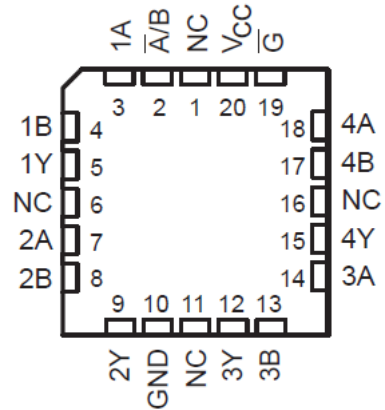
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- 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新..... 1

## 4 Pin Configuration and Functions



**J, D, N, NS, or PW package**  
**16-Pin CDIP, SOIC, PDIP, SO, TSSOP**  
**Top View**



NC – No internal connection

**FK package**  
**20-Pin LCCC**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	(V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )		±20 mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±35 mA
	Continuous current through V <sub>CC</sub> or GND			±70 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions<sup>(1)</sup>

		SN54HC257, SN54HC258			SN74HC257, SN74HC258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5	1.5		V	
		V <sub>CC</sub> = 4.5 V		3.15	3.15			
		V <sub>CC</sub> = 6 V		4.2	4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V			0.3	0.5	V	
		V <sub>CC</sub> = 4.5 V			0.9	1.35		
		V <sub>CC</sub> = 6 V			1.2	1.8		
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V	
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V	
t <sub>t</sub>	Input transition rise/fall time	V <sub>CC</sub> = 2 V			1000	1000	ns	
		V <sub>CC</sub> = 4.5 V			500	500		
		V <sub>CC</sub> = 6 V			400	400		
T <sub>A</sub>	Operating free-air temperature	-55		125	-40	85	°C	

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

### 5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	73	67	64	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC257, SN54HC258		SN74HC257, SN74HC258		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
	I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1	0.1	V	
		4.5 V		0.001	0.1		0.1	0.1		
		6 V		0.001	0.1		0.1	0.1		
	I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26		0.4	0.33		
	I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26		0.4	0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000	±1000	nA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0	6 V		±0.01	±0.5		±10	±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8		160	80	μA	
C <sub>i</sub>		2 V to 6 V		3	10		10	10	pF	

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.5 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (See [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			SN54HC257		SN74HC257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Any Y	2		50	100		150		125	ns
			4.5		10	20		30		25	
			6		9	17		25		21	
	$\bar{A}/B$	Any Y	2		50	100		150		125	
			4.5		10	20		30		25	
			6		9	17		25		21	
$t_{en}$	$\bar{G}$	Any Y	2		75	150		225		190	ns
			4.5		15	30		45		38	
			6		13	26		38		32	
$t_{dis}$	$\bar{G}$	Any Y	2		75	150		225		190	ns
			4.5		15	30		45		38	
			6		13	26		38		32	
$t_t$		Any Y	2		28	60		90		75	ns
			4.5		8	12		18		15	
			6		6	10		15		13	

## 5.5 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (See [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			SN54HCT257		SN74HC257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Any Y	2		75	150		245		190	ns
			4.5		15	30		45		38	
			6		13	26		38		32	
	$\bar{A}/B$	Any Y	2		75	150		245		190	
			4.5		15	30		45		38	
			6		13	26		38		32	
$t_{en}$	$\bar{G}$	Any Y	2		100	200		300		250	ns
			4.5		24	40		60		50	
			6		18	34		51		43	
$t_t$		Any Y	2		45	210		315		265	ns
			4.5		17	42		63		53	
			6		13	36		53		45	

## 5.5 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (See [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			SN54HC258		SN74HC258		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	A or B	Any Y	2	60	100	150	125	ns		
				4.5	13	20	30	25			
				6	12	17	25	21			
		$\bar{A}/B$	Any Y	2	60	115	175	145			
				4.5	13	23	35	29			
				6	12	20	30	25			
$t_{en}$	Enable time	$\bar{G}$	Any Y	2	70	150	225	190	ns		
				4.5	15	30	45	38			
				6	13	26	38	32			
$t_{dis}$	Diabile time	$\bar{G}$	Any Y	2	75	150	225	190	ns		
				4.5	15	30	45	38			
				6	13	26	38	32			
$t_t$	Transition time		Any Y	2	28	60	90	75	ns		
				4.5	8	12	18	15			
				6	6	10	15	13			

## 5.5 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (See [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			SN54HC258		SN74HC258		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	A or B	Any Y	2	95	150	245	190	ns		
				4.5	23	30	45	38			
				6	21	26	38	32			
		$\bar{A}/B$	Any Y	2	95	165	240	210			
				4.5	23	33	48	42			
				6	21	28	41	36			
$t_{en}$	Enable time	$\bar{G}$	Any Y	2	100	200	300	250	ns		
				4.5	24	40	60	50			
				6	18	34	51	43			
$t_t$	Transition time		Any Y	2	45	210	315	265	ns		
				4.5	17	42	63	53			
				6	13	36	53	45			

## 5.6 Operating Characteristics

$T_A = 25^\circ\text{C}$

		Test Conditions	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per multiplexer	No load	40	pF

## 6 Parameter Measurement Information

$t_{pd}$  is the maximum between  $t_{PLH}$  and  $t_{PHL}$

$t_t$  is the maximum between  $t_{TLH}$  and  $t_{THL}$

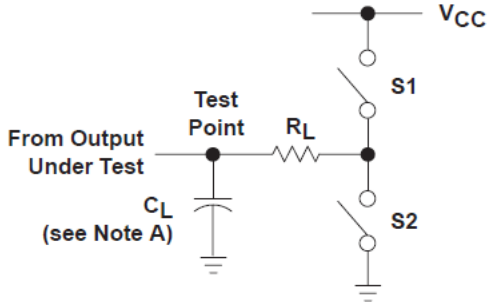


Figure 6-1. Load Circuit

PARAMETER		$R_L$	$C_L$	S1	S2
$t_{en}$	$t_{PZH}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
	$t_{PZL}$			Closed	Open
$t_{dis}$	$t_{PHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{PLZ}$			Closed	Open
$t_{pd}$ or $t_t$		--	50 pF or 150 pF	Open	Open

Figure 6-2.

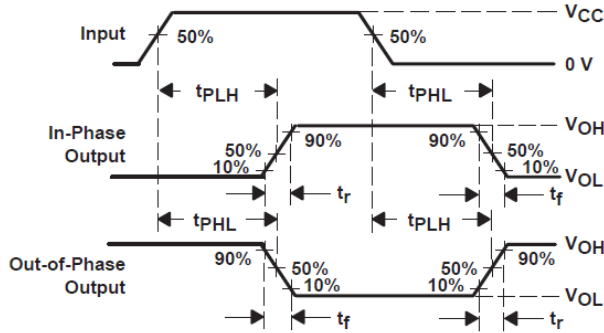


Figure 6-3. Voltage Waveforms  
 Propagation Delay and Output Transition Times

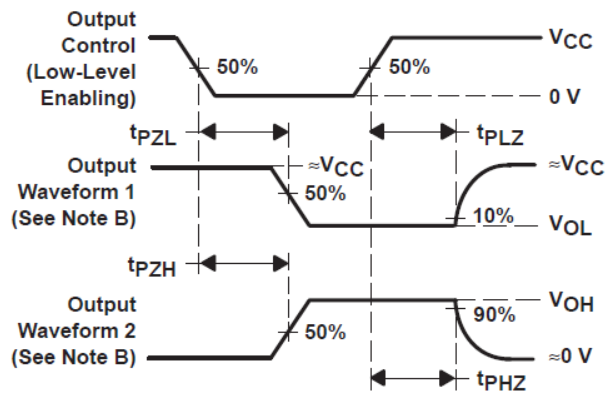


Figure 6-4. Voltage Waveforms  
 Enable and Disable Times For 3-State Outputs

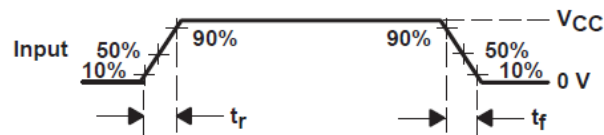


Figure 6-5. Voltage Waveform  
 Input Rise and Fall Times

A.  $C_L$  includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.

D. The outputs are measured one at a time with one input transition per measurement.

E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

## 7 Detailed Description

### 7.1 Overview

These devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ( $\overline{G}$ ) input is at a high logic level.

To ensure the high-impedance state during power up or power down,  $\overline{G}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram

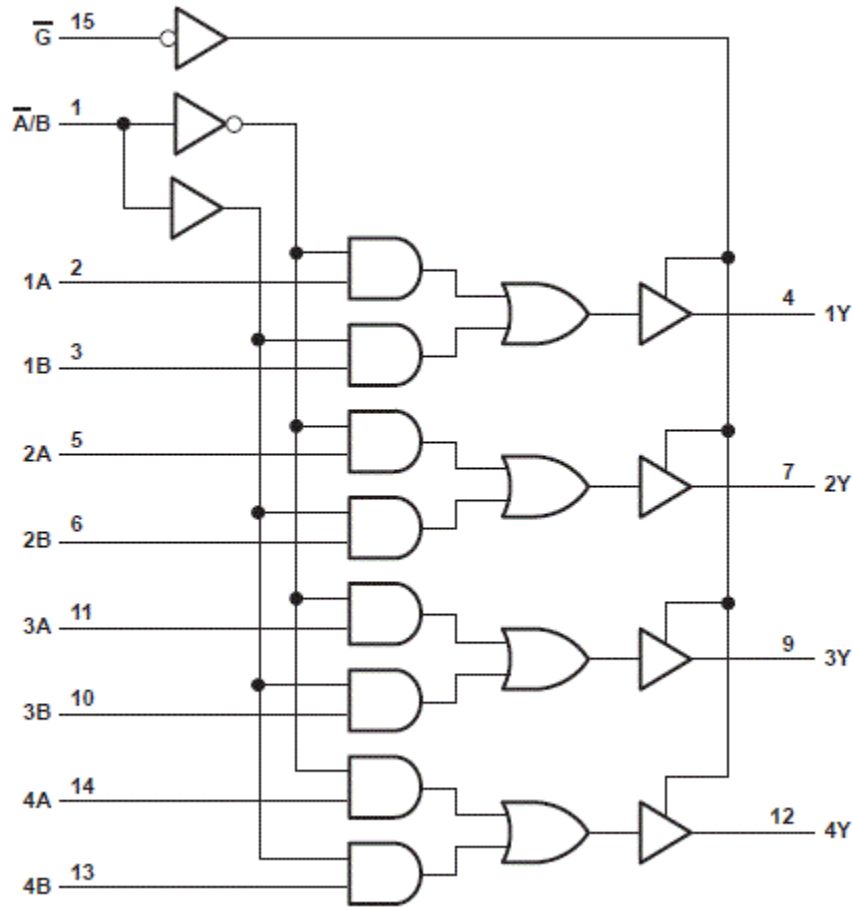


图 7-1. SN74HC257 Functional Block Diagram

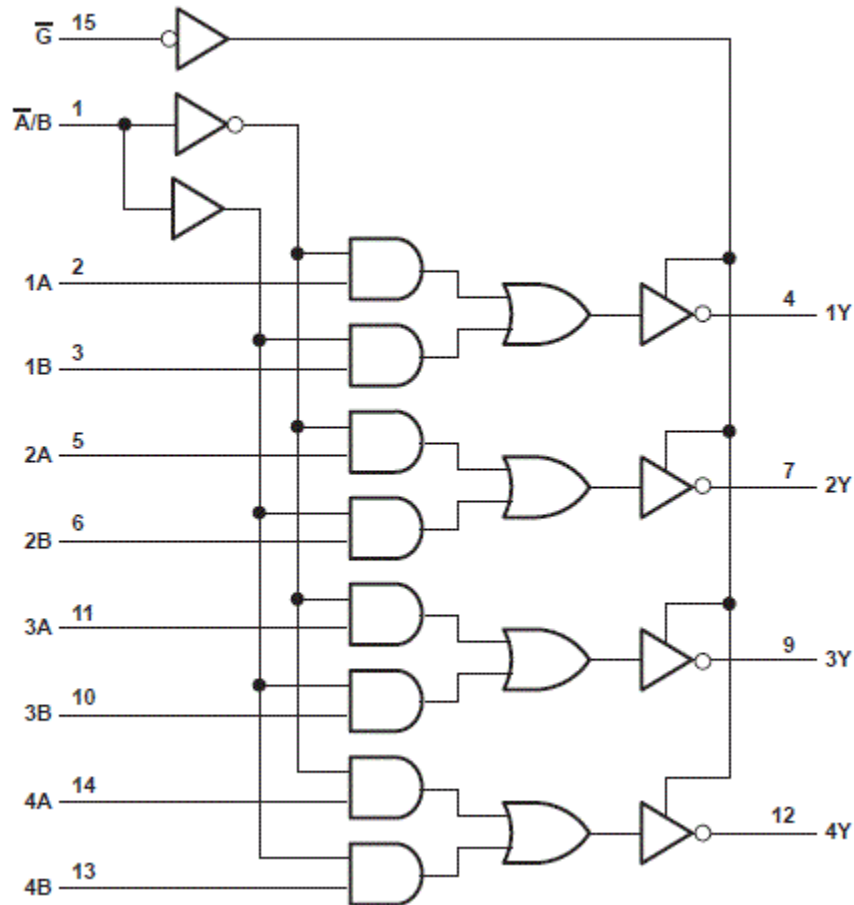


图 7-2. SN74HC258 Functional Block Diagram

### 7.3 Device Functional Modes

表 7-1. Function Table

INPUTS				OUTPUT Y	
$\bar{G}$	$\bar{A}/B$	A	B	'HC257	'HC258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
85124012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85124012A SNJ54HC 257FK
8512401EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512401EA SNJ54HC257J
<a href="#">SN54HC257J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC257J
SN54HC257J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC257J
<a href="#">SN74HC257D</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC257
<a href="#">SN74HC257DR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC257
SN74HC257DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257
SN74HC257DRG4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257
SN74HC257DRG4.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257
<a href="#">SN74HC257DT</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC257
<a href="#">SN74HC257N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC257N
SN74HC257N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC257N
<a href="#">SN74HC257NSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257
SN74HC257NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257
<a href="#">SN74HC257PW</a>	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	HC257
<a href="#">SN74HC257PWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC257
SN74HC257PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257
<a href="#">SN74HC257PWR1G4</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC257
<a href="#">SN74HC258D</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC258
<a href="#">SN74HC258DR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258
SN74HC258DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258
<a href="#">SN74HC258N</a>	NRND	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC258N
SN74HC258N.A	NRND	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC258N
<a href="#">SN74HC258NSR</a>	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258
SN74HC258NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258
<a href="#">SN74HC258PW</a>	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	HC258
<a href="#">SN74HC258PWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC258PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC258
<a href="#">SNJ54HC257FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85124012A SNJ54HC 257FK
SNJ54HC257FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85124012A SNJ54HC 257FK
<a href="#">SNJ54HC257J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512401EA SNJ54HC257J
SNJ54HC257J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8512401EA SNJ54HC257J

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54HC257, SN74HC257 :**

- Catalog : [SN74HC257](#)
- Military : [SN54HC257](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC257DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC257NSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC257PWR1G4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC258DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC258NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC258PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC257DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC257DRG4	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC257NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC257PWR1G4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC258DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC258NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC258PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
85124012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC257N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC257N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC257N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC258N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC257FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC257FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

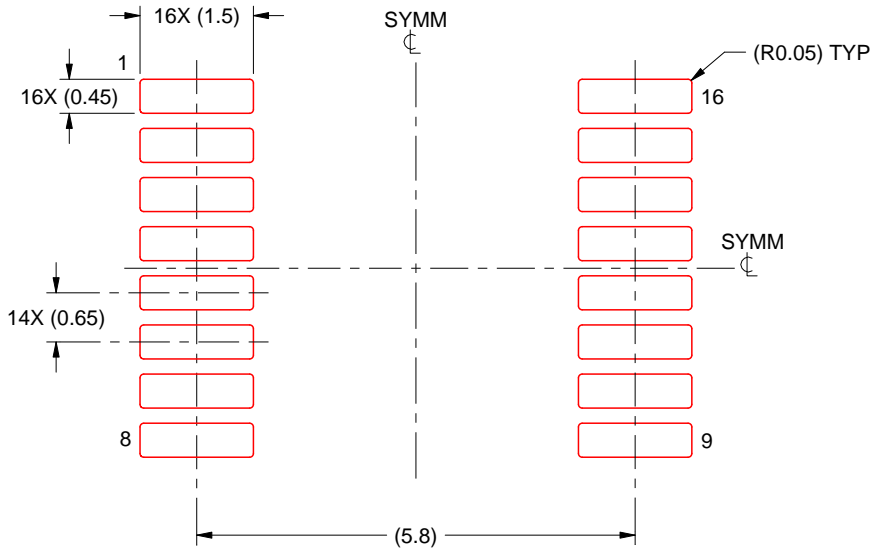
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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