SN74HCS245 3 ステート出力およびシュミット・トリガ入力搭載、オクタル・バス・トランシーバ

1 特長

- 広い動作電圧範囲：2V～6V
- シュミット・トリガ入力により低速の入力信号またはノイズの多い入力信号に対応
- 低い消費電力
  - I_{CC}：100nA (標準値)
  - 入力リーク電流：±100nA (標準値)
- 6V で±7.8mA の出力駆動能力
- 拡張周囲温度範囲：–40℃～+125℃、T_A

2 アプリケーション

- デジタル信号のイネーブルまたはディスエーブル
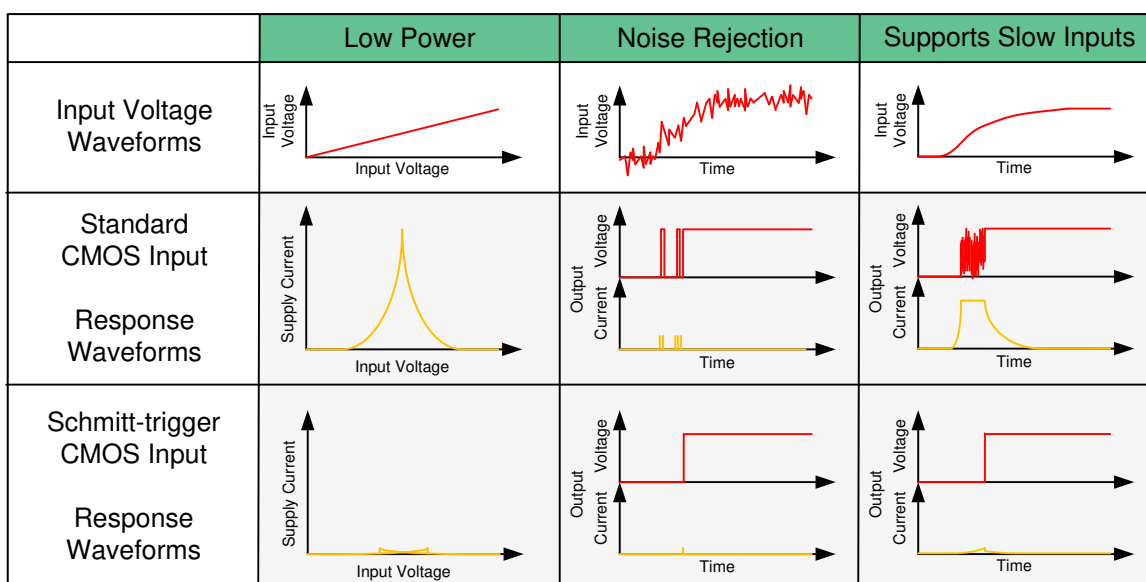- 低速またはノイズの多い信号の除去
- コントローラ・リセット時の信号保持
- スイッチのデバウンス

3 概要

SN74HCS245 は、3 ステート出力とシュミット・トリガ入力を備えたオクタル・バス・トランシーバです。8 つのチャネルはすべて、方向 (DIR) ピンと出力イネーブル ($\overline{OE}$) ピンにより制御されます。

パッケージ情報

部品番号	パッケージ [1]	本体サイズ (公称)
SN74HCS245	RKS (VQFN、20)	4.50mm × 2.50mm
	DGS (SOT、20)	5.10mm × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

	Low Power	Noise Rejection	Supports Slow Inputs
Input Voltage Waveforms			
Standard CMOS Input Response Waveforms			
Schmitt-trigger CMOS Input Response Waveforms			

シュミット・トリガ入力の利点

English Data Sheet: SCLS879

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

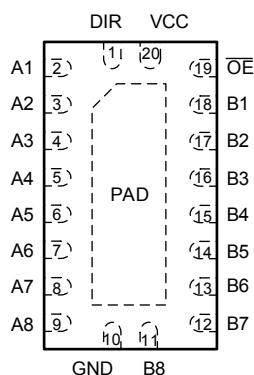| Changes from Revision * (January 2022) to Revision A (October 2022)	Page
• 事前情報から量産データに変更... 1	
• Added DGS package pinout diagram.. 3	
• Added DGS (SOT) Thermal Information.. 4	

5 Pin Configuration and Functions

図 5-1. RKS Package, 20-Pin VQFN (Top View)
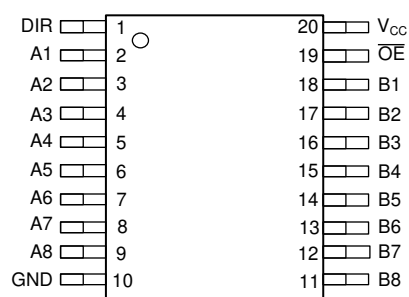
図 5-2. DGS Package, 20-Pin SOT (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DIR	1	I	Direction control input (L = B → A, H = A → B)
A1	2	I/O	Channel 1 output/input A
A2	3	I/O	Channel 2 output/input A
A3	4	I/O	Channel 3 output/input A
A4	5	I/O	Channel 4 output/input A
A5	6	I/O	Channel 5 output/input A
A6	7	I/O	Channel 6 output/input A
A7	8	I/O	Channel 7 output/input A
A8	9	I/O	Channel 8 output/input A
GND	10	G	Ground
B8	11	I/O	Channel 8 input/output B
B7	12	I/O	Channel 7 input/output B
B6	13	I/O	Channel 6 input/output B
B5	14	I/O	Channel 5 input/output B
B4	15	I/O	Channel 4 input/output B
B3	16	I/O	Channel 3 input/output B
B2	17	I/O	Channel 2 input/output B
B1	18	I/O	Channel 1 input/output B
$\overline{OE}$	19	I	Output enable, active low
V_{CC}	20	P	Positive supply
Thermal Pad[2]	—	—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) RKS Package Only

Product Folder Links: SN74HCS245

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
I_{IK}	Input clamp current[2]	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current[2]	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature[3]			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1)   Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2)   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3)   Specified by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), pper ANSI/ESDA/JEDEC JS-002[2]	±1500	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74HCS245		UNIT
		RKS (VQFN)	DGS (SOT)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.6	124.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.9	62.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.6	79.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.0	7.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	48.9	78.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	32.0	N/A	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})[1]			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$		V
			I_{OH} = -6 mA	4.5 V	4.0	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0	$V_I = V_{CC}$ or 0	6 V		±100	±1000	nA
I_{OZ}	Off-State (High-Impedance State) Output Current	$V_O = V_{CC}$ or 0	$V_O = V_{CC}$ or 0	6 V		0.01	2	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF

(1)   Specified by design.

6.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurment Information*. C_L = 50 pF.

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A or B	B or A	2 V		21	32			49	ns
				4.5 V		8	13			15	
				6 V		7	11			13	
t_{en}	Enable time	$\overline{OE}$	A or B	2 V		52	77			95	ns
				4.5 V		20	30			38	
				6 V		16	24			31	
t_{dis}	Disable time	$\overline{OE}$	A or B	2 V		36	54			63	ns
				4.5 V		16	24			30	
				6 V		14	21			25	
t_t	Transition-time		Any output	2 V			13			16	ns
				4.5 V			7			9	
				6 V			6			8	

Product Folder Links: *SN74HCS245*

6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		40		pF

6.8 Typical Characteristics

T_A = 25°C
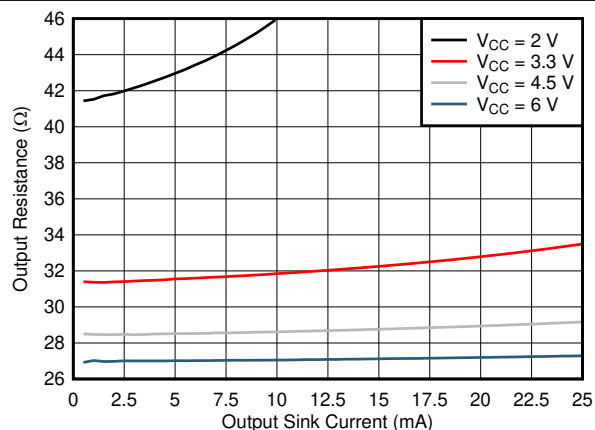
図 6-1. Output Driver Resistance in LOW State
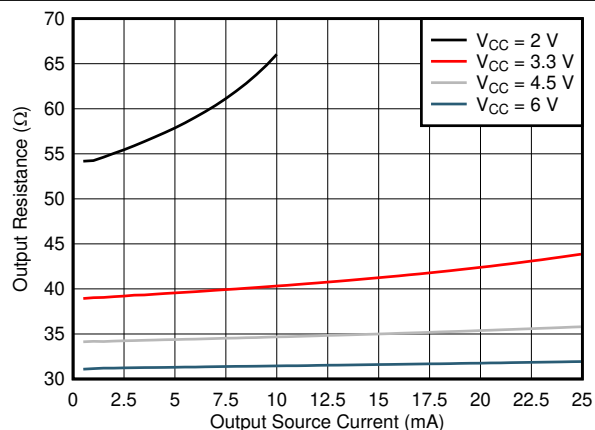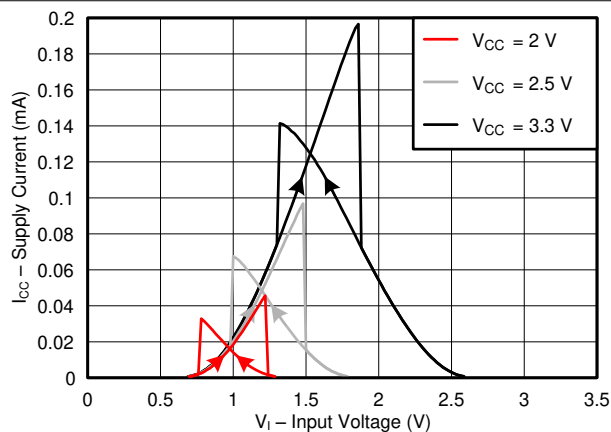

図 6-2. Output Driver Resistance in HIGH State.

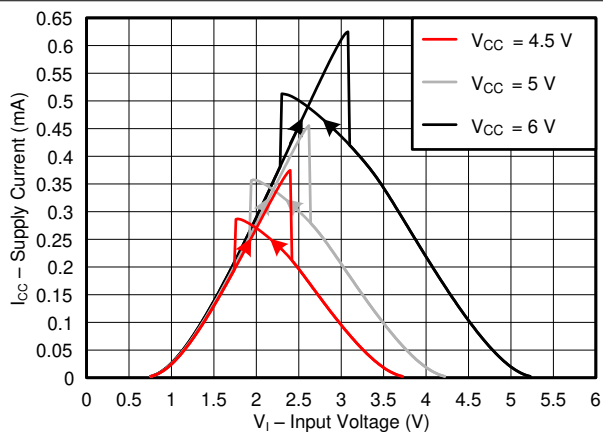図 6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply

図 6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply

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7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.
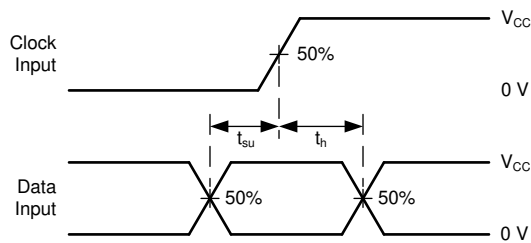
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.
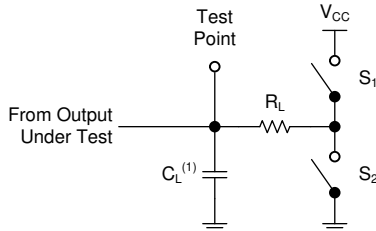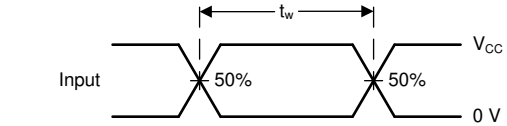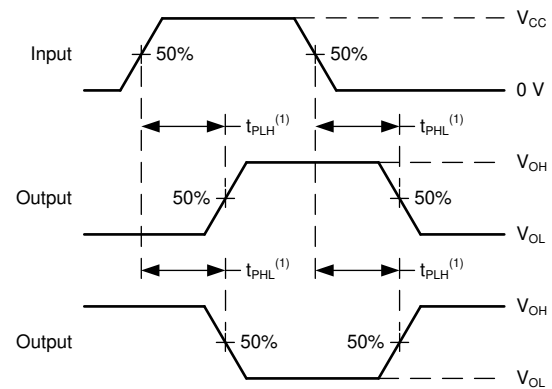

(1) C_L includes probe and test-fixture capacitance.

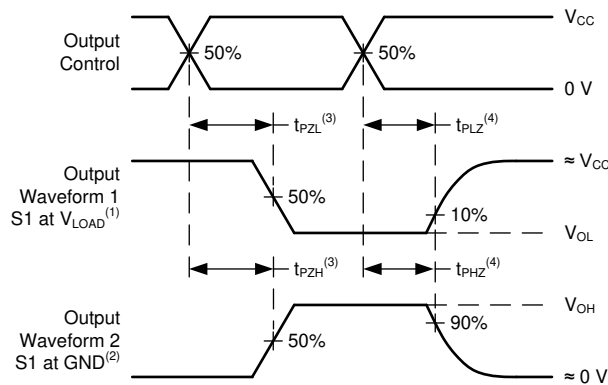**図 7-1. Load Circuit for 3-State Outputs**

図 7-2. Voltage Waveforms, Pulse Duration

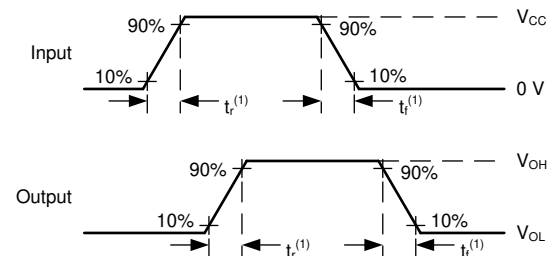**図 7-3. Voltage Waveforms, Setup and Hold Times**

(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 7-4. Voltage Waveforms Propagation Delays

図 7-5. Voltage Waveforms Propagation Delays

(1) The greater between t_r and t_f is the same as t_t.

図 7-6. Voltage Waveforms, Input and Output Transition Times

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8 Detailed Description

8.1 Overview

The SN74HCS245 contains 8 individual high speed CMOS transceivers with Schmitt-trigger inputs and 3-state outputs.

Each transceiver includes one buffer oriented from Ax to Bx and one from Bx to Ax, with at least one output disabled at all times. The direction (DIR) pin controls which buffer is active. The buffer that is not active has the output placed into the high-impedance state.

The output enable ($\overline{OE}$) controls all outputs in the device. When the $\overline{OE}$ pin is in the low state, the appropriate outputs as determined by the direction (DIR) pin are enabled. When the $\overline{OE}$ pin is in the high state, all outputs of the device are disabled. All disabled outputs are placed into the high-impedance state.

To ensure the high-impedance state during power up or power down, the $\overline{OE}$ pin should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table. Typically a 10-kΩ resistor will be sufficient.

8.2 Functional Block Diagram
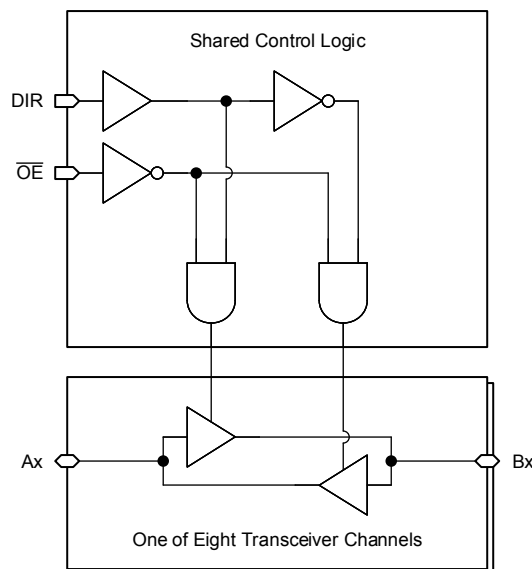
図 8-1. Logic Diagram (Positive Logic) for SN74HCS245

8.3 Feature Description

8.3.1 CMOS IOs

This device includes CMOS IOs. These pins can be configured as either an input or an output. The output has the balanced 3-state architecture, and the input has the Schmitt-trigger architecture.

The three states that these outputs can be in are driving high, driving low, and high impedance. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When the pin is configured as an input, the output is placed into a high-impedance state and it will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external

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factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. Because this pin also includes an input, the voltage should always be defined.

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Unused transceiver channels should be terminated as shown in Figure 8-2.

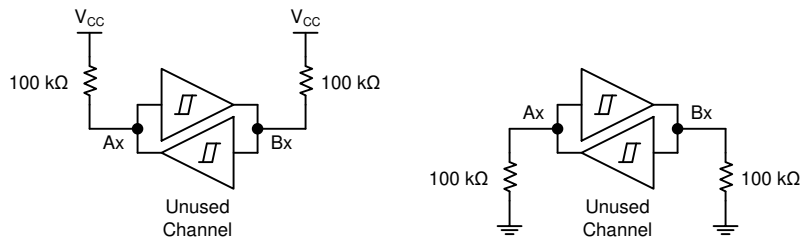**図 8-2. Proper termination of unused transceiver channels**

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

8.3.3 Clamp Diode Structure

As shown in 図 8-3, the inputs and outputs to this device have both positive and negative clamping diodes.

> **注意**
>
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
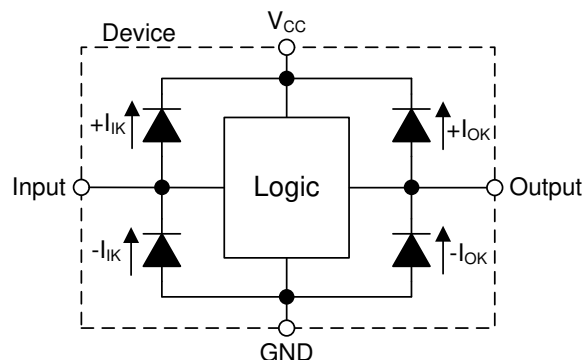

図 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Function Table lists the functional modes of the SN74HCS245.

表 8-1. Function Table

INPUTS[1]		OUTPUTS[2]	
OE	DIR	A	B
L	L	B	Z
L	H	Z	A
H	X	Z	Z

(1)   H = High voltage level, L = Low voltage level, X = Don't care
(2)   A = Logic value at 'A' input, B = Logic value at 'B' input, Z = High
       impedance

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9 Application and Implementation

> 注
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74HCS245 can be used to drive signals over relatively long traces or transmission lines. In order to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.
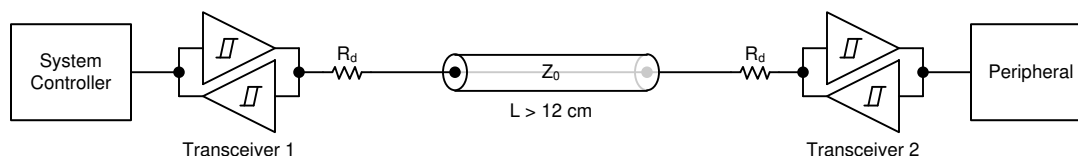
9.2 Typical Application

図 9-1. Application block diagram

9.2.1 Design Requirements

- All signals in the system operate at 5 V
- Avoid unstable state by not having LOW signals on both inputs
- Q output is HIGH when $\overline{S}$ is LOW
  - Q output remains HIGH until $\overline{R}$ is LOW

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS245 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS245 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS245 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74HCS245 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

注意

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74HCS245 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS245 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS245 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.
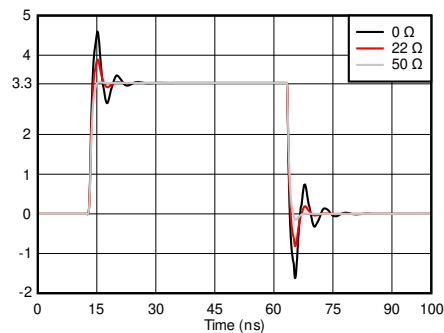
9.2.3 Application Curves

図 9-2. Simulated Signal Integrity at the Reciever With Different Damping Resistor (R_d) Values

Product Folder Links: *SN74HCS245*

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example
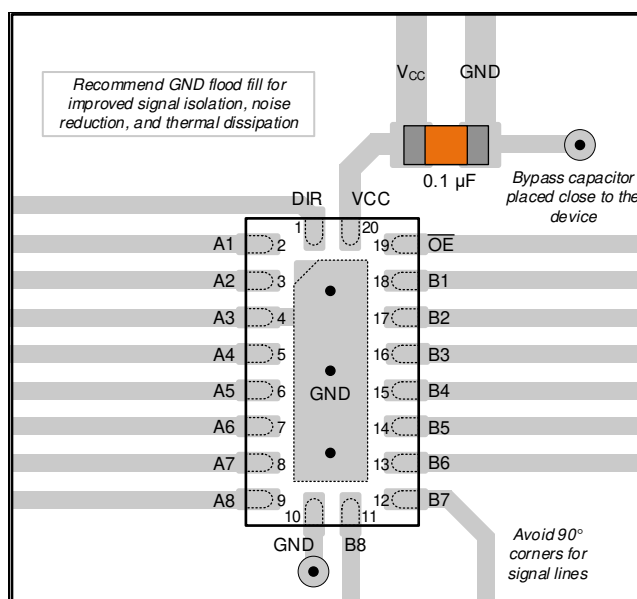
図 11-1. Example layout for the SN74HCS245 in the RKS package.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *SN74HCS245*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS245DGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HS245	Samples
SN74HCS245RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCS245 :

• Automotive : SN74HCS245-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

K0   P1

B0   W

Cavity   A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

| Q1 | Q2 | | Q1 | Q2 |

| Q3 | Q4 | | Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS245DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74HCS245RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS245DGSR	VSSOP	DGS	20	5000	356.0	356.0	35.0
SN74HCS245RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

RKS 20

2.5 x 4.5, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4226872/A

A | 2.6 / 2.4 | B

PIN 1 INDEX AREA

4.6 / 4.4

// | 0.1 | C

1.0 / 0.8

0.05 / 0.00

C

SEATING PLANE

⌒ | 0.08 | C

1 ± 0.1

2X | 0.5

14X | 0.5

10

11

9

12

EXPOSED THERMAL PAD

2X

3.5

3 ± 0.1

2

19

PIN 1 ID (OPTIONAL)

1   20

20X | 0.30 / 0.18

20X | 0.5 / 0.3

⊕ | 0.1 Ⓜ | C | A | B
      | 0.05 Ⓜ |

(0.2) TYP
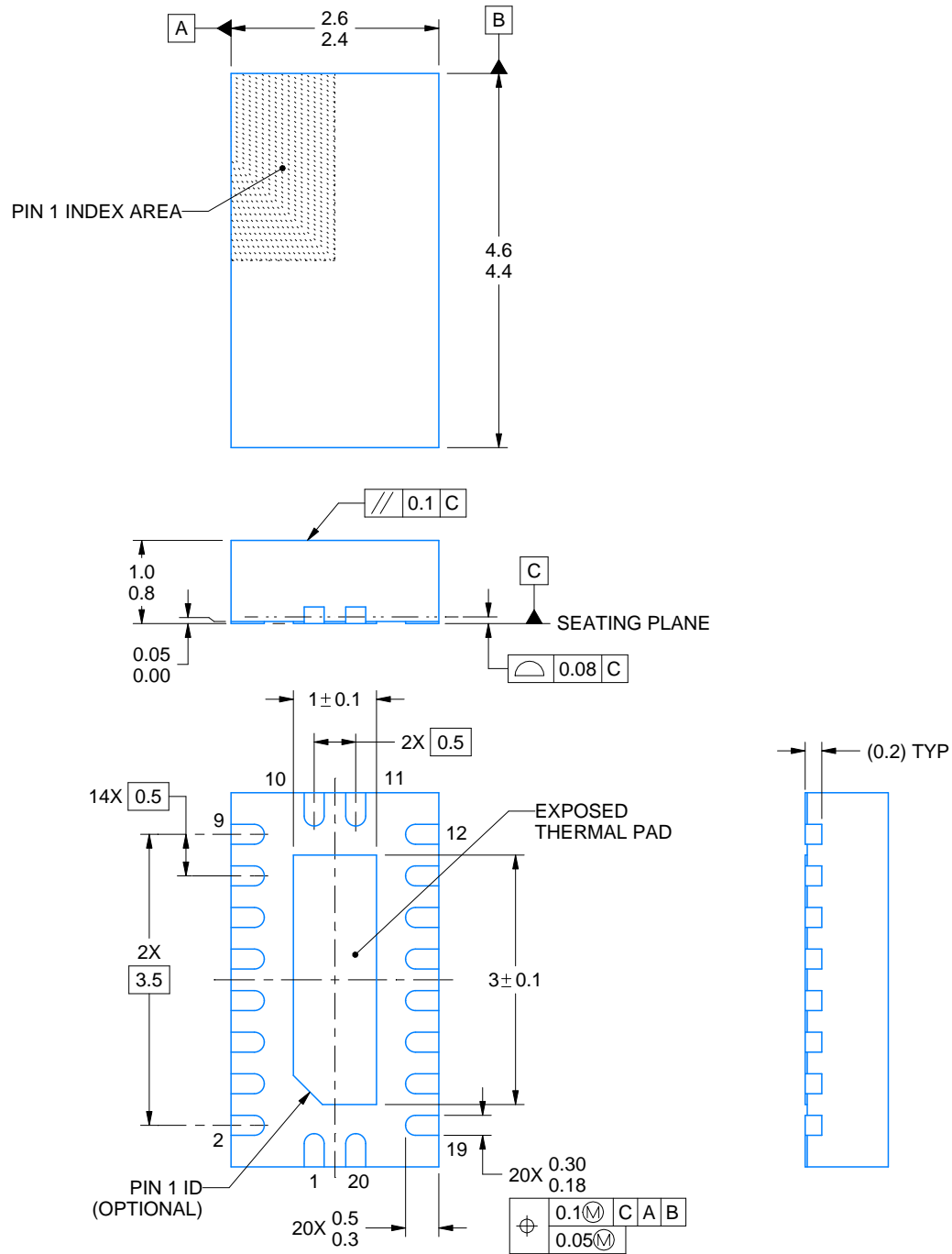
4222490/B   02/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

(1)

SYMM

20X (0.6)

2

20X (0.24)

SYMM

16X (0.5)

(R0.05) TYP

(⌀ 0.2) VIA TYP

(1.25)

(3)

(4.3)

(2.3)

1 20 19

9 12

10 11
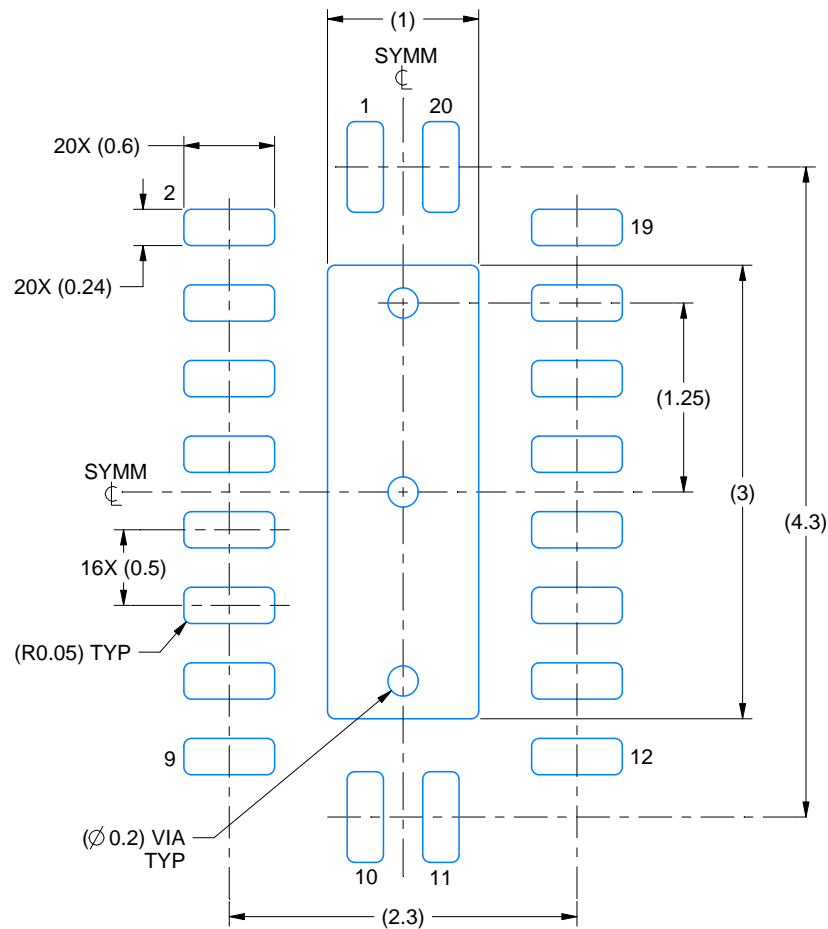
LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED
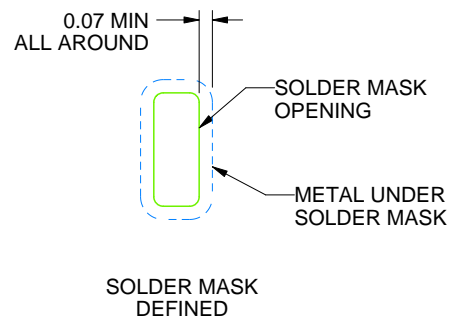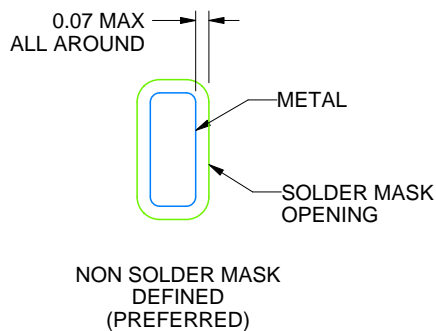
SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

2X (0.95)

1   20

20X (0.6)

2

20X (0.24)

19

16X (0.5)

2X (1.31)

SYMM
₵

(4.3)

(0.76)

METAL
TYP

9

12

(R0.05) TYP

10   11

SYMM
₵

(2.3)
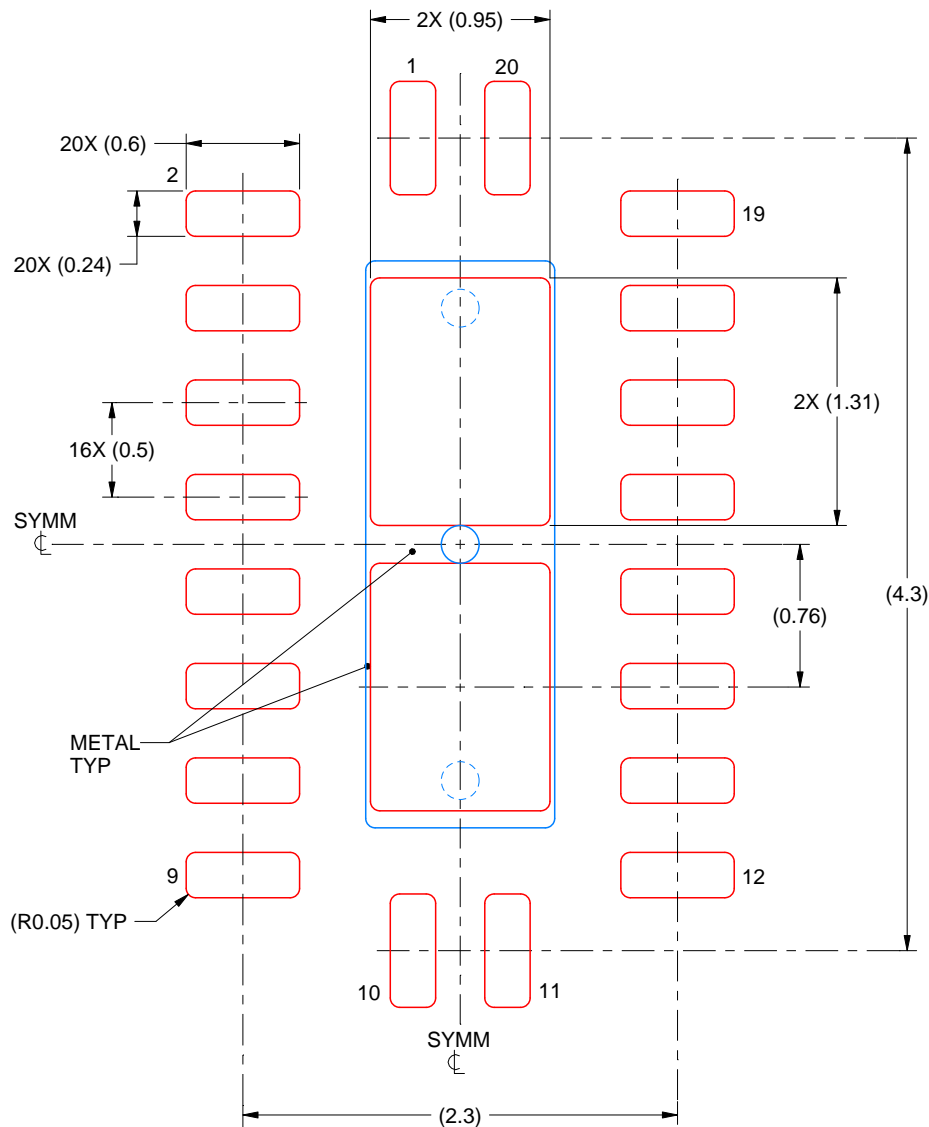
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B   02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.