

SN74HCS595 シュミット・トリガ入力および3ステート出力レジスタ付き、8ビット・シフト・レジスタ

1 特長

- 広い動作電圧範囲: 2V~6V
- シュミット・トリガ入力により低速の信号またはノイズの多い信号に対応
- 低消費電力
 - I_{CC} : 100nA (標準値)
 - 入力リーク電流: ± 100 nA (標準値)
- 6V で ± 7.8 mA の出力駆動能力
- 広い周囲温度範囲: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$, T_A

2 アプリケーション

- 出力拡張
- LED マトリクス制御
- 7 セグメント・ディスプレイ制御
- 8 ビット・データ・ストレージ

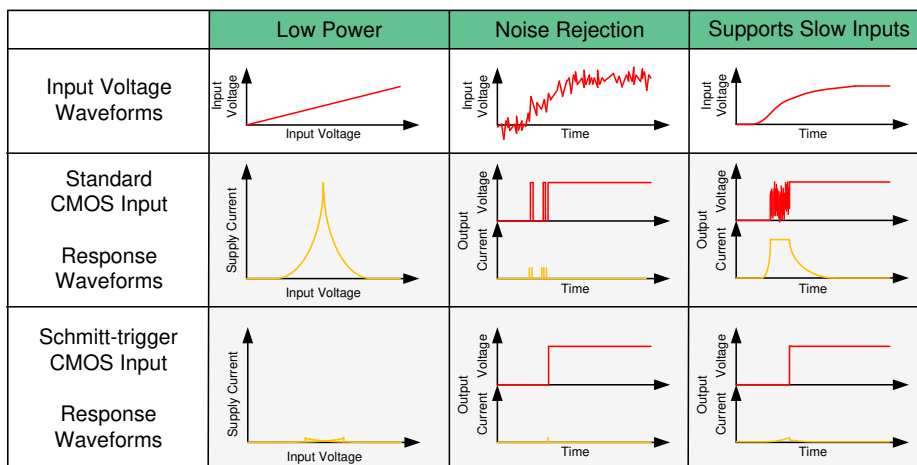
3 概要

SN74HCS595 デバイスには 8 ビットのシリアル・イン、パラレル・アウトのシフト・レジスタが搭載されており、8 ビットの D タイプ・ストレージ・レジスタへデータを供給します。すべての入力はシュミット・トリガを備えているため、低速エッジまたはノイズの多い入力信号による誤ったデータ出力を解消できます。ストレージ・レジスタはパラレルの 3 ステート出力を備えています。シフト・レジスタとストレージ・レジスタの両方に、それぞれ独立したクロックが供給されます。シフト・レジスタはダイレクト・オーバーライディング・クリア ($\overline{\text{SRCLR}}$) 入力、シリアル (SER) 入力、カスケード用シリアル出力 (Q_H) を備えています。出力イネーブル ($\overline{\text{OE}}$) 入力が HIGH のとき、ストレージ・レジスタ出力は高インピーダンス状態になります。内部レジスタ・データおよびシリアル出力 (Q_H) は、 $\overline{\text{OE}}$ 入力の動作による影響を受けません。

デバイス情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN74HCS595PW	TSSOP (16)	5.00mm × 4.40mm
SN74HCS595D	SOIC (16)	9.90mm × 3.90mm
SN74HCS595BQB	WQFN (16)	3.60mm × 2.60mm
SN74HCS595DYY	SOT-23-THN (16)	4.20mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



シュミット・トリガ入力の利点



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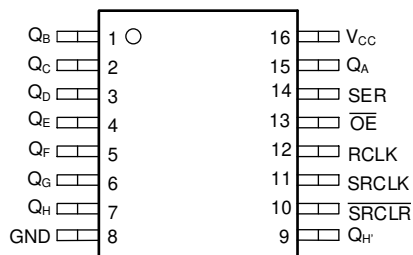
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

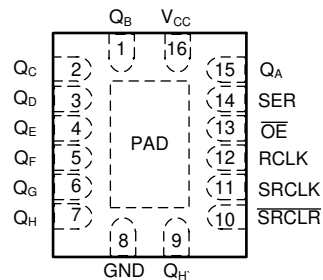
Changes from Revision * (August 2020) to Revision A (October 2020)	Page
• BQB および D パッケージを「アクティブ」ステータスに変更.....	1
• データシートのステータスを「量産データ」に変更.....	1

Changes from Revision A (October 2020) to Revision B (May 2021)	Page
• 「デバイス情報」表に DYY パッケージを追加.....	1
• Added DYY Package pinout diagram and information to <i>Pin Configuration and Functions</i>	3
• Added DYY Package to <i>Thermal Information</i> table.....	4

5 Pin Configuration and Functions



D, PW, or DYY Package
16-Pin SOIC, TSSOP, or SOT-23
Top View



BQB Package
16-Pin WQFN
Transparent Top View

ピン機能

ピン		種類	概要
名称	番号		
QB	1	出力	QB 出力
QC	2	出力	QC 出力
QD	3	出力	QD 出力
QE	4	出力	QE 出力
QF	5	出力	QF 出力
QG	6	出力	QG 出力
QH	7	出力	QH 出力
GND	8	—	グランド
QH'	9	出力	シリアル出力、カスケード用に使用可能
SRCLR	10	入力	シフト・レジスタ・クリア、アクティブ Low
SRCLK	11	入力	シフト・レジスタ・クロック、立ち上がりエッジがトリガされる
RCLK	12	入力	出力レジスタ・クロック、立ち上がりエッジがトリガされる
OE	13	入力	出力イネーブル、アクティブ Low
SER	14	入力	シリアル入力
QA	15	出力	QA 出力
VCC	16	—	正電源
サーマル・パッド ⁽¹⁾		—	サーマル・パッドは GND に接続するか、フローティングのままにすることができます。他の信号や電源には接続しないでください。

1. BQB パッケージのみ。

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		±20 mA
I_{OK}	Output clamp current ⁽²⁾	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		±20 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35 mA
	Continuous current through V_{CC} or GND			±70 mA
T_J	Junction temperature ⁽³⁾			150 °C
T_{stg}	Storage temperature			-65 150 °C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HCS595				UNIT
		PW (TSSOP)	D (SOIC)	BQB (WQFN)	DYY (SOT-23)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.2	122.2	108.4	186.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	80.9	77.3	109.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.8	80.6	74.4	111.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.7	40.4	12.6	18.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85.5	80.3	74.5	110.9	°C/W

THERMAL METRIC ⁽¹⁾		SN74HCS595				UNIT
		PW (TSSOP)	D (SOIC)	BQB (WQFN)	DYY (SOT-23)	
		16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	54.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP	MAX	UNIT
V _{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V _{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV _T	Hysteresis (V _{T+} - V _{T-}) ⁽¹⁾			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V _{OH}	High-level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V to 6 V	V _{CC} - 0.1	V _{CC} - 0.002		V
			I _{OH} = -6 mA	4.5 V	4.0	4.3		
			I _{OH} = -7.8 mA	6 V	5.4	5.75		
V _{OL}	Low-level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V to 6 V		0.002	0.1	V
			I _{OL} = 6 mA	4.5 V		0.18	0.30	
			I _{OL} = 7.8 mA	6 V		0.22	0.33	
I _I	Input leakage current	V _I = V _{CC} or 0		6 V		±0.1	±1	μA
I _{OZ}	Off-state (high-impedance state) output current	V _O = V _{CC} or 0		6 V		±0.5	±5	μA
I _{CC}	Supply current	V _I = V _{CC} or 0, I _O = 0		6 V		0.1	2	μA
C _i	Input capacitance			2 V to 6 V			5	pF

(1) Guaranteed by design.

6.6 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER			V _{CC}	Operating free-air temperature (T _A)				UNIT
				25°C		−40°C to 125°C		
				MIN	MAX	MIN	MAX	
t _w	Pulse duration	SRCLK or RCLK high or low	2 V	7		9	ns	
			4.5 V	7		7		
			6 V	7		7		
		SRCLR low	2 V	8		10		
			4.5 V	7		7		
			6 V	7		7		

$C_L = 50$ pF; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER			V _{CC}	Operating free-air temperature (T _A)				UNIT
				25°C		−40°C to 125°C		
				MIN	MAX	MIN	MAX	
t _{su}	Setup time	SER before SRCLK ↑	2 V	8		13	ns	
			4.5 V	4		5		
			6 V	3		4		
		SRCLK ↑ before RCLK ↑	2 V	11		18		
			4.5 V	5		7		
			6 V	4		6		
		SRCLR low before RCLK ↑	2 V	8		13		
			4.5 V	4		6		
			6 V	4		5		
		SRCLR high (inactive) before SRCLK ↑	2 V	8		13		
			4.5 V	4		6		
			6 V	4		5		
t _h	Hold time	SER after SRCLK ↑	2 V	0		0	ns	
			4.5 V	0		0		
			6 V	0		0		

6.7 Switching Characteristics

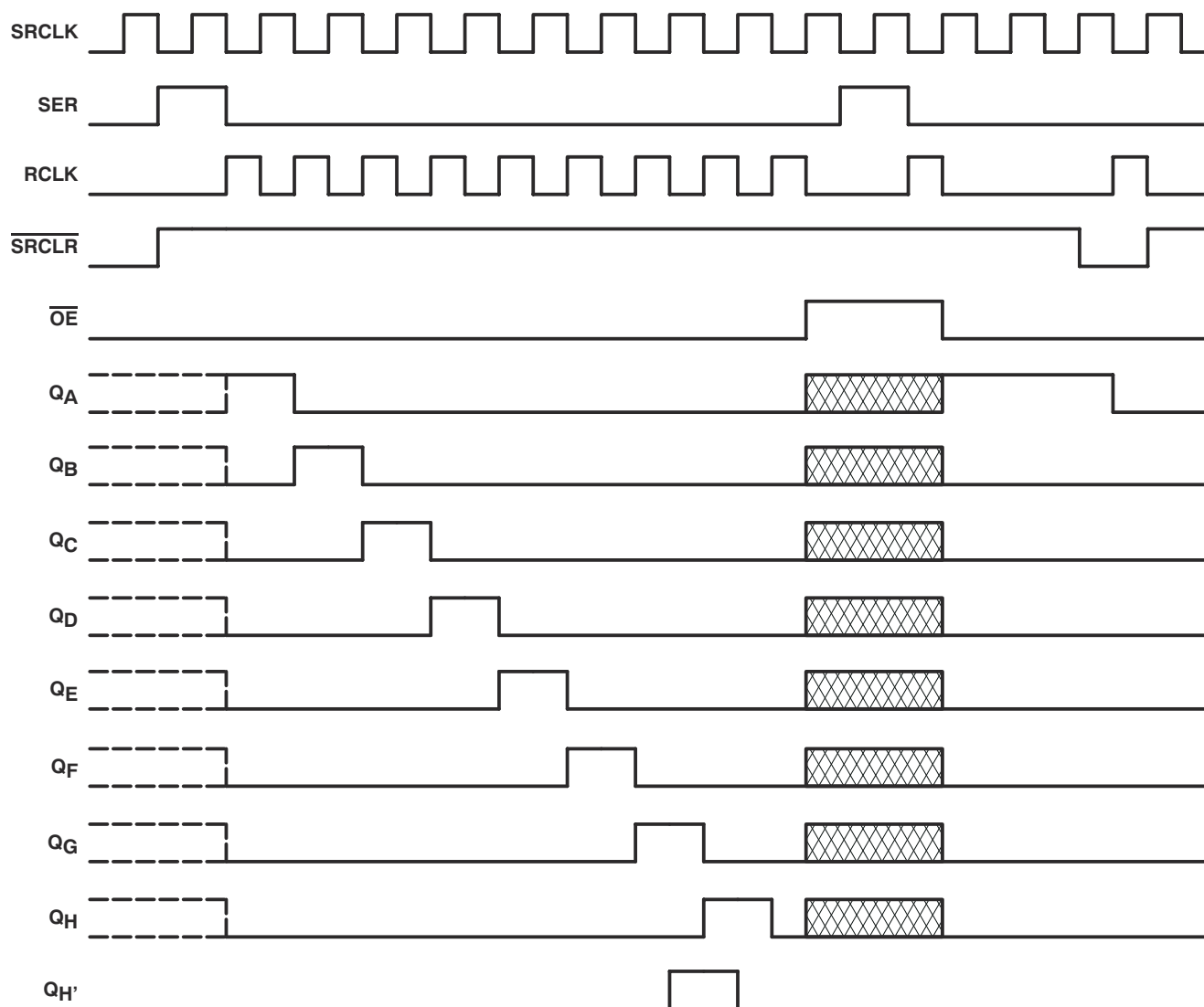
$C_L = 50$ pF; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).


PARAMETER		FROM	TO	V _{CC}	Operating free-air temperature (T _A)						UNIT
					25°C			−40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Max switching frequency			2 V	35			19			MHz
				4.5 V	110			60			
				6 V	130			75			
t _{pd}	Propagation delay	SRCLK	Q _H ¹	2 V	14		19	28			ns
				4.5 V	6		8	10			
				6 V	5		7	9			
		RCLK	Q _A - Q _H	2 V	16		21	37			
				4.5 V	6		9	12			
				6 V	6		8	10			
t _{PHL}	Propagation delay	SRCLR	Q _H ¹	2 V	13		19	27			ns
				4.5 V	6		8	11			
				6 V	6		8	10			
t _{en}	Enable time	OE	Q _A - Q _H	2 V	12		18	27			ns
				4.5 V	6		9	13			
				6 V	5		8	11			
t _{dis}	Disable time	OE	Q _A - Q _H	2 V	13		16	20			ns
				4.5 V	9		11	13			
				6 V	8		10	12			
t _t	Transition-time		Any output	2 V	9			16			ns
		4.5 V		5			9				
		6 V		4			8				

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		40		pF

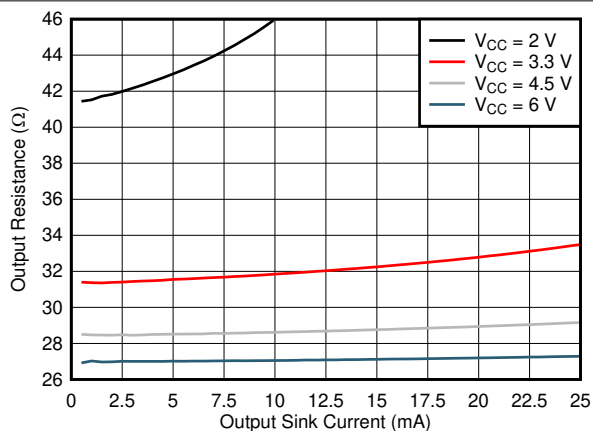


NOTE:  implies that the output is in 3-State mode.

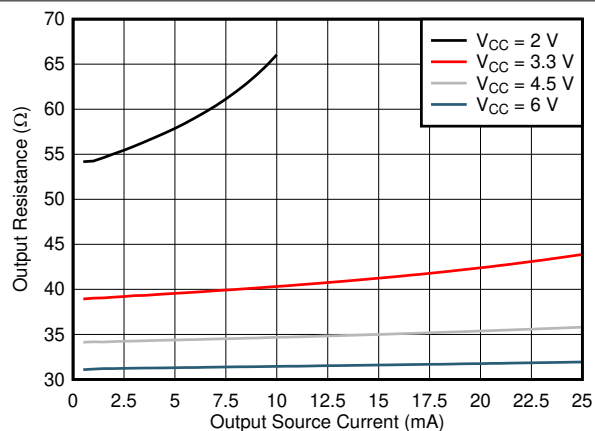
6-1. Timing Diagram

6.9 Typical Characteristics

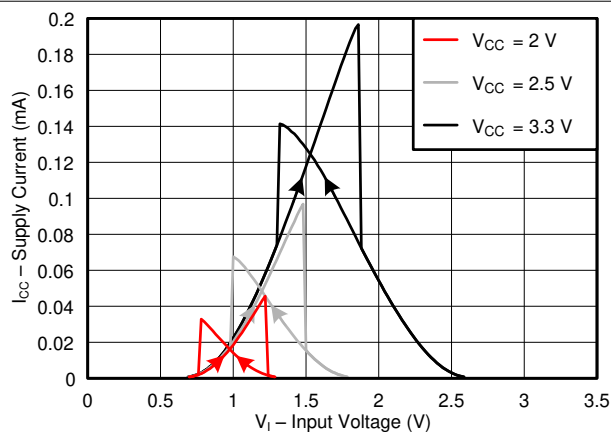
$T_A = 25^\circ\text{C}$



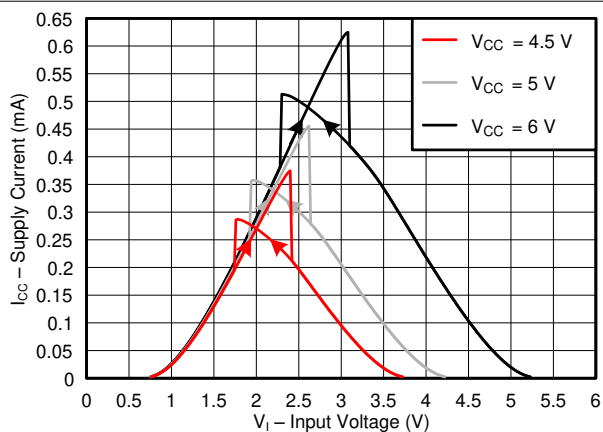
6-2. Output driver resistance in LOW state.



6-3. Output driver resistance in HIGH state.



6-4. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply



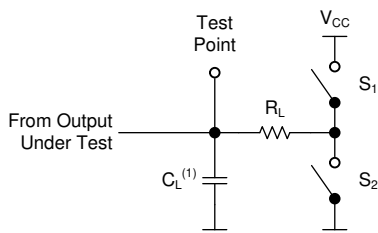
6-5. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 2.5 \text{ ns}$.

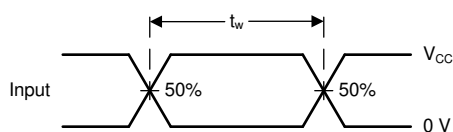
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

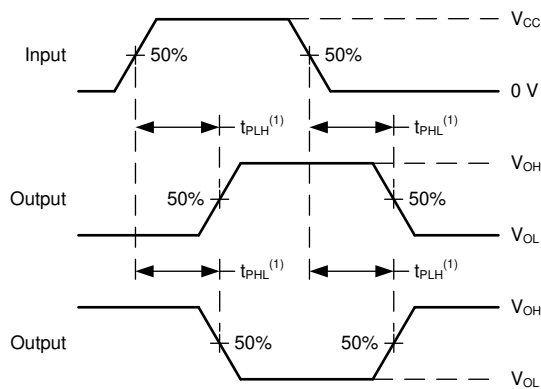


(1) C_L includes probe and test-fixture capacitance.

7-1. Load Circuit for 3-State Outputs

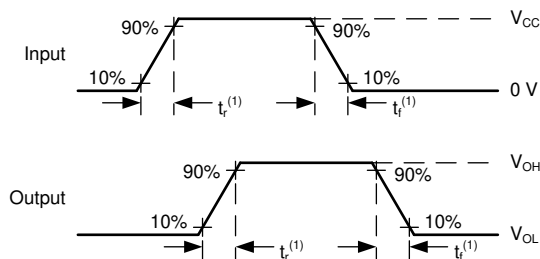


7-3. Voltage Waveforms, Pulse Duration



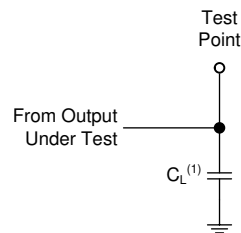
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

7-5. Voltage Waveforms Propagation Delays



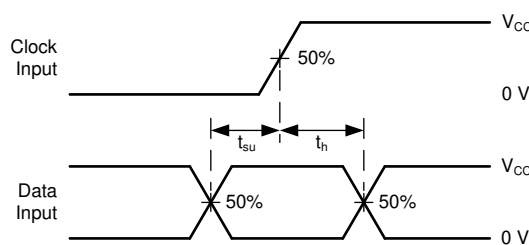
(1) The greater between t_r and t_f is the same as t_t .

7-7. Voltage Waveforms, Input and Output Transition Times

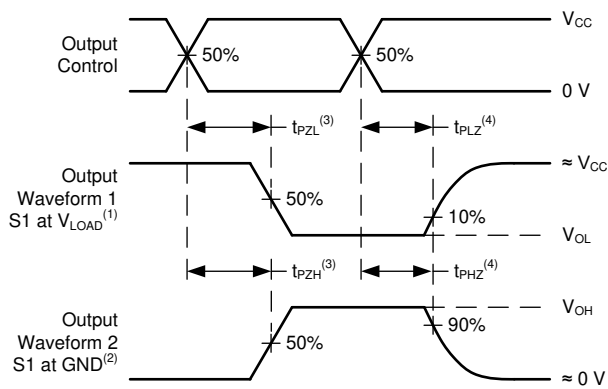


(1) C_L includes probe and test-fixture capacitance.

7-2. Load Circuit for Push-Pull Outputs



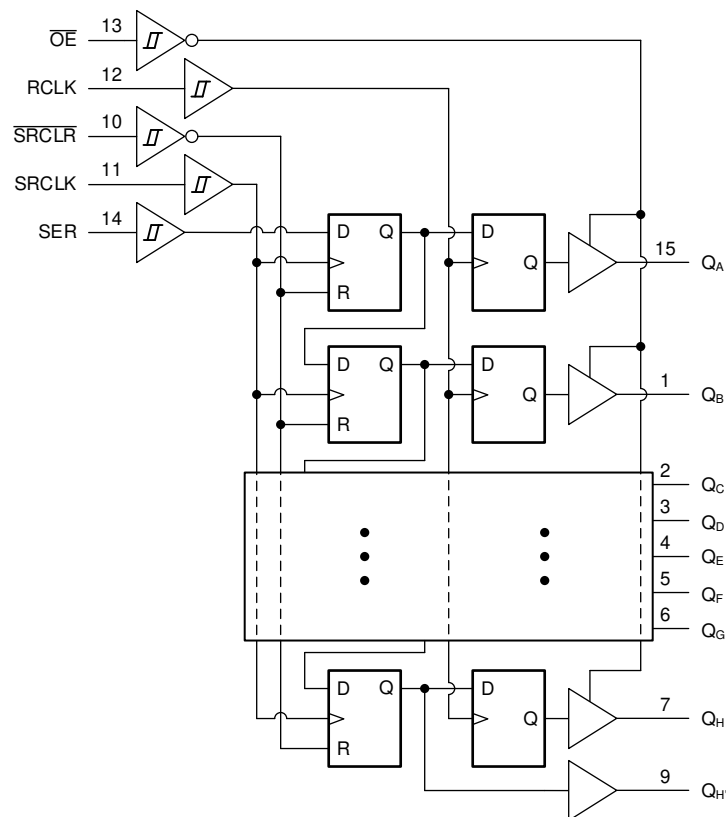
7-4. Voltage Waveforms, Setup and Hold Times



7-6. Voltage Waveforms Propagation Delays

8 Detailed Description

8.1 Functional Block Diagram



8-1. Logic Diagram (Positive Logic) for the SN74HCS595

8.2 Feature Description

8.2.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-State outputs. The three states that these outputs can be in are driving high, driving low, and high impedance. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10 kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.2.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable

of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.2.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.2.4 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Electrical Placement of Clamping Diodes for Each Input and Output](#).

注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

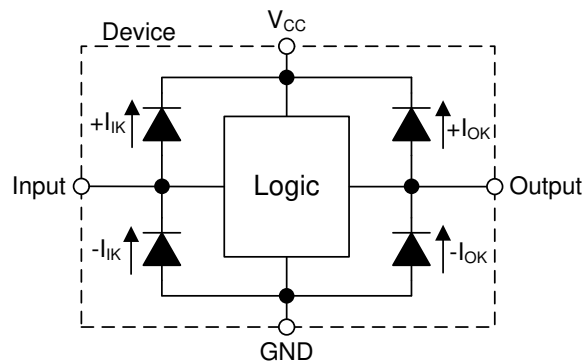


図 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3 Device Functional Modes

[Function Table](#) lists the functional modes of the SN74HCS595.

表 8-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	X	X	X	H	Outputs $Q_A - Q_H$ are disabled
X	X	X	X	L	Outputs $Q_A - Q_H$ are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.

表 8-1. Function Table (continued)

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証テストすることで、システムの機能を確認する必要があります。

9.1 Application Information

In this application, the SN74HCS595 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74HCS595 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The OE pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74HCS595 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74HCS595 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register. An RC can be connected to the $\overline{\text{SRCLR}}$ pin as shown in the [Typical application block diagram](#) to initialize the shift register to all zeros. With the $\overline{\text{OE}}$ pin pulled up with a resistor, this process can be performed while the outputs are in a high impedance state eliminating any erroneous data causing issues with the displays.

9.2 Typical Application

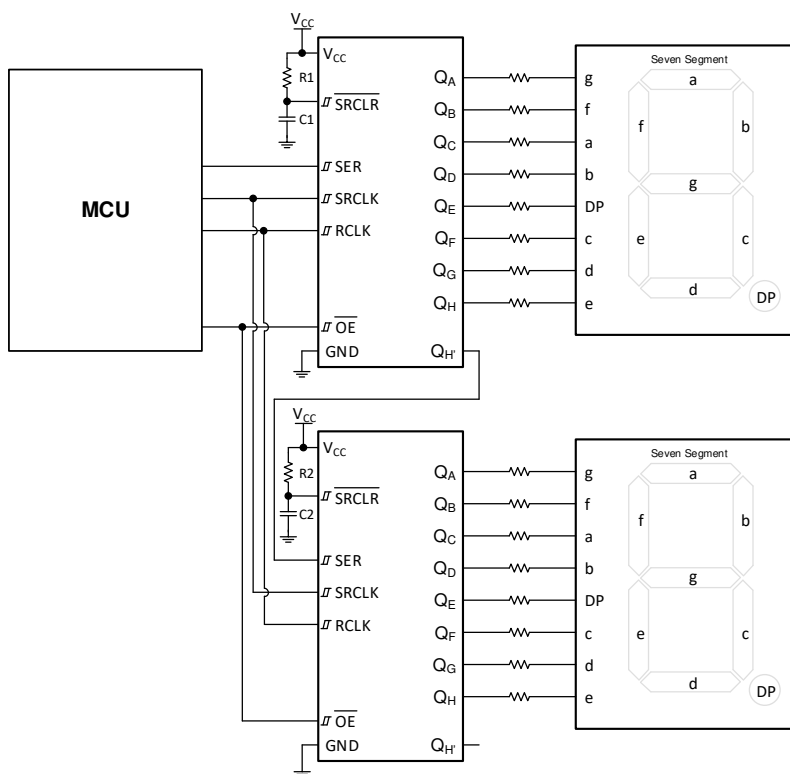


图 9-1. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS595 plus the maximum static supply current, I_{CC} , listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS595 plus the maximum supply current, I_{CC} , listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS595 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS595 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

注意

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t(min)}$ to be considered a logic LOW, and $V_{t(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS595, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HCS595 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS595 to the receiving device(s).
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.3 Application Curve

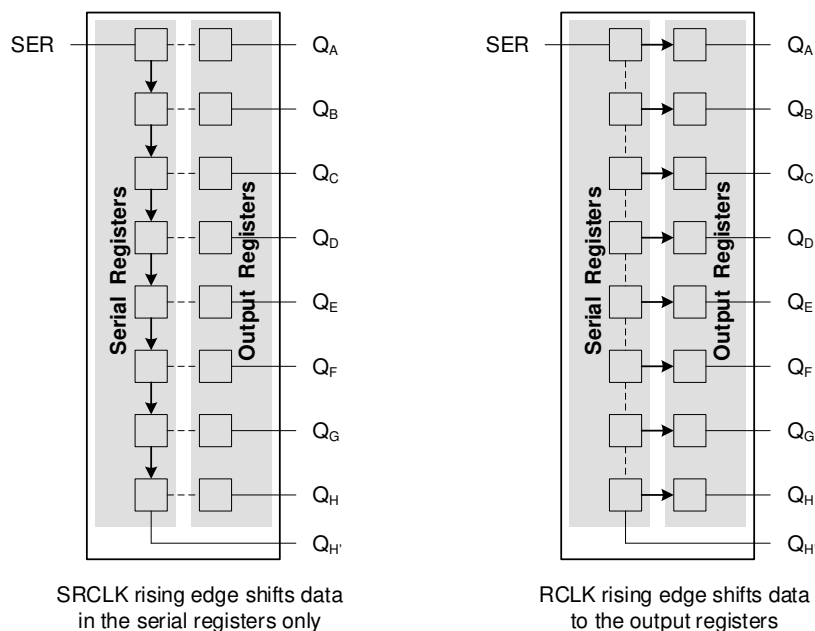


Figure 9-2. Simplified functional diagram showing clock operation

10 Power Supply Recommendations

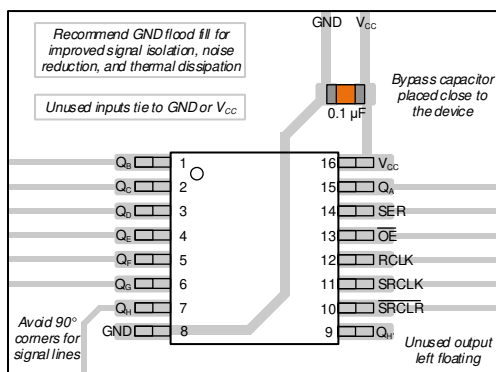
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example



11-1. Example layout for the SN74HCS595.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [HCMOS Design Considerations application report](#) (SCLA007)
- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application report](#) (SDYA009)
- Texas Instruments, [Designing With Logic application report](#)

12.2 ドキュメントの更新通知を受け取る方法

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12.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS595BQBR	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595
SN74HCS595BQBR.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595
SN74HCS595DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS595
SN74HCS595DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595
SN74HCS595DYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595
SN74HCS595DYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595
SN74HCS595PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS595
SN74HCS595PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74HCS595 :

- Automotive : [SN74HCS595-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS595BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74HCS595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCS595DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74HCS595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS595BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74HCS595DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HCS595DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74HCS595PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

GENERIC PACKAGE VIEW

BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

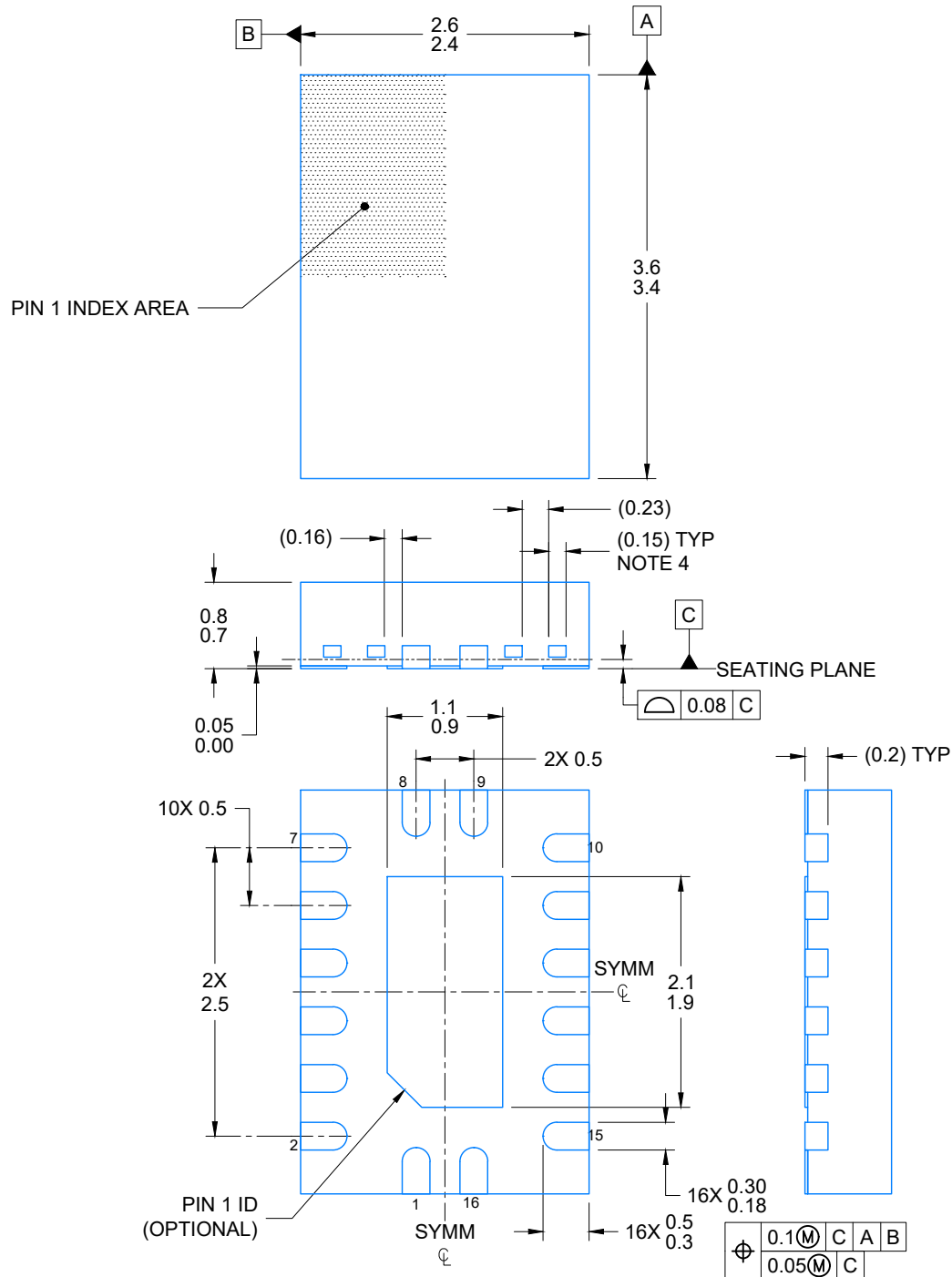


4226161/A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

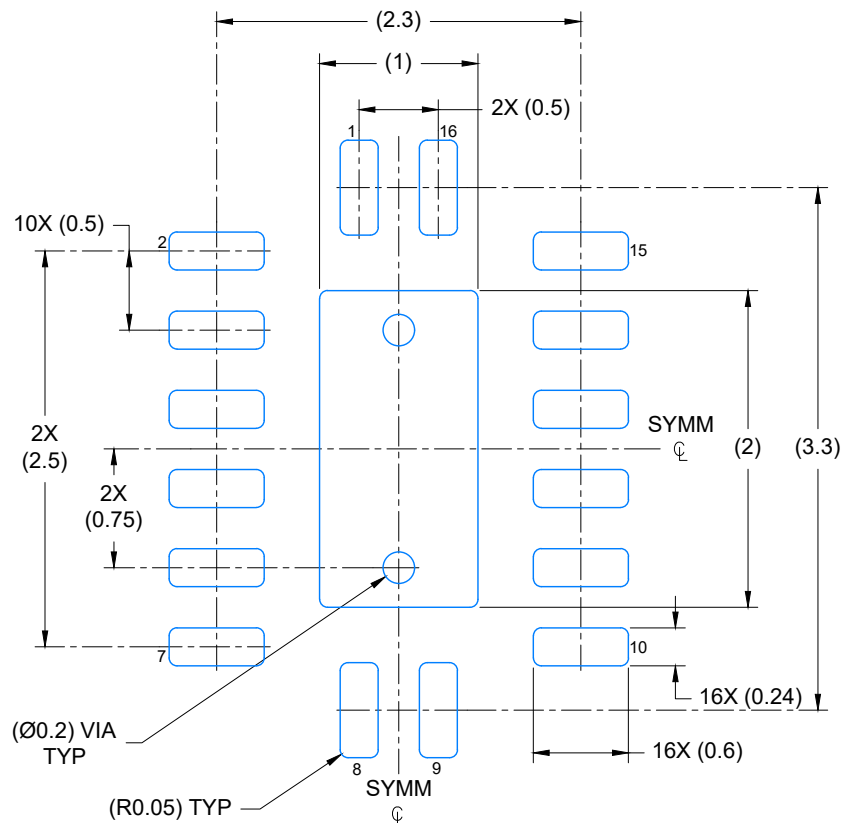
BQB0016A



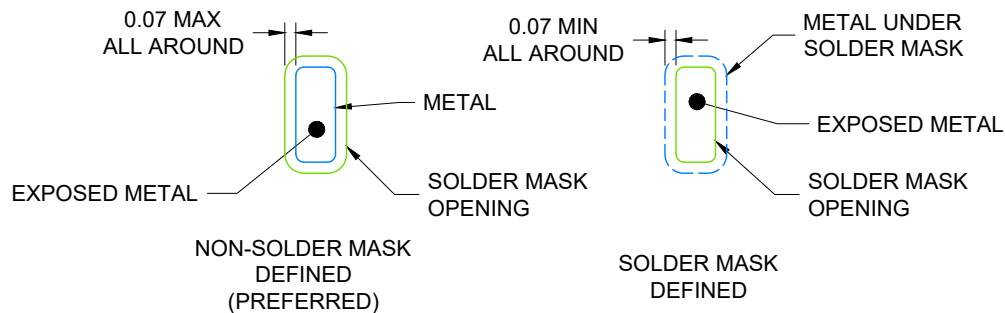
4224640/B 01/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present



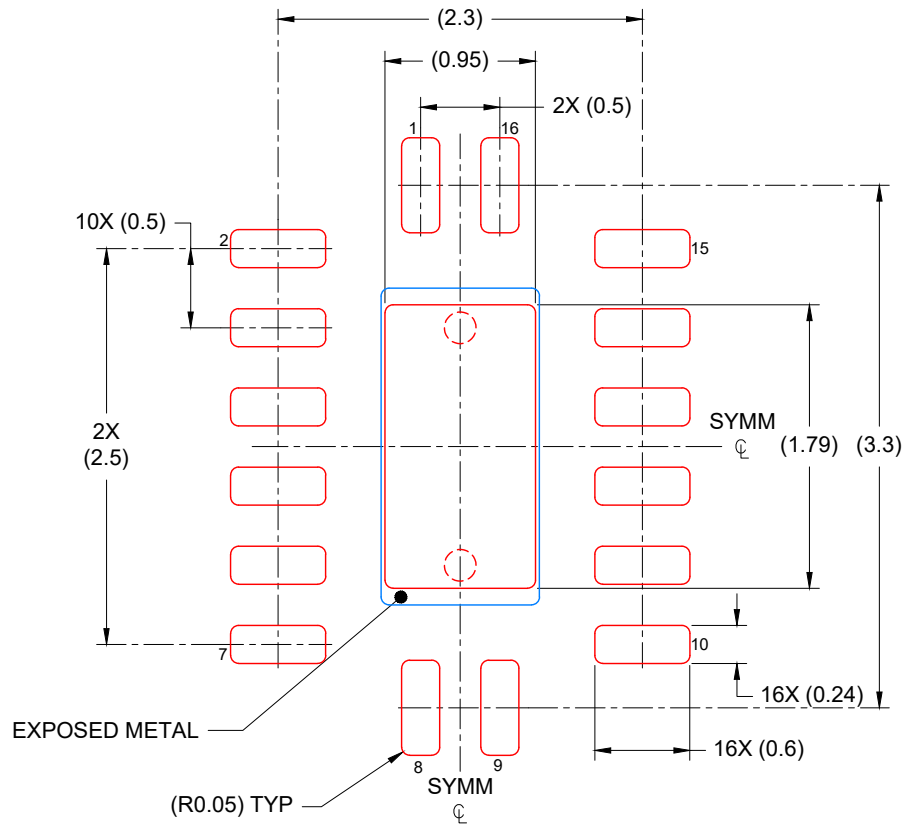
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



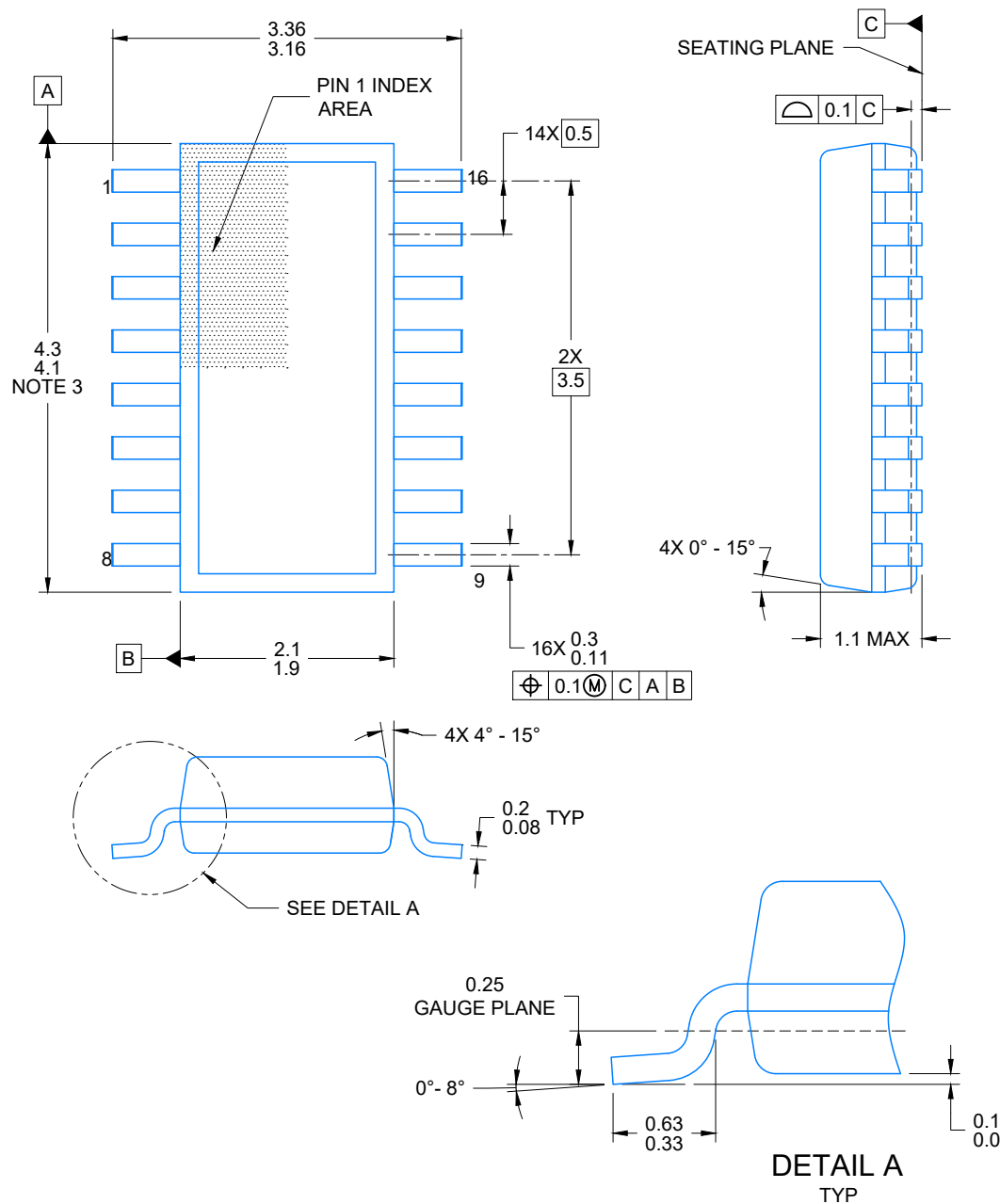
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

NOTES: (continued)

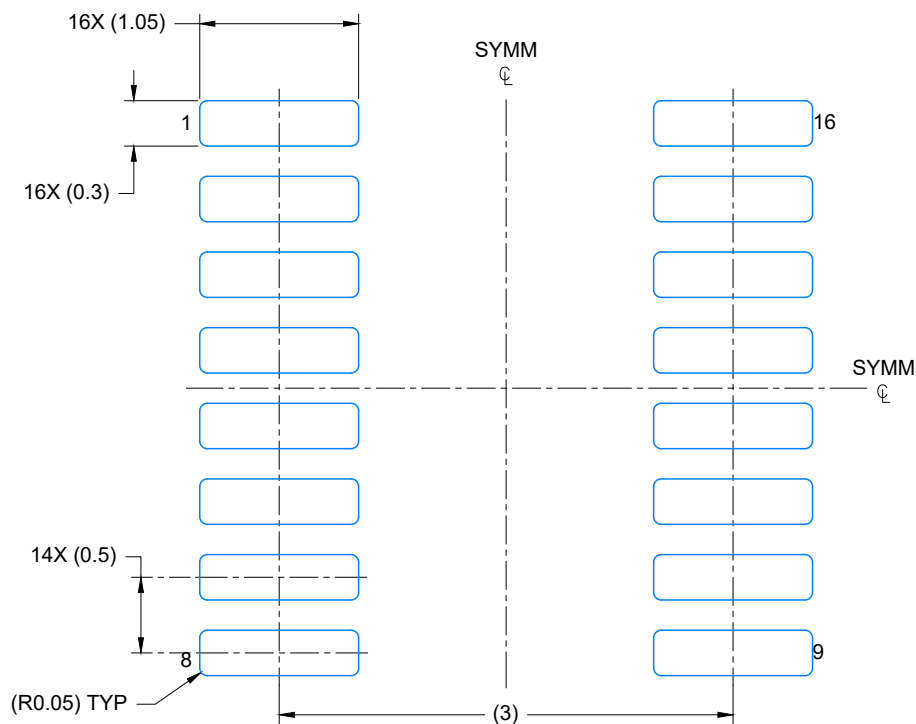
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



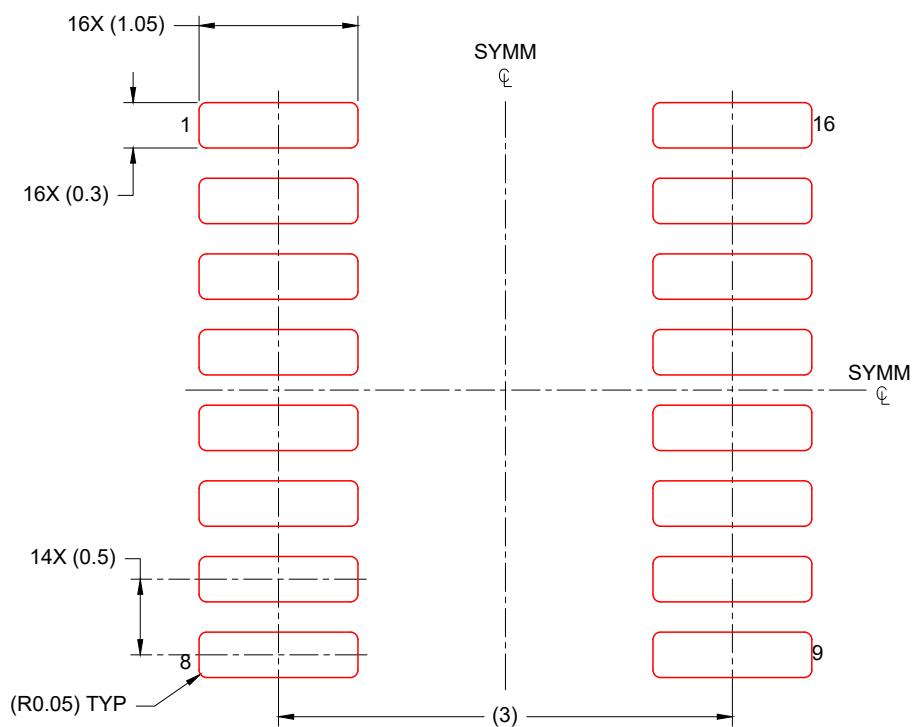
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月